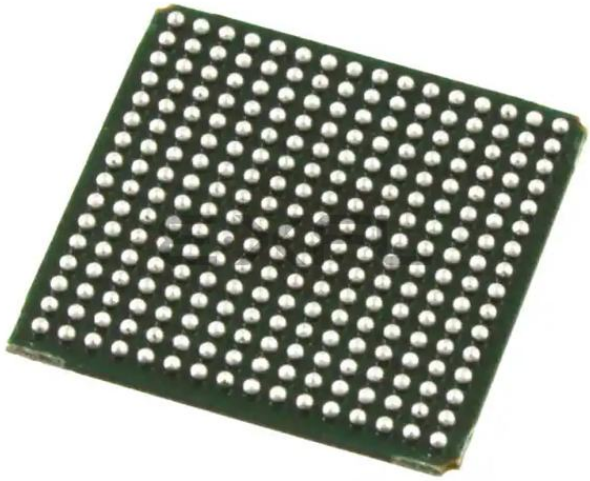
Lattice Semiconductor Corporation - LFX200EB-03FN256I Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	2704
Total RAM Bits	113664
Number of I/O	160
Number of Gates	210000
Voltage - Supply	2.3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 105°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfx200eb-03fn256i

Product Line	Ordering Part Number	Product Status	Reference PCN
LFX500B	LFX500B-03F516C	**Discontinued**	PCN#09-10
	LFX500B-04F516C		
	LFX500B-05F516C		
	LFX500B-03F900C		
	LFX500B-03FN900C		
	LFX500B-04F900C		
	LFX500B-04FN900C		
	LFX500B-05F900C		
	LFX500B-05FN900C		
LFX500C	LFX500C-03F516C	**Discontinued**	PCN#09-10
	LFX500C-04F516C		
	LFX500C-03F900C		
	LFX500C-03FN900C		
	LFX500C-04F900C		
	LFX500C-04FN900C		
LFX1200B	LFX1200B-03FE680C	**Discontinued**	PCN#03A-10
	LFX1200B-04FE680C		
	LFX1200B-05FE680C		
	LFX1200B-03F900C		
	LFX1200B-04F900C		
	LFX1200B-05F900C		
LFX1200C	LFX1200C-03FE680C	**Discontinued**	PCN#03A-10
	LFX1200C-04FE680C		
	LFX1200C-03F900C		
	LFX1200C-04F900C		
LFX125EB	LFX125EB-03F256C	Active / Orderable	
	LFX125EB-03FN256C		
	LFX125EB-04F256C		
	LFX125EB-04FN256C		
	LFX125EB-05F256C		
	LFX125EB-05FN256C		
	LFX125EB-03F256I		
	LFX125EB-03FN256I		
	LFX125EB-04F256I		
	LFX125EB-04FN256I		
	LFX125EB-03F516C	**Discontinued**	PCN#09-10
	LFX125EB-04F516C		
	LFX125EB-05F516C		
	LFX125EB-03F516I		
	LFX125EB-04F516I		
LFX125EC	LFX125EC-03F256C	**Discontinued**	PCN#09-10
	LFX125EC-03FN256C		
	LFX125EC-04F256C		
	LFX125EC-04FN256C		
	LFX125EC-03F256I		
	LFX125EC-03FN256I		

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Internet: http://www.latticesemi.com

Product Line	Ordering Part Number	Product Status	Reference PCN
LFX125EC (Cont'd)	LFX125EC-03F516C	**Discontinued**	PCN#09-10
	LFX125EC-04F516C		
	LFX125EC-03F516I		
LFX200EB	LFX200EB-03F256C	Active / Orderable	
	LFX200EB-03FN256C		
	LFX200EB-04F256C		
	LFX200EB-04FN256C		
	LFX200EB-05F256C		
	LFX200EB-05FN256C		
	LFX200EB-03F256I		
	LFX200EB-03FN256I		
	LFX200EB-04F256I		
	LFX200EB-04FN256I		
	LFX200EB-03F516C	**Discontinued**	PCN#09-10
	LFX200EB-04F516C		
	LFX200EB-05F516C		
	LFX200EB-03F516I		
	LFX200EB-04F516I		
LFX200EC	LFX200EC-03F256C	**Discontinued**	PCN#09-10
	LFX200EC-03FN256C		
	LFX200EC-04F256C		
	LFX200EC-04FN256C		
	LFX200EC-03F256I		
	LFX200EC-03FN256I		
	LFX200EC-03F516C		
	LFX200EC-04F516C		
	LFX200EC-03F516I		
LFX500EB	LFX500EB-03F516C	**Discontinued**	PCN#09-10
	LFX500EB-04F516C		
	LFX500EB-05F516C		
	LFX500EB-03F516I		
	LFX500EB-04F516I		
	LFX500EB-03F900C		
	LFX500EB-03FN900C		
	LFX500EB-04F900C		
	LFX500EB-04FN900C		
	LFX500EB-05F900C		
	LFX500EB-05FN900C		
	LFX500EB-03F900I		
	LFX500EB-03FN900I		
	LFX500EB-04F900I		
	LFX500EB-04FN900I		
LFX500EC	LFX500EC-03F516C	**Discontinued**	PCN#09-10
	LFX500EC-04F516C		
	LFX500EC-03F516I		

ispXPGA 125B/C & ispXPGA 125EB/EC EBR Timing Parameters

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Synchronous Write								
t_{EBSWAD_S}	Address Setup Delay	0.59	—	0.61	—	0.70	—	ns
t_{EBSWAD_H}	Address Hold Delay	-0.40	—	-0.39	—	-0.33	—	ns
$t_{EBSWCPW}$	Clock Pulse Width	3.16	—	3.40	—	3.91	—	ns
t_{EBSWWE_S}	Write Enable Setup Time	-0.12	—	-0.12	—	-0.10	—	ns
t_{EBSWWE_H}	Write Enable Hold Time	0.16	—	0.16	—	0.18	—	ns
t_{EBSWD_S}	Data Setup Time	0.27	—	0.28	—	0.32	—	ns
t_{EBSWD_H}	Data Hold Time	-0.27	—	-0.26	—	-0.22	—	ns
Synchronous Read								
t_{EBSR_CO}	Clock to Data Delay	—	2.04	—	2.19	—	2.52	ns
t_{EBSRAD_S}	Address Setup Delay	0.10	—	0.10	—	0.12	—	ns
t_{EBSRAD_H}	Address Hold Delay	-0.07	—	-0.07	—	-0.06	—	ns
$t_{EBSRCPW}$	Clock Pulse Width	3.16	—	3.40	—	3.91	—	ns
t_{EBSRCE_S}	Clock Enable Setup Time	-1.76	—	-1.71	—	-1.45	—	ns
t_{EBSRCE_H}	Clock Enable Hold Time	1.64	—	1.69	—	1.94	—	ns
t_{EBSRWE_S}	Write Enable Setup Time	-0.18	—	-0.17	—	-0.14	—	ns
t_{EBSRWE_H}	Write Enable Hold Time	0.12	—	0.12	—	0.14	—	ns
$t_{EBSRWEEN}$	Write Enable to Data Enable Time	—	1.02	—	1.05	—	1.21	ns
$t_{EBSRWEDIS}$	Write Enable to Data Disable Time	—	0.99	—	1.02	—	1.17	ns
t_{EBSREN}	Output Enable to Data Enable Time	—	1.02	—	1.05	—	1.21	ns
$t_{EBSRDIS}$	Output Enable to Data Disable Time	—	0.83	—	0.86	—	0.99	ns
Asynchronous Read								
$t_{EBARADO}$	Address to New Valid Data Delay	—	2.39	—	2.46	—	2.83	ns
t_{EBARAD_H}	Address to Previous Valid Data Delay	—	2.10	—	2.17	—	2.50	ns
$t_{EBARWEEN}$	Write Enable to Data Enable Time	—	1.01	—	1.04	—	1.20	ns
$t_{EBARWEDIS}$	Write Enable to Data Disable Time	—	0.98	—	1.01	—	1.16	ns
t_{EBAREN}	Output Enable to Data Enable Time	—	1.02	—	1.05	—	1.21	ns
$t_{EBARDIS}$	Output Enable to Data Disable Time	—	0.83	—	0.86	—	0.99	ns

1. Only available for ispXPGA 125B and ispXPGA 125EB (2.5V/3.3V) devices.

Timing v.0.3

ispXPGA 200B/C & ispXPGA 200EB/EC PFU Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Functional Delays								
LUTs								
t_{LUT4}	4-Input LUT Delay	—	0.41	—	0.44	—	0.51	ns
t_{LUT5}	5-Input LUT Delay	—	0.73	—	0.79	—	0.91	ns
t_{LUT6}	6-Input LUT Delay	—	0.86	—	0.93	—	1.07	ns
Shift Register (LUT)								
t_{LSR_S}	Shift Register Setup Time	-0.64	—	-0.62	—	-0.53	—	ns
t_{LSR_H}	Shift Register Hold Time	0.61	—	0.63	—	0.72	—	ns
t_{LSR_CO}	Shift Register Clock to Output Delay	—	0.70	—	0.75	—	0.86	ns
Arithmetic Functions								
$t_{LCTHRUR}$	MC (Macro Cell) Carry In to MC Carry Out Delay (Ripple)	—	0.08	—	0.09	—	0.10	ns
$t_{LCTHRUL}$[2]	MC Carry In to MC Carry Out Delay (Look Ahead)	—	0.05	—	0.05	—	0.06	ns
t_{LSTHRU}	MC Sum In to MC Sum Out Delay	—	0.42	—	0.45	—	0.52	ns
$t_{LSINCOUT}$	MC Sum In to MC Carry Out Delay	—	0.29	—	0.31	—	0.36	ns
$t_{LCINSOUTR}$	MC Carry In to MC Sum Out Delay (Ripple)	—	0.36	—	0.39	—	0.45	ns
$t_{LCINSOUTL}$	MC Carry In to MC Sum Out Delay (Look Ahead)	—	0.26	—	0.28	—	0.32	ns
Feed-thru								
t_{LFT}	PFU Feed-Thru Delay	—	0.15	—	0.16	—	0.18	ns
Distributed RAM								
t_{LRAM_CO}	Clock to RAM Output	—	1.24	—	1.33	—	1.53	ns
t_{LRAMAD_S}	Address Setup Time	-0.41	—	-0.40	—	-0.34	—	ns
t_{LRAMD_S}	Data Setup Time	0.21	—	0.22	—	0.25	—	ns
t_{LRAMWE_S}	Write Enable Setup Time	0.45	—	0.46	—	0.53	—	ns
t_{LRAMAD_H}	Address Hold Time	0.58	—	0.60	—	0.69	—	ns
t_{LRAMD_H}	Data Hold Time	0.11	—	0.11	—	0.13	—	ns
t_{LRAMWE_H}	Write Enable Hold Time	0.12	—	0.12	—	0.14	—	ns
$t_{LRAMCPW}$	Clock Pulse Width (High or Low)	2.91	—	3.00	—	3.45	—	ns
$t_{LRAMADO}$	Address to Output Delay	—	0.86	—	0.93	—	1.07	ns
Register/Latch Delays								
Registers								
t_{L_CO}	Register Clock to Output Delay	—	0.58	—	0.62	—	0.71	ns
t_{L_S}	Register Setup Time (Data before Clock)	0.14	—	0.14	—	0.16	—	ns
t_{L_H}	Register Hold Time (Data after Clock)	-0.12	—	-0.12	—	-0.10	—	ns
t_{LCE_S}	Register Clock Enable Setup Time	-0.11	—	-0.11	—	-0.09	—	ns
t_{LCE_H}	Register Clock Enable Hold Time	0.11	—	0.11	—	0.13	—	ns
Latches								
t_{L_GO}	Latch Gate to Output Delay	—	0.09	—	0.10	—	0.12	ns
t_{LL_S}	Latch Setup Time	0.14	—	0.14	—	0.16	—	ns
t_{LL_H}	Latch Hold Time	-0.12	—	-0.12	—	-0.10	—	ns
t_{LLPD}	Latch Propagation Delay (Transparent Mode)	—	0.09	—	0.10	—	0.12	ns

ispXPGA 200B/C & ispXPGA 200EB/EC EBR Timing Parameters

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Synchronous Write								
t_{EBSWAD_S}	Address Setup Delay	0.59	—	0.61	—	0.70	—	ns
t_{EBSWAD_H}	Address Hold Delay	-0.40	—	-0.39	—	-0.33	—	ns
$t_{EBSWCPW}$	Clock Pulse Width	3.16	—	3.40	—	3.91	—	ns
t_{EBSWWE_S}	Write Enable Setup Time	-0.12	—	-0.12	—	-0.10	—	ns
t_{EBSWWE_H}	Write Enable Hold Time	0.16	—	0.16	—	0.18	—	ns
t_{EBSWD_S}	Data Setup Time	0.27	—	0.28	—	0.32	—	ns
t_{EBSWD_H}	Data Hold Time	-0.27	—	-0.26	—	-0.22	—	ns
Synchronous Read								
t_{EBSR_CO}	Clock to Data Delay	—	2.04	—	2.19	—	2.52	ns
t_{EBSRAD_S}	Address Setup Delay	0.10	—	0.10	—	0.12	—	ns
t_{EBSRAD_H}	Address Hold Delay	-0.07	—	-0.07	—	-0.06	—	ns
$t_{EBSRCPW}$	Clock Pulse Width	3.16	—	3.40	—	3.91	—	ns
t_{EBSRCE_S}	Clock Enable Setup Time	-1.76	—	-1.71	—	-1.45	—	ns
t_{EBSRCE_H}	Clock Enable Hold Time	1.64	—	1.69	—	1.94	—	ns
t_{EBSRWE_S}	Write Enable Setup Time	-0.18	—	-0.17	—	-0.14	—	ns
t_{EBSRWE_H}	Write Enable Hold Time	0.12	—	0.12	—	0.14	—	ns
$t_{EBSRWEEN}$	Write Enable to Data Enable Time	—	1.02	—	1.05	—	1.21	ns
$t_{EBSRWEDIS}$	Write Enable to Data Disable Time	—	0.99	—	1.02	—	1.17	ns
t_{EBSREN}	Output Enable to Data Enable Time	—	1.02	—	1.05	—	1.21	ns
$t_{EBSRDIS}$	Output Enable to Data Disable Time	—	0.83	—	0.86	—	0.99	ns
Asynchronous Read								
$t_{EBARADO}$	Address to New Valid Data Delay	—	2.39	—	2.46	—	2.83	ns
t_{EBARAD_H}	Address to Previous Valid Data Delay	—	2.10	—	2.17	—	2.50	ns
$t_{EBARWEEN}$	Write Enable to Data Enable Time	—	1.01	—	1.04	—	1.20	ns
$t_{EBARWEDIS}$	Write Enable to Data Disable Time	—	0.98	—	1.01	—	1.16	ns
t_{EBAREN}	Output Enable to Data Enable Time	—	1.02	—	1.05	—	1.21	ns
$t_{EBARDIS}$	Output Enable to Data Disable Time	—	0.83	—	0.86	—	0.99	ns

1. Only available for ispXPGA 200B and ispXPGA 200EB (2.5V/3.3V) devices.

Timing v.0.3

ispXPGA 500B/C & ispXPGA 500EB/EC Timing Adders

Parameter	Description	Base Parameter	-5[1]		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Optional Adders									
$t_{IOINDLY}$	Input Delay	—	—	5.21	—	5.60	—	6.44	ns
t_{IOI} Input Adjusters									
LVTTL_in	Using 3.3V TTL	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_18_in	Using 1.8V CMOS	t_{IOIN}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_25_in	Using 2.5V CMOS	t_{IOIN}	—	0.3	—	0.3	—	0.3	ns
LVCMOS_33_in	Using 3.3V CMOS	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
AGP_1X_in	Using AGP 1x	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
CTT25_in	Using CTT 2.5V	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
CTT33_in	Using CTT 3.3V	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
GTL+_in	Using GTL+	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
HSTL_I_in	Using HSTL 2.5V, Class I	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
HSTL_III_in	Using HSTL 2.5V, Class III	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
LVDS_in	Using Low Voltage Differential Signaling (LVDS)	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
BLVDS_in	Using Bus Low Voltage Differential Signaling (BLVDS)	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
LVPECL_in	Using Low Voltage PECL	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
PCI_in	Using PCI	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
SSTL2_I_in	Using SSTL 2.5V, Class I	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
SSTL2_II_in	Using SSTL 2.5V, Class II	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
SSTL3_I_in	Using SSTL 3.3V, Class I	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
SSTL3_II_in	Using SSTL 3.3V, Class II	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
t_{IOO} Output Adjusters									
Slow Slew	Using Slow Slew (LVTTL and LVCMOS Outputs only)	t_{IOBUF}, t_{IOEN}	—	0.7	—	0.7	—	0.7	ns
LVTTL_out	Using 3.3V TTL Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVCMOS_18_4mA_out	Using 1.8V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.8	—	0.8	—	0.8	ns
LVCMOS_18_5.33mA_out	Using 1.8V CMOS Standard, 5.33mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	—	0.6	ns
LVCMOS_18_8mA_out	Using 1.8V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_18_12mA_out	Using 1.8V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.2	—	0.2	—	0.2	ns
LVCMOS_25_4mA_out	Using 2.5V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.7	—	0.7	—	0.7	ns
LVCMOS_25_5.33mA_out	Using 2.5V CMOS Standard, 5.33 mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_8mA_out	Using 2.5V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_12mA_out	Using 2.5V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_16mA_out	Using 2.5V CMOS Standard, 16mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns

ispXPGA 1200B/C & ispXPGA 1200EB/EC External Switching Characteristics

Over Recommended Operating Conditions

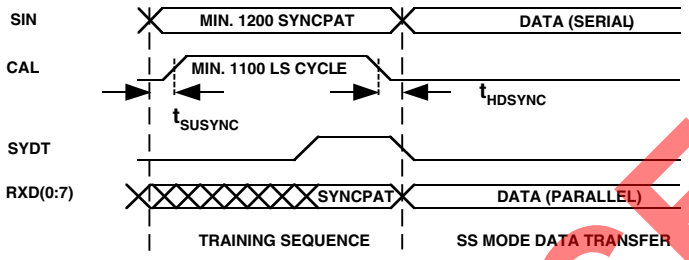
Parameter	Description	Conditions	-5[1]		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{CO}	Global Clock Input to Output	PIO Output Register	—	6.6	—	7.1	—	8.2	ns
t_S	Global Clock Input Setup	PIO Input Register without input delay	-2.7	—	-2.7	—	-2.3	—	ns
t_H	Global Clock Input Hold	PIO Input Register without input delay	4.5	—	4.6	—	5.3	—	ns
t_{SINDLY}	Global Clock Input Setup	PIO Input Register with input delay	3.8	—	3.8	—	4.4	—	ns
t_{HINDLY}	Global Clock Input Hold	PIO Input Register with input delay	0.0	—	0.0	—	0.0	—	
t_{COPLL}	Global Clock Input to Output	PIO Output Register using PLL without delay	—	3.1	—	3.3	—	3.8	ns
t_{SPLL}	Global Clock Input Setup	PIO Input Register without input delay using PLL without delay	0.5	—	0.5	—	0.6	—	ns
t_{HPLL}	Global Clock Input Hold	PIO Input Register without input delay using PLL without delay	0.8	—	0.8	—	1.0	—	ns
$t_{SINDLYPLL}$	Global Clock Input Setup	PIO Input Register with input delay using PLL without delay	7.6	—	7.6	—	8.8	—	ns
$t_{HINDLYPLL}$	Global Clock Input Hold	PIO Input Register with input delay using PLL without delay	-4.1	—	-4.0	—	-3.4	—	ns

1. Only available for ispXPGA 1200B and ispXPGA 1200EB (2.5V/3.3V) devices.

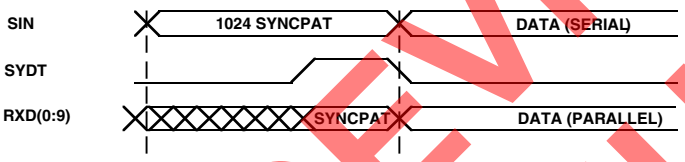
Timing v.0.2

Lock-in Timing

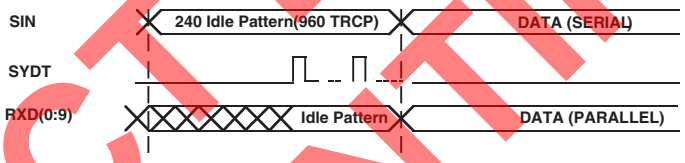
CDRX_SS LOCK-IN (DE-SKEW) TIMING



CDR_10B12B LOCK-IN TIMING

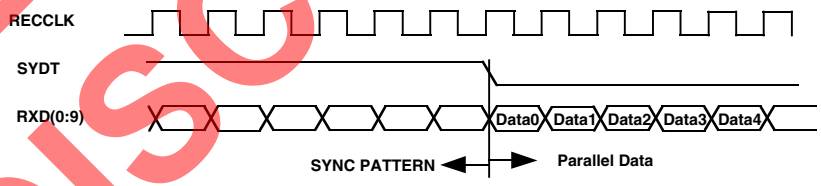


CDR_8B10B LOCK-IN TIMING

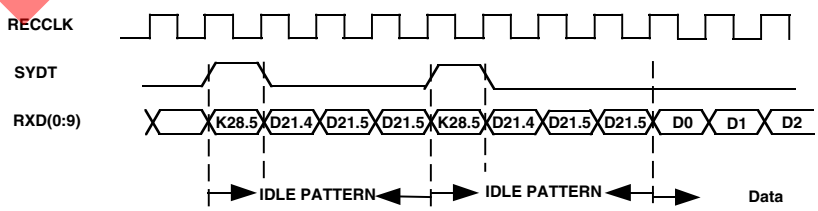


SYDT Timing

SYDT TIMING FOR CDRX_10B12B



SYDT TIMING FOR CDRX_8B10B



Signal Descriptions[1]

Signal Name	Signal Type	Description
General Purpose		
BK*y*_IO*x*[1,2]	Input/Output	General purpose I/O number x in I/O Bank y
GCLK*n*/I*n*[7]	Input	Global clock/input[8]
GSR	Input	Global Set/Reset
NC	—	No Connect
GND	GND	Ground
V_{CC}	VCC	Core logic power supply
V_{CCJ}	VCC	IEEE 1149.1 TAP power supply
V_{CCOy}[2]	VCC	I/O Bank y power supply
V_{REFy}[2]	Input	I/O Bank y reference voltage
D_{XN}, D_{XP}	Output	Temperature Sensing Diodes, provide a differential voltage, which corresponds to the temperature of the device.
Test and Program/Configuration		
TMS	Input	Test Mode Select
TCK	Input	Test Clock
TDI	Input	Test Data In
TDO	Output	Test Data Out
TOE	Input	Test Output Enable tri-states all I/O pins when driven low
CFG0	Input	Selects the SRAM memory configuration type (Peripheral or E^2CMOS Refresh)
PROGRAMb	Input	Initiates download from E^2CMOS or the peripheral port to SRAM memory (active low)
DONE	Bi-directional	Indicates when configuration is complete
INITb	Bi-directional	Indicates the device is ready for programming (active low)
READ	Input	Selects the READ operation when in sysCONFIG mode
CCLK	Input	sysCONFIG Configuration Clock
CSb	Input	sysCONFIG Chip Select (active low)
DATA[0:7]	Bi-directional	sysCONFIG Peripheral Port Data I/O
sysCLOCK PLL[3]		
PLL_FBK*z*	Input	Optional external feedback
PLL_RST*z*	Input	Optional external M divider reset
CLK_OUT*z*	Internal Signal	Clock output (routable to any I/O)
PLL_LOCK*z*	Internal Signal	Lock output (routable to any I/O)
GND_{P0}	GND	Left side PLL Ground
GND_{P1}	GND	Right side PLL Ground
V_{CCP0}	VCC	Left side PLL power supply
V_{CCP1}	VCC	Right side PLL power supply
sysHSI Block[4, 5]		
HSI*m*A_SINP, HSI*m*B_SINP	Input	P-side of differential serial data input
HSI*m*A_SINN, HSI*m*B_SINN	Input	N-side of differential serial data input
HSI*m*A_SOUTP, HSI*m*B_SOUTP	Output	P-side of differential serial data output
HSI*m*A_SOUTN, HSI*m*B_SOUTN	Output	N-side of differential serial data output
HSI*m*A_SYDT, HSI*m*B_SYDT	Internal Signal	Symbol alignment detect
HSI*m*A_RECCLK, HSI*m*B_RECCLK	Internal Signal	Recovered clock

ispXPGA Logic Signal Connections: 256-Ball fpBGA (Cont.)

256-fpBGA Ball	LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[2]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[2]
C8	BK7_IO1	-	91N	BK7_IO1	-	77N
B8	BK7_IO2	-	92P	BK7_IO2	-	78P
B7	BK7_IO3	-	92N	BK7_IO3	-	78N
A9	BK7_IO6	-	94P	BK7_IO4	-	79P
-	GND (Bank 7)	-	-	-	-	-
A8	BK7_IO7	-	94N	BK7_IO5	-	79N
C7	BK7_IO10	-	96P	BK7_IO6	-	80P
D7	BK7_IO11	-	96N	BK7_IO7	-	80N
D6	BK7_IO12	-	97P	BK7_IO8	-	81P
-	-	-	-	GND (Bank 7)	-	-
C6	BK7_IO13	-	97N	BK7_IO9	-	81N
B6	BK7_IO14	-	98P	BK7_IO10	-	82P
-	GND (Bank 7)	-	-	-	-	-
B5	BK7_IO15	-	98N	BK7_IO11	-	82N
A7	BK7_IO16	VREF7	99P	BK7_IO12	VREF7	83P
A6	BK7_IO17	-	99N	BK7_IO13	-	83N
D5	BK7_IO18	-	100P	BK7_IO14	-	84P
C5	BK7_IO19	-	100N	BK7_IO15	-	84N
A5	BK7_IO20	-	101P	BK7_IO16	-	85P
-	-	-	-	GND (Bank 7)	-	-
A4	BK7_IO21	-	101N	BK7_IO17	-	85N
B4	BK7_IO22	-	102P	BK7_IO18	-	86P
-	GND (Bank 7)	-	-	-	-	-
B3	BK7_IO23	-	102N	BK7_IO19	-	86N
A3	TDO	-	-	TDO	-	-
A2	VCCJ	-	-	VCCJ	-	-
C4	TDI	-	-	TDI	-	-

1. Not available for differential pairs.
2. If a sysHSI Block is used, the indicated sysHSI reserved pins are unavailable for general purpose I/O use.

ispXPGA Logic Signal Connections: 516-Ball fpBGA

516-Ball BGA Ball	LFX500			LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
E4	BK0_IO0	-	0P	BK0_IO0	-	0P/HSI0	NC	-	-
D3	BK0_IO1	-	0N	BK0_IO1	-	0N/HSI0	NC	-	-
E3	BK0_IO2	HSI0A_SOUTP	1P/HSI0	BK0_IO2	HSI0A_SOUTP	1P/HSI0	BK0_IO0	HSI0A_SOUTP	0P
-	GND (Bank 0)	-	-	GND (Bank 0)	-	-	-	-	-
F3	BK0_IO3	HSI0A_SOUTN	1N/HSI0	BK0_IO3	HSI0A_SOUTN	1N/HSI0	BK0_IO1	HSI0A_SOUTN	0N
C2	BK0_IO4	-	2P/HSI0	BK0_IO4	-	2P/HSI0	BK0_IO2	-	1P/HSI0
B1	BK0_IO5	-	2N/HSI0	BK0_IO5	-	2N/HSI0	BK0_IO3	-	1N/HSI0
G4	BK0_IO6	HSI0A_SINP	3P/HSI0	BK0_IO6	HSI0A_SINP	3P/HSI0	BK0_IO4	HSI0A_SINP	2P/HSI0
-	-	-	-	-	-	-	GND (Bank 0)	-	-
G3	BK0_IO7	HSI0A_SINN	3N/HSI0	BK0_IO7	HSI0A_SINN	3N/HSI0	BK0_IO5	HSI0A_SINN	2N/HSI0
C1	BK0_IO8	-	4P/HSI0	BK0_IO8	-	4P/HSI0	BK0_IO6	-	3P/HSI0
D2	BK0_IO9	VREF0	4N/HSI0	BK0_IO9	VREF0	4N/HSI0	BK0_IO7	VREF0	3N/HSI0
H4	BK0_IO10	HSI0B_SOUTP	5P/HSI0	BK0_IO10	HSI0B_SOUTP	5P/HSI0	BK0_IO8	HSI0B_SOUTP	4P/HSI0
-	GND (Bank 0)	-	-	GND (Bank 0)	-	-	-	-	-
H3	BK0_IO11	HSI0B_SOUTN	5N/HSI0	BK0_IO11	HSI0B_SOUTN	5N/HSI0	BK0_IO9	HSI0B_SOUTN	4N/HSI0
D1	BK0_IO12	-	6P/HSI0	BK0_IO12	-	6P/HSI0	BK0_IO10	-	5P/HSI0
E1	BK0_IO13	-	6N/HSI0	BK0_IO13	-	6N/HSI0	BK0_IO11	-	5N/HSI0
E2	BK0_IO14	HSI0B_SINP	7P/HSI0	BK0_IO14	HSI0B_SINP	7P/HSI0	BK0_IO12	HSI0B_SINP	6P/HSI0
-	-	-	-	-	-	-	GND (Bank 0)	-	-
F2	BK0_IO15	HSI0B_SINN	7N/HSI0	BK0_IO15	HSI0B_SINN	7N/HSI0	BK0_IO13	HSI0B_SINN	6N/HSI0
G2	BK0_IO16	-	8P/HSI0	NC	-	-	NC	-	-
F1	BK0_IO17	-	8N/HSI0	NC	-	-	NC	-	-
J3	BK0_IO18	HSI1A_SOUTP	9P	NC	-	-	NC	-	-
-	GND (Bank 0)	-	-	-	-	-	-	-	-
K3	BK0_IO19	HSI1A_SOUTN	9N	NC	-	-	NC	-	-
K4	BK0_IO20	-	10P	NC	-	-	NC	-	-
L4	BK0_IO21	-	10N	NC	-	-	NC	-	-
H2	BK0_IO22	HSI1A_SINP	11P	NC	-	-	NC	-	-
J2	BK0_IO23	HSI1A_SINN	11N	NC	-	-	NC	-	-
G1	BK0_IO24	-	12P	NC	-	-	NC	-	-
H1	BK0_IO25	-	12N	NC	-	-	NC	-	-
L3	BK0_IO26	HSI1B_SOUTP	13P	NC	-	-	NC	-	-
-	GND (Bank 0)	-	-	-	-	-	-	-	-
M3	BK0_IO27	HSI1B_SOUTN	13N	NC	-	-	NC	-	-
K2	BK0_IO28	-	14P	NC	-	-	NC	-	-
L2	BK0_IO29	-	14N	NC	-	-	NC	-	-
K1	BK0_IO30	HSI1B_SINP	15P	NC	-	-	NC	-	-
L1	BK0_IO31	HSI1B_SINN	15N	NC	-	-	NC	-	-
M2	BK0_IO32	-	16P	BK0_IO16	-	8P	NC	-	-
M1	BK0_IO33	-	16N	BK0_IO17	-	8N	NC	-	-
N3	BK0_IO34	PLL_FBK0	17P	BK0_IO18	PLL_FBK0	9P	BK0_IO14	PLL_FBK0	7P/HSI0
-	GND (Bank 0)	-	-	GND (Bank 0)	-	-	-	-	-
N4	BK0_IO35	PLL_RST1	17N	BK0_IO19	PLL_RST1	9N	BK0_IO15	PLL_RST1	7N/HSI0
N2	BK0_IO36	-	18P	BK0_IO20	-	10P	BK0_IO16	-	8P/HSI0
N1	BK0_IO37	PLL_FBK1	18N	BK0_IO21	PLL_FBK1	10N	BK0_IO17	PLL_FBK1	8N/HSI0
P1	BK0_IO38	PLL_RST0	19P	BK0_IO22	PLL_RST0	11P	BK0_IO18	PLL_RST0	9P
-	-	-	-	-	-	-	GND (Bank 0)	-	-
R1	BK0_IO39	-	19N	BK0_IO23	-	11N	BK0_IO19	-	9N
P3	BK0_IO40	CLK_OUT0	20P	BK0_IO24	CLK_OUT0	12P	BK0_IO20	CLK_OUT0	10P
-	GND (Bank 0)	-	-	-	-	-	-	-	-
P2	BK0_IO41	CLK_OUT1	20N	BK0_IO25	CLK_OUT1	12N	BK0_IO21	CLK_OUT1	10N

ispXPGA Logic Signal Connections: 516-Ball fpBGA (Cont.)

516-Ball BGA Ball	LFX500			LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
AE3	BK1_IO33	-	37N/HSI2	NC	-	-	NC	-	-
AG1	BK1_IO34	-	38P/HSI2	NC	-	-	NC	-	-
AH1	BK1_IO35	-	38N/HSI2	NC	-	-	NC	-	-
AG2	BK1_IO36	-	39P/HSI2	NC	-	-	NC	-	-
AF3	BK1_IO37	-	39N/HSI2	NC	-	-	NC	-	-
AJ1	BK1_IO38	-	40P/HSI2	NC	-	-	NC	-	-
-	GND (Bank 1)	-	-	-	-	-	-	-	-
AH2	BK1_IO39	-	40N/HSI2	NC	-	-	NC	-	-
AG3	BK1_IO40	-	41P	BK1_IO24	-	25P/HSI1	NC	-	-
AF4	BK1_IO41	-	41N	BK1_IO25	-	25N/HSI1	NC	-	-
AK2	TCK	-	-	TCK	-	-	TCK	-	-
AJ3	TMS	-	-	TMS	-	-	TMS	-	-
AG5	TOE	-	-	TOE	-	-	TOE	-	-
AH4	BK2_IO0	-	42P	BK2_IO0	-	26P	BK2_IO0	-	22P
AK3	BK2_IO1	-	42N	BK2_IO1	-	26N	BK2_IO1	-	22N
AJ4	BK2_IO2	-	43P	BK2_IO2	-	27P	BK2_IO2	-	23P
-	GND (Bank 2)	-	-	GND (Bank 2)	-	-	-	-	-
AH5	BK2_IO3	-	43N	BK2_IO3	-	27N	BK2_IO3	-	23N
AK4	BK2_IO4	-	44P	BK2_IO4	-	28P	BK2_IO4	-	24P
-	-	-	-	-	-	-	GND (Bank 2)	-	-
AJ5	BK2_IO5	-	44N	BK2_IO5	-	28N	BK2_IO5	-	24N
AG7	BK2_IO6	-	45P	BK2_IO6	-	29P	BK2_IO6	-	25P
AH6	BK2_IO7	-	45N	BK2_IO7	-	29N	BK2_IO7	-	25N
AK5	BK2_IO8	-	46P	NC	-	-	NC	-	-
AJ6	BK2_IO9	-	46N	NC	-	-	NC	-	-
AG8	BK2_IO10	-	47P	NC	-	-	NC	-	-
-	GND (Bank 2)	-	-	-	-	-	-	-	-
AH7	BK2_IO11	-	47N	NC	-	-	NC	-	-
AK6	BK2_IO12	-	48P	NC	-	-	NC	-	-
AJ7	BK2_IO13	-	48N	NC	-	-	NC	-	-
AH8	BK2_IO14	-	49P	NC	-	-	NC	-	-
AG10	BK2_IO15	-	49N	NC	-	-	NC	-	-
AK7	BK2_IO16	-	50P	NC	-	-	NC	-	-
AJ8	BK2_IO17	-	50N	NC	-	-	NC	-	-
AH9	BK2_IO18	-	51P	NC	-	-	NC	-	-
-	GND (Bank 2)	-	-	-	-	-	-	-	-
AG11	BK2_IO19	-	51N	NC	-	-	NC	-	-
AK8	BK2_IO20	-	52P	BK2_IO8	-	30P	BK2_IO8	-	26P
AJ9	BK2_IO21	VREF2	52N	BK2_IO9	VREF2	30N	BK2_IO9	VREF2	26N
AH10	BK2_IO22	-	53P	BK2_IO10	-	31P	BK2_IO10	-	27P
-	-	-	-	GND (Bank 2)	-	-	-	-	-
AH11	BK2_IO23	-	53N	BK2_IO11	-	31N	BK2_IO11	-	27N
AJ10	BK2_IO24	-	54P	BK2_IO12		32P	BK2_IO12	-	28P
AK10	BK2_IO25	-	54N	BK2_IO13	-	32N	BK2_IO13	-	28N
AH12	BK2_IO26	-	55P	BK2_IO14	-	33P	BK2_IO14	-	29P
-	GND (Bank 2)	-	-	-	-	-	-	-	-
AJ11	BK2_IO27	-	55N	BK2_IO15	-	33N	BK2_IO15	-	29N
AK11	BK2_IO28	-	56P	NC	-	-	NC	-	-
AJ12	BK2_IO29	-	56N	NC	-	-	NC	-	-
AG13	BK2_IO30	-	57P	BK2_IO16	-	34P	BK2_IO16	-	30P
AH13	BK2_IO31	-	57N	BK2_IO17	-	34N	BK2_IO17	-	30N

ispXPGA Logic Signal Connections: 516-Ball fpBGA (Cont.)

516-Ball BGA Ball	LFX500			LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
AJ25	BK3_IO32	-	79P	NC	-	-	NC	-	-
AG24	BK3_IO33	-	79N	NC	-	-	NC	-	-
AK26	BK3_IO34	-	80P	BK3_IO20	-	49P	BK3_IO16	-	41P
-	-	-	-	-	-	-	GND (Bank 3)	-	-
AH25	BK3_IO35	-	80N	BK3_IO21	-	49N	BK3_IO17	-	41N
AJ26	BK3_IO36	-	81P	BK3_IO22	-	50P	BK3_IO18	-	42P
-	-	-	-	GND (Bank 3)	-	-	-	-	-
AH26	BK3_IO37	-	81N	BK3_IO23	-	50N	BK3_IO19	-	42N
AK27	BK3_IO38	-	82P	NC	-	-	NC	-	-
-	GND (Bank 3)	-	-	-	-	-	-	-	-
AJ27	BK3_IO39	-	82N	NC	-	-	NC	-	-
AG26	BK3_IO40	-	83P	BK3_IO24	-	51P	BK3_IO20	-	43P
AH27	BK3_IO41	-	83N	BK3_IO25	-	51N	BK3_IO21	-	43N
AK28	GSR	-	-	GSR	-	-	GSR	-	-
AJ28	DXP	-	-	DXP	-	-	DXP	-	-
AK29	DXN	-	-	DXN	-	-	DXN	-	-
AH29	BK4_IO0	-	84P	BK4_IO0	-	52P/HSI2	BK4_IO0	-	44P
AG28	BK4_IO1	-	84N	BK4_IO1	-	52N/HSI2	BK4_IO1	-	44N
AF27	BK4_IO2	-	85P/HSI3	NC	-	-	NC	-	-
-	GND (Bank 4)	-	-	-	-	-	-	-	-
AF28	BK4_IO3	-	85N/HSI3	NC	-	-	NC	-	-
AJ30	BK4_IO4	-	86P/HSI3	NC	-	-	NC	-	-
AH30	BK4_IO5	-	86N/HSI3	NC	-	-	NC	-	-
AG29	BK4_IO6	-	87P/HSI3	NC	-	-	NC	-	-
AF29	BK4_IO7	-	87N/HSI3	NC	-	-	NC	-	-
AE28	BK4_IO8	-	88P/HSI3	NC	-	-	NC	-	-
AD27	BK4_IO9	-	88N/HSI3	NC	-	-	NC	-	-
AG30	BK4_IO10	HSI3A_SINP	89P/HSI3	BK4_IO2	HSI2A_SINP	53P/HSI2	BK4_IO2	-	45P
-	GND (Bank 4)	-	-	GND (Bank 4)	-	-	-	-	-
AF30	BK4_IO11	HSI3A_SINN	89N/HSI3	BK4_IO3	HSI2A_SINN	53N/HSI2	BK4_IO3	-	45N
AD28	BK4_IO12	-	90P/HSI3	BK4_IO4	-	54P/HSI2	BK4_IO4	-	46P
-	-	-	-	-	-	-	GND (Bank 4)	-	-
AC27	BK4_IO13	-	90N/HSI3	BK4_IO5	-	54N/HSI2	BK4_IO5	-	46N
AE29	BK4_IO14	HSI3A_SOUTP	91P/HSI3	BK4_IO6	HSI2A_SOUTP	55P/HSI2	NC	-	-
AE30	BK4_IO15	HSI3A_SOUTN	91N/HSI3	BK4_IO7	HSI2A_SOUTN	55N/HSI2	NC	-	-
AD29	BK4_IO16	-	92P/HSI3	BK4_IO8	-	56P/HSI2	BK4_IO6	-	47P
AD30	BK4_IO17	VREF4	92N/HSI3	BK4_IO9	VREF4	56N/HSI2	BK4_IO7	VREF4	47N
AC28	BK4_IO18	HSI3B_SINP	93P	BK4_IO10	HSI2B_SINP	57P/HSI2	NC	-	-
-	GND (Bank 4)	-	-	GND (Bank 4)	-	-	-	-	-
AB28	BK4_IO19	HSI3B_SINN	93N	BK4_IO11	HSI2B_SINN	57N/HSI2	NC	-	-
AA27	BK4_IO20	PLL_RST4	94P	BK4_IO12	PLL_RST4	58P/HSI2	BK4_IO8	PLL_RST4	48P
AB29	BK4_IO21	PLL_RST5	94N	BK4_IO13	PLL_RST5	58N/HSI2	BK4_IO9	PLL_RST5	48N
AC29	BK4_IO22	HSI3B_SOUTP	95P	BK4_IO14	HSI2B_SOUTP	59P/HSI2	BK4_IO10	-	49P
AC30	BK4_IO23	HSI3B_SOUTN	95N	BK4_IO15	HSI2B_SOUTN	59N/HSI2	BK4_IO11	-	49N
AA28	BK4_IO24	-	96P	NC	-	-	NC	-	-
Y27	BK4_IO25	-	96N	NC	-	-	NC	-	-
Y28	BK4_IO26	-	97P	NC	-	-	NC	-	-
-	GND (Bank 4)	-	-	-	-	-	-	-	-
AA29	BK4_IO27	-	97N	NC	-	-	NC	-	-
Y29	BK4_IO28	-	98P	BK4_IO16	-	60P	BK4_IO12	-	50P
-	-	-	-	-	-	-	GND (Bank 4)	-	-

ispXPGA Logic Signal Connections: 516-Ball fpBGA (Cont.)

516-Ball BGA Ball	LFX500			LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
AA30	BK4_IO29	-	98N	BK4_IO17	-	60N	BK4_IO13	-	50N
W28	BK4_IO30	SS_CLKIN1P	99P	BK4_IO18	SS_CLKIN1P	61P	BK4_IO14	SS_CLKIN1P	51P
-	-	-	-	GND (Bank 4)	-	-	-	-	-
W29	BK4_IO31	SS_CLKIN1N	99N	BK4_IO19	SS_CLKIN1N	61N	BK4_IO15	SS_CLKIN1N	51N
Y30	BK4_IO32	-	100P	NC	-	-	NC	-	-
W30	BK4_IO33	-	100N	NC	-	-	NC	-	-
V27	BK4_IO34	-	101P	NC	-	-	NC	-	-
-	GND (Bank 4)	-	-	-	-	-	-	-	-
V28	BK4_IO35	-	101N	NC	-	-	NC	-	-
V29	BK4_IO36	PLL_FBK4	102P	BK4_IO20	PLL_FBK4	62P	BK4_IO16	PLL_FBK4	52P
V30	BK4_IO37	PLL_FBK5	102N	BK4_IO21	PLL_FBK5	62N	BK4_IO17	PLL_FBK5	52N
U30	BK4_IO38	SS_CLKOUT1P	103P	BK4_IO22	SS_CLKOUT1P	63P	BK4_IO18	SS_CLKOUT1P	53P
U29	BK4_IO39	SS_CLKOUT1N	103N	BK4_IO23	SS_CLKOUT1N	63N	BK4_IO19	SS_CLKOUT1N	53N
U28	BK4_IO40	CLK_OUT4	104P	BK4_IO24	CLK_OUT4	64P	BK4_IO20	CLK_OUT4	54P
-	GND (Bank 4)	-	-	-	-	-	-	-	-
T27	BK4_IO41	CLK_OUT5	104N	BK4_IO25	CLK_OUT5	64N	BK4_IO21	CLK_OUT5	54N
-	-	-	-	GND (Bank 4)	-	-	-	-	-
T28	GCLK4	-	LVDS Pair2P	GCLK4	-	LVDS Pair2P	GCLK4	-	LVDS Pair2P
T29	GCLK5	-	LVDS Pair2N	GCLK5	-	LVDS Pair2N	GCLK5	-	LVDS Pair2N
T30	VCCP1	-	-	VCCP1	-	-	VCCP1	-	-
R29	GNDP1	-	-	GNDP1	-	-	GNDP1	-	-
R28	GCLK6	-	LVDS Pair3P	GCLK6	-	LVDS Pair3P	GCLK6	-	LVDS Pair3P
R27	GCLK7	-	LVDS Pair3N	GCLK7	-	LVDS Pair3N	GCLK7	-	LVDS Pair3N
-	-	-	-	GND (Bank 5)	-	-	-	-	-
R30	BK5_IO0	CLK_OUT6	105P	BK5_IO0	CLK_OUT6	65P	BK5_IO0	CLK_OUT6	55P
-	GND (Bank 5)	-	-	-	-	-	-	-	-
P30	BK5_IO1	CLK_OUT7	105N	BK5_IO1	CLK_OUT7	65N	BK5_IO1	CLK_OUT7	55N
P29	BK5_IO2	-	106P	BK5_IO2	-	66P	BK5_IO2	-	56P
-	-	-	-	-	-	-	GND (Bank 5)	-	-
P28	BK5_IO3	PLL_RST7	106N	BK5_IO3	PLL_RST7	66N	BK5_IO3	PLL_RST7	56N
N30	BK5_IO4	PLL_FBK6	107P	BK5_IO4	PLL_FBK6	67P	BK5_IO4	PLL_FBK6	57P/HSI1
N29	BK5_IO5	-	107N	BK5_IO5	-	67N	BK5_IO5	-	57N/HSI1
N28	BK5_IO6	PLL-RST6	108P	BK5_IO6	PLL_RST6	68P	BK5_IO6	PLL_RST6	58P//HSI1
-	GND (Bank 5)	-	-	GND (Bank 5)	-	-	-	-	-
N27	BK5_IO7	PLL_FBK7	108N	BK5_IO7	PLL_FBK7	68N	BK5_IO7	PLL_FBK7	58N/HSI1
M30	BK5_IO8	-	109P/HSI4	BK5_IO8	-	69P	NC	-	-
M29	BK5_IO9	-	109N/HSI4	BK5_IO9	-	69N	NC	-	-
L30	BK5_IO10	HSI4A_SINP	110P/HSI4	BK5_IO10	HSI3A_SINP	70P/HSI3	BK5_IO8	HSI1A_SINP	59P/HSI1
-	-	-	-	-	-	-	GND (Bank 5)	-	-
L29	BK5_IO11	HSI4A_SINN	110N/HSI4	BK5_IO11	HSI3A_SINN	70N/HSI3	BK5_IO9	HSI1A_SINN	59N/HSI1
M28	BK5_IO12	-	111P/HSI4	BK5_IO12	-	71P/HSI3	BK5_IO10	-	60P/HSI1
L28	BK5_IO13	-	111N/HSI4	BK5_IO13		71N/HSI3	BK5_IO11	-	60N/HSI1
K30	BK5_IO14	HSI4A_SOUTP	112P/HSI4	BK5_IO14	HSI3A_SOUTP	72P/HSI3	BK5_IO12	HSI1A_SOUTP	61P/HSI1
-	GND (Bank 5)	-	-	GND (Bank 5)	-	-	-	-	-
K29	BK5_IO15	HSI4A_SOUTN	112N/HSI4	BK5_IO15	HSI3A_SOUTN	72N/HSI3	BK5_IO13	HSI1A_SOUTN	61N/HSI1
L27	BK5_IO16	-	113P/HSI4	NC	-	-	NC	-	-
K28	BK5_IO17	-	113N/HSI4	NC	-	-	NC	-	-
H30	BK5_IO18	HSI4B_SINP	114P/HSI4	NC	-	-	NC	-	-
G30	BK5_IO19	HSI4B_SINN	114N/HSI4	NC	-	-	NC	-	-
J28	BK5_IO20	-	115P/HSI4	NC	-	-	NC	-	-
K27	BK5_IO21	-	115N/HSI4	NC	-	-	NC	-	-

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	Signal Name	Second Function	LVDS Pair/sysHSI Reserved[1]
-	GND (Bank 2)	-	-
K36	BK2_IO19	-	71N
H38	BK2_IO20	-	72P
J38	BK2_IO21	-	72N
J39	BK2_IO22	-	73P
L36	BK2_IO23	-	73N
K38	BK2_IO24	-	74P
M36	BK2_IO25	-	74N
L37	BK2_IO26	-	75P
-	GND (Bank 2)	-	-
K39	BK2_IO27	-	75N
L38	BK2_IO28	-	76P
P35	BK2_IO29	-	76N
N36	BK2_IO30	-	77P
M37	BK2_IO31	-	77N
L39	BK2_IO32	-	78P
M38	BK2_IO33	-	78N
M39	BK2_IO34	-	79P
-	GND (Bank 2)	-	-
P36	BK2_IO35	-	79N
R36	BK2_IO36	-	80P
N37	BK2_IO37	-	80N
P38	BK2_IO38	-	81P
T35	BK2_IO39	-	81N
R37	BK2_IO40	-	82P
R38	BK2_IO41	-	82N
P39	BK2_IO42	-	83P
-	GND (Bank 2)	-	-
R39	BK2_IO43	-	83N
T38	BK2_IO44	-	84P
T36	BK2_IO45	-	84N
T37	BK2_IO46	-	85P
U36	BK2_IO47	-	85N
U37	BK2_IO48	-	86P
T39	BK2_IO49	-	86N
V36	BK2_IO50	-	87P
-	GND (Bank 2)	-	-
U38	BK2_IO51	-	87N
U39	BK2_IO52	-	88P
V38	BK2_IO53	-	88N
V37	BK2_IO54	-	89P
W36	BK2_IO55	-	89N
W35	BK2_IO56	-	90P

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	Signal Name	Second Function	LVDS Pair/sysHSI Reserved[1]
AW35	BK4_IO4	-	126P
AV35	BK4_IO5	-	126N
AV34	BK4_IO6	HSI5A_SINP	127P
AU34	BK4_IO7	HSI5A_SINN	127N
AT34	BK4_IO8	-	128P
AU35	BK4_IO9	-	128N
AT33	BK4_IO10	HSI5A_SOUTP	129P/HSI5
-	GND (Bank 4)	-	-
AU33	BK4_IO11	HSI5A_SOUTN	129N/HSI5
AW34	BK4_IO12	VREF4	130P/HSI5
AV33	BK4_IO13	-	130N/HSI5
AR32	BK4_IO14	HSI5B_SINP	131P/HSI5
AT32	BK4_IO15	HSI5B_SINN	131N/HSI5
AU32	BK4_IO16	-	132P/HSI5
AW33	BK4_IO17	-	132N/HSI5
AV32	BK4_IO18	HSI5B_SOUTP	133P/HSI5
-	GND (Bank 4)	-	-
AV31	BK4_IO19	HSI5B_SOUTN	133N/HSI5
AU31	BK4_IO20	-	134P/HSI5
AW32	BK4_IO21	-	134N/HSI5
AR30	BK4_IO22	HSI6A_SINP	135P/HSI5
AT31	BK4_IO23	HSI6A_SINN	135N/HSI5
AW31	BK4_IO24	-	136P/HSI5
AV30	BK4_IO25	-	136N/HSI5
AT30	BK4_IO26	HSI6A_SOUTP	137P/HSI6
-	GND (Bank 4)	-	-
AT29	BK4_IO27	HSI6A_SOUTN	137N/HSI6
AW30	BK4_IO28	-	138P/HSI6
AU29	BK4_IO29	-	138N/HSI6
AT28	BK4_IO30	HSI6B_SINP	139P/HSI6
AU28	BK4_IO31	HSI6B_SINN	139N/HSI6
AV28	BK4_IO32	-	140P/HSI6
AT27	BK4_IO33	-	140N/HSI6
AU27	BK4_IO34	HSI6B_SOUTP	141P/HSI6
-	GND (Bank 4)	-	-
AV27	BK4_IO35	HSI6B_SOUTN	141N/HSI6
AW28	BK4_IO36	-	142P/HSI6
AR26	BK4_IO37	-	142N/HSI6
AW27	BK4_IO38	-	143P/HSI6
AT26	BK4_IO39	-	143N/HSI6
AV26	BK4_IO40	-	144P/HSI6
AR24	BK4_IO41	-	144N/HSI6
AT25	BK4_IO42	-	145P/HSI6

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	**Signal Name**	**Second Function**	**LVDS Pair/sysHSI Reserved[1]**
L3	BK7_IO35	-	234N
J1	BK7_IO36	-	235P
J2	BK7_IO37	-	235N
M4	BK7_IO38	-	236P
H1	BK7_IO39	-	236N
J3	BK7_IO40	-	237P
L4	BK7_IO41	-	237N
M5	BK7_IO42	-	238P
-	GND (Bank 7)	-	-
H2	BK7_IO43	-	238N
K4	BK7_IO44	-	239P
G1	BK7_IO45	-	239N
H3	BK7_IO46	-	240P
J4	BK7_IO47	VREF7	240N
K5	BK7_IO48	-	241P
G3	BK7_IO49	-	241N
H4	BK7_IO50	-	242P
-	GND (Bank 7)	-	-
F2	BK7_IO51	-	242N
G2	BK7_IO52	-	243P
H5	BK7_IO53	-	243N
F3	BK7_IO54	-	244P
F1	BK7_IO55	-	244N
G4	BK7_IO56	-	245P
E1	BK7_IO57	-	245N
F4	BK7_IO58	-	246P
-	GND (Bank 7)	-	-
E2	BK7_IO59	-	246N
F5	BK7_IO60	-	247P
E3	BK7_IO61	-	247N
D2	TDO	-	-
D3	VCCJ	-	-
D1	TDI	-	-

1. If a sysHSI Block is used, the indicated sysHSI reserved pins are unavailable for general purpose I/O use.

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
AJ18	BK3_IO14	-	100P	BK3_IO14	-	70P
-	-	-	-	GND (Bank 3)	-	-
AK18	BK3_IO15	-	100N	BK3_IO15	-	70N
AE18	BK3_IO16	-	101P	BK3_IO16	-	71P
AD18	BK3_IO17	-	101N	BK3_IO17	-	71N
AJ19	BK3_IO18	-	102P	BK3_IO18	-	72P
-	GND (Bank 3)	-	-	-	-	-
AK19	BK3_IO19	-	102N	BK3_IO19	-	72N
AH19	BK3_IO20	-	103P	NC	-	-
AG19	BK3_IO21	-	103N	NC	-	-
AK20	BK3_IO22	-	104P	NC	-	-
AJ20	BK3_IO23	-	104N	NC	-	-
AF19	BK3_IO24	-	105P	NC	-	-
AE19	BK3_IO25	-	105N	NC	-	-
AH20	BK3_IO26	-	106P	NC	-	-
-	GND (Bank 3)	-	-	-	-	-
AG20	BK3_IO27	-	106N	NC	-	-
AF20	BK3_IO28	-	107P	NC	-	-
AE20	BK3_IO29	-	107N	NC	-	-
AJ21	BK3_IO30	-	108P	NC	-	-
AK21	BK3_IO31	-	108N	NC	-	-
AG21	BK3_IO32	-	109P	NC	-	-
AF21	BK3_IO33	-	109N	NC	-	-
AK22	BK3_IO34	-	110P	NC	-	-
-	GND (Bank 3)	-	-	-	-	-
AJ22	BK3_IO35	-	110N	NC	-	-
AE21	BK3_IO36	-	111P	NC	-	-
AD21	BK3_IO37	-	111N	NC	-	-
AG22	BK3_IO38	-	112P	NC	-	-
AF22	BK3_IO39	-	112N	NC	-	-
AG23	BK3_IO40	-	113P	BK3_IO22	-	74P
-	-	-	-	GND (Bank 3)	-	-
AH23	BK3_IO41	-	113N	BK3_IO23	-	74N
AJ23	BK3_IO42	-	114P	BK3_IO24	-	75P
-	GND (Bank 3)	-	-	-	-	-
AK23	BK3_IO43	-	114N	BK3_IO25	-	75N
AF23	BK3_IO44	-	115P	BK3_IO26	-	76P
AE23	BK3_IO45	-	115N	BK3_IO27	-	76N
AJ24	BK3_IO46	-	116P	BK3_IO28	-	77P
AK24	BK3_IO47	-	116N	BK3_IO29	-	77N
AH24	BK3_IO48	-	117P	BK3_IO21	-	73N
AG24	BK3_IO49	VREF3	117N	BK3_IO20	VREF3	73P

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
AC27	BK4_IO21	-	134N/HSI5	NC	-	-
AD29	BK4_IO22	HSI6A_SINP	135P/HSI5	NC	-	-
AD30	BK4_IO23	HSI6A_SINN	135N/HSI5	NC	-	-
AB24	BK4_IO24	-	136P/HSI5	NC	-	-
AB25	BK4_IO25	-	136N/HSI5	NC	-	-
AC29	BK4_IO26	HSI6A_SOUTP	137P/HSI6	NC	-	-
-	GND (Bank 4)	-	-	-	-	-
AC30	BK4_IO27	HSI6A_SOUTN	137N/HSI6	NC	-	-
AB27	BK4_IO28	-	138P/HSI6	NC	-	-
AB26	BK4_IO29	-	138N/HSI6	NC	-	-
AB30	BK4_IO30	HSI6B_SINP	139P/HSI6	BK4_IO18	HSI3B_SINP	93P
-	-	-	-	GND (Bank 4)	-	-
AB29	BK4_IO31	HSI6B_SINN	139N/HSI6	BK4_IO19	HSI3B_SINN	93N
AA26	BK4_IO32	-	140P/HSI6	NC	-	-
AA27	BK4_IO33	-	140N/HSI6	NC	-	-
AA30	BK4_IO34	HSI6B_SOUTP	141P/HSI6	BK4_IO22	HSI3B_SOUTP	95P
-	GND (Bank 4)	-	-	-	-	-
AA29	BK4_IO35	HSI6B_SOUTN	141N/HSI6	BK4_IO23	HSI3B_SOUTN	95N
Y25	BK4_IO36	-	142P/HSI6	NC	-	-
Y26	BK4_IO37	-	142N/HSI6	NC	-	-
Y28	BK4_IO38	-	143P/HSI6	NC	-	-
Y27	BK4_IO39	-	143N/HSI6	NC	-	-
W25	BK4_IO40	-	144P/HSI6	NC	-	-
W26	BK4_IO41	-	144N/HSI6	NC	-	-
W27	BK4_IO42	-	145P	BK4_IO24	-	96P
-	GND (Bank 4)	-	-	-	-	-
W28	BK4_IO43	-	145N	BK4_IO25	-	96N
V24	BK4_IO44	-	146P	BK4_IO26	-	97P
-	-	-	-	GND (Bank 4)	-	-
V25	BK4_IO45	-	146N	BK4_IO27	-	97N
Y29	BK4_IO46	-	147P	BK4_IO32	-	100P
Y30	BK4_IO47	-	147N	BK4_IO33	-	100N
V27	BK4_IO48	PLL_RST4	148P	BK4_IO20	PLL_RST4	94P
V28	BK4_IO49	PLL_RST5	148N	BK4_IO21	PLL_RST5	94N
W29	BK4_IO50	-	149P	BK4_IO34	-	101P
-	GND (Bank 4)	-	-	GND (Bank 4)	-	-
W30	BK4_IO51	-	149N	BK4_IO35	-	101N
U25	BK4_IO52	-	150P	BK4_IO28	-	98P
U26	BK4_IO53	-	150N	BK4_IO29	-	98N
V29	BK4_IO54	SS_CLKIN1P	151P	BK4_IO30	SS_CLKIN1P	99P
V30	BK4_IO55	SS_CLKIN1N	151N	BK4_IO31	SS_CLKIN1N	99N
U28	BK4_IO56	PLL_FBK4	152P	BK4_IO36	PLL_FBK4	102P

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
F10	BK7_IO36	-	235P	NC	-	-
G10	BK7_IO37	-	235N	NC	-	-
A8	BK7_IO38	-	236P	NC	-	-
B8	BK7_IO39	-	236N	NC	-	-
D9	BK7_IO40	-	237P	BK7_IO22	-	158P
-	-	-	-	GND (Bank 7)	-	-
E9	BK7_IO41	-	237N	BK7_IO23	-	158N
A7	BK7_IO42	-	238P	BK7_IO24	-	159P
-	GND (Bank 7)	-	-		-	-
B7	BK7_IO43	-	238N	BK7_IO25	-	159N
C8	BK7_IO44	-	239P	BK7_IO26	-	160P
D8	BK7_IO45	-	239N	BK7_IO27	-	160N
A6	BK7_IO46	-	240P	BK7_IO21	-	157N
B6	BK7_IO47	VREF7	240N	BK7_IO20	VREF7	157P
E8	BK7_IO48	-	241P	BK7_IO28	-	161P
F8	BK7_IO49	-	241N	BK7_IO29	-	161N
C7	BK7_IO50	-	242P	BK7_IO30	-	162P
-	GND (Bank 7)	-	-	GND (Bank 7)	-	-
D7	BK7_IO51	-	242N	BK7_IO31	-	162N
E7	BK7_IO52	-	243P	BK7_IO32	-	163P
F7	BK7_IO53	-	243N	BK7_IO33	-	163N
A5	BK7_IO54	-	244P	BK7_IO34	-	164P
B5	BK7_IO55	-	244N	BK7_IO35	-	164N
C6	BK7_IO56	-	245P	BK7_IO36	-	165P
D6	BK7_IO57	-	245N	BK7_IO37	-	165N
D5	BK7_IO58	-	246P	BK7_IO38	-	166P
-	GND (Bank 7)	-	-	GND (Bank 7)	-	-
C5	BK7_IO59	-	246N	BK7_IO39	-	166N
B4	BK7_IO60	-	247P	BK7_IO40	-	167P
A4	BK7_IO61	-	247N	BK7_IO41	-	167N
A3	TDO	-	-	TDO	-	-
B3	VCCJ	-	-	VCCJ	-	-
C4	TDI	-	-	TDI	-	-

1. If a sysHSI Block is used, the indicated sysHSI reserved pins are unavailable for general purpose I/O use.