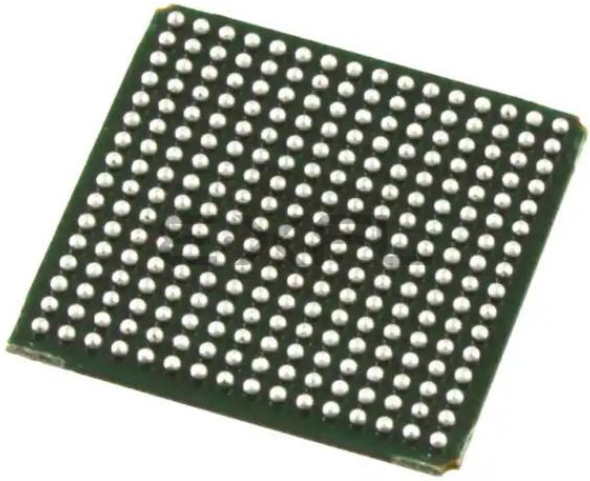
Lattice Semiconductor Corporation - LFX200EB-04F256C Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	2704
Total RAM Bits	113664
Number of I/O	160
Number of Gates	210000
Voltage - Supply	2.3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfx200eb-04f256c

Product Line	Ordering Part Number	Product Status	Reference PCN
LFX500EC (Cont'd)	LFX500EC-03F900C	**Discontinued**	PCN#09-10
	LFX500EC-03FN900C		
	LFX500EC-04F900C		
	LFX500EC-04FN900C		
	LFX500EC-03F900I		
	LFX500EC-03FN900I		
LFX1200EB	LFX1200EB-03FE680C	**Discontinued**	PCN#03A-10
	LFX1200EB-04FE680C		
	LFX1200EB-05FE680C		
	LFX1200EB-03FE680I		
	LFX1200EB-04FE680I		
	LFX1200EB-03F900C		
	LFX1200EB-04F900C		
	LFX1200EB-05F900C		
	LFX1200EB-03F900I		
	LFX1200EB-04F900I		
LFX1200EC	LFX1200EC-03FE680C	**Discontinued**	PCN#03A-10
	LFX1200EC-04FE680C		
	LFX1200EC-03FE680I		
	LFX1200EC-03F900C		
	LFX1200EC-04F900C		
	LFX1200EC-03F900I		

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Internet: http://www.latticesemi.com

Configurable Logic Element

The CLE is made up of a four-input Look-up Table (LUT-4), a Carry Chain Generator (CCG), and a two-input AND gate. The LUT-4 creates various combinatorial and memory elements, the CCG creates a single one-bit full adder, and the two-input AND gate can expand the CCG to incorporate Booth Multiplier capability by feeding the output of the AND gate to one of the inputs of the CCG.

Of the five inputs that feed each CLE, two are dedicated inputs into each LUT-4 and the remaining three take on varying functionality. The third and fourth inputs can be used as either inputs to the LUT-4 or as a Feed-Thru to the CSE via the WLG. The fifth input can be a data port when the LUT is configured as Distributed Memory, a select line for multiplexer operation, or a Feed-Thru directly to the CSE via the WLG (Figure 2).

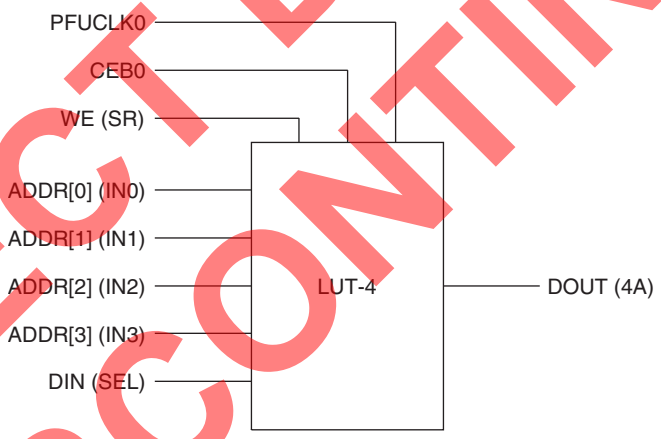
Look-Up Table – Combinatorial Mode

In combinatorial mode, the LUT-4 can implement any logic function up to four inputs. By using the carry chain and the WLG, each LUT-4 can be combined to form the enhanced functions listed in Table 3.

Look-Up Table – Distributed Memory Mode

In the distributed memory mode, the LUT functions as a memory element. The inputs to the LUT function as Address and Data. Each PFU is capable of implementing up to 64 SRAM bits. Both single and double port RAM can be performed in the PFU (Table 3). Furthermore, the distributed memory can be configured as either synchronous or asynchronous memory. Figure 3 illustrates the LUT while in distributed memory mode. When using any LUT in the PFU in memory mode, the Set/Reset signal will be used for Write Enable (WE(SR)) and the CLK0 signal will be used as the clock for synchronous read and write.

Figure 3. LUT in Distributed Memory Mode



Look-Up Table – Shift Register Mode

In the shift register mode, the LUT functions as a 1-bit to 8-bit shift register. This means that each PFU can implement up to four 8-bit shift registers or any cascaded combination. Figure 4 illustrates the LUT when configured in shift register mode.

sysIO Recommended Operating Conditions

Standard	V_{CCO} (V)[1]			V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVCMOS 3.3	3.0	3.3	3.6	-	-	-
LVCMOS 2.5	2.3	2.5	2.7	-	-	-
LVCMOS 1.8[2]	1.65	1.8	1.95	-	-	-
LVTTL	3.0	3.3	3.6	-	-	-
PCI 3.3	3.0	3.3	3.6	-	-	-
AGP-1X	3.15	3.3	3.45	-	-	-
SSTL 2	2.3	2.5	2.7	1.15	1.25	1.35
SSTL 3	3.0	3.3	3.6	1.3	1.5	1.7
CTT 3.3	3.0	3.3	3.6	1.35	1.5	1.65
CTT 2.5	2.3	2.5	2.7	1.35	1.5	1.65
HSTL Class I	1.4	1.5	1.6	0.68	0.75	0.9
HSTL Class III	1.4	1.5	1.6	-	0.9	-
GTL+	-	-	-	0.882	1.0	1.122
LVDS	2.3	2.5	2.7	-	-	-
LVPECL	3.0	3.3	3.6	-	-	-
BLVDS	2.3	2.5	2.7	-	-	-

1. Inputs independent of V_{CCO}.
2. Design tool default setting.

ispXPGA 200B/C & ispXPGA 200EB/EC External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description	Conditions	-5[1]		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{CO}	Global Clock Input to Output	PIO Output Register	—	5.5	—	5.9	—	6.8	ns
t_S	Global Clock Input Setup	PIO Input Register without input delay	-2.0	—	-2.0	—	-1.7	—	ns
t_H	Global Clock Input Hold	PIO Input Register without input delay	3.7	—	3.8	—	4.4	—	ns
t_{SINDLY}	Global Clock Input Setup	PIO Input Register with input delay	3.8	—	3.8	—	4.4	—	ns
t_{HINDLY}	Global Clock Input Hold	PIO Input Register with input delay	0.0	—	0.0	—	0.0	—	
t_{COPLL}	Global Clock Input to Output	PIO Output Register using PLL without delay	—	3.3	—	3.6	—	4.2	ns
t_{SPLL}	Global Clock Input Setup	PIO Input Register without input delay using PLL without delay	-0.2	—	-0.2	—	0.1	—	ns
t_{HPLL}	Global Clock Input Hold	PIO Input Register without input delay using PLL without delay	1.5	—	1.5	—	1.8	—	ns
$t_{SINDLYPLL}$	Global Clock Input Setup	PIO Input Register with input delay using PLL without delay	6.3	—	6.3	—	7.3	—	ns
$t_{HINDLYPLL}$	Global Clock Input Hold	PIO Input Register with input delay using PLL without delay	-2.7	—	-2.6	—	-2.2	—	ns

1. Only available for ispXPGA 200B and ispXPGA 200EB (2.5V/3.3V) devices.

Timing v.0.2

ispXPGA 200B/C & ispXPGA 200EB/EC Timing Adders

Parameter	Description	Base Parameter	-5[1]		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Optional Adders									
$t_{IOINDLY}$	Input Delay	—	—	4.84	—	5.2	—	5.98	ns
t_{IOI} Input Adjusters									
LVTTL_in	Using 3.3V TTL	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_18_in	Using 1.8V CMOS	t_{IOIN}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_25_in	Using 2.5V CMOS	t_{IOIN}	—	0.3	—	0.3	—	0.3	ns
LVCMOS_33_in	Using 3.3V CMOS	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
AGP_1X_in	Using AGP 1x	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
CTT25_in	Using CTT 2.5V	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
CTT33_in	Using CTT 3.3V	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
GTL+_in	Using GTL+	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
HSTL_I_in	Using HSTL 2.5V, Class I	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
HSTL_III_in	Using HSTL 2.5V, Class III	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
LVDS_in	Using Low Voltage Differential Signaling (LVDS)	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
BLVDS_in	Using Bus Low Voltage Differential Signaling (BLVDS)	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
LVPECL_in	Using Low Voltage PECL	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
PCI_in	Using PCI	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
SSTL2_I_in	Using SSTL 2.5V, Class I	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
SSTL2_II_in	Using SSTL 2.5V, Class II	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
SSTL3_I_in	Using SSTL 3.3V, Class I	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
SSTL3_II_in	Using SSTL 3.3V, Class II	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
t_{IOO} Output Adjusters									
Slow Slew	Using Slow Slew (LVTTL and LVCMOS Outputs only)	t_{IOBUF}, t_{IOEN}	—	0.7	—	0.7	—	0.7	ns
LVTTL_out	Using 3.3V TTL Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVCMOS_18_4mA_out	Using 1.8V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.8	—	0.8	—	0.8	ns
LVCMOS_18_5.33mA_out	Using 1.8V CMOS Standard, 5.33mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	—	0.6	ns
LVCMOS_18_8mA_out	Using 1.8V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_18_12mA_out	Using 1.8V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.2	—	0.2	—	0.2	ns
LVCMOS_25_4mA_out	Using 2.5V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.7	—	0.7	—	0.7	ns
LVCMOS_25_5.33mA_out	Using 2.5V CMOS Standard, 5.33 mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_8mA_out	Using 2.5V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_12mA_out	Using 2.5V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_16mA_out	Using 2.5V CMOS Standard, 16mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns

ispXPGA 500B/C & ispXPGA 500EB/EC PFU Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Functional Delays								
LUTs								
t_{LUT4}	4-Input LUT Delay	—	0.41	—	0.44	—	0.51	ns
t_{LUT5}	5-Input LUT Delay	—	0.73	—	0.79	—	0.91	ns
t_{LUT6}	6-Input LUT Delay	—	0.86	—	0.93	—	1.07	ns
Shift Register (LUT)								
t_{LSR_S}	Shift Register Setup Time	-0.64	—	-0.62	—	-0.53	—	ns
t_{LSR_H}	Shift Register Hold Time	0.61	—	0.63	—	0.72	—	ns
t_{LSR_CO}	Shift Register Clock to Output Delay	—	0.70	—	0.75	—	0.86	ns
Arithmetic Functions								
$t_{LCTHRUR}$	MC (Macro Cell) Carry In to MC Carry Out Delay (Ripple)	—	0.08	—	0.09	—	0.10	ns
$t_{LCTHRUL}$[2]	MC Carry In to MC Carry Out Delay (Look Ahead)	—	0.05	—	0.05	—	0.06	ns
t_{LSTHRU}	MC Sum In to MC Sum Out Delay	—	0.42	—	0.45	—	0.52	ns
$t_{LSINCOUT}$	MC Sum In to MC Carry Out Delay	—	0.29	—	0.31	—	0.36	ns
$t_{LCINSOUTR}$	MC Carry In to MC Sum Out Delay (Ripple)	—	0.36	—	0.39	—	0.45	ns
$t_{LCINSOUTL}$	MC Carry In to MC Sum Out Delay (Look Ahead)	—	0.26	—	0.28	—	0.32	ns
Feed-thru								
t_{LFT}	PFU Feed-Thru Delay	—	0.15	—	0.16	—	0.18	ns
Distributed RAM								
t_{LRAM_CO}	Clock to RAM Output	—	1.24	—	1.33	—	1.53	ns
t_{LRAMAD_S}	Address Setup Time	-0.41	—	-0.40	—	-0.34	—	ns
t_{LRAMD_S}	Data Setup Time	0.21	—	0.22	—	0.25	—	ns
t_{LRAMWE_S}	Write Enable Setup Time	0.45	—	0.46	—	0.53	—	ns
t_{LRAMAD_H}	Address Hold Time	0.58	—	0.60	—	0.69	—	ns
t_{LRAMD_H}	Data Hold Time	0.11	—	0.11	—	0.13	—	ns
t_{LRAMWE_H}	Write Enable Hold Time	0.12	—	0.12	—	0.14	—	ns
$t_{LRAMCPW}$	Clock Pulse Width (High or Low)	2.91	—	3.00	—	3.45	—	ns
$t_{LRAMADO}$	Address to Output Delay	—	0.86	—	0.93	—	1.07	ns
Register/Latch Delays								
Registers								
t_{L_CO}	Register Clock to Output Delay	—	0.58	—	0.62	—	0.71	ns
t_{L_S}	Register Setup Time (Data before Clock)	0.14	—	0.14	—	0.16	—	ns
t_{L_H}	Register Hold Time (Data after Clock)	-0.12	—	-0.12	—	-0.10	—	ns
t_{LCE_S}	Register Clock Enable Setup Time	-0.11	—	-0.11	—	-0.09	—	ns
t_{LCE_H}	Register Clock Enable Hold Time	0.11	—	0.11	—	0.13	—	ns
Latches								
t_{L_GO}	Latch Gate to Output Delay	—	0.09	—	0.10	—	0.12	ns
t_{LL_S}	Latch Setup Time	0.14	—	0.14	—	0.16	—	ns
t_{LL_H}	Latch Hold Time	-0.12	—	-0.12	—	-0.10	—	ns
t_{LLPD}	Latch Propagation Delay (Transparent Mode)	—	0.09	—	0.10	—	0.12	ns

ispXPGA 1200B/C & ispXPGA 1200EB/EC PFU Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Functional Delays								
LUTs								
t_{LUT4}	4-Input LUT Delay	—	0.41	—	0.44	—	0.51	ns
t_{LUT5}	5-Input LUT Delay	—	0.73	—	0.79	—	0.91	ns
t_{LUT6}	6-Input LUT Delay	—	0.86	—	0.93	—	1.07	ns
Shift Register (LUT)								
t_{LSR_S}	Shift Register Setup Time	-0.64	—	-0.62	—	-0.53	—	ns
t_{LSR_H}	Shift Register Hold Time	0.61	—	0.63	—	0.72	—	ns
t_{LSR_CO}	Shift Register Clock to Output Delay	—	0.70	—	0.75	—	0.86	ns
Arithmetic Functions								
$t_{LCTHRUR}$	MC (Macro Cell) Carry In to MC Carry Out Delay (Ripple)	—	0.08	—	0.09	—	0.10	ns
$t_{LCTHRUL}$[2]	MC Carry In to MC Carry Out Delay (Look Ahead)	—	0.05	—	0.05	—	0.06	ns
t_{LSTHRU}	MC Sum In to MC Sum Out Delay	—	0.42	—	0.45	—	0.52	ns
$t_{LSINCOUT}$	MC Sum In to MC Carry Out Delay	—	0.29	—	0.31	—	0.36	ns
$t_{LCINSOUTR}$	MC Carry In to MC Sum Out Delay (Ripple)	—	0.36	—	0.39	—	0.45	ns
$t_{LCINSOUTL}$	MC Carry In to MC Sum Out Delay (Look Ahead)	—	0.26	—	0.28	—	0.32	ns
Feed-thru								
t_{LFT}	PFU Feed-Thru Delay	—	0.15	—	0.16	—	0.18	ns
Distributed RAM								
t_{LRAM_CO}	Clock to RAM Output	—	1.24	—	1.33	—	1.53	ns
t_{LRAMAD_S}	Address Setup Time	-0.41	—	-0.40	—	-0.34	—	ns
t_{LRAMD_S}	Data Setup Time	0.21	—	0.22	—	0.25	—	ns
t_{LRAMWE_S}	Write Enable Setup Time	0.45	—	0.46	—	0.53	—	ns
t_{LRAMAD_H}	Address Hold Time	0.58	—	0.60	—	0.69	—	ns
t_{LRAMD_H}	Data Hold Time	0.11	—	0.11	—	0.13	—	ns
t_{LRAMWE_H}	Write Enable Hold Time	0.12	—	0.12	—	0.14	—	ns
$t_{LRAMCPW}$	Clock Pulse Width (High or Low)	2.91	—	3.00	—	3.45	—	ns
$t_{LRAMADO}$	Address to Output Delay	—	0.86	—	0.93	—	1.07	ns
Register/Latch Delays								
Registers								
t_{L_CO}	Register Clock to Output Delay	—	0.58	—	0.62	—	0.71	ns
t_{L_S}	Register Setup Time (Data before Clock)	0.14	—	0.14	—	0.16	—	ns
t_{L_H}	Register Hold Time (Data after Clock)	-0.12	—	-0.12	—	-0.10	—	ns
t_{LCE_S}	Register Clock Enable Setup Time	-0.11	—	-0.11	—	-0.09	—	ns
t_{LCE_H}	Register Clock Enable Hold Time	0.11	—	0.11	—	0.13	—	ns
Latches								
t_{L_GO}	Latch Gate to Output Delay	—	0.09	—	0.10	—	0.12	ns
t_{LL_S}	Latch Setup Time	0.14	—	0.14	—	0.16	—	ns
t_{LL_H}	Latch Hold Time	-0.12	—	-0.12	—	-0.10	—	ns
t_{LLPD}	Latch Propagation Delay (Transparent Mode)	—	0.09	—	0.10	—	0.12	ns

sysHSI Block AC Specifications

Operating Frequency Ranges

Symbol	Description	Mode	Test Condition	Device	-5[1]		-4		-3		Units
					Min.	Max.	Min.	Max.	Min.	Max.	
f_{CLK}	Reference Clock Frequency	SS:CAL		LFX125B/C	50	200	50	200	50	200	MHz
				LFX200B/C	50	188	50	188	50	188	
				LFX500B/C	50	188	50	188	50	188	
				LFX1200B/C	50	175	50	175	50	175	
		10B12B		LFX125B/C	33	67	33	67	33	67	MHz
				LFX200B/C	33	63	33	63	33	63	
				LFX500B/C	33	63	33	63	33	63	
				LFX1200B/C	33	58	33	58	33	58	
		8B10B		LFX125B/C	40	80	40	80	40	80	MHz
				LFX200B/C	40	75	40	75	40	75	
				LFX500B/C	40	75	40	75	40	75	
				LFX1200B/C	40	70	40	70	40	70	
f_{SIN}[2]	Serial Input	SS:CAL	with eoSIN	LFX125B/C	400	800	400	800	400	800	Mbps
				LFX200B/C	400	750	400	750	400	750	
				LFX500B/C	400	750	400	750	400	750	
				LFX1200B/C	400	700	400	700	400	700	
		10B12B	with eoSIN	LFX125B/C	400	800	400	800	400	800	Mbps
				LFX200B/C	400	750	400	750	400	750	
				LFX500B/C	400	750	400	750	400	750	
				LFX1200B/C	400	700	400	700	400	700	
		8B10B	with eoSIN	LFX125B/C	400	800	400	800	400	800	Mbps
				LFX200B/C	400	750	400	750	400	750	
				LFX500B/C	400	750	400	750	400	750	
				LFX1200B/C	400	700	400	700	400	700	
f_{OUT}[2]	Serial Out	LVDS	CL = 5 pF, RL = 100¾ f_{CLK} with no jitter	LFX125B/C	400	800	400	800	400	800	Mbps
				LFX200B/C	400	750	400	750	400	750	
				LFX500B/C	400	750	400	750	400	750	
				LFX1200B/C	400	700	400	700	400	700	

1. Only available for ispXPGA 125B, 200B, 500B and 1200B (2.5V/3.3V) devices.
2. f_{SIN} and f_{SOUT} speeds are supported at V_{CC} and V_{CCP} at 1.7V to 1.9V for ispXPGA 1.8V devices.

LOCKIN Time

Symbol	Description	Mode	Condition	Min	Max	Unit
t_{SCLOCK}	CSPLL Lock Time	All	After input is stabilized		25	µS
$t_{CDRLOCK}$	CDRPLL Lock-in Time	SS	With SS mode sync pattern		1024	t_{RCP}[1]
		10B12B	With 10B12B sync pattern		1024	t_{RCP}
		8B10B	With 8B10B idle pattern		960	t_{RCP}
t_{SYNC}	SyncPat Length	SS		1200		t_{RCP}
t_{CAL}	CAL Duration	SS		1100		t_{RCP}
t_{SUSYNC}	SyncPat Set-up Time to CAL	SS		50		t_{RCP}
t_{HDSYNC}	SyncPat Hold Time from CAL	SS		50		t_{RCP}

1. REFCLK clock period.

Signal Descriptions[1]

Signal Name	Signal Type	Description
General Purpose		
BK*y*_IO*x*[1,2]	Input/Output	General purpose I/O number x in I/O Bank y
GCLK*n*/I*n*[7]	Input	Global clock/input[8]
GSR	Input	Global Set/Reset
NC	—	No Connect
GND	GND	Ground
V_{CC}	VCC	Core logic power supply
V_{CCJ}	VCC	IEEE 1149.1 TAP power supply
V_{CCOy}[2]	VCC	I/O Bank y power supply
V_{REFy}[2]	Input	I/O Bank y reference voltage
D_{XN}, D_{XP}	Output	Temperature Sensing Diodes, provide a differential voltage, which corresponds to the temperature of the device.
Test and Program/Configuration		
TMS	Input	Test Mode Select
TCK	Input	Test Clock
TDI	Input	Test Data In
TDO	Output	Test Data Out
TOE	Input	Test Output Enable tri-states all I/O pins when driven low
CFG0	Input	Selects the SRAM memory configuration type (Peripheral or E^2CMOS Refresh)
PROGRAMb	Input	Initiates download from E^2CMOS or the peripheral port to SRAM memory (active low)
DONE	Bi-directional	Indicates when configuration is complete
INITb	Bi-directional	Indicates the device is ready for programming (active low)
READ	Input	Selects the READ operation when in sysCONFIG mode
CCLK	Input	sysCONFIG Configuration Clock
CSb	Input	sysCONFIG Chip Select (active low)
DATA[0:7]	Bi-directional	sysCONFIG Peripheral Port Data I/O
sysCLOCK PLL[3]		
PLL_FBK*z*	Input	Optional external feedback
PLL_RST*z*	Input	Optional external M divider reset
CLK_OUT*z*	Internal Signal	Clock output (routable to any I/O)
PLL_LOCK*z*	Internal Signal	Lock output (routable to any I/O)
GND_{P0}	GND	Left side PLL Ground
GND_{P1}	GND	Right side PLL Ground
V_{CCP0}	VCC	Left side PLL power supply
V_{CCP1}	VCC	Right side PLL power supply
sysHSI Block[4, 5]		
HSI*m*A_SINP, HSI*m*B_SINP	Input	P-side of differential serial data input
HSI*m*A_SINN, HSI*m*B_SINN	Input	N-side of differential serial data input
HSI*m*A_SOUTP, HSI*m*B_SOUTP	Output	P-side of differential serial data output
HSI*m*A_SOUTN, HSI*m*B_SOUTN	Output	N-side of differential serial data output
HSI*m*A_SYDT, HSI*m*B_SYDT	Internal Signal	Symbol alignment detect
HSI*m*A_RECCLK, HSI*m*B_RECCLK	Internal Signal	Recovered clock

ispXPGA Power Supply and NC Connections[1] (Continued)

Signal	680-Ball fpBGA[3]	900-Ball fpBGA[3]
NC[2]	A3, B29, AW3, AV3, AW11, AV11, AV29, AW29, AW37, B3, AV37, C39, C38, AU39, AU38, AJ39, AJ38, N38, N39, C2, C1, AU1, AU2, AJ2, AJ1, N2, N1, B11, A11, A37, B37, A29	**LFX500:** A8, A9, A10, A11, A19, A20, A21, A22, B8, B9, B10, B11, B19, B20, B21, B22, C1, C2, C11, C12, C19, C20, C23, D3, D10, D11, D12, D19, D20, D21, D22, D23, E3, E5, E6, E10, E11, E12, E21, E22, E25, E26, E28, E29, E30, F1, F2, F6, F9, F10, F11, F12, F21, F22, F25, F26, F29, F30, G1, G2, G3, G4, G7, G8, G9, G10, G11, G12, G14, G15, G16, G17, G19, G20, G21, G22, G23, G24, G25, G26, G27, G28, G29, G30, H1, H2, H3, H4, H5, H6, H7, H8, H9, H10, H11, H12, H13, H14, H15, H16, H17, H18, H19, H20, H21, H22, H23, H24, H27, H28, H29, H30, J1, J2, J4, J5, J6, J7, J8, J9, J10, J11, J12, J13, J14, J15, J16, J17, J18, J19, J20, J21, J22, J23, J24, J25, J26, J27, K6, K7, K8, K9, K10, K12, K13, K14, K15, K16, K17, K18, K19, K21, K22, K23, K24, K25, L7, L8, L9, L22, L23, L24, M7, M8, M9, M10, M21, M22, M23, M24, N8, N9, N10, N21, N22, N23, P7, P8, P9, P10, P21, P22, P23, P24, R8, R9, R10, R21, R22, R23, R24, R25, T6, T7, T8, T9, T10, T21, T22, T23, T24, T25, U7, U8, U9, U10, U21, U22, U23, U24, V8, V9, V10, V21, V22, V23, W7, W8, W9, W10, W21, W22, W23, W24, W25, W26, Y3, Y4, Y5, Y6, Y7, Y8, Y9, Y22, Y23, Y24, Y25, Y26, Y27, Y28, AA4, AA5, AA6, AA7, AA8, AA9, AA10, AA12, AA13, AA14, AA15, AA16, AA17, AA18, AA19, AA21, AA22, AA23, AA24, AA25, AA26, AA27, AB1, AB2, AB4, AB5, AB6, AB7, AB8, AB9, AB10, AB11, AB12, AB13, AB14, AB15, AB16, AB17, AB18, AB19, AB20, AB21, AB22, AB23, AB24, AB25, AB26, AB27, AC1, AC2, AC3, AC4, AC5, AC6, AC7, AC8, AC9, AC10, AC11, AC12, AC13, AC14, AC15, AC16, AC17' AC18' AC19, AC20, AC21, AC22, AC23, AC24, AC27, AC28, AC29, AC30, AD1, AD2, AD7, AD8, AD9, AD10, AD11, AD12, AD14, AD15, AD16, AD17, AD19, AD20, AD21, AD22, AD23, AD24, AD29, AD30, AE6, AE9, AE10, AE11, AE12, AE19, AE20, AE21, AE22, AE25, AE29, AE30, AF5, AF6, AF10, AF11, AF12, AF19, AF20, AF21, AF22, AF25, AF26, AG10, AG11, AG12, AG19, AG20, AG21, AG22, AH11, AH12, AH19, AH20, AJ8, AJ9, AJ10, AJ11, AJ20, AJ21, AJ22, AK8, AK9, AK10, AK11, AK20, AK21, AK22 **LFX1200:** AA22, AA23, AA24, AA25, AB23, AC24, T21, T22, T23, T24, T25, U21, U22, U23, U24, V21, V22, V23, W21, W22, W23, W24, Y22, Y23, Y24, AA16, AA17, AA18, AA19, AA21, AB16, AB17, AB18, AB19, AB20, AB21, AB22, AC16, AC17, AC18, AC19, AC20, AC21, AC22, AC23, AD16, AD17, AD19, AD20, AD22, AD23, AD24, AE22, AE25, AF25, AF26, AA10, AA12, AA13, AA14, AA15, AB10, AB11, AB12, AB13, AB14, AB15, AB9, AC10, AC11, AC12, AC13, AC14, AC15, AC8, AC9, AD11, AD12, AD14, AD15, AD7, AD8, AD9, AE6, AE9, AF5, AF6, H24, J23, K22, K23, K24, K25, L22, L23, L24, M21, M22, M23, M24, N21, N22, N23, P21, P22, P23, P24, R21, R22, R23, R24, R25, AA6, AA7, AA8, AA9, AB8, AC7, T10, T6, T7, T8, T9, U10, U7, U8, U9, V10, V8, V9, W10, W7, W8, W9, Y7, Y8, Y9, H5, H6, H7, J8, K6, K7, K8, K9, L7, L8, L9, M10, M7, M8, M9, N10, N8, N9, P10, P7, P8, P9, R10, R8, R9, E25, E26, F22, F25, G16, G17, G19, G20, G22, G23, G24, H16, H17, H18, H19, H20, H21, H22, H23, J16, J17, J18, J19, J20, J21, J22, K16, K17, K18, K19, K21, E5, E6, F6, F9, G11, G12, G14, G15, G7, G8, G9, H10, H11, H12, H13, H14, H15, H8, H9, J10, J11, J12, J13, J14, J15, J9, K10, K12, K13, K14, K15

1. All grounds must be electrically connected at the board level.
2. NC pins should not be connected to any active signals, V_{CC} or GND.
3. Balls for GND, V_{CC} and V_{CCOx} are connected within the substrate to their respective common signals. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.

ispXPGA Logic Signal Connections: 256-Ball fpBGA (Cont.)

256-fpBGA Ball	LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[2]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[2]
-	GND (Bank 1)	-	-	-	-	-
L3	BK1_IO7	SS_CLKIN0N	16N	BK1_IO7	SS_CLKIN0N	14N
K2	BK1_IO8	-	17P	BK1_IO8	-	15P
-	-	-	-	GND (Bank 1)	-	-
L2	BK1_IO9	-	17N	BK1_IO9	-	15N
M1	BK1_IO10	HSI1A_SOUTP	18P/HSI1	BK1_IO10	-	16P
N1	BK1_IO11	HSI1A_SOUTN	18N/HSI1	BK1_IO11	-	16N
M3	BK1_IO12	PLL_RST2	19P/HSI1	BK1_IO12	PLL_RST2	17P
M4	BK1_IO13	PLL_RST3	19N/HSI1	BK1_IO13	PLL_RST3	17N
-	GND (Bank 1)	-	-	-	-	-
M2	BK1_IO16[1]	VREF1	-	BK1_IO14[1]	VREF1	-
P1	BK1_IO18	HSI1B_SOUTP	22P/HSI1	BK1_IO16	-	19P
-	-	-	-	GND (Bank 1)	-	-
R1	BK1_IO19	HSI1B_SOUTN	22N/HSI1	BK1_IO17	-	19N
N3	BK1_IO20[1]	-	-	BK1_IO18[1]	-	-
N2	BK1_IO22	HSI1B_SINP	24P/HSI1	BK1_IO20	-	21P
-	GND (Bank 1)	-	-	-	-	-
P2	BK1_IO23	HSI1B_SINN	24N/HSI1	BK1_IO21	-	21N
P4	TCK	-	-	TCK	-	-
T2	TMS	-	-	TMS	-	-
T3	TOE	-	-	TOE	-	-
R3	BK2_IO0	-	26P	BK2_IO0	-	22P
R4	BK2_IO1	-	26N	BK2_IO1	-	22N
N5	BK2_IO2	-	27P	BK2_IO2	-	23P
-	GND (Bank 2)	-	-	-	-	-
P5	BK2_IO3	-	27N	BK2_IO3	-	23N
-	-	-	-	GND (Bank 2)	-	-
T4	BK2_IO6	-	29P	BK2_IO6	-	25P
T5	BK2_IO7	-	29N	BK2_IO7	-	25N
N6	BK2_IO8	-	30P	BK2_IO8	-	26P
P6	BK2_IO9	VREF2	30N	BK2_IO9	VREF2	26N
R5	BK2_IO10	-	31P	BK2_IO10	-	27P
-	GND (Bank 2)	-	-	-	-	-
R6	BK2_IO11	-	31N	BK2_IO11	-	27N
N7	BK2_IO12	-	32P	BK2_IO12	-	28P
-	-	-	-	GND (Bank 2)	-	-
P7	BK2_IO13	-	32N	BK2_IO13	-	28N
T6	BK2_IO14	-	33P	BK2_IO14	-	29P
T7	BK2_IO15	-	33N	BK2_IO15	-	29N
M8	BK2_IO16	-	34P	BK2_IO16	-	30P
M9	BK2_IO17	-	34N	BK2_IO17	-	30N
R7	BK2_IO18	-	35P	BK2_IO18	-	31P

ispXPGA Logic Signal Connections: 256-Ball fpBGA (Cont.)

256-fpBGA Ball	LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[2]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[2]
M15	BK4_IO5	-	54N/HSI2	BK4_IO5	-	46N
M14	BK4_IO8	-	56P/HSI2	BK4_IO6	-	47P
M13	BK4_IO9	VREF4	56N/HSI2	BK4_IO7	VREF4	47N
-	GND (Bank 4)	-	-	-	-	-
L13	BK4_IO12	PLL_RST4	58P/HSI2	BK4_IO8	PLL_RST4	48P
L14	BK4_IO13	PLL_RST5	58N/HSI2	BK4_IO9	PLL_RST5	48N
N16	BK4_IO14	HSI2B_SOUTP	59P/HSI2	BK4_IO10	-	49P
M16	BK4_IO15	HSI2B_SOUTN	59N/HSI2	BK4_IO11	-	49N
-	-	-	-	GND (Bank 4)	-	-
L15	BK4_IO18	SS_CLKIN1P	61P	BK4_IO14	SS_CLKIN1P	51P
-	GND (Bank 4)	-	-	-	-	-
K15	BK4_IO19	SS_CLKIN1N	61N	BK4_IO15	SS_CLKIN1N	51N
K14	BK4_IO20	PLL_FBK4	62P	BK4_IO16	PLL_FBK4	52P
K13	BK4_IO21	PLL_FBK5	62N	BK4_IO17	PLL_FBK5	52N
L16	BK4_IO22	SS_CLKOUT1P	63P	BK4_IO18	SS_CLKOUT1P	53P
-	-	-	-	GND (Bank 4)	-	-
K16	BK4_IO23	SS_CLKOUT1N	63N	BK4_IO19	SS_CLKOUT1N	53N
J13	BK4_IO24	CLK_OUT4	64P	BK4_IO20	CLK_OUT4	54P
J12	BK4_IO25	CLK_OUT5	64N	BK4_IO21	CLK_OUT5	54N
-	GND (Bank 4)	-	-	-	-	-
J14	GCLK4	-	LVDS Pair2P	GCLK4	-	LVDS Pair2P
H14	GCLK5	-	LVDS Pair2N	GCLK5	-	LVDS Pair2N
J15	VCCP1	-	-	VCCP1	-	-
H15	GNDP1	-	-	GNDP1	-	-
J16	GCLK6	-	LVDS Pair3P	GCLK6	-	LVDS Pair3P
H16	GCLK7	-	LVDS Pair3N	GCLK7	-	LVDS Pair3N
-	GND (Bank 5)	-	-	-	-	-
H12	BK5_IO0	CLK_OUT6	65P	BK5_IO0	CLK_OUT6	55P
H13	BK5_IO1	CLK_OUT7	65N	BK5_IO1	CLK_OUT7	55N
G14	BK5_IO2	-	66P	BK5_IO2	-	56P
-	-	-	-	GND (Bank 5)	-	-
G15	BK5_IO3	PLL_RST7	66N	BK5_IO3	PLL_RST7	56N
G13	BK5_IO6	PLL_RST6	68P	BK5_IO6	PLL_RST6	58P/HSI1
-	GND (Bank 5)	-	-	-	-	-
F13	BK5_IO7	PLL_FBK7	68N	BK5_IO7	PLL_FBK7	58N/HSI1
G16	BK5_IO10	HSI3A_SINP	70P	BK5_IO8	HSI1A_SINP	59P/HSI1
-	-	-	-	GND (Bank 5)	-	-
F16	BK5_IO11	HSI3A_SINN	70N/HSI3	BK5_IO9	HSI1A-SINN	59N/HSI1
F14	BK5_IO12	-	71P/HSI3	BK5_IO10	-	60P/HSI1
F15	BK5_IO13	-	71N/HSI3	BK5_IO11	-	60N/HSI1
E16	BK5_IO14	HSI3A_SOUTP	72P/HSI3	BK5_IO12	HSI1A_SOUTP	61P/HSI1
-	GND (Bank 5)	-	-	-	-	-

ispXPGA Logic Signal Connections: 256-Ball fpBGA (Cont.)

256-fpBGA Ball	LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[2]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[2]
C8	BK7_IO1	-	91N	BK7_IO1	-	77N
B8	BK7_IO2	-	92P	BK7_IO2	-	78P
B7	BK7_IO3	-	92N	BK7_IO3	-	78N
A9	BK7_IO6	-	94P	BK7_IO4	-	79P
-	GND (Bank 7)	-	-	-	-	-
A8	BK7_IO7	-	94N	BK7_IO5	-	79N
C7	BK7_IO10	-	96P	BK7_IO6	-	80P
D7	BK7_IO11	-	96N	BK7_IO7	-	80N
D6	BK7_IO12	-	97P	BK7_IO8	-	81P
-	-	-	-	GND (Bank 7)	-	-
C6	BK7_IO13	-	97N	BK7_IO9	-	81N
B6	BK7_IO14	-	98P	BK7_IO10	-	82P
-	GND (Bank 7)	-	-	-	-	-
B5	BK7_IO15	-	98N	BK7_IO11	-	82N
A7	BK7_IO16	VREF7	99P	BK7_IO12	VREF7	83P
A6	BK7_IO17	-	99N	BK7_IO13	-	83N
D5	BK7_IO18	-	100P	BK7_IO14	-	84P
C5	BK7_IO19	-	100N	BK7_IO15	-	84N
A5	BK7_IO20	-	101P	BK7_IO16	-	85P
-	-	-	-	GND (Bank 7)	-	-
A4	BK7_IO21	-	101N	BK7_IO17	-	85N
B4	BK7_IO22	-	102P	BK7_IO18	-	86P
-	GND (Bank 7)	-	-	-	-	-
B3	BK7_IO23	-	102N	BK7_IO19	-	86N
A3	TDO	-	-	TDO	-	-
A2	VCCJ	-	-	VCCJ	-	-
C4	TDI	-	-	TDI	-	-

1. Not available for differential pairs.
2. If a sysHSI Block is used, the indicated sysHSI reserved pins are unavailable for general purpose I/O use.

ispXPGA Logic Signal Connections: 516-Ball fpBGA (Cont.)

516-Ball BGA Ball	LFX500			LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
J29	BK5_IO22	HSI4B_SOUTP	116P/HSI4	NC	-	-	NC	-	-
-	GND (Bank 5)	-	-	-	-	-	-	-	-
H29	BK5_IO23	HSI4B_SOUTN	116N/HSI4	NC	-	-	NC	-	-
F30	BK5_IO24	-	117P/HSI5	NC	-	-	NC	-	-
G29	BK5_IO25	-	117N/HSI5	NC	-	-	NC	-	-
H28	BK5_IO26	HSI5A_SINP	118P/HSI5	NC	-	-	NC	-	-
H27	BK5_IO27	HSI5A_SINN	118N/HSI5	NC	-	-	NC	-	-
E30	BK5_IO28	-	119P/HSI5	NC	-	-	NC	-	-
F29	BK5_IO29	-	119N/HSI5	NC	-	-	NC	-	-
G28	BK5_IO30	HSI5A_SOUTP	120P/HSI5	NC	-	-	NC	-	-
-	GND (Bank 5)	-	-	-	-	-	-	-	-
G27	BK5_IO31	HSI5A_SOUTN	120N/HSI5	NC	-	-	NC	-	-
E29	BK5_IO32	VREF5	121P/HSI5	BK5_IO16	VREF5	73P/HSI3	BK5_IO14	VREF5	62P/HSI1
F28	BK5_IO33	-	121N/HSI5	BK5_IO17	-	73N/HSI3	BK5_IO15	-	62N/HSI1
D30	BK5_IO34	HSI5B_SINP	122P/HSI5	BK5_IO18	HSI3B_SINP	74P/HSI3	BK5_IO16	HSI1B_SINP	63P/HSI1
-	-	-	-	-	-	-	GND (Bank 5)	-	-
C30	BK5_IO35	HSI5B_SINN	122N/HSI5	BK5_IO19	HSI3B_SINN	74N/HSI3	BK5_IO17	HSI1B_SINN	63N/HSI1
D29	BK5_IO36	-	123P/HSI5	BK5_IO20		75P/HSI3	NC	-	-
D28	BK5_IO37	-	123N/HSI5	BK5_IO21		75N/HSI3	NC	-	-
E28	BK5_IO38	HSI5B_SOUTP	124P/HSI5	BK5_IO22	HSI3B_SOUTP	76P/HSI3	BK5_IO20	HSI1B_SOUTP	65P/HSI1
-	GND (Bank 5)	-	-	GND (Bank 5)	-	-	-	-	-
E27	BK5_IO39	HSI5B_SOUTN	124N/HSI5	BK5_IO23	HSI3B_SOUTN	76N/HSI3	BK5_IO21	HSI1B_SOUTN	65N/HSI1
C29	BK5_IO40	-	125P	BK5_IO24	-	77P/HSI3	BK5_IO18	-	64P/HSI1
B30	BK5_IO41	-	125N	BK5_IO25	-	77N/HSI3	BK5_IO19	-	64N/HSI1
A29	CFG0	-	-	CFG0	-	-	CFG0	-	-
B28	DONE	-	-	DONE	-	-	DONE	-	-
A28	PROGRAMb	-	-	PROGRAMb	-	-	PROGRAMb	-	-
D26	BK6_IO0	INITb	126P	BK6_IO0	INITb	78P	BK6_IO0	INITb	66P
C27	BK6_IO1	CCLK	126N	BK6_IO1	CCLK	78N	BK6_IO1	CCLK	66N
B27	BK6_IO2	-	127P	BK6_IO2	-	79P	BK6_IO2	-	67P
-	GND (Bank 6)	-	-	GND (Bank 6)	-	-	-	-	-
A27	BK6_IO3	-	127N	BK6_IO3	-	79N	BK6_IO3	-	67N
C26	BK6_IO4	CSb	128P	BK6_IO4	CSb	80P	BK6_IO4	CSb	68P
-	-	-	-	-	-	-	GND (Bank 6)	-	-
B26	BK6_IO5	Read	128N	BK6_IO5	Read	80N	BK6_IO5	Read	68N
A26	BK6_IO6	-	129P	NC	-	-	NC	-	-
C25	BK6_IO7	-	129N	NC	-	-	NC	-	-
D24	BK6_IO8	-	130P	NC	-	-	NC	-	-
B25	BK6_IO9	-	130N	NC	-	-	NC	-	-
A25	BK6_IO10	-	131P	NC	-	-	NC	-	-
-	GND (Bank 6)	-	-	-	-	-	-	-	-
C24	BK6_IO11	-	131N	NC	-	-	NC	-	-
D23	BK6_IO12	-	132P	NC	-	-	NC	-	-
B24	BK6_IO13	-	132N	NC	-	-	NC	-	-
C23	BK6_IO14	-	133P	NC	-	-	NC	-	-
A24	BK6_IO15	-	133N	NC	-	-	NC	-	-
C22	BK6_IO16	-	134P	NC	-	-	NC	-	-
B23	BK6_IO17	-	134N	NC	-	-	NC	-	-
B22	BK6_IO18	DATA7	135P	BK6_IO6	DATA7	81P	BK6_IO6	DATA7	69P
-	GND (Bank 6)	-	-	-	-	-	-	-	-
A23	BK6_IO19	DATA6	135N	BK6_IO7	DATA6	81N	BK6_IO7	DATA6	69N

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	Signal Name	Second Function	LVDS Pair/sysHSI Reserved[1]
AW35	BK4_IO4	-	126P
AV35	BK4_IO5	-	126N
AV34	BK4_IO6	HSI5A_SINP	127P
AU34	BK4_IO7	HSI5A_SINN	127N
AT34	BK4_IO8	-	128P
AU35	BK4_IO9	-	128N
AT33	BK4_IO10	HSI5A_SOUTP	129P/HSI5
-	GND (Bank 4)	-	-
AU33	BK4_IO11	HSI5A_SOUTN	129N/HSI5
AW34	BK4_IO12	VREF4	130P/HSI5
AV33	BK4_IO13	-	130N/HSI5
AR32	BK4_IO14	HSI5B_SINP	131P/HSI5
AT32	BK4_IO15	HSI5B_SINN	131N/HSI5
AU32	BK4_IO16	-	132P/HSI5
AW33	BK4_IO17	-	132N/HSI5
AV32	BK4_IO18	HSI5B_SOUTP	133P/HSI5
-	GND (Bank 4)	-	-
AV31	BK4_IO19	HSI5B_SOUTN	133N/HSI5
AU31	BK4_IO20	-	134P/HSI5
AW32	BK4_IO21	-	134N/HSI5
AR30	BK4_IO22	HSI6A_SINP	135P/HSI5
AT31	BK4_IO23	HSI6A_SINN	135N/HSI5
AW31	BK4_IO24	-	136P/HSI5
AV30	BK4_IO25	-	136N/HSI5
AT30	BK4_IO26	HSI6A_SOUTP	137P/HSI6
-	GND (Bank 4)	-	-
AT29	BK4_IO27	HSI6A_SOUTN	137N/HSI6
AW30	BK4_IO28	-	138P/HSI6
AU29	BK4_IO29	-	138N/HSI6
AT28	BK4_IO30	HSI6B_SINP	139P/HSI6
AU28	BK4_IO31	HSI6B_SINN	139N/HSI6
AV28	BK4_IO32	-	140P/HSI6
AT27	BK4_IO33	-	140N/HSI6
AU27	BK4_IO34	HSI6B_SOUTP	141P/HSI6
-	GND (Bank 4)	-	-
AV27	BK4_IO35	HSI6B_SOUTN	141N/HSI6
AW28	BK4_IO36	-	142P/HSI6
AR26	BK4_IO37	-	142N/HSI6
AW27	BK4_IO38	-	143P/HSI6
AT26	BK4_IO39	-	143N/HSI6
AV26	BK4_IO40	-	144P/HSI6
AR24	BK4_IO41	-	144N/HSI6
AT25	BK4_IO42	-	145P/HSI6

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
-	-	-	-	GND (Bank 1)	-	-
T1	BK1_IO1	CLK_OUT3	31N	BK1_IO1	CLK_OUT3	21N
U2	BK1_IO2	SS_CLKOUT0P	32P	BK1_IO2	SS_CLKOUT0P	22P
-	GND (Bank 1)	-	-	-	-	-
U1	BK1_IO3	SS_CLKOUT0N	32N	BK1_IO3	SS_CLKOUT0N	22N
U3	BK1_IO4	PLL_FBK2	33P	BK1_IO4	PLL_FBK2	23P
U4	BK1_IO5	PLL_FBK3	33N	BK1_IO5	PLL_FBK3	23N
V1	BK1_IO6	SS_CLKIN0P	34P	BK1_IO10	SS_CLKIN0P	26P
V2	BK1_IO7	SS_CLKIN0N	34N	BK1_IO11	SS_CLKIN0N	26N
U5	BK1_IO8	-	35P	BK1_IO12	-	27P
U6	BK1_IO9	-	35N	BK1_IO13	-	27N
V4	BK1_IO10	-	36P	BK1_IO6	-	24P
-	GND (Bank 1)	-	-	GND (Bank 1)	-	-
V3	BK1_IO11	-	36N	BK1_IO7	-	24N
V6	BK1_IO12	PLL_RST2	37P	BK1_IO20	PLL_RST2	31P
V7	BK1_IO13	PLL_RST3	37N	BK1_IO21	PLL_RST3	31N
W1	BK1_IO14	-	38P	BK1_IO8	-	25P
W2	BK1_IO15	-	38N	BK1_IO9	-	25N
W3	BK1_IO16	-	39P	BK1_IO14	-	28P
-	-	-	-	GND (Bank 1)	-	-
W4	BK1_IO17	-	39N	BK1_IO15	-	28N
W5	BK1_IO18	-	40P	BK1_IO16	-	29P
-	GND (Bank 1)	-	-	-	-	-
W6	BK1_IO19	-	40N	BK1_IO17	-	29N
Y6	BK1_IO20	-	41P/HSI3	NC	-	-
Y5	BK1_IO21	-	41N/HSI3	NC	-	-
Y4	BK1_IO22	-	42P/HSI3	NC	-	-
Y3	BK1_IO23	-	42N/HSI3	NC	-	-
AA5	BK1_IO24	-	43P/HSI3	NC	-	-
AA4	BK1_IO25	-	43N/HSI3	NC	-	-
Y2	BK1_IO26	HSI3A_SOUTP	44P/HSI3	BK1_IO18	HSI2A_SOUTP	30P
-	GND (Bank 1)	-	-	-	-	-
Y1	BK1_IO27	HSI3A_SOUTN	44N/HSI3	BK1_IO19	HSI2A_SOUTN	30N
AB7	BK1_IO28	-	45P/HSI3	NC	-	-
AB6	BK1_IO29	-	45N/HSI3	NC	-	-
AA2	BK1_IO30	HSI3A_SINP	46P/HSI3	BK1_IO22	HSI2A_SINP	32P
-	-	-	-	GND (Bank 1)	-	-
AA1	BK1_IO31	HSI3A_SINN	46N/HSI3	BK1_IO23	HSI2A_SINN	32N
AB5	BK1_IO32	-	47P/HSI3	NC	-	-
AB4	BK1_IO33	-	47N/HSI3	NC	-	-
AB2	BK1_IO34	HSI3B_SOUTP	48P/HSI3	NC	-	-
-	GND (Bank 1)	-	-	-	-	-

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
AJ12	BK2_IO43	-	83N	BK2_IO23	-	53N
AD13	BK2_IO44	-	84P	BK2_IO24	-	54P
AE13	BK2_IO45	-	84N	BK2_IO25	-	54N
AK13	BK2_IO46	-	85P	BK2_IO26	-	55P
-	-	-	-	GND (Bank 2)	-	-
AJ13	BK2_IO47	-	85N	BK2_IO27	-	55N
AG13	BK2_IO48	-	86P	BK2_IO28	-	56P
AH13	BK2_IO49	-	86N	BK2_IO29	-	56N
AE14	BK2_IO50	-	87P	BK2_IO30	-	57P
-	GND (Bank 2)	-	-	-	-	-
AF14	BK2_IO51	-	87N	BK2_IO31	-	57N
AG14	BK2_IO52	-	88P	BK2_IO32	-	58P
AH14	BK2_IO53	-	88N	BK2_IO33	-	58N
AJ14	BK2_IO54	-	89P	BK2_IO34	-	59P
-	-	-	-	GND (Bank 2)	-	-
AK14	BK2_IO55	-	89N	BK2_IO35	-	59N
AE15	BK2_IO56	-	90P	BK2_IO36	-	60P
AF15	BK2_IO57	-	90N	BK2_IO37	-	60N
AG15	BK2_IO58	-	91P	BK2_IO38	-	61P
-	GND (Bank 2)	-	-	-	-	-
AH15	BK2_IO59	-	91N	BK2_IO39	-	61N
AJ15	BK2_IO60	-	92P	BK2_IO40	-	62P
AK15	BK2_IO61	-	92N	BK2_IO41	-	62N
-	GND (Bank 2)	-	-	GND (Bank 2)	-	-
-	GND (Bank 3)	-	-	GND (Bank 3)	-	-
AK16	BK3_IO0	-	93P	BK3_IO0	-	63P
AJ16	BK3_IO1	-	93N	BK3_IO1	-	63N
AH16	BK3_IO2	-	94P	BK3_IO2	-	64P
-	GND (Bank 3)	-	-	-	-	-
AG16	BK3_IO3	-	94N	BK3_IO3	-	64N
AF16	BK3_IO4	-	95P	BK3_IO4	-	65P
AE16	BK3_IO5	-	95N	BK3_IO5	-	65N
AK17	BK3_IO6	-	96P	BK3_IO6	-	66P
-	-	-	-	GND (Bank 3)	-	-
AJ17	BK3_IO7	-	96N	BK3_IO7	-	66N
AH17	BK3_IO8	-	97P	BK3_IO8	-	67P
AG17	BK3_IO9	-	97N	BK3_IO9	-	67N
AF17	BK3_IO10	-	98P	BK3_IO10	-	68P
-	GND (Bank 3)	-	-	-	-	-
AE17	BK3_IO11	-	98N	BK3_IO11	-	68N
AH18	BK3_IO12	-	99P	BK3_IO12	-	69P
AG18	BK3_IO13	-	99N	BK3_IO13	-	69N

"E-Series" Commercial (Cont.)

Part Number	Gates	Voltage	Speed Grade	Package	Balls
LFX500EC-03F900C	476K	1.8	-3	fpBGA	900
LFX1200EB-05F900C[2]	1.25M	2.5/3.3	-5	fpBGA	900
LFX1200EB-04F900C[2]	1.25M	2.5/3.3	-4	fpBGA	900
LFX1200EB-03F900C[2]	1.25M	2.5/3.3	-3	fpBGA	900
LFX1200EC-04F900C[2]	1.25M	1.8	-4	fpBGA	900
LFX1200EC-03F900C[2]	1.25M	1.8	-3	fpBGA	900
LFX1200EB-05FE680C[2]	1.25M	2.5/3.3	-5	fpSBGA	680
LFX1200EB-04FE680C[2]	1.25M	2.5/3.3	-4	fpSBGA	680
LFX1200EB-03FE680C[2]	1.25M	2.5/3.3	-3	fpSBGA	680
LFX1200EC-04FE680C[2]	1.25M	1.8	-4	fpSBGA	680
LFX1200EC-03FE680C[2]	1.25M	1.8	-3	fpSBGA	680

1. FH516 package was converted to F516 via PCN #09A-08.
2. Discontinued via PCN #03A-10.

"E-Series" Industrial

Part Number	Gates	Voltage	Speed Grade	Package	Balls
LFX125EB-04F256I	139K	2.5/3.3	-4	fpBGA	256
LFX125EB-03F256I	139K	2.5/3.3	-3	fpBGA	256
LFX125EC-03F256I	139K	1.8	-3	fpBGA	256
LFX125EB-04F516I	139K	2.5/3.3	-4	fpBGA	516
LFX125EB-03F516I	139K	2.5/3.3	-3	fpBGA	516
LFX125EC-03F516I	139K	1.8	-3	fpBGA	516
LFX125EB-04FH516I[1]	139K	2.5/3.3	-4	fpBGA	516
LFX125EB-03FH516I[1]	139K	2.5/3.3	-3	fpBGA	516
LFX125EC-03FH516I[1]	139K	1.8	-3	fpBGA	516
LFX200EB-04F256I	210K	2.5/3.3	-4	fpBGA	256
LFX200EB-03F256I	210K	2.5/3.3	-3	fpBGA	256
LFX200EC-03F256I	210K	1.8	-3	fpBGA	256
LFX200EB-04F516I	210K	2.5/3.3	-4	fpBGA	516
LFX200EB-03F516I	210K	2.5/3.3	-3	fpBGA	516
LFX200EC-03F516I	210K	1.8	-3	fpBGA	516
LFX200EB-04FH516I[1]	210K	2.5/3.3	-4	fpBGA	516
LFX200EB-03FH516I[1]	210K	2.5/3.3	-3	fpBGA	516
LFX200EC-03FH516I[1]	210K	1.8	-3	fpBGA	516
LFX500EB-04F516I	476K	2.5/3.3	-4	fpBGA	516
LFX500EB-03F516I	476K	2.5/3.3	-3	fpBGA	516
LFX500EC-03F516I	476K	1.8	-3	fpBGA	516
LFX500EB-04FH516I[1]	476K	2.5/3.3	-4	fpBGA	516
LFX500EB-03FH516I[1]	476K	2.5/3.3	-3	fpBGA	516
LFX500EC-03FH516I[1]	476K	1.8	-3	fpBGA	516
LFX500EB-04F900I	476K	2.5/3.3	-4	fpBGA	900
LFX500EB-03F900I	476K	2.5/3.3	-3	fpBGA	900
LFX500EC-03F900I	476K	1.8	-3	fpBGA	900

"E-Series" Commercial (Cont.)

Part Number	Gates	Voltage	Speed Grade	Package	Balls
LFX500EC-04FN900C	476K	1.8	-4	Lead-Free fpBGA	900
LFX500EC-03FN900C	476K	1.8	-3	Lead-Free fpBGA	900

"E-Series" Industrial

Part Number	Gates	Voltage	Speed Grade	Package	Balls
LFX125EB-04FN256I	139K	2.5/3.3	-4	Lead-Free fpBGA	256
LFX125EB-03FN256I	139K	2.5/3.3	-3	Lead-Free fpBGA	256
LFX125EC-03FN256I	139K	1.8	-3	Lead-Free fpBGA	256
LFX200EB-04FN256I	210K	2.5/3.3	-4	Lead-Free fpBGA	256
LFX200EB-03FN256I	210K	2.5/3.3	-3	Lead-Free fpBGA	256
LFX200EC-03FN256I	210K	1.8	-3	Lead-Free fpBGA	256
LFX500EB-04FN900I	476K	2.5/3.3	-4	Lead-Free fpBGA	900
LFX500EB-03FN900I	476K	2.5/3.3	-3	Lead-Free fpBGA	900
LFX500EC-03FN900I	476K	1.8	-3	Lead-Free fpBGA	900

For Further Information

In addition to this data sheet, the following Lattice technical notes may be helpful when designing with the ispXPGA Family:

- TN1028, ispXPGA Memory Usage Guidelines
- TN1003, sysCLOCK PLL Usage and Design Guidelines
- TN1000, sysIO Usage Guidelines for Lattice Devices
- TN1026, ispXP Configuration Usage Guidelines
- TN1020, sysHSI Usage Guidelines
- TN1043, Power Estimation in ispXPGA Devices

Revision History

Date	Version	Change Summary
—	—	Previous Lattice releases.
September 2003	07	Improved typical Icc data for LFX125B/C and LFX500B/C.
		Improved external switching characteristics timing numbers for LFX125B/C.
		Improved PIC timing numbers for LFX125B/C.
		Improved $t_{IOINDLY}$ timing numbers for LFX125B/C.
		Improved external switching characteristics timing numbers for LFX500B/C.
		Improved PIC timing numbers for LFX500B/C.
		Improved $t_{IOINDLY}$ timing numbers for LFX500B/C.
		Enhanced CDR functionality description.
		Logic Signal Connections and Signal Descriptions - removed CDRLOCK, LOSS and EXLOSS descriptions.
January 2004	07.1	Added lead-free package designators.
June 2004	08.0	Updated CDR specifications and reference notes. Removed Source Synchronous (SS:No CAL) mode references for the sysHSI blocks.
		Revised Figures 16 and 24 for clarification.
		Clarification of VCC sysHSI Block for 1.8V devices.
		Updated IIL and IIH max specification.
		Updated LVTTL and PCI 3.3 to support 5V tolerance.

Revision History (Cont.)

Date	Version	Change Summary
June 2004 (cont.)	08.0 (cont.)	Updated Global Clock Input Setup time specifications.
		Clarification of Serial Out LVDS test condition.
		Clarification of REFCLK, SS_CLKIN peak-to-peak period jitter condition.
		Added sysHSI Reserved pins and footnote.
		Removed industrial ordering part numbers.
July 2004	09.0	Added “E” Series product family.
August 2004	10.0	Final release.
December 2004	10.1	Updated NC Connections table.
April 2005	10.2	Clarification of IDK specification.
April 2005	11.0	Select lead-free packages release.
July 2005	12.0	Added lead-free 516 fpBGA ordering part numbers.
April 2007	13.0	Removed lead-free 680 fpSBGA information from Part Number Description and Ordering Part Number tables. Removed lead-free 516 fpBGA for LFX125 from Ordering Part Number tables.
November 2007	14.0	Removed lead-free 516 fpBGA information from Part Number Description and Ordering Part Number tables.
July 2008	14.1	Added 516 fpBGA package without heat spreader to Part Number Description and Ordering Part Number tables.
February 2010	15.0	Ordering part numbers and ispXPGA Family Selection Guide table have been updated per PCN #03A-10 (discontinuation of the ispXPGA 1200 devices).
		References to "system gates" changed to "functional gates."