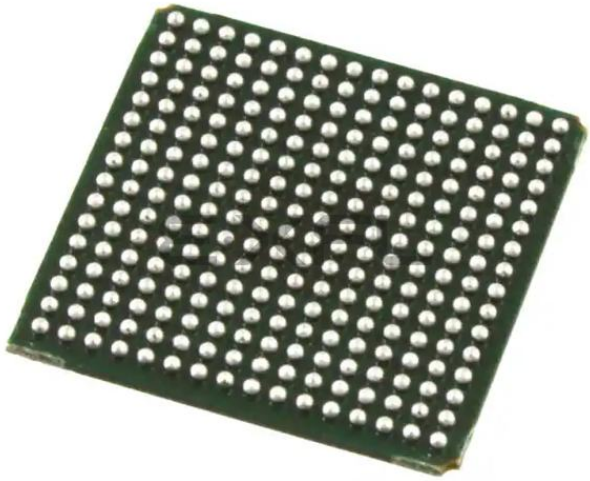

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	2704
Total RAM Bits	113664
Number of I/O	160
Number of Gates	210000
Voltage - Supply	2.3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 105°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfx200eb-04f256i

Product Line	Ordering Part Number	Product Status	Reference PCN
LFX500B	LFX500B-03F516C	**Discontinued**	PCN#09-10
	LFX500B-04F516C		
	LFX500B-05F516C		
	LFX500B-03F900C		
	LFX500B-03FN900C		
	LFX500B-04F900C		
	LFX500B-04FN900C		
	LFX500B-05F900C		
	LFX500B-05FN900C		
LFX500C	LFX500C-03F516C	**Discontinued**	PCN#09-10
	LFX500C-04F516C		
	LFX500C-03F900C		
	LFX500C-03FN900C		
	LFX500C-04F900C		
	LFX500C-04FN900C		
LFX1200B	LFX1200B-03FE680C	**Discontinued**	PCN#03A-10
	LFX1200B-04FE680C		
	LFX1200B-05FE680C		
	LFX1200B-03F900C		
	LFX1200B-04F900C		
	LFX1200B-05F900C		
LFX1200C	LFX1200C-03FE680C	**Discontinued**	PCN#03A-10
	LFX1200C-04FE680C		
	LFX1200C-03F900C		
	LFX1200C-04F900C		
LFX125EB	LFX125EB-03F256C	Active / Orderable	
	LFX125EB-03FN256C		
	LFX125EB-04F256C		
	LFX125EB-04FN256C		
	LFX125EB-05F256C		
	LFX125EB-05FN256C		
	LFX125EB-03F256I		
	LFX125EB-03FN256I		
	LFX125EB-04F256I		
	LFX125EB-04FN256I		
	LFX125EB-03F516C	**Discontinued**	PCN#09-10
	LFX125EB-04F516C		
	LFX125EB-05F516C		
	LFX125EB-03F516I		
	LFX125EB-04F516I		
LFX125EC	LFX125EC-03F256C	**Discontinued**	PCN#09-10
	LFX125EC-03FN256C		
	LFX125EC-04F256C		
	LFX125EC-04FN256C		
	LFX125EC-03F256I		
	LFX125EC-03FN256I		

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Product Line	Ordering Part Number	Product Status	Reference PCN
LFX125EC (Cont'd)	LFX125EC-03F516C	**Discontinued**	PCN#09-10
	LFX125EC-04F516C		
	LFX125EC-03F516I		
LFX200EB	LFX200EB-03F256C	Active / Orderable	
	LFX200EB-03FN256C		
	LFX200EB-04F256C		
	LFX200EB-04FN256C		
	LFX200EB-05F256C		
	LFX200EB-05FN256C		
	LFX200EB-03F256I		
	LFX200EB-03FN256I		
	LFX200EB-04F256I		
	LFX200EB-04FN256I		
	LFX200EB-03F516C	**Discontinued**	PCN#09-10
	LFX200EB-04F516C		
	LFX200EB-05F516C		
	LFX200EB-03F516I		
	LFX200EB-04F516I		
LFX200EC	LFX200EC-03F256C	**Discontinued**	PCN#09-10
	LFX200EC-03FN256C		
	LFX200EC-04F256C		
	LFX200EC-04FN256C		
	LFX200EC-03F256I		
	LFX200EC-03FN256I		
	LFX200EC-03F516C		
	LFX200EC-04F516C		
	LFX200EC-03F516I		
LFX500EB	LFX500EB-03F516C	**Discontinued**	PCN#09-10
	LFX500EB-04F516C		
	LFX500EB-05F516C		
	LFX500EB-03F516I		
	LFX500EB-04F516I		
	LFX500EB-03F900C		
	LFX500EB-03FN900C		
	LFX500EB-04F900C		
	LFX500EB-04FN900C		
	LFX500EB-05F900C		
	LFX500EB-05FN900C		
	LFX500EB-03F900I		
	LFX500EB-03FN900I		
	LFX500EB-04F900I		
	LFX500EB-04FN900I		
LFX500EC	LFX500EC-03F516C	**Discontinued**	PCN#09-10
	LFX500EC-04F516C		
	LFX500EC-03F516I		

Product Line	Ordering Part Number	Product Status	Reference PCN
LFX500EC (Cont'd)	LFX500EC-03F900C	**Discontinued**	PCN#09-10
	LFX500EC-03FN900C		
	LFX500EC-04F900C		
	LFX500EC-04FN900C		
	LFX500EC-03F900I		
	LFX500EC-03FN900I		
LFX1200EB	LFX1200EB-03FE680C	**Discontinued**	PCN#03A-10
	LFX1200EB-04FE680C		
	LFX1200EB-05FE680C		
	LFX1200EB-03FE680I		
	LFX1200EB-04FE680I		
	LFX1200EB-03F900C		
	LFX1200EB-04F900C		
	LFX1200EB-05F900C		
	LFX1200EB-03F900I		
	LFX1200EB-04F900I		
LFX1200EC	LFX1200EC-03FE680C	**Discontinued**	PCN#03A-10
	LFX1200EC-04FE680C		
	LFX1200EC-03FE680I		
	LFX1200EC-03F900C		
	LFX1200EC-04F900C		
	LFX1200EC-03F900I		

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ispXPGA Family Overview

The ispXPGA family of devices provides the ideal vehicle for the creation of high-performance logic designs that are both non-volatile and infinitely re-programmable. Other FPGA solutions force a compromise, being either re-programmable or non-volatile. This family couples this capability with a mainstream architecture containing the features required for today's system-level design.

The ispXPGA family is available in two options. The standard device supports sysHSI capability for ultra fast serial communications while the lower-cost "E-Series" supports the same high-performance FPGA fabric without the sysHSI Block.

Electrically Erasable CMOS (E^2CMOS) memory cells provide the ispXPGA family with non-volatile capability. These allow logic to be functional microseconds after power is applied, allowing easy interfacing in many applications. This capability also means that expensive external configuration memories are not required and that designs can be secured from unauthorized read back. Internal SRAM cells allow the device to be infinitely reconfigured if desired. Both the SRAM and E^2CMOS cells can be programmed and verified through the IEEE 1532 industry standard. Additionally, the SRAM cells can be configured and read-back through the sysCONFIG™ peripheral port.

The family spans the density and I/O range required for the majority of today's logic designs, 139K to 1.25M functional gates and 160 to 496 I/O. The devices are available for operation from 1.8V, 2.5V, and 3.3V power supplies, providing easy integration into the overall system.

System-level design needs are met through the incorporation of sysMEM dual-port memory blocks, sysIO advanced I/O support, and sysCLOCK Phase Locked Loops (PLLs). High-speed serial communications are supported through multiple sysHSI blocks, which provide clock data recovery (CDR) and serialization/de-serialization (SERDES).

The ispLEVER™ design tool from Lattice allows easy implementation of designs using the ispXPGA product. Synthesis library support is available for major logic synthesis tools. The ispLEVER tool takes the output from these common synthesis packages and place and routes the design in the ispXPGA product. The tool supports floor planning and the management of other constraints within the device. The tool also provides outputs to common timing analysis tools for timing analysis.

To increase designer productivity, Lattice provides a variety of pre-designed modules referred to as IP cores for the ispXPGA product. These IP cores allow designers to concentrate on the unique portions of their design while using pre-designed blocks to implement standard functions such as bus interfaces, standard communication interfaces, and memory controllers.

Through the use of advanced technology and innovative architecture the ispXPGA FPGA devices provide designers with excellent speed performance. Although design dependent, many typical designs can run at over 150MHz. Certain designs can run at over 300MHz. Table 2 details the performance of several building blocks commonly used by logic designers.

Table 2. ispXPGA Speed Performance for Typical Building Blocks

Function	Performance
8:1 Asynch MUX	150 MHz
1:32 Asynch Demultiplexer	125 MHz
8 x 8 2-LL Pipelined Multiplier	225 MHz
32-bit Up/Down Counter	290 MHz
32-bit Shift Register	360 MHz

Configurable Logic Element

The CLE is made up of a four-input Look-up Table (LUT-4), a Carry Chain Generator (CCG), and a two-input AND gate. The LUT-4 creates various combinatorial and memory elements, the CCG creates a single one-bit full adder, and the two-input AND gate can expand the CCG to incorporate Booth Multiplier capability by feeding the output of the AND gate to one of the inputs of the CCG.

Of the five inputs that feed each CLE, two are dedicated inputs into each LUT-4 and the remaining three take on varying functionality. The third and fourth inputs can be used as either inputs to the LUT-4 or as a Feed-Thru to the CSE via the WLG. The fifth input can be a data port when the LUT is configured as Distributed Memory, a select line for multiplexer operation, or a Feed-Thru directly to the CSE via the WLG (Figure 2).

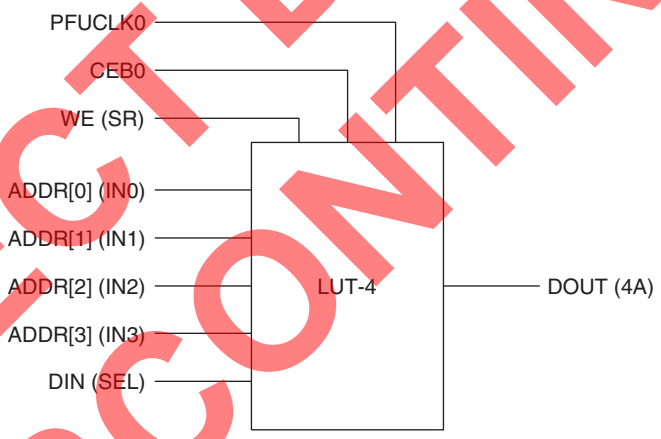
Look-Up Table – Combinatorial Mode

In combinatorial mode, the LUT-4 can implement any logic function up to four inputs. By using the carry chain and the WLG, each LUT-4 can be combined to form the enhanced functions listed in Table 3.

Look-Up Table – Distributed Memory Mode

In the distributed memory mode, the LUT functions as a memory element. The inputs to the LUT function as Address and Data. Each PFU is capable of implementing up to 64 SRAM bits. Both single and double port RAM can be performed in the PFU (Table 3). Furthermore, the distributed memory can be configured as either synchronous or asynchronous memory. Figure 3 illustrates the LUT while in distributed memory mode. When using any LUT in the PFU in memory mode, the Set/Reset signal will be used for Write Enable (WE(SR)) and the CLK0 signal will be used as the clock for synchronous read and write.

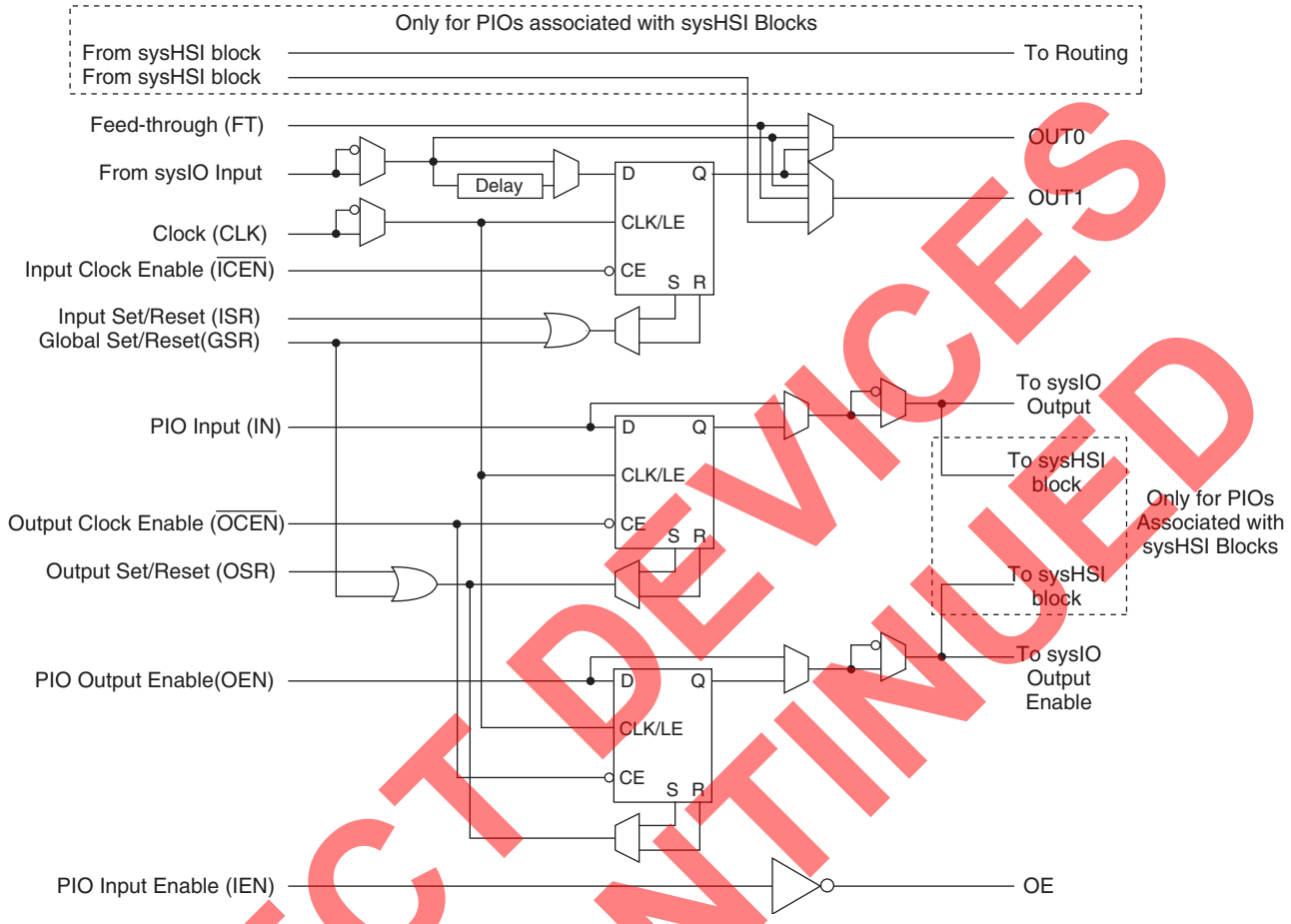
Figure 3. LUT in Distributed Memory Mode



Look-Up Table – Shift Register Mode

In the shift register mode, the LUT functions as a 1-bit to 8-bit shift register. This means that each PFU can implement up to four 8-bit shift registers or any cascaded combination. Figure 4 illustrates the LUT when configured in shift register mode.

Figure 11. ispXPGA PIO



VLI Routing Resources

The ispXPGA architecture contains a Variable-Length-Interconnect (VLI) routing technology connecting the PFUs, PICs, and EBRs in the device. There are four types of routing resources, Global Lines, Long Lines, General Interconnect, and Local Lines forming the global routing structure. This allows a signal to be routed to any element in the device with the optimal delay.

The Global Lines consist of global clock lines and a global set/reset line. These lines are routed to all elements in the device. They are specifically designed for high speed, predictable timing regardless of fan-out. The global clock lines can also be used as dedicated inputs.

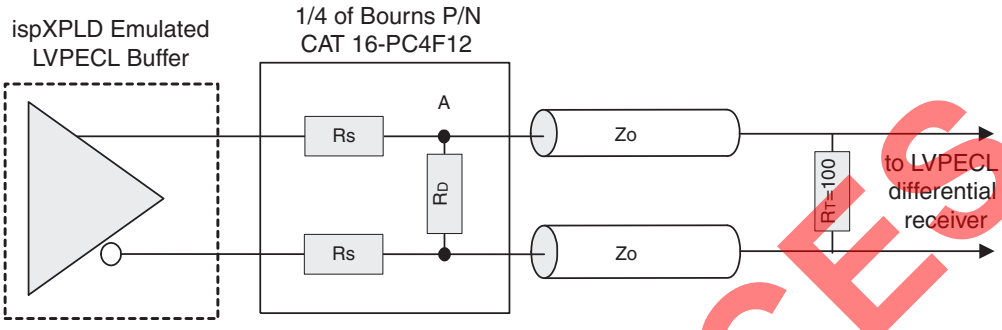
The Long Lines consist of Horizontal and Vertical Long Lines (HLL and VLL). The VLL and HLL are tri-statable lines spanning the entire device. These lines allow fast routing for high fan-out nets and general-purpose functions.

The General Interconnect consists of Double and Deca Lines. The Double Lines connect up to three elements (two plus the driving element), while the Deca Lines connect up to eleven elements (ten plus the driving element).

The Local Lines are extremely fast routing paths consisting of Feedback and Direct Connect Lines. The Feedback Lines are internal routing paths from the PFU outputs to the PFU inputs. The Direct Connect Lines connect all adjacent elements.

The Common Interface Block (CIB) provides the link between the logic element (PFU, PIC, or EBR) and the VLI Routing resources. The CIB is a switch matrix that can be programmed to connect virtually any routing resource to any input or output of the logic element.

Figure 23. LVPECL Driver with Three Resistor Pack



ispXPGA 125B/C & ispXPGA 125EB/EC External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description	Conditions	-5[1]		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{CO}	Global Clock Input to Output	PIO Output Register	—	5.3	—	5.7	—	6.6	ns
t_{S}	Global Clock Input Setup	PIO Input Register without input delay	-1.9	—	-1.8	—	-1.5	—	ns
t_{H}	Global Clock Input Hold	PIO Input Register without input delay	2.7	—	2.9	—	3.3	—	ns
t_{SINDLY}	Global Clock Input Setup	PIO Input Register with input delay	3.1	—	3.3	—	3.8	—	ns
t_{HINDLY}	Global Clock Input Hold	PIO Input Register with input delay	0.0	—	0.0	—	0.0	—	
t_{COPLL}	Global Clock Input to Output	PIO Output Register using PLL without delay	—	3.6	—	3.9	—	4.5	ns
t_{SPLL}	Global Clock Input Setup	PIO Input Register without input delay using PLL without delay	0	—	0.1	—	0.3	—	ns
t_{HPLL}	Global Clock Input Hold	PIO Input Register without input delay using PLL without delay	0.9	—	1.0	—	1.2	—	ns
$t_{SINDLYPLL}$	Global Clock Input Setup	PIO Input Register with input delay using PLL without delay	5.1	—	5.5	—	6.3	—	ns
$t_{HINDLYPLL}$	Global Clock Input Hold	PIO Input Register with input delay using PLL without delay	-3.0	—	-2.8	—	-2.4	—	ns

1. Only available for ispXPGA 125B and ispXPGA 125EB (2.5V/3.3V) devices.

Timing v.0.3

ispXPGA 125B/C & ispXPGA 125EB/EC PFU Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Reset/Set								
t_{LASSRO}	Asynchronous Set/Reset to Output	—	1.09	—	1.17	—	1.35	ns
$t_{LASSRPW}$	Asynchronous Set/Reset Pulse Width	4.19	—	4.50	—	5.18	—	ns
t_{LASSRR}	Asynchronous Set/Reset Recovery	—	0.51	—	0.55	—	0.63	ns
t_{LSSR_S}	Synchronous Set/Reset Setup Time	-0.03	—	-0.03	—	-0.03	—	ns
t_{LSSR_H}	Synchronous Set/Reset Hold Time	0.03	—	0.03	—	0.03	—	ns

1. Only available for ispXPGA 125B and ispXPGA 125EB (2.5V/3.3V) devices.
2. $t_{LCTHRUL}$ quoted bit by bit.

Timing v.0.3

ispXPGA 125B/C & ispXPGA 125EB/EC PIC Timing Parameters

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Register/Latch Delays								
t_{IO_CO}	Register Clock to Output Delay	—	0.89	—	0.96	—	1.10	ns
t_{IO_S}	Register Setup Time (Data before Clock)	0.05	—	0.05	—	0.06	—	ns
t_{IO_H}	Register Hold Time (Data after Clock)	0.06	—	0.06	—	0.07	—	ns
t_{IOCE_S}	Register Clock Enable Setup Time	-0.03	—	-0.03	—	-0.03	—	ns
t_{IOCE_H}	Register Clock Enable Hold Time	0.13	—	0.13	—	0.15	—	ns
t_{IO_GO}	Latch Gate to Output Delay	—	0.68	—	0.73	—	0.84	ns
t_{IOL_S}	Latch Setup Time	0.05	—	0.05	—	0.06	—	ns
t_{IOL_H}	Latch Hold Time	0.06	—	0.06	—	0.07	—	ns
t_{IOLPD}	Latch Propagation Delay (Transparent Mode)	—	0.09	—	0.10	—	0.12	ns
t_{IOASRO}	Asynchronous Set/Reset to Output	—	1.00	—	1.08	—	1.24	ns
$t_{IOASRPW}$	Asynchronous Set/Reset Pulse Width	4.19	—	4.50	—	5.18	—	ns
t_{IOASRR}	Asynchronous Set/Reset Recovery Time	—	0.23	—	0.25	—	0.29	ns
Input/Output Delays								
t_{IOBUF}	Output Buffer Delay	—	0.97	—	1.04	—	1.20	ns
t_{IOIN}	Input Buffer Delay	—	0.57	—	0.61	—	0.70	ns
t_{IOEN}	Output Enable Delay	—	0.53	—	0.57	—	0.66	ns
t_{IODIS}	Output Disable Delay	—	-0.14	—	-0.13	—	-0.11	ns
t_{IOFT}	Feed-thru Delay	—	0.19	—	0.20	—	0.23	ns

1. Only available for ispXPGA 125B and ispXPGA 125EB (2.5V/3.3V) devices.

Timing v.0.3

ispXPGA 500B/C & ispXPGA 500EB/EC PFU Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Functional Delays								
LUTs								
t_{LUT4}	4-Input LUT Delay	—	0.41	—	0.44	—	0.51	ns
t_{LUT5}	5-Input LUT Delay	—	0.73	—	0.79	—	0.91	ns
t_{LUT6}	6-Input LUT Delay	—	0.86	—	0.93	—	1.07	ns
Shift Register (LUT)								
t_{LSR_S}	Shift Register Setup Time	-0.64	—	-0.62	—	-0.53	—	ns
t_{LSR_H}	Shift Register Hold Time	0.61	—	0.63	—	0.72	—	ns
t_{LSR_CO}	Shift Register Clock to Output Delay	—	0.70	—	0.75	—	0.86	ns
Arithmetic Functions								
$t_{LCTHRUR}$	MC (Macro Cell) Carry In to MC Carry Out Delay (Ripple)	—	0.08	—	0.09	—	0.10	ns
$t_{LCTHRUL}$[2]	MC Carry In to MC Carry Out Delay (Look Ahead)	—	0.05	—	0.05	—	0.06	ns
t_{LSTHRU}	MC Sum In to MC Sum Out Delay	—	0.42	—	0.45	—	0.52	ns
$t_{LSINCOUT}$	MC Sum In to MC Carry Out Delay	—	0.29	—	0.31	—	0.36	ns
$t_{LCINSOUTR}$	MC Carry In to MC Sum Out Delay (Ripple)	—	0.36	—	0.39	—	0.45	ns
$t_{LCINSOUTL}$	MC Carry In to MC Sum Out Delay (Look Ahead)	—	0.26	—	0.28	—	0.32	ns
Feed-thru								
t_{LFT}	PFU Feed-Thru Delay	—	0.15	—	0.16	—	0.18	ns
Distributed RAM								
t_{LRAM_CO}	Clock to RAM Output	—	1.24	—	1.33	—	1.53	ns
t_{LRAMAD_S}	Address Setup Time	-0.41	—	-0.40	—	-0.34	—	ns
t_{LRAMD_S}	Data Setup Time	0.21	—	0.22	—	0.25	—	ns
t_{LRAMWE_S}	Write Enable Setup Time	0.45	—	0.46	—	0.53	—	ns
t_{LRAMAD_H}	Address Hold Time	0.58	—	0.60	—	0.69	—	ns
t_{LRAMD_H}	Data Hold Time	0.11	—	0.11	—	0.13	—	ns
t_{LRAMWE_H}	Write Enable Hold Time	0.12	—	0.12	—	0.14	—	ns
$t_{LRAMCPW}$	Clock Pulse Width (High or Low)	2.91	—	3.00	—	3.45	—	ns
$t_{LRAMADO}$	Address to Output Delay	—	0.86	—	0.93	—	1.07	ns
Register/Latch Delays								
Registers								
t_{L_CO}	Register Clock to Output Delay	—	0.58	—	0.62	—	0.71	ns
t_{L_S}	Register Setup Time (Data before Clock)	0.14	—	0.14	—	0.16	—	ns
t_{L_H}	Register Hold Time (Data after Clock)	-0.12	—	-0.12	—	-0.10	—	ns
t_{LCE_S}	Register Clock Enable Setup Time	-0.11	—	-0.11	—	-0.09	—	ns
t_{LCE_H}	Register Clock Enable Hold Time	0.11	—	0.11	—	0.13	—	ns
Latches								
t_{L_GO}	Latch Gate to Output Delay	—	0.09	—	0.10	—	0.12	ns
t_{LL_S}	Latch Setup Time	0.14	—	0.14	—	0.16	—	ns
t_{LL_H}	Latch Hold Time	-0.12	—	-0.12	—	-0.10	—	ns
t_{LLPD}	Latch Propagation Delay (Transparent Mode)	—	0.09	—	0.10	—	0.12	ns

sysCLOCK PLL Timing

Over Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Units
t_{PWH}	Input clock, high time	80% to 80%	1.2	—	ns
t_{PWL}	Input clock, low time	20% to 20%	1.2	—	ns
t_R, t_F	Input Clock, rise and fall time	20% to 80%	—	3.0	ns
t_{INSTB}	Input clock stability, cycle to cycle (peak)		—	+/- 250	ps
f_{MDIVIN}	M Divider input, frequency range		10	320	MHz
$f_{MDIVOUT}$	M Divider output, frequency range		10	320	MHz
f_{NDIVIN}	N Divider input, frequency range		10	320	MHz
$f_{NDIVOUT}$	N Divider output, frequency range		10	320	MHz
f_{VDIVIN}	V Divider input, frequency range		100	400	MHz
$f_{VDIVOUT}$	V Divider output, frequency range		10	320	MHz
$t_{OUTDUTY}$	output clock, duty cycle		40	60	%
$t_{JIT(CC)}$	Output clock, cycle to cycle jitter (peak)	Clean reference[1] 10MHz ð $f_{MDIVOUT}$ ð 40MHz or 100MHz ð f_{VDIVIN} ð 160MHz	—	+/- 600	ps
		Clean reference[1] 40MHz ð $f_{MDIVOUT}$ ð 320MHz and 160MHz ð f_{VDIVIN} ð 400MHz	—	+/- 150	ps
$t_{JIT(PER)}$[2]	Output clock, period jitter (peak)	Clean reference[1] 10MHz ð $f_{MDIVOUT}$ ð 40MHz or 100MHz ð f_{VDIVIN} ð 160MHz	—	+/- 600	ps
		Clean reference[1] 40MHz ð $f_{MDIVOUT}$ ð 320MHz and 160MHz ð f_{VDIVIN} ð 400MHz	—	+/- 150	ps
$t_{CLK\_OUT\_DELAY}$	Input clock to CLK_OUT delay	Internal feedback	—	3.0	ns
t_{PHASE}	Input clock to external feedback delta	External feedback	—	1.5	ns
t_{LOCK}	Time to acquire phase lock after input stable		—	25	us
t_{PLL_DELAY}	Delay increment (Lead/Lag)	Typical = +/- 250ps	+/- 120	+/- 550	ps
t_{RANGE}	Total output delay range (lead/lag)		+/- 0.84	+/- 3.85	ns
t_{PLL_RSTW}	Minimum reset pulse width		1.8	—	ns
t_{CLK_IN}[3]	Global clock input delay		—	1.0	ns
$t_{PLL\_SEC\_DELAY}$	Secondary PLL output delay		—	1.5	ns

1. This condition assures that the output phase jitter will remain within specifications. Jitter spec is based on optimized M, N and V settings determined by the ispLEVER software.
2. Accumulated jitter measured over 10,000 waveform samples
3. Internal timing for reference only.

ispXPGA Logic Signal Connections: 256-Ball fpBGA (Cont.)

256-fpBGA Ball	LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[2]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[2]
-	GND (Bank 2)	-	-	GND (Bank 2)	-	-
R8	BK2_IO19	-	35N	BK2_IO19	-	31N
N8	BK2_IO20	-	36P	BK2_IO20	-	32P
P8	BK2_IO21	-	36N	BK2_IO21	-	32N
-	GND (Bank 2)	-	-	-	-	-
-	GND (Bank 3)	-	-	-	-	-
T8	BK3_IO0	-	39P	BK3_IO0	-	33P
T9	BK3_IO1	-	39N	BK3_IO1	-	33N
R9	BK3_IO2	-	40P	BK3_IO2	-	34P
-	-	-	-	GND (Bank 3)	-	-
R10	BK3_IO3	-	40N	BK3_IO3	-	34N
P9	BK3_IO4	-	41P	BK3_IO4	-	35P
N9	BK3_IO5	-	41N	BK3_IO5	-	35N
T10	BK3_IO6	-	42P	BK3_IO6	-	36P
-	GND (Bank 3)	-	-	-	-	-
T11	BK3_IO7	-	42N	BK3_IO7	-	36N
P10	BK3_IO8	-	43P	BK3_IO8	-	37P
-	-	-	-	GND (Bank 3)	-	-
N10	BK3_IO9	-	43N	BK3_IO9	-	37N
R11	BK3_IO14	-	46P	BK3_IO10	-	38P
-	GND (Bank 3)	-	-	-	-	-
R12	BK3_IO15	-	46N	BK3_IO11	-	38N
P11	BK3_IO16	VREF3	47P	BK3_IO12	VREF3	39P
N11	BK3_IO17	-	47N	BK3_IO13	-	39N
T12	BK3_IO18	-	48P	BK3_IO14	-	40P
T13	BK3_IO19	-	48N	BK3_IO15	-	40N
R13	BK3_IO20	-	49P	BK3_IO16	-	41P
-	-	-	-	GND (Bank 3)	-	-
R14	BK3_IO21	-	49N	BK3_IO17	-	41N
P12	BK3_IO22	-	50P	BK3_IO18	-	42P
-	GND (Bank 3)	-	-	-	-	-
N12	BK3_IO23	-	50N	BK3_IO19	-	42N
T14	GSR	-	-	GSR	-	-
T15	DXP	-	-	DXP	-	-
P13	DXN	-	-	DXN	-	-
P15	BK4_IO0	-	52P/HSI2	BK4_IO0	-	44P
N14	BK4_IO1	-	52N/HSI2	BK4_IO1	-	44N
R16	BK4_IO2	HSI2A_SINP	53P/HSI2	BK4_IO2	-	45P
-	GND (Bank 4)	-	-	-	-	-
P16	BK4_IO3	HSI2A_SINN	53N/HSI2	BK4_IO3	-	45N
N15	BK4_IO4	-	54P/HSI2	BK4_IO4	-	46P
-	-	-	-	GND (Bank 4)	-	-

ispXPGA Logic Signal Connections: 516-Ball fpBGA (Cont.)

516-Ball BGA Ball	LFX500			LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
AA30	BK4_IO29	-	98N	BK4_IO17	-	60N	BK4_IO13	-	50N
W28	BK4_IO30	SS_CLKIN1P	99P	BK4_IO18	SS_CLKIN1P	61P	BK4_IO14	SS_CLKIN1P	51P
-	-	-	-	GND (Bank 4)	-	-	-	-	-
W29	BK4_IO31	SS_CLKIN1N	99N	BK4_IO19	SS_CLKIN1N	61N	BK4_IO15	SS_CLKIN1N	51N
Y30	BK4_IO32	-	100P	NC	-	-	NC	-	-
W30	BK4_IO33	-	100N	NC	-	-	NC	-	-
V27	BK4_IO34	-	101P	NC	-	-	NC	-	-
-	GND (Bank 4)	-	-	-	-	-	-	-	-
V28	BK4_IO35	-	101N	NC	-	-	NC	-	-
V29	BK4_IO36	PLL_FBK4	102P	BK4_IO20	PLL_FBK4	62P	BK4_IO16	PLL_FBK4	52P
V30	BK4_IO37	PLL_FBK5	102N	BK4_IO21	PLL_FBK5	62N	BK4_IO17	PLL_FBK5	52N
U30	BK4_IO38	SS_CLKOUT1P	103P	BK4_IO22	SS_CLKOUT1P	63P	BK4_IO18	SS_CLKOUT1P	53P
U29	BK4_IO39	SS_CLKOUT1N	103N	BK4_IO23	SS_CLKOUT1N	63N	BK4_IO19	SS_CLKOUT1N	53N
U28	BK4_IO40	CLK_OUT4	104P	BK4_IO24	CLK_OUT4	64P	BK4_IO20	CLK_OUT4	54P
-	GND (Bank 4)	-	-	-	-	-	-	-	-
T27	BK4_IO41	CLK_OUT5	104N	BK4_IO25	CLK_OUT5	64N	BK4_IO21	CLK_OUT5	54N
-	-	-	-	GND (Bank 4)	-	-	-	-	-
T28	GCLK4	-	LVDS Pair2P	GCLK4	-	LVDS Pair2P	GCLK4	-	LVDS Pair2P
T29	GCLK5	-	LVDS Pair2N	GCLK5	-	LVDS Pair2N	GCLK5	-	LVDS Pair2N
T30	VCCP1	-	-	VCCP1	-	-	VCCP1	-	-
R29	GNDP1	-	-	GNDP1	-	-	GNDP1	-	-
R28	GCLK6	-	LVDS Pair3P	GCLK6	-	LVDS Pair3P	GCLK6	-	LVDS Pair3P
R27	GCLK7	-	LVDS Pair3N	GCLK7	-	LVDS Pair3N	GCLK7	-	LVDS Pair3N
-	-	-	-	GND (Bank 5)	-	-	-	-	-
R30	BK5_IO0	CLK_OUT6	105P	BK5_IO0	CLK_OUT6	65P	BK5_IO0	CLK_OUT6	55P
-	GND (Bank 5)	-	-	-	-	-	-	-	-
P30	BK5_IO1	CLK_OUT7	105N	BK5_IO1	CLK_OUT7	65N	BK5_IO1	CLK_OUT7	55N
P29	BK5_IO2	-	106P	BK5_IO2	-	66P	BK5_IO2	-	56P
-	-	-	-	-	-	-	GND (Bank 5)	-	-
P28	BK5_IO3	PLL_RST7	106N	BK5_IO3	PLL_RST7	66N	BK5_IO3	PLL_RST7	56N
N30	BK5_IO4	PLL_FBK6	107P	BK5_IO4	PLL_FBK6	67P	BK5_IO4	PLL_FBK6	57P/HSI1
N29	BK5_IO5	-	107N	BK5_IO5	-	67N	BK5_IO5	-	57N/HSI1
N28	BK5_IO6	PLL-RST6	108P	BK5_IO6	PLL_RST6	68P	BK5_IO6	PLL_RST6	58P//HSI1
-	GND (Bank 5)	-	-	GND (Bank 5)	-	-	-	-	-
N27	BK5_IO7	PLL_FBK7	108N	BK5_IO7	PLL_FBK7	68N	BK5_IO7	PLL_FBK7	58N/HSI1
M30	BK5_IO8	-	109P/HSI4	BK5_IO8	-	69P	NC	-	-
M29	BK5_IO9	-	109N/HSI4	BK5_IO9	-	69N	NC	-	-
L30	BK5_IO10	HSI4A_SINP	110P/HSI4	BK5_IO10	HSI3A_SINP	70P/HSI3	BK5_IO8	HSI1A_SINP	59P/HSI1
-	-	-	-	-	-	-	GND (Bank 5)	-	-
L29	BK5_IO11	HSI4A_SINN	110N/HSI4	BK5_IO11	HSI3A_SINN	70N/HSI3	BK5_IO9	HSI1A_SINN	59N/HSI1
M28	BK5_IO12	-	111P/HSI4	BK5_IO12	-	71P/HSI3	BK5_IO10	-	60P/HSI1
L28	BK5_IO13	-	111N/HSI4	BK5_IO13		71N/HSI3	BK5_IO11	-	60N/HSI1
K30	BK5_IO14	HSI4A_SOUTP	112P/HSI4	BK5_IO14	HSI3A_SOUTP	72P/HSI3	BK5_IO12	HSI1A_SOUTP	61P/HSI1
-	GND (Bank 5)	-	-	GND (Bank 5)	-	-	-	-	-
K29	BK5_IO15	HSI4A_SOUTN	112N/HSI4	BK5_IO15	HSI3A_SOUTN	72N/HSI3	BK5_IO13	HSI1A_SOUTN	61N/HSI1
L27	BK5_IO16	-	113P/HSI4	NC	-	-	NC	-	-
K28	BK5_IO17	-	113N/HSI4	NC	-	-	NC	-	-
H30	BK5_IO18	HSI4B_SINP	114P/HSI4	NC	-	-	NC	-	-
G30	BK5_IO19	HSI4B_SINN	114N/HSI4	NC	-	-	NC	-	-
J28	BK5_IO20	-	115P/HSI4	NC	-	-	NC	-	-
K27	BK5_IO21	-	115N/HSI4	NC	-	-	NC	-	-

ispXPGA Logic Signal Connections: 516-Ball fpBGA (Cont.)

516-Ball BGA Ball	LFX500			LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
J29	BK5_IO22	HSI4B_SOUTP	116P/HSI4	NC	-	-	NC	-	-
-	GND (Bank 5)	-	-	-	-	-	-	-	-
H29	BK5_IO23	HSI4B_SOUTN	116N/HSI4	NC	-	-	NC	-	-
F30	BK5_IO24	-	117P/HSI5	NC	-	-	NC	-	-
G29	BK5_IO25	-	117N/HSI5	NC	-	-	NC	-	-
H28	BK5_IO26	HSI5A_SINP	118P/HSI5	NC	-	-	NC	-	-
H27	BK5_IO27	HSI5A_SINN	118N/HSI5	NC	-	-	NC	-	-
E30	BK5_IO28	-	119P/HSI5	NC	-	-	NC	-	-
F29	BK5_IO29	-	119N/HSI5	NC	-	-	NC	-	-
G28	BK5_IO30	HSI5A_SOUTP	120P/HSI5	NC	-	-	NC	-	-
-	GND (Bank 5)	-	-	-	-	-	-	-	-
G27	BK5_IO31	HSI5A_SOUTN	120N/HSI5	NC	-	-	NC	-	-
E29	BK5_IO32	VREF5	121P/HSI5	BK5_IO16	VREF5	73P/HSI3	BK5_IO14	VREF5	62P/HSI1
F28	BK5_IO33	-	121N/HSI5	BK5_IO17	-	73N/HSI3	BK5_IO15	-	62N/HSI1
D30	BK5_IO34	HSI5B_SINP	122P/HSI5	BK5_IO18	HSI3B_SINP	74P/HSI3	BK5_IO16	HSI1B_SINP	63P/HSI1
-	-	-	-	-	-	-	GND (Bank 5)	-	-
C30	BK5_IO35	HSI5B_SINN	122N/HSI5	BK5_IO19	HSI3B_SINN	74N/HSI3	BK5_IO17	HSI1B_SINN	63N/HSI1
D29	BK5_IO36	-	123P/HSI5	BK5_IO20		75P/HSI3	NC	-	-
D28	BK5_IO37	-	123N/HSI5	BK5_IO21		75N/HSI3	NC	-	-
E28	BK5_IO38	HSI5B_SOUTP	124P/HSI5	BK5_IO22	HSI3B_SOUTP	76P/HSI3	BK5_IO20	HSI1B_SOUTP	65P/HSI1
-	GND (Bank 5)	-	-	GND (Bank 5)	-	-	-	-	-
E27	BK5_IO39	HSI5B_SOUTN	124N/HSI5	BK5_IO23	HSI3B_SOUTN	76N/HSI3	BK5_IO21	HSI1B_SOUTN	65N/HSI1
C29	BK5_IO40	-	125P	BK5_IO24	-	77P/HSI3	BK5_IO18	-	64P/HSI1
B30	BK5_IO41	-	125N	BK5_IO25	-	77N/HSI3	BK5_IO19	-	64N/HSI1
A29	CFG0	-	-	CFG0	-	-	CFG0	-	-
B28	DONE	-	-	DONE	-	-	DONE	-	-
A28	PROGRAMb	-	-	PROGRAMb	-	-	PROGRAMb	-	-
D26	BK6_IO0	INITb	126P	BK6_IO0	INITb	78P	BK6_IO0	INITb	66P
C27	BK6_IO1	CCLK	126N	BK6_IO1	CCLK	78N	BK6_IO1	CCLK	66N
B27	BK6_IO2	-	127P	BK6_IO2	-	79P	BK6_IO2	-	67P
-	GND (Bank 6)	-	-	GND (Bank 6)	-	-	-	-	-
A27	BK6_IO3	-	127N	BK6_IO3	-	79N	BK6_IO3	-	67N
C26	BK6_IO4	CSb	128P	BK6_IO4	CSb	80P	BK6_IO4	CSb	68P
-	-	-	-	-	-	-	GND (Bank 6)	-	-
B26	BK6_IO5	Read	128N	BK6_IO5	Read	80N	BK6_IO5	Read	68N
A26	BK6_IO6	-	129P	NC	-	-	NC	-	-
C25	BK6_IO7	-	129N	NC	-	-	NC	-	-
D24	BK6_IO8	-	130P	NC	-	-	NC	-	-
B25	BK6_IO9	-	130N	NC	-	-	NC	-	-
A25	BK6_IO10	-	131P	NC	-	-	NC	-	-
-	GND (Bank 6)	-	-	-	-	-	-	-	-
C24	BK6_IO11	-	131N	NC	-	-	NC	-	-
D23	BK6_IO12	-	132P	NC	-	-	NC	-	-
B24	BK6_IO13	-	132N	NC	-	-	NC	-	-
C23	BK6_IO14	-	133P	NC	-	-	NC	-	-
A24	BK6_IO15	-	133N	NC	-	-	NC	-	-
C22	BK6_IO16	-	134P	NC	-	-	NC	-	-
B23	BK6_IO17	-	134N	NC	-	-	NC	-	-
B22	BK6_IO18	DATA7	135P	BK6_IO6	DATA7	81P	BK6_IO6	DATA7	69P
-	GND (Bank 6)	-	-	-	-	-	-	-	-
A23	BK6_IO19	DATA6	135N	BK6_IO7	DATA6	81N	BK6_IO7	DATA6	69N

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	Signal Name	Second Function	LVDS Pair/sysHSI Reserved[1]
AW35	BK4_IO4	-	126P
AV35	BK4_IO5	-	126N
AV34	BK4_IO6	HSI5A_SINP	127P
AU34	BK4_IO7	HSI5A_SINN	127N
AT34	BK4_IO8	-	128P
AU35	BK4_IO9	-	128N
AT33	BK4_IO10	HSI5A_SOUTP	129P/HSI5
-	GND (Bank 4)	-	-
AU33	BK4_IO11	HSI5A_SOUTN	129N/HSI5
AW34	BK4_IO12	VREF4	130P/HSI5
AV33	BK4_IO13	-	130N/HSI5
AR32	BK4_IO14	HSI5B_SINP	131P/HSI5
AT32	BK4_IO15	HSI5B_SINN	131N/HSI5
AU32	BK4_IO16	-	132P/HSI5
AW33	BK4_IO17	-	132N/HSI5
AV32	BK4_IO18	HSI5B_SOUTP	133P/HSI5
-	GND (Bank 4)	-	-
AV31	BK4_IO19	HSI5B_SOUTN	133N/HSI5
AU31	BK4_IO20	-	134P/HSI5
AW32	BK4_IO21	-	134N/HSI5
AR30	BK4_IO22	HSI6A_SINP	135P/HSI5
AT31	BK4_IO23	HSI6A_SINN	135N/HSI5
AW31	BK4_IO24	-	136P/HSI5
AV30	BK4_IO25	-	136N/HSI5
AT30	BK4_IO26	HSI6A_SOUTP	137P/HSI6
-	GND (Bank 4)	-	-
AT29	BK4_IO27	HSI6A_SOUTN	137N/HSI6
AW30	BK4_IO28	-	138P/HSI6
AU29	BK4_IO29	-	138N/HSI6
AT28	BK4_IO30	HSI6B_SINP	139P/HSI6
AU28	BK4_IO31	HSI6B_SINN	139N/HSI6
AV28	BK4_IO32	-	140P/HSI6
AT27	BK4_IO33	-	140N/HSI6
AU27	BK4_IO34	HSI6B_SOUTP	141P/HSI6
-	GND (Bank 4)	-	-
AV27	BK4_IO35	HSI6B_SOUTN	141N/HSI6
AW28	BK4_IO36	-	142P/HSI6
AR26	BK4_IO37	-	142N/HSI6
AW27	BK4_IO38	-	143P/HSI6
AT26	BK4_IO39	-	143N/HSI6
AV26	BK4_IO40	-	144P/HSI6
AR24	BK4_IO41	-	144N/HSI6
AT25	BK4_IO42	-	145P/HSI6

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	Signal Name	Second Function	LVDS Pair/sysHSI Reserved[1]
-	GND (Bank 4)	-	-
AW26	BK4_IO43	-	145N
AV25	BK4_IO44	-	146P
AT24	BK4_IO45	-	146N
AU24	BK4_IO46	-	147P
AU25	BK4_IO47	-	147N
AW25	BK4_IO48	PLL_RST4	148P
AW24	BK4_IO49	PLL_RST5	148N
AU23	BK4_IO50	-	149P
-	GND (Bank 4)	-	-
AT23	BK4_IO51	-	149N
AV24	BK4_IO52	-	150P
AW23	BK4_IO53	-	150N
AV23	BK4_IO54	SS_CLKIN1P	151P
AU22	BK4_IO55	SS_CLKIN1N	151N
AR21	BK4_IO56	PLL_FBK4	152P
AT22	BK4_IO57	PLL_FBK5	152N
AV22	BK4_IO58	SS_CLKOUT1P	153P
-	GND (Bank 4)	-	-
AV21	BK4_IO59	SS_CLKOUT1N	153N
AT21	BK4_IO60	CLK_OUT4	154P
AU21	BK4_IO61	CLK_OUT5	154N
-	GND (Bank 4)	-	-
AT19	GCLK4	-	LVDS Pair2P
AU19	GCLK5	-	LVDS Pair2N
AW22	VCCP1	-	-
AR20	GNDP1	-	-
AU18	GCLK6	-	LVDS Pair3P
AT18	GCLK7	-	LVDS Pair3N
-	GND (Bank 5)	-	-
AV17	BK5_IO0	CLK_OUT6	155P
AV18	BK5_IO1	CLK_OUT7	155N
AW21	BK5_IO2	PLL_FBK6	156P
-	GND (Bank 5)	-	-
AV19	BK5_IO3	PLL_FBK7	156N
AR19	BK5_IO4	-	157P/HSI7
AW19	BK5_IO5	-	157N/HSI7
AW18	BK5_IO6	PLL_RST6	158P/HSI7
AW17	BK5_IO7	PLL_RST7	158N/HSI7
AT17	BK5_IO8	-	159P/HSI7
AV16	BK5_IO9	-	159N/HSI7
AU17	BK5_IO10	HSI7A_SINP	160P/HSI7
-	GND (Bank 5)	-	-

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	**Signal Name**	**Second Function**	**LVDS Pair/sysHSI Reserved[1]**
AU6	BK5_IO50	HSI9B_SINP	180P/HSI9
-	GND (Bank 5)	-	-
AV6	BK5_IO51	HSI9B_SINN	180N/HSI9
AR8	BK5_IO52	-	181P
AT7	BK5_IO53	-	181N
AU5	BK5_IO54	HSI9B_SOUTP	182P
AV5	BK5_IO55	HSI9B_SOUTN	182N
AW5	BK5_IO56	-	183P
AW4	BK5_IO57	-	183N
AT6	BK5_IO58	-	184P
-	GND (Bank 5)	-	-
AV4	BK5_IO59	-	184N
AR6	BK5_IO60	-	185P
AU4	BK5_IO61	-	185N
AT1	CFG0	-	-
AT3	DONE	-	-
AT2	PROGRAMb	-	-
AP4	BK6_IO0	INITb	186P
AP5	BK6_IO1	CCLK	186N
AR3	BK6_IO2	-	187P
-	GND (Bank 6)	-	-
AR2	BK6_IO3	-	187N
AP3	BK6_IO4	CSb	188P
AR1	BK6_IO5	Read	188N
AP2	BK6_IO6	-	189P
AP1	BK6_IO7	-	189N
AN4	BK6_IO8	-	190P
AM5	BK6_IO9	-	190N
AN3	BK6_IO10	-	191P
-	GND (Bank 6)	-	-
AN2	BK6_IO11	-	191N
AM4	BK6_IO12	VREF6	192P
AM3	BK6_IO13	-	192N
AN1	BK6_IO14	-	193P
AM2	BK6_IO15	-	193N
AL4	BK6_IO16	-	194P
AK5	BK6_IO17	-	194N
AM1	BK6_IO18	-	195P
-	GND (Bank 6)	-	-
AK4	BK6_IO19	-	195N
AL3	BK6_IO20	-	196P
AL2	BK6_IO21	-	196N
AL1	BK6_IO22	-	197P

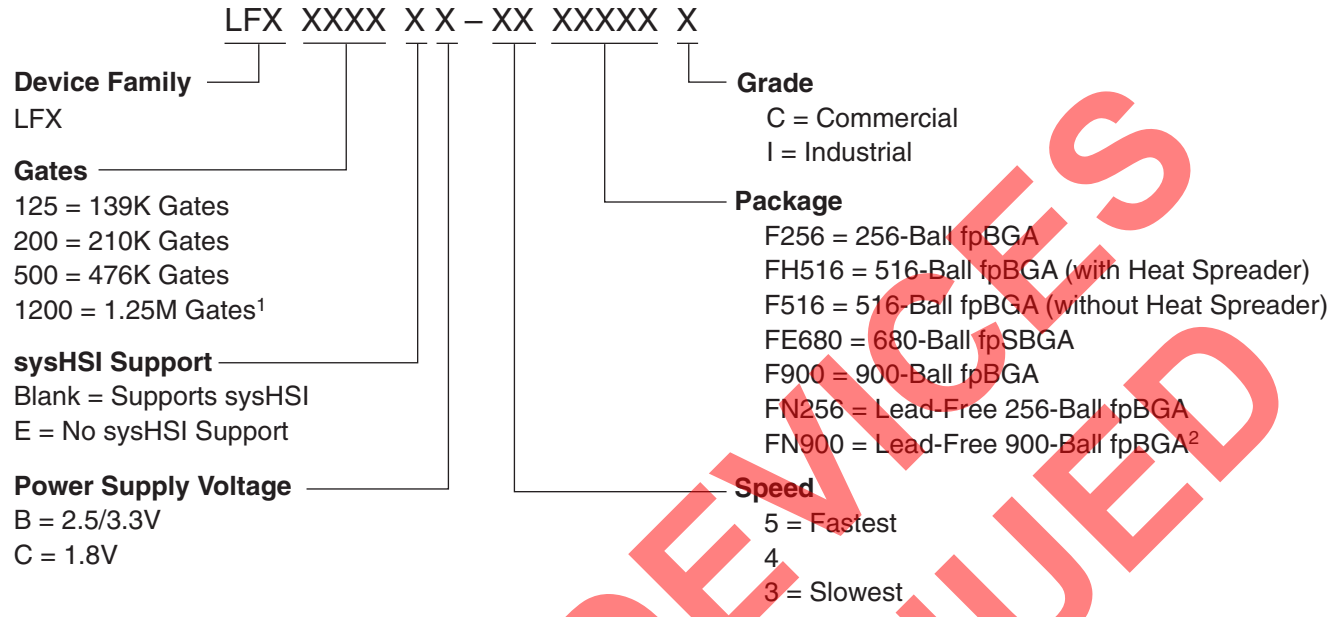
ispXPGA Logic Signal Connections: 900-Ball fpBGA

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
D3	BK0_IO0	-	0P	NC	-	-
E3	BK0_IO1	-	0N	NC	-	-
C2	BK0_IO2	-	1P	NC	-	-
-	GND (Bank 0)	-	-	-	-	-
C1	BK0_IO3	-	1N	NC	-	-
E4	BK0_IO4	-	2P	BK0_IO0	-	0P
F5	BK0_IO5	-	2N	BK0_IO1	-	0N
D2	BK0_IO6	HSI0A_SOUTP	3P	BK0_IO2	HSI0A_SOUTP	1P/HSI0
-	-	-	-	GND (Bank 0)	-	-
D1	BK0_IO7	HSI0A_SOUTN	3N	BK0_IO3	HSI0A_SOUTN	1N/HSI0
F4	BK0_IO8	-	4P	BK0_IO4	-	2P/HSI0
F3	BK0_IO9	-	4N	BK0_IO5	-	2N/HSI0
E2	BK0_IO10	HSI0A_SINP	5P/HSI0	BK0_IO6	HSI0A_SINP	3P/HSI0
-	GND (Bank 0)	-	-	-	-	-
E1	BK0_IO11	HSI0A_SINN	5N/HSI0	BK0_IO7	HSI0A_SINN	3N/HSI0
G6	BK0_IO12	VREF0	6P/HSI0	BK0_IO9	VREF0	4N/HSI0
G5	BK0_IO13	-	6N/HSI0	BK0_IO8	-	4P/HSI0
F1	BK0_IO14	HSI0B_SOUTP	7P/HSI0	NC	-	-
F2	BK0_IO15	HSI0B_SOUTN	7N/HSI0	NC	-	-
G4	BK0_IO16	-	8P/HSI0	NC	-	-
G3	BK0_IO17	-	8N/HSI0	NC	-	-
G2	BK0_IO18	HSI0B_SINP	9P/HSI0	NC	-	-
-	GND (Bank 0)	-	-	-	-	-
G1	BK0_IO19	HSI0B_SINN	9N/HSI0	NC	-	-
H3	BK0_IO20	-	10P/HSI0	NC	-	-
H4	BK0_IO21	-	10N/HSI0	NC	-	-
H1	BK0_IO22	HSI1A_SOUTP	11P/HSI0	NC	-	-
H2	BK0_IO23	HSI1A_SOUTN	11N/HSI0	NC	-	-
J7	BK0_IO24	-	12P/HSI0	NC	-	-
J6	BK0_IO25	-	12N/HSI0	NC	-	-
J1	BK0_IO26	HSI1A_SINP	13P/HSI1	NC	-	-
-	GND (Bank 0)	-	-	-	-	-
J2	BK0_IO27	HSI1A_SINN	13N/HSI1	NC	-	-
J4	BK0_IO28	-	14P/HSI1	NC	-	-
J5	BK0_IO29	-	14N/HSI1	NC	-	-
K1	BK0_IO30	HSI1B_SOUTP	15P/HSI1	BK0_IO10	HSI0B_SOUTP	5P/HSI0
-	-	-	-	GND (Bank 0)	-	-
K2	BK0_IO31	HSI1B_SOUTN	15N/HSI1	BK0_IO11	HSI0B_SOUTN	5N/HSI0
K5	BK0_IO32	-	16P/HSI1	BK0_IO12	-	6P/HSI0
K4	BK0_IO33	-	16N/HSI1	BK0_IO13	-	6N/HSI0
L1	BK0_IO34	HSI1B_SINP	17P/HSI1	BK0_IO14	HSI0B_SINP	7P/HSI0
-	GND (Bank 0)	-	-	-	-	-

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
AJ12	BK2_IO43	-	83N	BK2_IO23	-	53N
AD13	BK2_IO44	-	84P	BK2_IO24	-	54P
AE13	BK2_IO45	-	84N	BK2_IO25	-	54N
AK13	BK2_IO46	-	85P	BK2_IO26	-	55P
-	-	-	-	GND (Bank 2)	-	-
AJ13	BK2_IO47	-	85N	BK2_IO27	-	55N
AG13	BK2_IO48	-	86P	BK2_IO28	-	56P
AH13	BK2_IO49	-	86N	BK2_IO29	-	56N
AE14	BK2_IO50	-	87P	BK2_IO30	-	57P
-	GND (Bank 2)	-	-	-	-	-
AF14	BK2_IO51	-	87N	BK2_IO31	-	57N
AG14	BK2_IO52	-	88P	BK2_IO32	-	58P
AH14	BK2_IO53	-	88N	BK2_IO33	-	58N
AJ14	BK2_IO54	-	89P	BK2_IO34	-	59P
-	-	-	-	GND (Bank 2)	-	-
AK14	BK2_IO55	-	89N	BK2_IO35	-	59N
AE15	BK2_IO56	-	90P	BK2_IO36	-	60P
AF15	BK2_IO57	-	90N	BK2_IO37	-	60N
AG15	BK2_IO58	-	91P	BK2_IO38	-	61P
-	GND (Bank 2)	-	-	-	-	-
AH15	BK2_IO59	-	91N	BK2_IO39	-	61N
AJ15	BK2_IO60	-	92P	BK2_IO40	-	62P
AK15	BK2_IO61	-	92N	BK2_IO41	-	62N
-	GND (Bank 2)	-	-	GND (Bank 2)	-	-
-	GND (Bank 3)	-	-	GND (Bank 3)	-	-
AK16	BK3_IO0	-	93P	BK3_IO0	-	63P
AJ16	BK3_IO1	-	93N	BK3_IO1	-	63N
AH16	BK3_IO2	-	94P	BK3_IO2	-	64P
-	GND (Bank 3)	-	-	-	-	-
AG16	BK3_IO3	-	94N	BK3_IO3	-	64N
AF16	BK3_IO4	-	95P	BK3_IO4	-	65P
AE16	BK3_IO5	-	95N	BK3_IO5	-	65N
AK17	BK3_IO6	-	96P	BK3_IO6	-	66P
-	-	-	-	GND (Bank 3)	-	-
AJ17	BK3_IO7	-	96N	BK3_IO7	-	66N
AH17	BK3_IO8	-	97P	BK3_IO8	-	67P
AG17	BK3_IO9	-	97N	BK3_IO9	-	67N
AF17	BK3_IO10	-	98P	BK3_IO10	-	68P
-	GND (Bank 3)	-	-	-	-	-
AE17	BK3_IO11	-	98N	BK3_IO11	-	68N
AH18	BK3_IO12	-	99P	BK3_IO12	-	69P
AG18	BK3_IO13	-	99N	BK3_IO13	-	69N

Part Number Description



1. Discontinued via PCN #03A-10.
2. Select products only. See Ordering Information tables below for specific support.

Ordering Information

Conventional Packaging

Commercial

Part Number	Gates	Voltage	Speed Grade	Package	Balls
LFX125B-05F256C	139K	2.5/3.3	-5	fpBGA	256
LFX125B-04F256C	139K	2.5/3.3	-4	fpBGA	256
LFX125B-03F256C	139K	2.5/3.3	-3	fpBGA	256
LFX125C-04F256C	139K	1.8	-4	fpBGA	256
LFX125C-03F256C	139K	1.8	-3	fpBGA	256
LFX125B-05F516C	139K	2.5/3.3	-5	fpBGA	516
LFX125B-04F516C	139K	2.5/3.3	-4	fpBGA	516
LFX125B-03F516C	139K	2.5/3.3	-3	fpBGA	516
LFX125C-04F516C	139K	1.8	-4	fpBGA	516
LFX125C-03F516C	139K	1.8	-3	fpBGA	516
LFX125B-05FH516C[1]	139K	2.5/3.3	-5	fpBGA	516
LFX125B-04FH516C[1]	139K	2.5/3.3	-4	fpBGA	516
LFX125B-03FH516C[1]	139K	2.5/3.3	-3	fpBGA	516
LFX125C-04FH516C[1]	139K	1.8	-4	fpBGA	516
LFX125C-03FH516C[1]	139K	1.8	-3	fpBGA	516
LFX200B-05F256C	210K	2.5/3.3	-5	fpBGA	256
LFX200B-04F256C	210K	2.5/3.3	-4	fpBGA	256
LFX200B-03F256C	210K	2.5/3.3	-3	fpBGA	256
LFX200C-04F256C	210K	1.8	-4	fpBGA	256
LFX200C-03F256C	210K	1.8	-3	fpBGA	256

"E-Series" Commercial

Part Number	Gates	Voltage	Speed Grade	Package	Balls
LFX125EB-05F256C	139K	2.5/3.3	-5	fpBGA	256
LFX125EB-04F256C	139K	2.5/3.3	-4	fpBGA	256
LFX125EB-03F256C	139K	2.5/3.3	-3	fpBGA	256
LFX125EC-04F256C	139K	1.8	-4	fpBGA	256
LFX125EC-03F256C	139K	1.8	-3	fpBGA	256
LFX125EB-05F516C	139K	2.5/3.3	-5	fpBGA	516
LFX125EB-04F516C	139K	2.5/3.3	-4	fpBGA	516
LFX125EB-03F516C	139K	2.5/3.3	-3	fpBGA	516
LFX125EC-04F516C	139K	1.8	-4	fpBGA	516
LFX125EC-03F516C	139K	1.8	-3	fpBGA	516
LFX125EB-05FH516C[1]	139K	2.5/3.3	-5	fpBGA	516
LFX125EB-04FH516C[1]	139K	2.5/3.3	-4	fpBGA	516
LFX125EB-03FH516C[1]	139K	2.5/3.3	-3	fpBGA	516
LFX125EC-04FH516C[1]	139K	1.8	-4	fpBGA	516
LFX125EC-03FH516C[1]	139K	1.8	-3	fpBGA	516
LFX200EB-05F256C	210K	2.5/3.3	-5	fpBGA	256
LFX200EB-04F256C	210K	2.5/3.3	-4	fpBGA	256
LFX200EB-03F256C	210K	2.5/3.3	-3	fpBGA	256
LFX200EC-04F256C	210K	1.8	-4	fpBGA	256
LFX200EC-03F256C	210K	1.8	-3	fpBGA	256
LFX200EB-05F516C	210K	2.5/3.3	-5	fpBGA	516
LFX200EB-04F516C	210K	2.5/3.3	-4	fpBGA	516
LFX200EB-03F516C	210K	2.5/3.3	-3	fpBGA	516
LFX200EC-04F516C	210K	1.8	-4	fpBGA	516
LFX200EC-03F516C	210K	1.8	-3	fpBGA	516
LFX200EB-05FH516C[1]	210K	2.5/3.3	-5	fpBGA	516
LFX200EB-04FH516C[1]	210K	2.5/3.3	-4	fpBGA	516
LFX200EB-03FH516C[1]	210K	2.5/3.3	-3	fpBGA	516
LFX200EC-04FH516C[1]	210K	1.8	-4	fpBGA	516
LFX200EC-03FH516C[1]	210K	1.8	-3	fpBGA	516
LFX500EB-05F516C	476K	2.5/3.3	-5	fpBGA	516
LFX500EB-04F516C	476K	2.5/3.3	-4	fpBGA	516
LFX500EB-03F516C	476K	2.5/3.3	-3	fpBGA	516
LFX500EC-04F516C	476K	1.8	-4	fpBGA	516
LFX500EC-03F516C	476K	1.8	-3	fpBGA	516
LFX500EB-05FH516C[1]	476K	2.5/3.3	-5	fpBGA	516
LFX500EB-04FH516C[1]	476K	2.5/3.3	-4	fpBGA	516
LFX500EB-03FH516C[1]	476K	2.5/3.3	-3	fpBGA	516
LFX500EC-04FH516C[1]	476K	1.8	-4	fpBGA	516
LFX500EC-03FH516C[1]	476K	1.8	-3	fpBGA	516
LFX500EB-05F900C	476K	2.5/3.3	-5	fpBGA	900
LFX500EB-04F900C	476K	2.5/3.3	-4	fpBGA	900
LFX500EB-03F900C	476K	2.5/3.3	-3	fpBGA	900
LFX500EC-04F900C	476K	1.8	-4	fpBGA	900