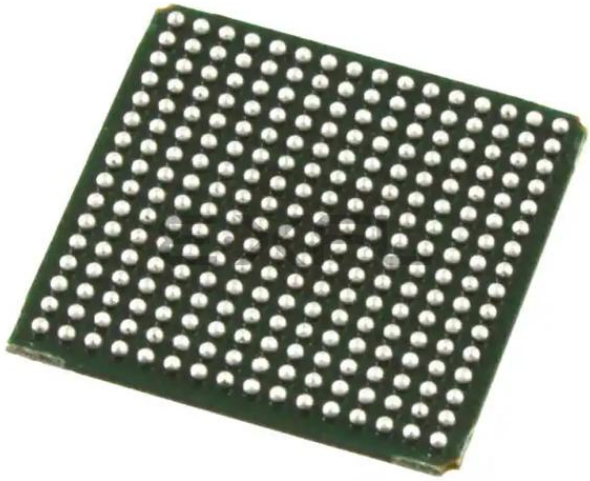
Lattice Semiconductor Corporation - LFX200EB-05F256C Datasheet



Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	2704
Total RAM Bits	113664
Number of I/O	160
Number of Gates	210000
Voltage - Supply	2.3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfx200eb-05f256c

Product Line	Ordering Part Number	Product Status	Reference PCN
LFX125EC (Cont'd)	LFX125EC-03F516C	**Discontinued**	PCN#09-10
	LFX125EC-04F516C		
	LFX125EC-03F516I		
LFX200EB	LFX200EB-03F256C	Active / Orderable	
	LFX200EB-03FN256C		
	LFX200EB-04F256C		
	LFX200EB-04FN256C		
	LFX200EB-05F256C		
	LFX200EB-05FN256C		
	LFX200EB-03F256I		
	LFX200EB-03FN256I		
	LFX200EB-04F256I		
	LFX200EB-04FN256I		
	LFX200EB-03F516C	**Discontinued**	PCN#09-10
	LFX200EB-04F516C		
	LFX200EB-05F516C		
	LFX200EB-03F516I		
	LFX200EB-04F516I		
LFX200EC	LFX200EC-03F256C	**Discontinued**	PCN#09-10
	LFX200EC-03FN256C		
	LFX200EC-04F256C		
	LFX200EC-04FN256C		
	LFX200EC-03F256I		
	LFX200EC-03FN256I		
	LFX200EC-03F516C		
	LFX200EC-04F516C		
	LFX200EC-03F516I		
LFX500EB	LFX500EB-03F516C	**Discontinued**	PCN#09-10
	LFX500EB-04F516C		
	LFX500EB-05F516C		
	LFX500EB-03F516I		
	LFX500EB-04F516I		
	LFX500EB-03F900C		
	LFX500EB-03FN900C		
	LFX500EB-04F900C		
	LFX500EB-04FN900C		
	LFX500EB-05F900C		
	LFX500EB-05FN900C		
	LFX500EB-03F900I		
	LFX500EB-03FN900I		
	LFX500EB-04F900I		
	LFX500EB-04FN900I		
LFX500EC	LFX500EC-03F516C	**Discontinued**	PCN#09-10
	LFX500EC-04F516C		
	LFX500EC-03F516I		

Architecture Overview

The ispXPGA architecture is a symmetrical architecture consisting of an array of Programmable Function Units (PFUs) enclosed by Input Output Groups (PICs) with columns of sysMEM Embedded Block RAMs (EBRs) distributed throughout the array. Figure 1 illustrates the ispXPGA architecture. Each PIC has two corresponding sysIO blocks, each of which includes one input and output buffer. On two sides of the device, between the PICs and the sysIO blocks, there are sysHSI High-Speed Interface blocks. The symmetrical architecture allows designers to easily implement their designs, since any logic function can be placed in any section of the device.

The PFUs contain the basic building blocks to create logic, memory, arithmetic, and register functions. They are optimized for speed and flexibility allowing complex designs to be implemented quickly and efficiently.

The PICs interface the PFUs and EBRs to the external pins of the device. They allow the signals to be registered quickly to minimize setup times for high-speed designs. They also allow connections directly to the different logic elements for fast access to combinatorial functions.

The sysMEM EBRs are large, fast memory elements that can be configured as RAM, ROM, FIFO, and other storage types. They are designed to facilitate both single and dual-port memory for high-speed applications.

These three components of the architecture are interconnected via a high-speed, flexible routing array. The routing array consists of Variable Length Interconnect (VLI) lines between the PICs, PFUs, and EBRs. There is additional routing available to the PFU for feedback and direct routing of signals to adjacent PFUs or PICs.

The sysIO blocks consist of configurable input and output buffers connected directly to the PICs. These buffers can be configured to interface with 16 different I/O standards. This allows the ispXPGA to interface with other devices without the need for external transceivers.

The sysHSI blocks provide the necessary components to allow the ispXPGA device to transfer data at up to 800Mbps using the LVDS standard. These components include serializing, de-serializing, and clock data recovery (CDR) logic.

The sysCLOCK blocks provide clock multiplication/division, clock distribution, delay compensation, and increased performance through the use of PLL circuitry that manipulates the global clocks. There is one sysCLOCK block for each global clock tree in the device.

sysIO Differential Standards DC Electrical Characteristics[1]

Parameter	Description	Test Conditions	Min.	Typ.	Max.
LVDS[2]					
V_{INP}, V_{INM}	Input voltage		0V	—	2.4V
V_{THD}	Differential input threshold	0.2V ð V_{CM} ð 1.8V	+/-100mV	—	—
I_{IN}	Input current	Power on	—	—	+/-10uA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	RT = 100 Ohm	—	1.38V	1.60V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	RT = 100 Ohm	0.9V	1.03V	—
V_{OD}	Output Voltage Differential	$\|V_{OP} - V_{OM}\|$, R_T = 100 ohm	250mV	350mV	450mV
ΔV_{OD}	Change in V_{OD} between high and low		—	—	50mV
V_{OS}	Output Voltage Offset	$\|V_{OP} + V_{OM}\|/2$, R_T = 100 ohm	1.125V	1.25V	1.375V
ΔV_{OS}	Change in V_{OS} between H and L		—	—	50mV
I_{OSD}	Output short circuit current	V_{OD} = 0V Driver outputs shorted	—	—	24mA
BLVDS[1]					
V_{INP}, V_{INM}	Input voltage		0V	—	2.4V
V_{THD}	Differential input threshold	0.2V ð V_{CM} ð 1.8V	+/-100mV	—	—
I_{IN}	Input current	Power on	—	—	+/-10uA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	R_T = 27Ω	—	1.4V	1.80V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	R_T = 27Ω	0.95V	1.1V	—
V_{OD}	Output Voltage Differential	$\|V_{OP} - V_{OM}\|$, RT = 27Ω	240mV	300mV	460mV
ΔV_{OD}	Change in V_{OD} Between H and L				27mV
V_{OS}	Output Voltage Offset	$\|V_{OP} + V_{OM}\|$ /2, RT = 27Ω	1.1V	1.3V	1.5V
ΔV_{OS}	Change in V_{OS} Between H and L				27mV
I_{OSD}	Output Short Circuit Current	V_{OD} = 0. Driver Outputs Shorted.		36mA	65mA

1. Refer to TN1000, sysIO Usage Guidelines for Lattice Devices.
2. V_{OP} and V_{OM} are the two outputs of the LVDS/BLVDS output buffer.

LVPECL[1]								
DC Parameter	**Parameter Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
V_{CCO}		**3.0**		**3.3**		**3.6**		**V**
V_{IH}	Input Voltage High	1.49	2.72	1.49	2.72	1.49	2.72	V
V_{IL}	Input Voltage Low	0.86	2.125	0.86	2.125	0.86	2.125	V
V_{OH}	Output Voltage High	1.8	2.11	1.92	2.28	2.13	2.41	V
V_{OL}	Output Voltage Low	0.96	1.27	1.06	1.43	1.3	1.57	V
V_{DIFF}[2]	Differential Input threshold	0.3	—	0.3	—	0.3	—	V

1. These values are valid at the output of the source termination pack as shown above with 100-ohm differential load only (see Figure 23). The V_{OH} levels are 200mV below the standard LVPECL levels and are compatible with devices tolerant of the lower common mode ranges.
2. Valid for 0.2 ð V_{CM} ð 1.8V.

ispXPGA 125B/C & ispXPGA 125EB/EC EBR Timing Parameters

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Synchronous Write								
t_{EBSWAD_S}	Address Setup Delay	0.59	—	0.61	—	0.70	—	ns
t_{EBSWAD_H}	Address Hold Delay	-0.40	—	-0.39	—	-0.33	—	ns
$t_{EBSWCPW}$	Clock Pulse Width	3.16	—	3.40	—	3.91	—	ns
t_{EBSWWE_S}	Write Enable Setup Time	-0.12	—	-0.12	—	-0.10	—	ns
t_{EBSWWE_H}	Write Enable Hold Time	0.16	—	0.16	—	0.18	—	ns
t_{EBSWD_S}	Data Setup Time	0.27	—	0.28	—	0.32	—	ns
t_{EBSWD_H}	Data Hold Time	-0.27	—	-0.26	—	-0.22	—	ns
Synchronous Read								
t_{EBSR_CO}	Clock to Data Delay	—	2.04	—	2.19	—	2.52	ns
t_{EBSRAD_S}	Address Setup Delay	0.10	—	0.10	—	0.12	—	ns
t_{EBSRAD_H}	Address Hold Delay	-0.07	—	-0.07	—	-0.06	—	ns
$t_{EBSRCPW}$	Clock Pulse Width	3.16	—	3.40	—	3.91	—	ns
t_{EBSRCE_S}	Clock Enable Setup Time	-1.76	—	-1.71	—	-1.45	—	ns
t_{EBSRCE_H}	Clock Enable Hold Time	1.64	—	1.69	—	1.94	—	ns
t_{EBSRWE_S}	Write Enable Setup Time	-0.18	—	-0.17	—	-0.14	—	ns
t_{EBSRWE_H}	Write Enable Hold Time	0.12	—	0.12	—	0.14	—	ns
$t_{EBSRWEEN}$	Write Enable to Data Enable Time	—	1.02	—	1.05	—	1.21	ns
$t_{EBSRWEDIS}$	Write Enable to Data Disable Time	—	0.99	—	1.02	—	1.17	ns
t_{EBSREN}	Output Enable to Data Enable Time	—	1.02	—	1.05	—	1.21	ns
$t_{EBSRDIS}$	Output Enable to Data Disable Time	—	0.83	—	0.86	—	0.99	ns
Asynchronous Read								
$t_{EBARADO}$	Address to New Valid Data Delay	—	2.39	—	2.46	—	2.83	ns
t_{EBARAD_H}	Address to Previous Valid Data Delay	—	2.10	—	2.17	—	2.50	ns
$t_{EBARWEEN}$	Write Enable to Data Enable Time	—	1.01	—	1.04	—	1.20	ns
$t_{EBARWEDIS}$	Write Enable to Data Disable Time	—	0.98	—	1.01	—	1.16	ns
t_{EBAREN}	Output Enable to Data Enable Time	—	1.02	—	1.05	—	1.21	ns
$t_{EBARDIS}$	Output Enable to Data Disable Time	—	0.83	—	0.86	—	0.99	ns

1. Only available for ispXPGA 125B and ispXPGA 125EB (2.5V/3.3V) devices.

Timing v.0.3

ispXPGA 200B/C & ispXPGA 200EB/EC PFU Timing Parameters

Over Recommended Operating Conditions

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Functional Delays								
LUTs								
t_{LUT4}	4-Input LUT Delay	—	0.41	—	0.44	—	0.51	ns
t_{LUT5}	5-Input LUT Delay	—	0.73	—	0.79	—	0.91	ns
t_{LUT6}	6-Input LUT Delay	—	0.86	—	0.93	—	1.07	ns
Shift Register (LUT)								
t_{LSR_S}	Shift Register Setup Time	-0.64	—	-0.62	—	-0.53	—	ns
t_{LSR_H}	Shift Register Hold Time	0.61	—	0.63	—	0.72	—	ns
t_{LSR_CO}	Shift Register Clock to Output Delay	—	0.70	—	0.75	—	0.86	ns
Arithmetic Functions								
$t_{LCTHRUR}$	MC (Macro Cell) Carry In to MC Carry Out Delay (Ripple)	—	0.08	—	0.09	—	0.10	ns
$t_{LCTHRUL}$[2]	MC Carry In to MC Carry Out Delay (Look Ahead)	—	0.05	—	0.05	—	0.06	ns
t_{LSTHRU}	MC Sum In to MC Sum Out Delay	—	0.42	—	0.45	—	0.52	ns
$t_{LSINCOUT}$	MC Sum In to MC Carry Out Delay	—	0.29	—	0.31	—	0.36	ns
$t_{LCINSOUTR}$	MC Carry In to MC Sum Out Delay (Ripple)	—	0.36	—	0.39	—	0.45	ns
$t_{LCINSOUTL}$	MC Carry In to MC Sum Out Delay (Look Ahead)	—	0.26	—	0.28	—	0.32	ns
Feed-thru								
t_{LFT}	PFU Feed-Thru Delay	—	0.15	—	0.16	—	0.18	ns
Distributed RAM								
t_{LRAM_CO}	Clock to RAM Output	—	1.24	—	1.33	—	1.53	ns
t_{LRAMAD_S}	Address Setup Time	-0.41	—	-0.40	—	-0.34	—	ns
t_{LRAMD_S}	Data Setup Time	0.21	—	0.22	—	0.25	—	ns
t_{LRAMWE_S}	Write Enable Setup Time	0.45	—	0.46	—	0.53	—	ns
t_{LRAMAD_H}	Address Hold Time	0.58	—	0.60	—	0.69	—	ns
t_{LRAMD_H}	Data Hold Time	0.11	—	0.11	—	0.13	—	ns
t_{LRAMWE_H}	Write Enable Hold Time	0.12	—	0.12	—	0.14	—	ns
$t_{LRAMCPW}$	Clock Pulse Width (High or Low)	2.91	—	3.00	—	3.45	—	ns
$t_{LRAMADO}$	Address to Output Delay	—	0.86	—	0.93	—	1.07	ns
Register/Latch Delays								
Registers								
t_{L_CO}	Register Clock to Output Delay	—	0.58	—	0.62	—	0.71	ns
t_{L_S}	Register Setup Time (Data before Clock)	0.14	—	0.14	—	0.16	—	ns
t_{L_H}	Register Hold Time (Data after Clock)	-0.12	—	-0.12	—	-0.10	—	ns
t_{LCE_S}	Register Clock Enable Setup Time	-0.11	—	-0.11	—	-0.09	—	ns
t_{LCE_H}	Register Clock Enable Hold Time	0.11	—	0.11	—	0.13	—	ns
Latches								
t_{L_GO}	Latch Gate to Output Delay	—	0.09	—	0.10	—	0.12	ns
t_{LL_S}	Latch Setup Time	0.14	—	0.14	—	0.16	—	ns
t_{LL_H}	Latch Hold Time	-0.12	—	-0.12	—	-0.10	—	ns
t_{LLPD}	Latch Propagation Delay (Transparent Mode)	—	0.09	—	0.10	—	0.12	ns

ispXPGA 200B/C & ispXPGA 200EB/EC EBR Timing Parameters

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Synchronous Write								
t_{EBSWAD_S}	Address Setup Delay	0.59	—	0.61	—	0.70	—	ns
t_{EBSWAD_H}	Address Hold Delay	-0.40	—	-0.39	—	-0.33	—	ns
$t_{EBSWCPW}$	Clock Pulse Width	3.16	—	3.40	—	3.91	—	ns
t_{EBSWWE_S}	Write Enable Setup Time	-0.12	—	-0.12	—	-0.10	—	ns
t_{EBSWWE_H}	Write Enable Hold Time	0.16	—	0.16	—	0.18	—	ns
t_{EBSWD_S}	Data Setup Time	0.27	—	0.28	—	0.32	—	ns
t_{EBSWD_H}	Data Hold Time	-0.27	—	-0.26	—	-0.22	—	ns
Synchronous Read								
t_{EBSR_CO}	Clock to Data Delay	—	2.04	—	2.19	—	2.52	ns
t_{EBSRAD_S}	Address Setup Delay	0.10	—	0.10	—	0.12	—	ns
t_{EBSRAD_H}	Address Hold Delay	-0.07	—	-0.07	—	-0.06	—	ns
$t_{EBSRCPW}$	Clock Pulse Width	3.16	—	3.40	—	3.91	—	ns
t_{EBSRCE_S}	Clock Enable Setup Time	-1.76	—	-1.71	—	-1.45	—	ns
t_{EBSRCE_H}	Clock Enable Hold Time	1.64	—	1.69	—	1.94	—	ns
t_{EBSRWE_S}	Write Enable Setup Time	-0.18	—	-0.17	—	-0.14	—	ns
t_{EBSRWE_H}	Write Enable Hold Time	0.12	—	0.12	—	0.14	—	ns
$t_{EBSRWEEN}$	Write Enable to Data Enable Time	—	1.02	—	1.05	—	1.21	ns
$t_{EBSRWEDIS}$	Write Enable to Data Disable Time	—	0.99	—	1.02	—	1.17	ns
t_{EBSREN}	Output Enable to Data Enable Time	—	1.02	—	1.05	—	1.21	ns
$t_{EBSRDIS}$	Output Enable to Data Disable Time	—	0.83	—	0.86	—	0.99	ns
Asynchronous Read								
$t_{EBARADO}$	Address to New Valid Data Delay	—	2.39	—	2.46	—	2.83	ns
t_{EBARAD_H}	Address to Previous Valid Data Delay	—	2.10	—	2.17	—	2.50	ns
$t_{EBARWEEN}$	Write Enable to Data Enable Time	—	1.01	—	1.04	—	1.20	ns
$t_{EBARWEDIS}$	Write Enable to Data Disable Time	—	0.98	—	1.01	—	1.16	ns
t_{EBAREN}	Output Enable to Data Enable Time	—	1.02	—	1.05	—	1.21	ns
$t_{EBARDIS}$	Output Enable to Data Disable Time	—	0.83	—	0.86	—	0.99	ns

1. Only available for ispXPGA 200B and ispXPGA 200EB (2.5V/3.3V) devices.

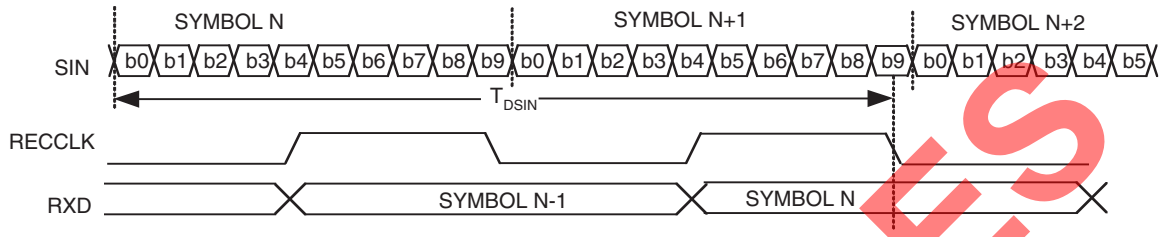
Timing v.0.3

ispXPGA 1200B/C & ispXPGA 1200EB/EC Timing Adders

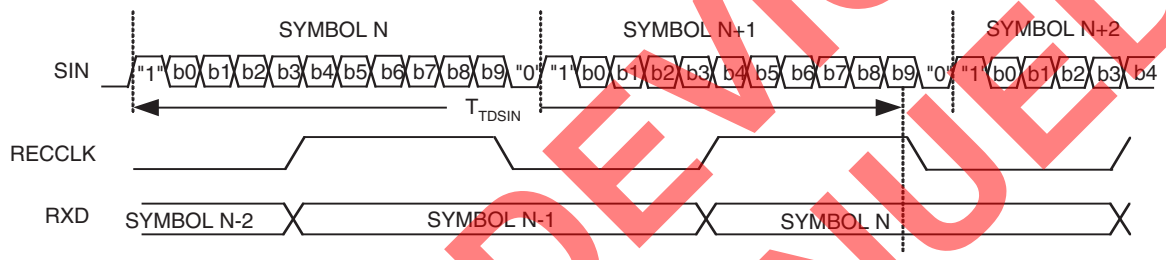
Parameter	Description	Base Parameter	-5[1]		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Optional Adders									
$t_{IOINDLY}$	Input Delay	—	—	5.58	—	6.0	—	6.90	ns
t_{IOI} Input Adjusters									
LVTTL_in	Using 3.3V TTL	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_18_in	Using 1.8V CMOS	t_{IOIN}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_25_in	Using 2.5V CMOS	t_{IOIN}	—	0.3	—	0.3	—	0.3	ns
LVCMOS_33_in	Using 3.3V CMOS	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
AGP_1X_in	Using AGP 1x	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
CTT25_in	Using CTT 2.5V	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
CTT33_in	Using CTT 3.3V	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
GTL+_in	Using GTL+	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
HSTL_I_in	Using HSTL 2.5V, Class I	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
HSTL_III_in	Using HSTL 2.5V, Class III	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
LVDS_in	Using Low Voltage Differential Signaling (LVDS)	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
BLVDS_in	Using Bus Low Voltage Differential Signaling (BLVDS)	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
LVPECL_in	Using Low Voltage PECL	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
PCI_in	Using PCI	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
SSTL2_I_in	Using SSTL 2.5V, Class I	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
SSTL2_II_in	Using SSTL 2.5V, Class II	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
SSTL3_I_in	Using SSTL 3.3V, Class I	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
SSTL3_II_in	Using SSTL 3.3V, Class II	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
t_{IOO} Output Adjusters									
Slow Slew	Using Slow Slew (LVTTL and LVCMOS Outputs only)	t_{IOBUF}, t_{IOEN}	—	0.7	—	0.7	—	0.7	ns
LVTTL_out	Using 3.3V TTL Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVCMOS_18_4mA_out	Using 1.8V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.8	—	0.8	—	0.8	ns
LVCMOS_18_5.33mA_out	Using 1.8V CMOS Standard, 5.33mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	—	0.6	ns
LVCMOS_18_8mA_out	Using 1.8V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_18_12mA_out	Using 1.8V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.2	—	0.2	—	0.2	ns
LVCMOS_25_4mA_out	Using 2.5V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.7	—	0.7	—	0.7	ns
LVCMOS_25_5.33mA_out	Using 2.5V CMOS Standard, 5.33 mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_8mA_out	Using 2.5V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_12mA_out	Using 2.5V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_16mA_out	Using 2.5V CMOS Standard, 16mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns

Deserializer Timing

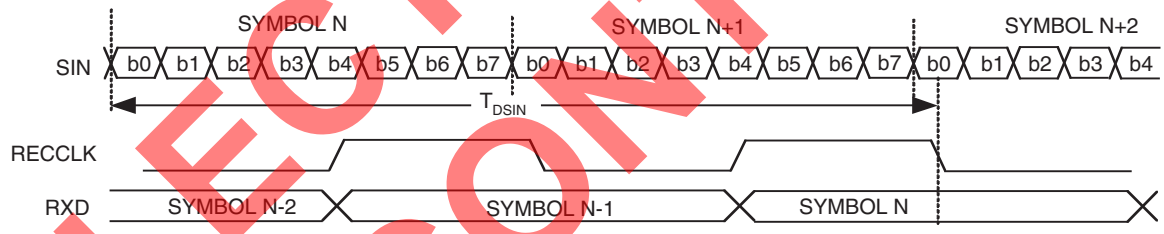
8B/10B DESERIALIZER DELAY TIMING



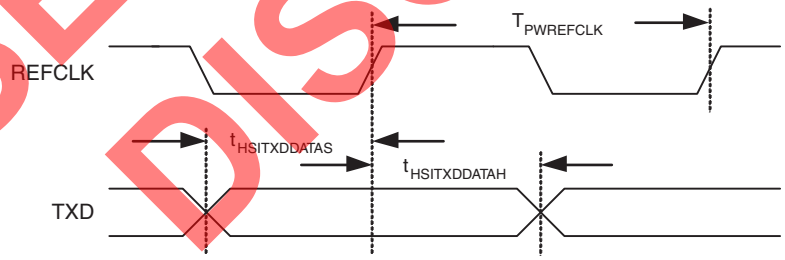
10B/12B DESERIALIZER DELAY TIMING



CDRX_SS DESERIALIZER DELAY TIMING



INTERNAL TIMING FOR sysHSI BLOCK



sysCLOCK PLL Timing

Over Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Units
t_{PWH}	Input clock, high time	80% to 80%	1.2	—	ns
t_{PWL}	Input clock, low time	20% to 20%	1.2	—	ns
t_R, t_F	Input Clock, rise and fall time	20% to 80%	—	3.0	ns
t_{INSTB}	Input clock stability, cycle to cycle (peak)		—	+/- 250	ps
f_{MDIVIN}	M Divider input, frequency range		10	320	MHz
$f_{MDIVOUT}$	M Divider output, frequency range		10	320	MHz
f_{NDIVIN}	N Divider input, frequency range		10	320	MHz
$f_{NDIVOUT}$	N Divider output, frequency range		10	320	MHz
f_{VDIVIN}	V Divider input, frequency range		100	400	MHz
$f_{VDIVOUT}$	V Divider output, frequency range		10	320	MHz
$t_{OUTDUTY}$	output clock, duty cycle		40	60	%
$t_{JIT(CC)}$	Output clock, cycle to cycle jitter (peak)	Clean reference[1] 10MHz ð $f_{MDIVOUT}$ ð 40MHz or 100MHz ð f_{VDIVIN} ð 160MHz	—	+/- 600	ps
		Clean reference[1] 40MHz ð $f_{MDIVOUT}$ ð 320MHz and 160MHz ð f_{VDIVIN} ð 400MHz	—	+/- 150	ps
$t_{JIT(PER)}$[2]	Output clock, period jitter (peak)	Clean reference[1] 10MHz ð $f_{MDIVOUT}$ ð 40MHz or 100MHz ð f_{VDIVIN} ð 160MHz	—	+/- 600	ps
		Clean reference[1] 40MHz ð $f_{MDIVOUT}$ ð 320MHz and 160MHz ð f_{VDIVIN} ð 400MHz	—	+/- 150	ps
$t_{CLK\_OUT\_DELAY}$	Input clock to CLK_OUT delay	Internal feedback	—	3.0	ns
t_{PHASE}	Input clock to external feedback delta	External feedback	—	1.5	ns
t_{LOCK}	Time to acquire phase lock after input stable		—	25	us
t_{PLL_DELAY}	Delay increment (Lead/Lag)	Typical = +/- 250ps	+/- 120	+/- 550	ps
t_{RANGE}	Total output delay range (lead/lag)		+/- 0.84	+/- 3.85	ns
t_{PLL_RSTW}	Minimum reset pulse width		1.8	—	ns
t_{CLK_IN}[3]	Global clock input delay		—	1.0	ns
$t_{PLL\_SEC\_DELAY}$	Secondary PLL output delay		—	1.5	ns

1. This condition assures that the output phase jitter will remain within specifications. Jitter spec is based on optimized M, N and V settings determined by the ispLEVER software.
2. Accumulated jitter measured over 10,000 waveform samples
3. Internal timing for reference only.

ispXPGA Logic Signal Connections: 256-Ball fpBGA (Cont.)

256-fpBGA Ball	LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[2]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[2]
-	GND (Bank 1)	-	-	-	-	-
L3	BK1_IO7	SS_CLKIN0N	16N	BK1_IO7	SS_CLKIN0N	14N
K2	BK1_IO8	-	17P	BK1_IO8	-	15P
-	-	-	-	GND (Bank 1)	-	-
L2	BK1_IO9	-	17N	BK1_IO9	-	15N
M1	BK1_IO10	HSI1A_SOUTP	18P/HSI1	BK1_IO10	-	16P
N1	BK1_IO11	HSI1A_SOUTN	18N/HSI1	BK1_IO11	-	16N
M3	BK1_IO12	PLL_RST2	19P/HSI1	BK1_IO12	PLL_RST2	17P
M4	BK1_IO13	PLL_RST3	19N/HSI1	BK1_IO13	PLL_RST3	17N
-	GND (Bank 1)	-	-	-	-	-
M2	BK1_IO16[1]	VREF1	-	BK1_IO14[1]	VREF1	-
P1	BK1_IO18	HSI1B_SOUTP	22P/HSI1	BK1_IO16	-	19P
-	-	-	-	GND (Bank 1)	-	-
R1	BK1_IO19	HSI1B_SOUTN	22N/HSI1	BK1_IO17	-	19N
N3	BK1_IO20[1]	-	-	BK1_IO18[1]	-	-
N2	BK1_IO22	HSI1B_SINP	24P/HSI1	BK1_IO20	-	21P
-	GND (Bank 1)	-	-	-	-	-
P2	BK1_IO23	HSI1B_SINN	24N/HSI1	BK1_IO21	-	21N
P4	TCK	-	-	TCK	-	-
T2	TMS	-	-	TMS	-	-
T3	TOE	-	-	TOE	-	-
R3	BK2_IO0	-	26P	BK2_IO0	-	22P
R4	BK2_IO1	-	26N	BK2_IO1	-	22N
N5	BK2_IO2	-	27P	BK2_IO2	-	23P
-	GND (Bank 2)	-	-	-	-	-
P5	BK2_IO3	-	27N	BK2_IO3	-	23N
-	-	-	-	GND (Bank 2)	-	-
T4	BK2_IO6	-	29P	BK2_IO6	-	25P
T5	BK2_IO7	-	29N	BK2_IO7	-	25N
N6	BK2_IO8	-	30P	BK2_IO8	-	26P
P6	BK2_IO9	VREF2	30N	BK2_IO9	VREF2	26N
R5	BK2_IO10	-	31P	BK2_IO10	-	27P
-	GND (Bank 2)	-	-	-	-	-
R6	BK2_IO11	-	31N	BK2_IO11	-	27N
N7	BK2_IO12	-	32P	BK2_IO12	-	28P
-	-	-	-	GND (Bank 2)	-	-
P7	BK2_IO13	-	32N	BK2_IO13	-	28N
T6	BK2_IO14	-	33P	BK2_IO14	-	29P
T7	BK2_IO15	-	33N	BK2_IO15	-	29N
M8	BK2_IO16	-	34P	BK2_IO16	-	30P
M9	BK2_IO17	-	34N	BK2_IO17	-	30N
R7	BK2_IO18	-	35P	BK2_IO18	-	31P

ispXPGA Logic Signal Connections: 256-Ball fpBGA (Cont.)

256-fpBGA Ball	LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[2]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[2]
D16	BK5_IO15	HSI3A_SOUTN	72N/HSI3	BK5_IO13	HSI1A_SOUTN	61N/HSI1
E13	BK5_IO16	VREF5	73P/HSI3	BK5_IO14	VREF5	62P/HSI1
E14	BK5_IO17	-	73N/HSI3	BK5_IO15	-	62N/HSI1
E15	BK5_IO18	HSI3B_SINP	74P/HSI3	BK5_IO16	HSI1B_SINP	63P/HSI1
-	-	-	-	GND (Bank 5)	-	-
D15	BK5_IO19	HSI3B_SINN	74N/HSI3	BK5_IO17	HSI1B_SINN	63N/HSI1
C16	BK5_IO22	HSI3B_SOUTP	76P/HSI3	BK5_IO20	HSI1B_SOUTP	65P/HSI1
-	GND (Bank 5)	-	-	-	-	-
B16	BK5_IO23	HSI3B_SOUTN	76N/HSI3	BK5_IO21	HSI1B_SOUTN	65N/HSI1
D14	BK5_IO24	-	77P/HSI3	BK5_IO18	-	64P/HSI1
C15	BK5_IO25	-	77N/HSI3	BK5_IO19	-	64N/HSI1
C13	CFG0	-	-	CFG0	-	-
A15	DONE	-	-	DONE	-	-
A14	PROGRAMb	-	-	PROGRAMb	-	-
D12	BK6_IO0	INITb	78P	BK6_IO0	INITb	66P
C12	BK6_IO1	CCLK	78N	BK6_IO1	CCLK	66N
B14	BK6_IO2	-	79P	BK6_IO2	-	67P
-	GND (Bank 6)	-	-	-	-	-
B13	BK6_IO3	-	79N	BK6_IO3	-	67N
A13	BK6_IO4	CSb	80P	BK6_IO4	CSb	68P
-	-	-	-	GND (Bank 6)	-	-
A12	BK6_IO5	Read	80N	BK6_IO5	READ	68N
D11	BK6_IO6	DATA7	81P	BK6_IO6	DATA7	69P
C11	BK6_IO7	DATA6	81N	BK6_IO7	DATA6	69N
B12	BK6_IO8	-	82P	BK6_IO8	-	70P
B11	BK6_IO9	VREF6	82N	BK6_IO9	VREF6	70N
D10	BK6_IO10	DATA5	83P	BK6_IO10	DATA5	71P
-	GND (Bank 6)	-	-	-	-	-
C10	BK6_IO11	DATA4	83N	BK6_IO11	DATA4	71N
-	-	-	-	GND (Bank 6)	-	-
A11	BK6_IO14	DATA3	85P	BK6_IO14	DATA3	73P
A10	BK6_IO15	DATA2	85N	BK6_IO15	DATA2	73N
D9	BK6_IO16	-	86P	BK6_IO16	-	74P
C9	BK6_IO17	-	86N	BK6_IO17	-	74N
B10	BK6_IO18	DATA1	87P	BK6_IO18	DATA1	75P
-	GND (Bank 6)	-	-	GND (Bank 6)	-	-
B9	BK6_IO19	DATA0	87N	BK6_IO19	DATA0	75N
E9	BK6_IO20	-	88P	BK6_IO20	-	76P
E8	BK6_IO21	-	88N	BK6_IO21	-	76N
-	GND (Bank 6)	-	-	-	-	-
-	GND (Bank 7)	-	-	-	-	-
D8	BK7_IO0	-	91P	BK7_IO0	-	77P

ispXPGA Logic Signal Connections: 516-Ball fpBGA (Cont.)

516-Ball BGA Ball	LFX500			LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
AJ13	BK2_IO32	-	58P	BK2_IO18	-	35P	BK2_IO18	-	31P
-	-	-	-	GND (Bank 2)	-	-	GND (Bank 2)	-	-
AK12	BK2_IO33	-	58N	BK2_IO19	-	35N	BK2_IO19	-	31N
AK13	BK2_IO34	-	59P	BK2_IO20	-	36P	BK2_IO20	-	32P
-	GND (Bank 2)	-	-	-	-	-	-	-	-
AH14	BK2_IO35	-	59N	BK2_IO21	-	36N	BK2_IO21	-	32N
AJ14	BK2_IO36	-	60P	BK2_IO22	-	37P	NC	-	-
AK14	BK2_IO37	-	60N	BK2_IO23	-	37N	NC	-	-
AG15	BK2_IO38	-	61P	BK2_IO24	-	38P	NC	-	-
AH15	BK2_IO39	-	61N	BK2_IO25	-	38N	NC	-	-
AJ15	BK2_IO40	-	62P	NC	-	-	NC	-	-
AK15	BK2_IO41	-	62N	NC	-	-	NC	-	-
-	GND (Bank 2)	-	-	GND (Bank 2)	-	-	-	-	-
-	GND (Bank 3)	-	-	GND (Bank 3)	-	-	-	-	-
AK16	BK3_IO0	-	63P	BK3_IO0	-	39P	BK3_IO0	-	33P
AJ16	BK3_IO1	-	63N	BK3_IO1	-	39N	BK3_IO1	-	33N
AH16	BK3_IO2	-	64P	BK3_IO2	-	40P	BK3_IO2	-	34P
AG16	BK3_IO3	-	64N	BK3_IO3	-	40N	BK3_IO3	-	34N
AK17	BK3_IO4	-	65P	BK3_IO4	-	41P	BK3_IO4	-	35P
AJ17	BK3_IO5	-	65N	BK3_IO5	-	41N	BK3_IO5	-	35N
AH17	BK3_IO6	-	66P	BK3_IO6	-	42P	BK3_IO6	-	36P
-	GND (Bank 3)	-	-	GND (Bank 3)	-	-	-	-	-
AJ18	BK3_IO7	-	66N	BK3_IO7	-	42N	BK3_IO7	-	36N
AH18	BK3_IO8	-	67P	BK3_IO8	-	43P	BK3_IO8	-	37P
-	-	-	-	-	-	-	GND (Bank 3)	-	-
AG18	BK3_IO9	-	67N	BK3_IO9	-	43N	BK3_IO9	-	37N
AK18	BK3_IO10	-	68P	BK3_IO10	-	44P	BK3_IO10	-	38P
AK19	BK3_IO11	-	68N	BK3_IO11	-	44N	BK3_IO11	-	38N
AJ19	BK3_IO12	-	69P	BK3_IO12	-	45P	NC	-	-
AH19	BK3_IO13	-	69N	BK3_IO13		45N	NC	-	-
AK20	BK3_IO14	-	70P	BK3_IO14	-	46P	NC	-	-
-	GND (Bank 3)	-	-	GND (Bank 3)	-	-	-	-	-
AJ20	BK3_IO15	-	70N	BK3_IO15	-	46N	NC	-	-
AH20	BK3_IO16	-	71P	NC	-	-	NC	-	-
AG20	BK3_IO17	-	71N	NC	-	-	NC	-	-
AK21	BK3_IO18	-	72P	NC	-	-	NC	-	-
AJ21	BK3_IO19	-	72N	NC	-	-	NC	-	-
AH21	BK3_IO20	VREF3	73P	BK3_IO16	VREF3	47P	BK3_IO12	VREF3	39P
AG21	BK3_IO21	-	73N	BK3_IO17	-	47N	BK3_IO13	-	39N
AJ22	BK3_IO22	-	74P	BK3_IO18	-	48P	BK3_IO14	-	40P
-	GND (Bank 3)	-	-	-	-	-	-	-	-
AH22	BK3_IO23	-	74N	BK3_IO19	-	48N	BK3_IO15	-	40N
AK23	BK3_IO24	-	75P	NC	-	-	NC	-	-
AJ23	BK3_IO25	-	75N	NC	-	-	NC	-	-
AH23	BK3_IO26	-	76P	NC	-	-	NC	-	-
AK24	BK3_IO27	-	76N	NC	-	-	NC	-	-
AJ24	BK3_IO28	-	77P	NC	-	-	NC	-	-
AG23	BK3_IO29	-	77N	NC	-	-	NC	-	-
AH24	BK3_IO30	-	78P	NC	-	-	NC	-	-
-	GND (Bank 3)	-	-		-	-	-	-	-
AK25	BK3_IO31	-	78N	NC	-	-	NC	-	-

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	**Signal Name**	**Second Function**	**LVDS Pair/sysHSI Reserved[1]**
AU6	BK5_IO50	HSI9B_SINP	180P/HSI9
-	GND (Bank 5)	-	-
AV6	BK5_IO51	HSI9B_SINN	180N/HSI9
AR8	BK5_IO52	-	181P
AT7	BK5_IO53	-	181N
AU5	BK5_IO54	HSI9B_SOUTP	182P
AV5	BK5_IO55	HSI9B_SOUTN	182N
AW5	BK5_IO56	-	183P
AW4	BK5_IO57	-	183N
AT6	BK5_IO58	-	184P
-	GND (Bank 5)	-	-
AV4	BK5_IO59	-	184N
AR6	BK5_IO60	-	185P
AU4	BK5_IO61	-	185N
AT1	CFG0	-	-
AT3	DONE	-	-
AT2	PROGRAMb	-	-
AP4	BK6_IO0	INITb	186P
AP5	BK6_IO1	CCLK	186N
AR3	BK6_IO2	-	187P
-	GND (Bank 6)	-	-
AR2	BK6_IO3	-	187N
AP3	BK6_IO4	CSb	188P
AR1	BK6_IO5	Read	188N
AP2	BK6_IO6	-	189P
AP1	BK6_IO7	-	189N
AN4	BK6_IO8	-	190P
AM5	BK6_IO9	-	190N
AN3	BK6_IO10	-	191P
-	GND (Bank 6)	-	-
AN2	BK6_IO11	-	191N
AM4	BK6_IO12	VREF6	192P
AM3	BK6_IO13	-	192N
AN1	BK6_IO14	-	193P
AM2	BK6_IO15	-	193N
AL4	BK6_IO16	-	194P
AK5	BK6_IO17	-	194N
AM1	BK6_IO18	-	195P
-	GND (Bank 6)	-	-
AK4	BK6_IO19	-	195N
AL3	BK6_IO20	-	196P
AL2	BK6_IO21	-	196N
AL1	BK6_IO22	-	197P

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	Signal Name	Second Function	LVDS Pair/sysHSI Reserved[1]
AK2	BK6_IO23	-	197N
AK1	BK6_IO24	-	198P
AJ4	BK6_IO25	-	198N
AJ3	BK6_IO26	-	199P
-	GND (Bank 6)	-	-
AH4	BK6_IO27	-	199N
AH3	BK6_IO28	-	200P
AH2	BK6_IO29	-	200N
AH1	BK6_IO30	-	201P
AG4	BK6_IO31	-	201N
AF5	BK6_IO32	DATA7	202P
AG3	BK6_IO33	DATA6	202N
AG2	BK6_IO34	-	203P
-	GND (Bank 6)	-	-
AF4	BK6_IO35	-	203N
AF3	BK6_IO36	DATA5	204P
AG1	BK6_IO37	DATA4	204N
AE2	BK6_IO38	-	205P
AF1	BK6_IO39	-	205N
AF2	BK6_IO40	-	206P
AE1	BK6_IO41	-	206N
AE4	BK6_IO42	-	207P
-	GND (Bank 6)	-	-
AD4	BK6_IO43	-	207N
AD5	BK6_IO44	-	208P
AD3	BK6_IO45	-	208N
AD2	BK6_IO46	-	209P
AD1	BK6_IO47	-	209N
AC4	BK6_IO48	-	210P
AC3	BK6_IO49	-	210N
AC2	BK6_IO50	DATA3	211P
-	GND (Bank 6)	-	-
AC1	BK6_IO51	DATA2	211N
AB3	BK6_IO52	-	212P
AB4	BK6_IO53	-	212N
AB2	BK6_IO54	DATA1	213P
AB1	BK6_IO55	DATA0	213N
AA3	BK6_IO56	-	214P
AA4	BK6_IO57	-	214N
AA5	BK6_IO58	-	215P
-	GND (Bank 6)	-	-
AA2	BK6_IO59	-	215N
AA1	BK6_IO60	-	216P

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	**Signal Name**	**Second Function**	**LVDS Pair/sysHSI Reserved[1]**
L3	BK7_IO35	-	234N
J1	BK7_IO36	-	235P
J2	BK7_IO37	-	235N
M4	BK7_IO38	-	236P
H1	BK7_IO39	-	236N
J3	BK7_IO40	-	237P
L4	BK7_IO41	-	237N
M5	BK7_IO42	-	238P
-	GND (Bank 7)	-	-
H2	BK7_IO43	-	238N
K4	BK7_IO44	-	239P
G1	BK7_IO45	-	239N
H3	BK7_IO46	-	240P
J4	BK7_IO47	VREF7	240N
K5	BK7_IO48	-	241P
G3	BK7_IO49	-	241N
H4	BK7_IO50	-	242P
-	GND (Bank 7)	-	-
F2	BK7_IO51	-	242N
G2	BK7_IO52	-	243P
H5	BK7_IO53	-	243N
F3	BK7_IO54	-	244P
F1	BK7_IO55	-	244N
G4	BK7_IO56	-	245P
E1	BK7_IO57	-	245N
F4	BK7_IO58	-	246P
-	GND (Bank 7)	-	-
E2	BK7_IO59	-	246N
F5	BK7_IO60	-	247P
E3	BK7_IO61	-	247N
D2	TDO	-	-
D3	VCCJ	-	-
D1	TDI	-	-

1. If a sysHSI Block is used, the indicated sysHSI reserved pins are unavailable for general purpose I/O use.

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
AJ12	BK2_IO43	-	83N	BK2_IO23	-	53N
AD13	BK2_IO44	-	84P	BK2_IO24	-	54P
AE13	BK2_IO45	-	84N	BK2_IO25	-	54N
AK13	BK2_IO46	-	85P	BK2_IO26	-	55P
-	-	-	-	GND (Bank 2)	-	-
AJ13	BK2_IO47	-	85N	BK2_IO27	-	55N
AG13	BK2_IO48	-	86P	BK2_IO28	-	56P
AH13	BK2_IO49	-	86N	BK2_IO29	-	56N
AE14	BK2_IO50	-	87P	BK2_IO30	-	57P
-	GND (Bank 2)	-	-	-	-	-
AF14	BK2_IO51	-	87N	BK2_IO31	-	57N
AG14	BK2_IO52	-	88P	BK2_IO32	-	58P
AH14	BK2_IO53	-	88N	BK2_IO33	-	58N
AJ14	BK2_IO54	-	89P	BK2_IO34	-	59P
-	-	-	-	GND (Bank 2)	-	-
AK14	BK2_IO55	-	89N	BK2_IO35	-	59N
AE15	BK2_IO56	-	90P	BK2_IO36	-	60P
AF15	BK2_IO57	-	90N	BK2_IO37	-	60N
AG15	BK2_IO58	-	91P	BK2_IO38	-	61P
-	GND (Bank 2)	-	-	-	-	-
AH15	BK2_IO59	-	91N	BK2_IO39	-	61N
AJ15	BK2_IO60	-	92P	BK2_IO40	-	62P
AK15	BK2_IO61	-	92N	BK2_IO41	-	62N
-	GND (Bank 2)	-	-	GND (Bank 2)	-	-
-	GND (Bank 3)	-	-	GND (Bank 3)	-	-
AK16	BK3_IO0	-	93P	BK3_IO0	-	63P
AJ16	BK3_IO1	-	93N	BK3_IO1	-	63N
AH16	BK3_IO2	-	94P	BK3_IO2	-	64P
-	GND (Bank 3)	-	-	-	-	-
AG16	BK3_IO3	-	94N	BK3_IO3	-	64N
AF16	BK3_IO4	-	95P	BK3_IO4	-	65P
AE16	BK3_IO5	-	95N	BK3_IO5	-	65N
AK17	BK3_IO6	-	96P	BK3_IO6	-	66P
-	-	-	-	GND (Bank 3)	-	-
AJ17	BK3_IO7	-	96N	BK3_IO7	-	66N
AH17	BK3_IO8	-	97P	BK3_IO8	-	67P
AG17	BK3_IO9	-	97N	BK3_IO9	-	67N
AF17	BK3_IO10	-	98P	BK3_IO10	-	68P
-	GND (Bank 3)	-	-	-	-	-
AE17	BK3_IO11	-	98N	BK3_IO11	-	68N
AH18	BK3_IO12	-	99P	BK3_IO12	-	69P
AG18	BK3_IO13	-	99N	BK3_IO13	-	69N

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
K30	BK5_IO22	HSI7B_SOUTP	166P/HSI8	BK5_IO22	HSI4B_SOUTP	116P/HSI4
-	-	-	-	GND (Bank 5)	-	-
K29	BK5_IO23	HSI7B_SOUTN	166N/HSI8	BK5_IO23	HSI4B_SOUTN	116N/HSI4
L28	BK5_IO24	-	167P/HSI8	BK5_IO24	-	117P/HSI5
L27	BK5_IO25	-	167N/HSI8	BK5_IO25	-	117N/HSI5
L26	BK5_IO26	HSI8A_SINP	168P/HSI8	BK5_IO26	HSI5A_SINP	118P/HSI5
-	GND (Bank 5)	-	-	-	-	-
L25	BK5_IO27	HSI8A_SINN	168N/HSI8	BK5_IO27	HSI5A_SINN	118N/HSI5
K27	BK5_IO28	-	169P/HSI8	BK5_IO28	-	119P/HSI5
K26	BK5_IO29	-	169N/HSI8	BK5_IO29	-	119N/HSI5
J30	BK5_IO30	HSI8A_SOUTP	170P/HSI8	BK5_IO30	HSI5A_SOUTP	120P/HSI5
-	-	-	-	GND (Bank 5)	-	-
J29	BK5_IO31	HSI8A_SOUTN	170N/HSI8	BK5_IO31	HSI5A_SOUTN	120N/HSI5
J26	BK5_IO32	-	171P/HSI8	NC	-	-
J27	BK5_IO33	-	171N/HSI8	NC	-	-
H30	BK5_IO34	HSI8B_SINP	172P/HSI8	NC	-	-
-	GND (Bank 5)	-	-	-	-	-
H29	BK5_IO35	HSI8B_SINN	172N/HSI8	NC	-	-
J25	BK5_IO36	-	173P/HSI9	NC	-	-
J24	BK5_IO37	-	173N/HSI9	NC	-	-
G30	BK5_IO38	HSI8B_SOUTP	174P/HSI9	NC	-	-
G29	BK5_IO39	HSI8B_SOUTN	174N/HSI9	NC	-	-
H27	BK5_IO40	-	175P/HSI9	NC	-	-
H28	BK5_IO41	-	175N/HSI9	NC	-	-
F30	BK5_IO42	HSI9A_SINP	176P/HSI9	NC	-	-
-	GND (Bank 5)	-	-	-	-	-
F29	BK5_IO43	HSI9A_SINN	176N/HSI9	NC	-	-
G27	BK5_IO44	-	177P/HSI9	NC	-	-
G28	BK5_IO45	-	177N/HSI9	NC	-	-
E30	BK5_IO46	HSI9A_SOUTP	178P/HSI9	NC	-	-
E29	BK5_IO47	HSI9A_SOUTN	178N/HSI9	NC	-	-
H26	BK5_IO48	-	179P/HSI9	BK5_IO33	-	121N/HSI5
H25	BK5_IO49	VREF5	179N/HSI9	BK5_IO32	VREF5	121P/HSI5
D30	BK5_IO50	HSI9B_SINP	180P/HSI9	BK5_IO34	HSI5B_SINP	122P/HSI5
-	GND (Bank 5)	-	-	-	-	-
D29	BK5_IO51	HSI9B_SINN	180N/HSI9	BK5_IO35	HSI5B_SINN	122N/HSI5
F28	BK5_IO52	-	181P	BK5_IO36	-	123P/HSI5
F27	BK5_IO53	-	181N	BK5_IO37	-	123N/HSI5
C30	BK5_IO54	HSI9B_SOUTP	182P	BK5_IO38	HSI5B_SOUTP	124P/HSI5
-	-	-	-	GND (Bank 5)	-	-
C29	BK5_IO55	HSI9B_SOUTN	182N	BK5_IO39	HSI5B_SOUTN	124N/HSI5
G26	BK5_IO56	-	183P	NC	-	-

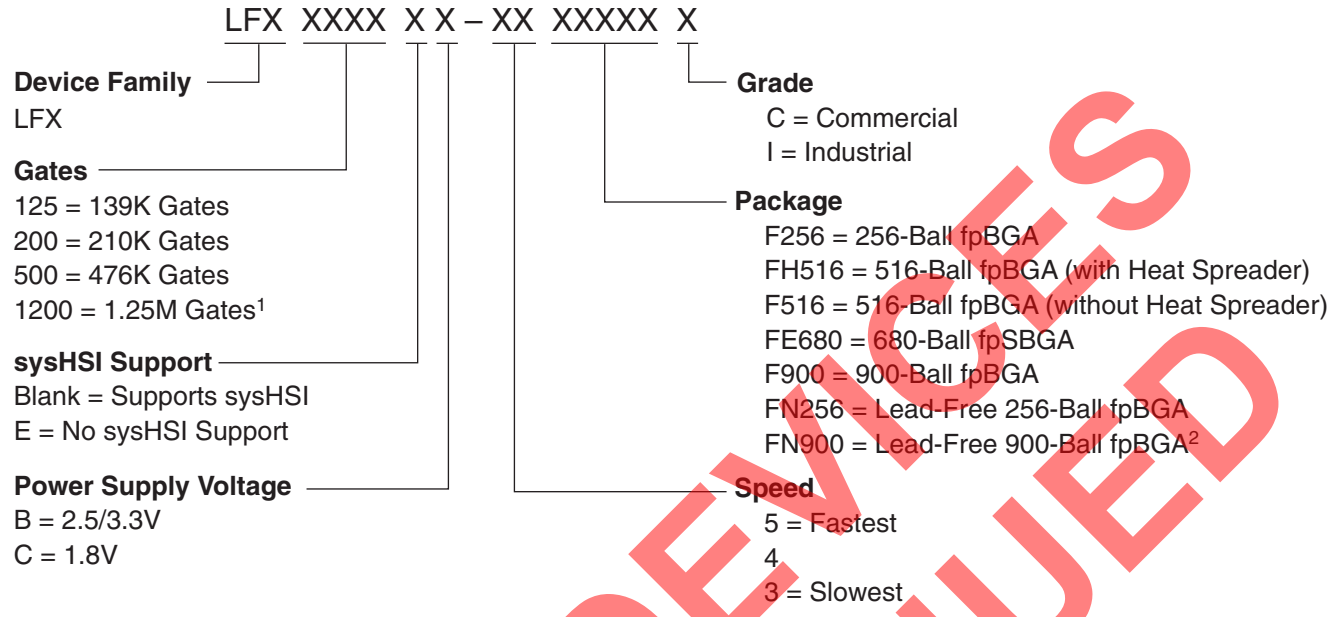
ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
D21	BK6_IO29	-	200N	NC	-	-
A21	BK6_IO30	-	201P	NC	-	-
B21	BK6_IO31	-	201N	NC	-	-
F20	BK6_IO32	DATA7	202P	BK6_IO18	DATA7	135P
-	-	-	-	GND (Bank 6)	-	-
E20	BK6_IO33	DATA6	202N	BK6_IO19	DATA6	135N
D20	BK6_IO34	-	203P	NC	-	-
-	GND (Bank 6)	-	-	-	-	-
C20	BK6_IO35		203N	NC	-	-
F19	BK6_IO36	DATA5	204P	BK6_IO22	DATA5	137P
E19	BK6_IO37	DATA4	204N	BK6_IO23	DATA4	137N
B20	BK6_IO38	-	205P	NC	-	-
A20	BK6_IO39	-	205N	NC	-	-
D19	BK6_IO40	-	206P	NC	-	-
C19	BK6_IO41	-	206N	NC	-	-
A19	BK6_IO42	-	207P	NC	-	-
-	GND (Bank 6)	-	-	-	-	-
B19	BK6_IO43	-	207N	NC	-	-
G18	BK6_IO44	-	208P	BK6_IO24	-	138P
F18	BK6_IO45	-	208N	BK6_IO25	-	138N
A18	BK6_IO46	-	209P	BK6_IO32	-	142P
B18	BK6_IO47	-	209N	BK6_IO33	-	142N
D18	BK6_IO48	-	210P	BK6_IO34	-	143P
-	-	-	-	GND (Bank 6)	-	-
C18	BK6_IO49	-	210N	BK6_IO35	-	143N
F17	BK6_IO50	DATA3	211P	BK6_IO26	DATA3	139P
-	GND (Bank 6)	-	-	GND (Bank 6)	-	-
E17	BK6_IO51	DATA2	211N	BK6_IO27	DATA2	139N
D17	BK6_IO52	-	212P	BK6_IO28	-	140P
C17	BK6_IO53	-	212N	BK6_IO29	-	140N
B17	BK6_IO54	DATA1	213P	BK6_IO30	DATA1	141P
A17	BK6_IO55	DATA0	213N	BK6_IO31	DATA0	141N
F16	BK6_IO56	-	214P	BK6_IO36	-	144P
E16	BK6_IO57	-	214N	BK6_IO37	-	144N
D16	BK6_IO58	-	215P	BK6_IO38	-	145P
-	GND (Bank 6)	-	-	-	-	-
C16	BK6_IO59	-	215N	BK6_IO39	-	145N
B16	BK6_IO60	-	216P	BK6_IO40	-	146P
A16	BK6_IO61	-	216N	BK6_IO41	-	146N
-	GND (Bank 6)	-	-	GND (Bank 6)	-	-
-	GND (Bank 7)	-	-	GND (Bank 7)	-	-
A15	BK7_IO0	-	217P	BK7_IO0	-	147P

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
B15	BK7_IO1	-	217N	BK7_IO1	-	147N
C15	BK7_IO2	-	218P	BK7_IO2	-	148P
-	GND (Bank 7)	-	-		-	-
D15	BK7_IO3	-	218N	BK7_IO3	-	148N
E15	BK7_IO4	-	219P	BK7_IO4	-	149P
F15	BK7_IO5	-	219N	BK7_IO5	-	149N
A14	BK7_IO6	-	220P	BK7_IO6	-	150P
-	-	-	-	GND (Bank 7)	-	-
B14	BK7_IO7	-	220N	BK7_IO7	-	150N
C14	BK7_IO8	-	221P	BK7_IO8	-	151P
D14	BK7_IO9	-	221N	BK7_IO9	-	151N
E14	BK7_IO10	-	222P	BK7_IO10	-	152P
-	GND (Bank 7)	-	-	-	-	-
F14	BK7_IO11	-	222N	BK7_IO11	-	152N
C13	BK7_IO12	-	223P	BK7_IO12	-	153P
D13	BK7_IO13	-	223N	BK7_IO13	-	153N
B13	BK7_IO14	-	224P	BK7_IO14	-	154P
-	-	-	-	GND (Bank 7)	-	-
A13	BK7_IO15	-	224N	BK7_IO15	-	154N
F13	BK7_IO16	-	225P	BK7_IO16	-	155P
G13	BK7_IO17	-	225N	BK7_IO17	-	155N
A12	BK7_IO18	-	226P	BK7_IO18	-	156P
-	GND (Bank 7)	-	-	-	-	-
B12	BK7_IO19	-	226N	BK7_IO19	-	156N
C12	BK7_IO20	-	227P	NC	-	-
D12	BK7_IO21	-	227N	NC	-	-
A11	BK7_IO22	-	228P	NC	-	-
B11	BK7_IO23	-	228N	NC	-	-
E12	BK7_IO24	-	229P	NC	-	-
F12	BK7_IO25	-	229N	NC	-	-
C11	BK7_IO26	-	230P	NC	-	-
-	GND (Bank 7)	-	-	-	-	-
D11	BK7_IO27	-	230N	NC	-	-
E11	BK7_IO28	-	231P	NC	-	-
F11	BK7_IO29	-	231N	NC	-	-
B10	BK7_IO30	-	232P	NC	-	-
A10	BK7_IO31	-	232N	NC	-	-
D10	BK7_IO32	-	233P	NC	-	-
E10	BK7_IO33	-	233N	NC	-	-
A9	BK7_IO34	-	234P	NC	-	-
-	GND (Bank 7)	-	-	-	-	-
B9	BK7_IO35	-	234N	NC	-	-

Part Number Description



1. Discontinued via PCN #03A-10.
2. Select products only. See Ordering Information tables below for specific support.

Ordering Information

Conventional Packaging

Commercial

Part Number	Gates	Voltage	Speed Grade	Package	Balls
LFX125B-05F256C	139K	2.5/3.3	-5	fpBGA	256
LFX125B-04F256C	139K	2.5/3.3	-4	fpBGA	256
LFX125B-03F256C	139K	2.5/3.3	-3	fpBGA	256
LFX125C-04F256C	139K	1.8	-4	fpBGA	256
LFX125C-03F256C	139K	1.8	-3	fpBGA	256
LFX125B-05F516C	139K	2.5/3.3	-5	fpBGA	516
LFX125B-04F516C	139K	2.5/3.3	-4	fpBGA	516
LFX125B-03F516C	139K	2.5/3.3	-3	fpBGA	516
LFX125C-04F516C	139K	1.8	-4	fpBGA	516
LFX125C-03F516C	139K	1.8	-3	fpBGA	516
LFX125B-05FH516C[1]	139K	2.5/3.3	-5	fpBGA	516
LFX125B-04FH516C[1]	139K	2.5/3.3	-4	fpBGA	516
LFX125B-03FH516C[1]	139K	2.5/3.3	-3	fpBGA	516
LFX125C-04FH516C[1]	139K	1.8	-4	fpBGA	516
LFX125C-03FH516C[1]	139K	1.8	-3	fpBGA	516
LFX200B-05F256C	210K	2.5/3.3	-5	fpBGA	256
LFX200B-04F256C	210K	2.5/3.3	-4	fpBGA	256
LFX200B-03F256C	210K	2.5/3.3	-3	fpBGA	256
LFX200C-04F256C	210K	1.8	-4	fpBGA	256
LFX200C-03F256C	210K	1.8	-3	fpBGA	256