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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	2704
Total RAM Bits	113664
Number of I/O	208
Number of Gates	210000
Voltage - Supply	2.3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	516-BBGA
Supplier Device Package	516-FPBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfx200eb-05f516c

Configurable Logic Element

The CLE is made up of a four-input Look-up Table (LUT-4), a Carry Chain Generator (CCG), and a two-input AND gate. The LUT-4 creates various combinatorial and memory elements, the CCG creates a single one-bit full adder, and the two-input AND gate can expand the CCG to incorporate Booth Multiplier capability by feeding the output of the AND gate to one of the inputs of the CCG.

Of the five inputs that feed each CLE, two are dedicated inputs into each LUT-4 and the remaining three take on varying functionality. The third and fourth inputs can be used as either inputs to the LUT-4 or as a Feed-Thru to the CSE via the WLG. The fifth input can be a data port when the LUT is configured as Distributed Memory, a select line for multiplexer operation, or a Feed-Thru directly to the CSE via the WLG (Figure 2).

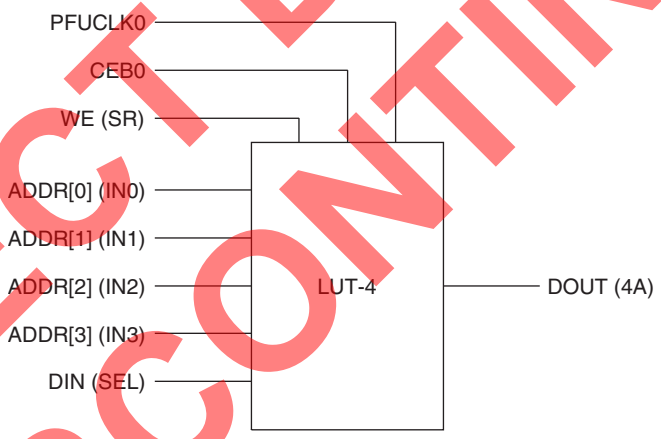
Look-Up Table – Combinatorial Mode

In combinatorial mode, the LUT-4 can implement any logic function up to four inputs. By using the carry chain and the WLG, each LUT-4 can be combined to form the enhanced functions listed in Table 3.

Look-Up Table – Distributed Memory Mode

In the distributed memory mode, the LUT functions as a memory element. The inputs to the LUT function as Address and Data. Each PFU is capable of implementing up to 64 SRAM bits. Both single and double port RAM can be performed in the PFU (Table 3). Furthermore, the distributed memory can be configured as either synchronous or asynchronous memory. Figure 3 illustrates the LUT while in distributed memory mode. When using any LUT in the PFU in memory mode, the Set/Reset signal will be used for Write Enable (WE(SR)) and the CLK0 signal will be used as the clock for synchronous read and write.

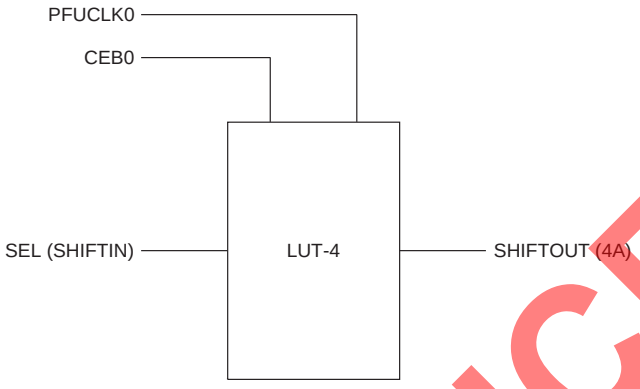
Figure 3. LUT in Distributed Memory Mode



Look-Up Table – Shift Register Mode

In the shift register mode, the LUT functions as a 1-bit to 8-bit shift register. This means that each PFU can implement up to four 8-bit shift registers or any cascaded combination. Figure 4 illustrates the LUT when configured in shift register mode.

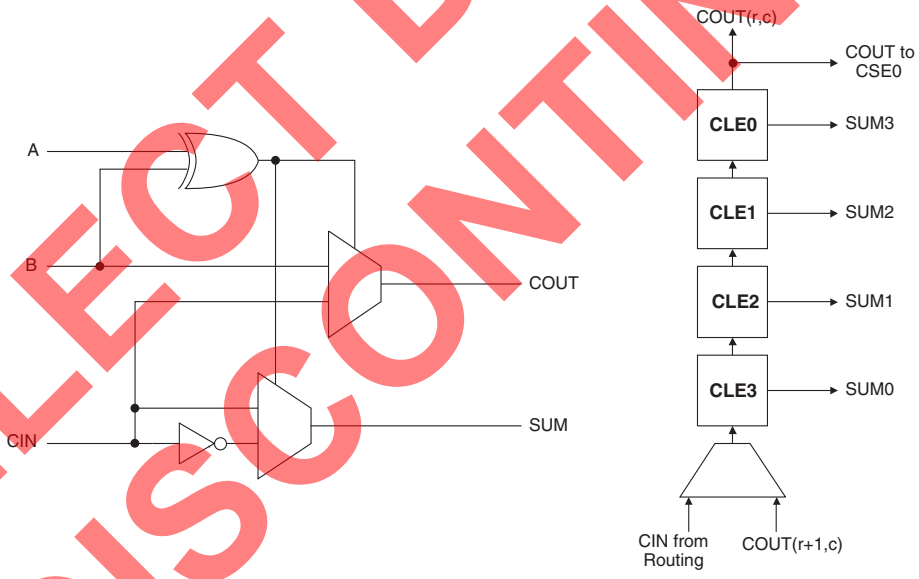
Figure 4. LUT in Shift Register Mode



Carry Chain Generator

The Carry Chain Generator is useful for implementing high-speed arithmetic functions. The CCG consists of a two-input XOR gate whose carryout can be cascaded with the input of the adjacent CCG. As shown in Figure 5, the carryin signal feeds CLE3 of the PFU and is propagated through CLE2 and CLE1 before reaching CLE0. The sum output of the CCG can be fed to the CSE through the WLG. The carryout must propagate to CLE0 for use outside the PFU. The carryout from the PFU can feed the W0 input of CSE0. The CCG also helps to effectively implement wider functions by using its logic elements to expand the capabilities of the LUT-4.

Figure 5. Carry Chain Generator



Wide Logic Generator

The WLG contains the logic necessary to implement wide gate functions. This is made up of a set of multiplexers that are located between the CLE and the CSE. The WLG helps in enhancing the wide gating capability of the PFU. The outputs of each CLE can be cascaded in the WLG to build wide gating functions. Wide multiplexing functions are also possible with a similar use of the WLG. Figure 6 illustrates the WLG.

Set/Reset signal controls all the registers for each PFU. This common Set/Reset signal is composed of the logical OR term of the Global Set/Reset signal (GSR) and the selected signal from routing. The polarity of this signal is not controllable inside the PFU. The polarity of the Global Set/Reset signal (GSR) is programmable. Figure 9 shows the Clock Enable and Output Enable selection for each PFU.

Figure 7. Clock Selection per PFU

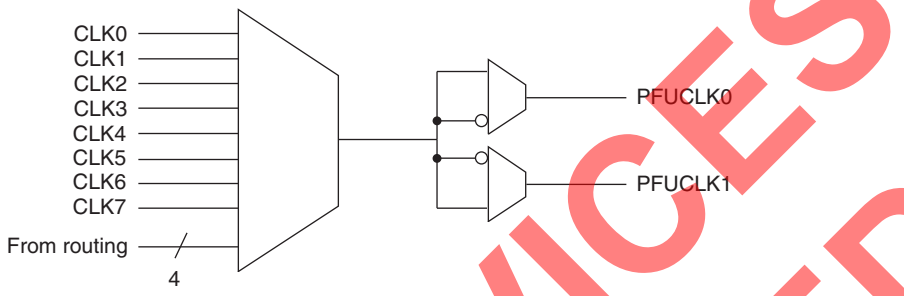


Figure 8. Set/Reset Selection per PFU

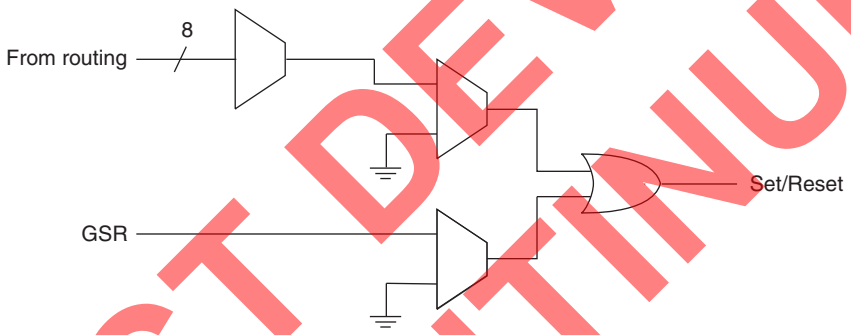
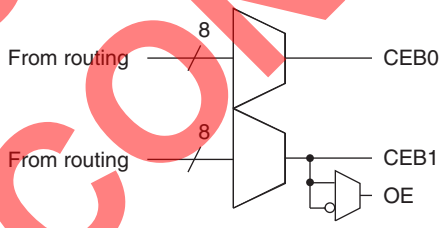


Figure 9. Clock Enable and Output Enable Selection per PFU



Programmable Input/Output Cell

The Programmable Input/Output Cell (PIC) is an essential part of the symmetrical architecture of the ispXPGA Family. The PICs interface the PFUs and EBRs to the sysIO and sysHSI blocks of the device.

Each PIC contains two Programmable Input/Outputs (PIOs) with a total of 21 inputs and 10 outputs. There are 18 inputs from routing, two inputs from the sysIO buffers, and the Global Set/Reset signal. Four outputs of the PIC connect to routing and two outputs are available as Output Enables for the tri-statable Long Lines. The remaining four outputs feed the sysIO buffers directly (one output enable and one output to each). Each PIC associated with a sysHSI block has four additional inputs and six additional outputs to support the sysHSI blocks. The four additional inputs come from the sysHSI block associated with the PIC. The four of the six additional outputs come from the PIC outputs and feed the sysHSI block, while the remaining two outputs feed routing. Figure 10 shows the block diagram of the PIC with the sysHSI block inputs and outputs.

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{IL}, I_{IH}[1]	Input or I/O Low Leakage	0 ð V_{IN} < (V_{CCO} - 0.2V)	—	—	10	µA
		(V_{CCO} - 0.2V) ð V_{IN} ð 3.6V	—	—	300	µA
I_{IH}[2]	Input High Leakage Current	3.6V < V_{IN} ð 5.5V and 3.0V ð V_{CCO} ð 3.6V	—	—	3	mA
I_{PU}	I/O Active Pull-up Current	0 ð V_{IN} ð 0.7 V_{CCO}	-30	—	-150	µA
I_{PD}	I/O Active Pull-down Current	V_{IL} (MAX) ð V_{IN} ð V_{IH} (MAX)	30	—	150	µA
I_{BHLS}	Bus Hold Low Sustaining Current	V_{IN} = V_{IL} (MAX)	30	—	—	µA
I_{BHHS}	Bus Hold High Sustaining Current	V_{IN} = 0.7 V_{CCO}	-30	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive Current	0 ð V_{IN} ð V_{IH} (MAX)	—	—	150	µA
I_{BHHO}	Bus Hold High Overdrive Current	0 ð V_{IN} ð V_{IH} (MAX)	—	—	-150	µA
V_{BHT}	Bus Hold Trip Points		V_{CCO} * 0.35	—	V_{CCO} * 0.65	V
C_1	I/O Capacitance[3]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	8	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—	
C_2	Clock Capacitance[3]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	8	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—	
C_3	Global Input Capacitance[3]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	6	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—	

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. 5V tolerant inputs and I/Os should be placed in banks where 3.0V ð V_{CCO} ð 3.6V. The JTAG and sysCONFIG ports are not included for the 5V tolerant interface.
3. T_A = 25°C, f = 1.0MHz.

sysIO DC Electrical Characteristics

Over Recommended Operating Conditions

Standard	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} (mA)	I_{OH} (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
LVCMOS 3.3	-0.3	0.8	2.0	5.5	0.4	V_{CCO} - 0.4	20, 16, 12, 8, 5.33, 4	-20, -16,-12, -8, -5.33, -4
					0.2	V_{CCO} - 0.2	0.1	-0.1
LVCMOS 2.5	-0.3	0.7	1.7	3.6	0.4	V_{CCO} - 0.4	16, 12, 8, 5.33, 4	-16, -12, -8, -5.33, -4
					0.2	V_{CCO} - 0.2	0.1	-0.1
LVCMOS 1.8[1]	-0.3	0.68[3]	1.07[3]	3.6	0.4	V_{CCO} - 0.4	12, 8[1], 5.33, 4	-12, -8[1], -5.33, -4
		0.35V_{CC}	0.65V_{CC}		0.2	V_{CCO} - 0.2	0.1	-0.1
LVTTL	-0.3	0.8	2.0	5.5	0.4	V_{CCO} - 0.4	4	-4
					0.2	V_{CCO} - 0.2	0.1	-0.1
PCI 3.3	-0.3	1.08[3]	1.5[3]	5.5	0.1 V_{CCO}	0.9 V_{CCO}	1.5	-0.5
		0.3V_{CCO}	0.5 V_{CCO}					
AGP-1X	-0.3	1.08[3]	1.5[3]	3.6	0.1 V_{CCO}	0.9 V_{CCO}	1.5	-0.5
		0.3 V_{CCO}	0.5 V_{CCO}					
SSTL 3 Class I	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.7	V_{CCO} - 1.1	8	-8
SSTL 3 Class II	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.5	V_{CCO} - 0.9	16	-16
SSTL 2 Class I	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.54	V_{CCO} - 0.62	7.6	-7.6
SSTL 2 Class II	-0.3	V_{REF} - 0.18	V_{REF} + 0.18	3.6	0.35	V_{CCO} - 0.43	15.2	-15.2
CTT 3.3	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	V_{REF} - 0.4	V_{REF} + 0.4	8	-8
CTT 2.5	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	V_{REF} - 0.4	V_{REF} + 0.4	8	-8
HSTL Class I	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} - 0.4	8	-8
HSTL Class III	-0.3	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} - 0.4	24	-8
GTL+	-0.3	V_{REF} - 0.2	V_{REF} + 0.2	3.6	0.6	N/A	36	N/A

1. Design tool default setting.
2. The average DC current drawn by I/Os between adjacent bank GND connections, or between the last GND in an I/O bank and the end of the I/O bank, as shown in the logic signals connection table, shall not exceed n*8mA. Where n is the number of I/Os between bank GND connections or between the last GND in a bank and the end of a bank
3. Applicable for ispXPGA B devices.

sysIO Differential Standards DC Electrical Characteristics[1]

Parameter	Description	Test Conditions	Min.	Typ.	Max.
LVDS[2]					
V_{INP}, V_{INM}	Input voltage		0V	—	2.4V
V_{THD}	Differential input threshold	0.2V ð V_{CM} ð 1.8V	+/-100mV	—	—
I_{IN}	Input current	Power on	—	—	+/-10uA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	RT = 100 Ohm	—	1.38V	1.60V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	RT = 100 Ohm	0.9V	1.03V	—
V_{OD}	Output Voltage Differential	$\|V_{OP} - V_{OM}\|$, R_T = 100 ohm	250mV	350mV	450mV
ΔV_{OD}	Change in V_{OD} between high and low		—	—	50mV
V_{OS}	Output Voltage Offset	$\|V_{OP} + V_{OM}\|/2$, R_T = 100 ohm	1.125V	1.25V	1.375V
ΔV_{OS}	Change in V_{OS} between H and L		—	—	50mV
I_{OSD}	Output short circuit current	V_{OD} = 0V Driver outputs shorted	—	—	24mA
BLVDS[1]					
V_{INP}, V_{INM}	Input voltage		0V	—	2.4V
V_{THD}	Differential input threshold	0.2V ð V_{CM} ð 1.8V	+/-100mV	—	—
I_{IN}	Input current	Power on	—	—	+/-10uA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	R_T = 27Ω	—	1.4V	1.80V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	R_T = 27Ω	0.95V	1.1V	—
V_{OD}	Output Voltage Differential	$\|V_{OP} - V_{OM}\|$, RT = 27Ω	240mV	300mV	460mV
ΔV_{OD}	Change in V_{OD} Between H and L				27mV
V_{OS}	Output Voltage Offset	$\|V_{OP} + V_{OM}\|$ /2, RT = 27Ω	1.1V	1.3V	1.5V
ΔV_{OS}	Change in V_{OS} Between H and L				27mV
I_{OSD}	Output Short Circuit Current	V_{OD} = 0. Driver Outputs Shorted.		36mA	65mA

1. Refer to TN1000, sysIO Usage Guidelines for Lattice Devices.
2. V_{OP} and V_{OM} are the two outputs of the LVDS/BLVDS output buffer.

LVPECL[1]								
DC Parameter	**Parameter Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
V_{CCO}		**3.0**		**3.3**		**3.6**		**V**
V_{IH}	Input Voltage High	1.49	2.72	1.49	2.72	1.49	2.72	V
V_{IL}	Input Voltage Low	0.86	2.125	0.86	2.125	0.86	2.125	V
V_{OH}	Output Voltage High	1.8	2.11	1.92	2.28	2.13	2.41	V
V_{OL}	Output Voltage Low	0.96	1.27	1.06	1.43	1.3	1.57	V
V_{DIFF}[2]	Differential Input threshold	0.3	—	0.3	—	0.3	—	V

1. These values are valid at the output of the source termination pack as shown above with 100-ohm differential load only (see Figure 23). The V_{OH} levels are 200mV below the standard LVPECL levels and are compatible with devices tolerant of the lower common mode ranges.
2. Valid for 0.2 ð V_{CM} ð 1.8V.

ispXPGA 200B/C & ispXPGA 200EB/EC EBR Timing Parameters

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Synchronous Write								
t_{EBSWAD_S}	Address Setup Delay	0.59	—	0.61	—	0.70	—	ns
t_{EBSWAD_H}	Address Hold Delay	-0.40	—	-0.39	—	-0.33	—	ns
$t_{EBSWCPW}$	Clock Pulse Width	3.16	—	3.40	—	3.91	—	ns
t_{EBSWWE_S}	Write Enable Setup Time	-0.12	—	-0.12	—	-0.10	—	ns
t_{EBSWWE_H}	Write Enable Hold Time	0.16	—	0.16	—	0.18	—	ns
t_{EBSWD_S}	Data Setup Time	0.27	—	0.28	—	0.32	—	ns
t_{EBSWD_H}	Data Hold Time	-0.27	—	-0.26	—	-0.22	—	ns
Synchronous Read								
t_{EBSR_CO}	Clock to Data Delay	—	2.04	—	2.19	—	2.52	ns
t_{EBSRAD_S}	Address Setup Delay	0.10	—	0.10	—	0.12	—	ns
t_{EBSRAD_H}	Address Hold Delay	-0.07	—	-0.07	—	-0.06	—	ns
$t_{EBSRCPW}$	Clock Pulse Width	3.16	—	3.40	—	3.91	—	ns
t_{EBSRCE_S}	Clock Enable Setup Time	-1.76	—	-1.71	—	-1.45	—	ns
t_{EBSRCE_H}	Clock Enable Hold Time	1.64	—	1.69	—	1.94	—	ns
t_{EBSRWE_S}	Write Enable Setup Time	-0.18	—	-0.17	—	-0.14	—	ns
t_{EBSRWE_H}	Write Enable Hold Time	0.12	—	0.12	—	0.14	—	ns
$t_{EBSRWEEN}$	Write Enable to Data Enable Time	—	1.02	—	1.05	—	1.21	ns
$t_{EBSRWEDIS}$	Write Enable to Data Disable Time	—	0.99	—	1.02	—	1.17	ns
t_{EBSREN}	Output Enable to Data Enable Time	—	1.02	—	1.05	—	1.21	ns
$t_{EBSRDIS}$	Output Enable to Data Disable Time	—	0.83	—	0.86	—	0.99	ns
Asynchronous Read								
$t_{EBARADO}$	Address to New Valid Data Delay	—	2.39	—	2.46	—	2.83	ns
t_{EBARAD_H}	Address to Previous Valid Data Delay	—	2.10	—	2.17	—	2.50	ns
$t_{EBARWEEN}$	Write Enable to Data Enable Time	—	1.01	—	1.04	—	1.20	ns
$t_{EBARWEDIS}$	Write Enable to Data Disable Time	—	0.98	—	1.01	—	1.16	ns
t_{EBAREN}	Output Enable to Data Enable Time	—	1.02	—	1.05	—	1.21	ns
$t_{EBARDIS}$	Output Enable to Data Disable Time	—	0.83	—	0.86	—	0.99	ns

1. Only available for ispXPGA 200B and ispXPGA 200EB (2.5V/3.3V) devices.

Timing v.0.3

ispXPGA 200B/C & ispXPGA 200EB/EC Timing Adders

Parameter	Description	Base Parameter	-5[1]		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Optional Adders									
$t_{IOINDLY}$	Input Delay	—	—	4.84	—	5.2	—	5.98	ns
t_{IOI} Input Adjusters									
LVTTL_in	Using 3.3V TTL	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_18_in	Using 1.8V CMOS	t_{IOIN}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_25_in	Using 2.5V CMOS	t_{IOIN}	—	0.3	—	0.3	—	0.3	ns
LVCMOS_33_in	Using 3.3V CMOS	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
AGP_1X_in	Using AGP 1x	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
CTT25_in	Using CTT 2.5V	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
CTT33_in	Using CTT 3.3V	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
GTL+_in	Using GTL+	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
HSTL_I_in	Using HSTL 2.5V, Class I	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
HSTL_III_in	Using HSTL 2.5V, Class III	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
LVDS_in	Using Low Voltage Differential Signaling (LVDS)	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
BLVDS_in	Using Bus Low Voltage Differential Signaling (BLVDS)	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
LVPECL_in	Using Low Voltage PECL	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
PCI_in	Using PCI	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
SSTL2_I_in	Using SSTL 2.5V, Class I	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
SSTL2_II_in	Using SSTL 2.5V, Class II	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
SSTL3_I_in	Using SSTL 3.3V, Class I	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
SSTL3_II_in	Using SSTL 3.3V, Class II	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
t_{IOO} Output Adjusters									
Slow Slew	Using Slow Slew (LVTTL and LVCMOS Outputs only)	t_{IOBUF}, t_{IOEN}	—	0.7	—	0.7	—	0.7	ns
LVTTL_out	Using 3.3V TTL Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVCMOS_18_4mA_out	Using 1.8V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.8	—	0.8	—	0.8	ns
LVCMOS_18_5.33mA_out	Using 1.8V CMOS Standard, 5.33mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	—	0.6	ns
LVCMOS_18_8mA_out	Using 1.8V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_18_12mA_out	Using 1.8V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.2	—	0.2	—	0.2	ns
LVCMOS_25_4mA_out	Using 2.5V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.7	—	0.7	—	0.7	ns
LVCMOS_25_5.33mA_out	Using 2.5V CMOS Standard, 5.33 mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_8mA_out	Using 2.5V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_12mA_out	Using 2.5V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_16mA_out	Using 2.5V CMOS Standard, 16mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns

ispXPGA 500B/C & ispXPGA 500EB/EC PFU Timing Parameters (Cont.)

Over Recommended Operating Conditions

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Reset/Set								
t_{LASSRO}	Asynchronous Set/Reset to Output	—	1.09	—	1.17	—	1.35	ns
$t_{LASSRPW}$	Asynchronous Set/Reset Pulse Width	4.19	—	4.50	—	5.18	—	ns
t_{LASSRR}	Asynchronous Set/Reset Recovery	—	0.51	—	0.55	—	0.63	ns
t_{LSSR_S}	Synchronous Set/Reset Setup Time	-0.03	—	-0.03	—	-0.03	—	ns
t_{LSSR_H}	Synchronous Set/Reset Hold Time	0.03	—	0.03	—	0.03	—	ns

1. Only available for ispXPGA 500B and ispXPGA 500EB (2.5V/3.3V) devices.
2. $t_{LCTHRUL}$ quoted bit by bit.

Timing v.0.3

ispXPGA 500B/C & ispXPGA 500EB/EC PIC Timing Parameters

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Register/Latch Delays								
t_{IO_CO}	Register Clock to Output Delay	—	1.00	—	1.07	—	1.23	ns
t_{IO_S}	Register Setup Time (Data before Clock)	0.05	—	0.05	—	0.06	—	ns
t_{IO_H}	Register Hold Time (Data after Clock)	0.06	—	0.06	—	0.07	—	ns
t_{IOCE_S}	Register Clock Enable Setup Time	-0.03	—	-0.03	—	-0.03	—	ns
t_{IOCE_H}	Register Clock Enable Hold Time	0.13	—	0.13	—	0.15	—	ns
t_{IO_GO}	Latch Gate to Output Delay	—	0.78	—	0.84	—	0.97	ns
t_{IOL_S}	Latch Setup Time	0.05	—	0.05	—	0.06	—	ns
t_{IOL_H}	Latch Hold Time	0.06	—	0.06	—	0.07	—	ns
t_{IOLPD}	Latch Propagation Delay (Transparent Mode)	—	0.09	—	0.10	—	0.12	ns
t_{IOASRO}	Asynchronous Set/Reset to Output	—	1.11	—	1.19	—	1.37	ns
$t_{IOASRPW}$	Asynchronous Set/Reset Pulse Width	4.19	—	4.50	—	5.18	—	ns
t_{IOASRR}	Asynchronous Set/Reset Recovery Time	—	0.23	—	0.25	—	0.29	ns
Input/Output Delays								
t_{IOBUF}	Output Buffer Delay	—	0.98	—	1.05	—	1.21	ns
t_{IOIN}	Input Buffer Delay	—	0.65	—	0.70	—	0.81	ns
t_{IOEN}	Output Enable Delay	—	0.52	—	0.56	—	0.64	ns
t_{IODIS}	Output Disable Delay	—	-0.12	—	-0.11	—	-0.09	ns
t_{IOFT}	Feed-thru Delay	—	0.19	—	0.20	—	0.23	ns

1. Only available for ispXPGA 500B and ispXPGA 500EB (2.5V/3.3V) devices.

Timing v.0.3

ispXPGA 500B/C & ispXPGA 500EB/EC Timing Adders

Parameter	Description	Base Parameter	-5[1]		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
Optional Adders									
$t_{IOINDLY}$	Input Delay	—	—	5.21	—	5.60	—	6.44	ns
t_{IOI} Input Adjusters									
LVTTL_in	Using 3.3V TTL	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_18_in	Using 1.8V CMOS	t_{IOIN}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_25_in	Using 2.5V CMOS	t_{IOIN}	—	0.3	—	0.3	—	0.3	ns
LVCMOS_33_in	Using 3.3V CMOS	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
AGP_1X_in	Using AGP 1x	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
CTT25_in	Using CTT 2.5V	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
CTT33_in	Using CTT 3.3V	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
GTL+_in	Using GTL+	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
HSTL_I_in	Using HSTL 2.5V, Class I	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
HSTL_III_in	Using HSTL 2.5V, Class III	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
LVDS_in	Using Low Voltage Differential Signaling (LVDS)	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
BLVDS_in	Using Bus Low Voltage Differential Signaling (BLVDS)	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
LVPECL_in	Using Low Voltage PECL	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
PCI_in	Using PCI	t_{IOIN}	—	1.0	—	1.0	—	1.0	ns
SSTL2_I_in	Using SSTL 2.5V, Class I	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
SSTL2_II_in	Using SSTL 2.5V, Class II	t_{IOIN}	—	0.5	—	0.5	—	0.5	ns
SSTL3_I_in	Using SSTL 3.3V, Class I	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
SSTL3_II_in	Using SSTL 3.3V, Class II	t_{IOIN}	—	0.8	—	0.8	—	0.8	ns
t_{IOO} Output Adjusters									
Slow Slew	Using Slow Slew (LVTTL and LVCMOS Outputs only)	t_{IOBUF}, t_{IOEN}	—	0.7	—	0.7	—	0.7	ns
LVTTL_out	Using 3.3V TTL Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	1.0	—	1.0	—	1.0	ns
LVCMOS_18_4mA_out	Using 1.8V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.8	—	0.8	—	0.8	ns
LVCMOS_18_5.33mA_out	Using 1.8V CMOS Standard, 5.33mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.6	—	0.6	—	0.6	ns
LVCMOS_18_8mA_out	Using 1.8V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.0	—	0.0	—	0.0	ns
LVCMOS_18_12mA_out	Using 1.8V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.2	—	0.2	—	0.2	ns
LVCMOS_25_4mA_out	Using 2.5V CMOS Standard, 4mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.7	—	0.7	—	0.7	ns
LVCMOS_25_5.33mA_out	Using 2.5V CMOS Standard, 5.33 mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_8mA_out	Using 2.5V CMOS Standard, 8mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_12mA_out	Using 2.5V CMOS Standard, 12mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns
LVCMOS_25_16mA_out	Using 2.5V CMOS Standard, 16mA Drive	t_{IOBUF}, t_{IOEN}, t_{IODIS}	—	0.5	—	0.5	—	0.5	ns

ispXPGA Power Supply and NC Connections[1]

Signal	256-Ball fpBGA[3]	516-Ball fpBGA[3]
V_{CC}	C3, C14, D4, D13, E5, E12, F6, F11, L6, L11, M5, M12, N4, N13, P3, P14	A9, A22, D4, D27, J1, J30, L11, L12, L15, L16, L19, L20, M11, M20, R11, R20, T11, T20, W11, W20, Y11, Y12, Y15, Y16, Y19, Y20, AB1, AB30, AG4, AG27, AK9, AK22
V_{CCO0}	F5, G5	F4, J4, M4, N11, P4, P11
V_{CCO1}	K5, L5	U4, U11, V11, W4, AB4, AE4
V_{CCO2}	M6, M7	Y13, Y14, AG6, AG9, AG12, AG14
V_{CCO3}	M10, M11	Y17, Y18, AG17, AG19, AG22, AG25
V_{CCO4}	K12, L12	U20, U27, V20, W27, AB27, AE27
V_{CCO5}	G12, F12	F27, J27, M27, N20, P20, P27
V_{CCO6}	E10, E11	D17, D19, D22, D25, L17, L18
V_{CCO7}	E6, E7	D6, D9, D12, D14, L13, L14
V_{CCP}	H3, J15	R4, T30
V_{CCJ}	A2	C4
GND	A1, A16, B2, B15, F7, F8, F9, F10, G6, G7, G8, G9, G10, G11, H6, H7, H8, H9, H10, H11, J6, J7, J8, J9, J10, J11, K6, K7, K8, K9, K10, K11, L7, L8, L9, L10, R2, R15, T1, T16	A1, A30, B2, B29, C3, C28, M12, M13, M14, M15, M16, M17, M18, M19, N12, N13, N14, N15, N16, N17, N18, N19, P12, P13, P14, P15, P16, P17, P18, P19, R12, R13, R14, R15, R16, R17, R18, R19, T12, T13, T14, T15, T16, T17, T18, T19, U12, U13, U14, U15, U16, U17, U18, U19, V12, V13, V14, V15, V16, V17, V18, V19, W12, W13, W14, W15, W16, W17, W18, W19, AH3, AH28, AJ2, AJ29, AK1, AK30
GND_P	H15, J4	R29, T4
NC[2]	—	**LFX125:** A10, A13, A16, A17, A24, A25, A26, A4, A5, A6, A7, AA1, AA2, AA28, AA29, AA3, AB28, AC1, AC28, AD1, AD27, AD4, AE28, AE29, AE3, AE30, AF27, AF28, AF29, AF3, AF4, AG1, AG10, AG11, AG15, AG2, AG20, AG23, AG24, AG29, AG3, AG8, AH1, AH15, AH19, AH2, AH20, AH23, AH24, AH30, AH7, AH8, AH9, AJ1, AJ12, AJ14, AJ15, AJ19, AJ20, AJ21, AJ23, AJ24, AJ25, AJ27, AJ30, AJ6, AJ7, AJ8, AK11, AK14, AK15, AK20, AK21, AK23, AK24, AK25, AK27, AK5, AK6, AK7, B10, B13, B16, B17, B18, B23, B24, B25, B5, B6, B7, C11, C13, C14, C16, C17, C22, C23, C24, C25, C6, C7, C8, D11, D16, D23, D24, D28, D29, D3, D7, D8, E30, E4, F1, F29, F30, G1, G2, G27, G28, G29, G30, H1, H2, H27, H28, H29, H30, J2, J28, J29, J3, K1, K2, K27, K28, K3, K4, L1, L2, L27, L3, L4, M1, M2, M29, M3, M30, V27, V28, V3, V4, W1, W30, Y1, Y27, Y28, Y3, Y30 **LFX200:** A26, A25, A24, A17, A10, A7, A6, A5, A4, B25, B24, B23, B17, B10, B7, B6, B5, C25, C24, C23, C22, C16, C11, C8, C7, C6, D24, D23, D16, D11, D8, D7, E30, F30, F29, F1, G30, G29, G28, G27, G2, G1, H30, H29, H28, H27, H2, H1, J29, J28, J3, J2, K28, K27, K4, K3, K2, K1, L27, L4, L3, L2, L1, M3, V28, V27, V4, V3, W30, W1, Y30, Y28, Y27, Y3, Y1, AA29, AA28, AA3, AA2, AA1, AD27, AD4, AE28, AE3, AF29, AF28, AF27, AF3, AG29, AG24, AG23, AG20, AG11, AG10, AG8, AG2, AG1, AH30, AH24, AH23, AH20, AH9, AH8, AH7, AH2, AH1, AJ30, AJ27, AJ25, AJ24, AJ23, AJ21, AJ15, AJ12, AJ8, AJ7, AJ6, AJ1, AK27, AK25, AK24, AK23, AK21, AK15, AK11, AK7, AK6, AK5

1. All grounds must be electrically connected at the board level.
2. NC pins should not be connected to any active signals, V_{CC} or GND.
3. Balls for GND, V_{CC} and V_{CCOx} are connected within the substrate to their respective common signals. Pin orientation A1 starts from the upper left corner of the top side view with alphabetical order ascending vertically and numerical order ascending horizontally.

ispXPGA Logic Signal Connections: 516-Ball fpBGA (Cont.)

516-Ball BGA Ball	LFX500			LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
AE3	BK1_IO33	-	37N/HSI2	NC	-	-	NC	-	-
AG1	BK1_IO34	-	38P/HSI2	NC	-	-	NC	-	-
AH1	BK1_IO35	-	38N/HSI2	NC	-	-	NC	-	-
AG2	BK1_IO36	-	39P/HSI2	NC	-	-	NC	-	-
AF3	BK1_IO37	-	39N/HSI2	NC	-	-	NC	-	-
AJ1	BK1_IO38	-	40P/HSI2	NC	-	-	NC	-	-
-	GND (Bank 1)	-	-	-	-	-	-	-	-
AH2	BK1_IO39	-	40N/HSI2	NC	-	-	NC	-	-
AG3	BK1_IO40	-	41P	BK1_IO24	-	25P/HSI1	NC	-	-
AF4	BK1_IO41	-	41N	BK1_IO25	-	25N/HSI1	NC	-	-
AK2	TCK	-	-	TCK	-	-	TCK	-	-
AJ3	TMS	-	-	TMS	-	-	TMS	-	-
AG5	TOE	-	-	TOE	-	-	TOE	-	-
AH4	BK2_IO0	-	42P	BK2_IO0	-	26P	BK2_IO0	-	22P
AK3	BK2_IO1	-	42N	BK2_IO1	-	26N	BK2_IO1	-	22N
AJ4	BK2_IO2	-	43P	BK2_IO2	-	27P	BK2_IO2	-	23P
-	GND (Bank 2)	-	-	GND (Bank 2)	-	-	-	-	-
AH5	BK2_IO3	-	43N	BK2_IO3	-	27N	BK2_IO3	-	23N
AK4	BK2_IO4	-	44P	BK2_IO4	-	28P	BK2_IO4	-	24P
-	-	-	-	-	-	-	GND (Bank 2)	-	-
AJ5	BK2_IO5	-	44N	BK2_IO5	-	28N	BK2_IO5	-	24N
AG7	BK2_IO6	-	45P	BK2_IO6	-	29P	BK2_IO6	-	25P
AH6	BK2_IO7	-	45N	BK2_IO7	-	29N	BK2_IO7	-	25N
AK5	BK2_IO8	-	46P	NC	-	-	NC	-	-
AJ6	BK2_IO9	-	46N	NC	-	-	NC	-	-
AG8	BK2_IO10	-	47P	NC	-	-	NC	-	-
-	GND (Bank 2)	-	-	-	-	-	-	-	-
AH7	BK2_IO11	-	47N	NC	-	-	NC	-	-
AK6	BK2_IO12	-	48P	NC	-	-	NC	-	-
AJ7	BK2_IO13	-	48N	NC	-	-	NC	-	-
AH8	BK2_IO14	-	49P	NC	-	-	NC	-	-
AG10	BK2_IO15	-	49N	NC	-	-	NC	-	-
AK7	BK2_IO16	-	50P	NC	-	-	NC	-	-
AJ8	BK2_IO17	-	50N	NC	-	-	NC	-	-
AH9	BK2_IO18	-	51P	NC	-	-	NC	-	-
-	GND (Bank 2)	-	-	-	-	-	-	-	-
AG11	BK2_IO19	-	51N	NC	-	-	NC	-	-
AK8	BK2_IO20	-	52P	BK2_IO8	-	30P	BK2_IO8	-	26P
AJ9	BK2_IO21	VREF2	52N	BK2_IO9	VREF2	30N	BK2_IO9	VREF2	26N
AH10	BK2_IO22	-	53P	BK2_IO10	-	31P	BK2_IO10	-	27P
-	-	-	-	GND (Bank 2)	-	-	-	-	-
AH11	BK2_IO23	-	53N	BK2_IO11	-	31N	BK2_IO11	-	27N
AJ10	BK2_IO24	-	54P	BK2_IO12		32P	BK2_IO12	-	28P
AK10	BK2_IO25	-	54N	BK2_IO13	-	32N	BK2_IO13	-	28N
AH12	BK2_IO26	-	55P	BK2_IO14	-	33P	BK2_IO14	-	29P
-	GND (Bank 2)	-	-	-	-	-	-	-	-
AJ11	BK2_IO27	-	55N	BK2_IO15	-	33N	BK2_IO15	-	29N
AK11	BK2_IO28	-	56P	NC	-	-	NC	-	-
AJ12	BK2_IO29	-	56N	NC	-	-	NC	-	-
AG13	BK2_IO30	-	57P	BK2_IO16	-	34P	BK2_IO16	-	30P
AH13	BK2_IO31	-	57N	BK2_IO17	-	34N	BK2_IO17	-	30N

ispXPGA Logic Signal Connections: 516-Ball fpBGA (Cont.)

516-Ball BGA Ball	LFX500			LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
AJ25	BK3_IO32	-	79P	NC	-	-	NC	-	-
AG24	BK3_IO33	-	79N	NC	-	-	NC	-	-
AK26	BK3_IO34	-	80P	BK3_IO20	-	49P	BK3_IO16	-	41P
-	-	-	-	-	-	-	GND (Bank 3)	-	-
AH25	BK3_IO35	-	80N	BK3_IO21	-	49N	BK3_IO17	-	41N
AJ26	BK3_IO36	-	81P	BK3_IO22	-	50P	BK3_IO18	-	42P
-	-	-	-	GND (Bank 3)	-	-	-	-	-
AH26	BK3_IO37	-	81N	BK3_IO23	-	50N	BK3_IO19	-	42N
AK27	BK3_IO38	-	82P	NC	-	-	NC	-	-
-	GND (Bank 3)	-	-	-	-	-	-	-	-
AJ27	BK3_IO39	-	82N	NC	-	-	NC	-	-
AG26	BK3_IO40	-	83P	BK3_IO24	-	51P	BK3_IO20	-	43P
AH27	BK3_IO41	-	83N	BK3_IO25	-	51N	BK3_IO21	-	43N
AK28	GSR	-	-	GSR	-	-	GSR	-	-
AJ28	DXP	-	-	DXP	-	-	DXP	-	-
AK29	DXN	-	-	DXN	-	-	DXN	-	-
AH29	BK4_IO0	-	84P	BK4_IO0	-	52P/HSI2	BK4_IO0	-	44P
AG28	BK4_IO1	-	84N	BK4_IO1	-	52N/HSI2	BK4_IO1	-	44N
AF27	BK4_IO2	-	85P/HSI3	NC	-	-	NC	-	-
-	GND (Bank 4)	-	-	-	-	-	-	-	-
AF28	BK4_IO3	-	85N/HSI3	NC	-	-	NC	-	-
AJ30	BK4_IO4	-	86P/HSI3	NC	-	-	NC	-	-
AH30	BK4_IO5	-	86N/HSI3	NC	-	-	NC	-	-
AG29	BK4_IO6	-	87P/HSI3	NC	-	-	NC	-	-
AF29	BK4_IO7	-	87N/HSI3	NC	-	-	NC	-	-
AE28	BK4_IO8	-	88P/HSI3	NC	-	-	NC	-	-
AD27	BK4_IO9	-	88N/HSI3	NC	-	-	NC	-	-
AG30	BK4_IO10	HSI3A_SINP	89P/HSI3	BK4_IO2	HSI2A_SINP	53P/HSI2	BK4_IO2	-	45P
-	GND (Bank 4)	-	-	GND (Bank 4)	-	-	-	-	-
AF30	BK4_IO11	HSI3A_SINN	89N/HSI3	BK4_IO3	HSI2A_SINN	53N/HSI2	BK4_IO3	-	45N
AD28	BK4_IO12	-	90P/HSI3	BK4_IO4	-	54P/HSI2	BK4_IO4	-	46P
-	-	-	-	-	-	-	GND (Bank 4)	-	-
AC27	BK4_IO13	-	90N/HSI3	BK4_IO5	-	54N/HSI2	BK4_IO5	-	46N
AE29	BK4_IO14	HSI3A_SOUTP	91P/HSI3	BK4_IO6	HSI2A_SOUTP	55P/HSI2	NC	-	-
AE30	BK4_IO15	HSI3A_SOUTN	91N/HSI3	BK4_IO7	HSI2A_SOUTN	55N/HSI2	NC	-	-
AD29	BK4_IO16	-	92P/HSI3	BK4_IO8	-	56P/HSI2	BK4_IO6	-	47P
AD30	BK4_IO17	VREF4	92N/HSI3	BK4_IO9	VREF4	56N/HSI2	BK4_IO7	VREF4	47N
AC28	BK4_IO18	HSI3B_SINP	93P	BK4_IO10	HSI2B_SINP	57P/HSI2	NC	-	-
-	GND (Bank 4)	-	-	GND (Bank 4)	-	-	-	-	-
AB28	BK4_IO19	HSI3B_SINN	93N	BK4_IO11	HSI2B_SINN	57N/HSI2	NC	-	-
AA27	BK4_IO20	PLL_RST4	94P	BK4_IO12	PLL_RST4	58P/HSI2	BK4_IO8	PLL_RST4	48P
AB29	BK4_IO21	PLL_RST5	94N	BK4_IO13	PLL_RST5	58N/HSI2	BK4_IO9	PLL_RST5	48N
AC29	BK4_IO22	HSI3B_SOUTP	95P	BK4_IO14	HSI2B_SOUTP	59P/HSI2	BK4_IO10	-	49P
AC30	BK4_IO23	HSI3B_SOUTN	95N	BK4_IO15	HSI2B_SOUTN	59N/HSI2	BK4_IO11	-	49N
AA28	BK4_IO24	-	96P	NC	-	-	NC	-	-
Y27	BK4_IO25	-	96N	NC	-	-	NC	-	-
Y28	BK4_IO26	-	97P	NC	-	-	NC	-	-
-	GND (Bank 4)	-	-	-	-	-	-	-	-
AA29	BK4_IO27	-	97N	NC	-	-	NC	-	-
Y29	BK4_IO28	-	98P	BK4_IO16	-	60P	BK4_IO12	-	50P
-	-	-	-	-	-	-	GND (Bank 4)	-	-

ispXPGA Logic Signal Connections: 516-Ball fpBGA (Cont.)

516-Ball BGA Ball	LFX500			LFX200			LFX125		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
D21	BK6_IO20	-	136P	BK6_IO8	-	82P	BK6_IO8	-	70P
C21	BK6_IO21	VREF6	136N	BK6_IO9	VREF6	82N	BK6_IO9	VREF6	70N
B21	BK6_IO22	DATA5	137P	BK6_IO10	DATA5	83P	BK6_IO10	DATA5	71P
-	-	-	-	GND (Bank 6)	-	-	-	-	-
A21	BK6_IO23	DATA4	137N	BK6_IO11	DATA4	83N	BK6_IO11	DATA4	71N
D20	BK6_IO24	-	138P	BK6_IO12	-	84P	BK6_IO12	-	72P
-	-	-	-	-	-	-	GND (Bank 6)	-	-
C20	BK6_IO25	-	138N	BK6_IO13	-	84N	BK6_IO13	-	72N
B20	BK6_IO26	DATA3	139P	BK6_IO14	DATA3	85P	BK6_IO14	DATA3	73P
-	GND (Bank 6)	-	-	-	-	-	-	-	-
A20	BK6_IO27	DATA2	139N	BK6_IO15	DATA2	85N	BK6_IO15	DATA2	73N
C19	BK6_IO28	-	140P	BK6_IO16		86P	BK6_IO16	-	74P
B19	BK6_IO29	-	140N	BK6_IO17		86N	BK6_IO17	-	74N
A19	BK6_IO30	DATA1	141P	BK6_IO18	DATA1	87P	BK6_IO18	DATA1	75P
-	-	-	-	GND (Bank 6)	-	-	GND (Bank 6)	-	-
A18	BK6_IO31	DATA0	141N	BK6_IO19	DATA0	87N	BK6_IO19	DATA0	75N
D18	BK6_IO32	-	142P	BK6_IO20		88P	BK6_IO20	-	76P
C18	BK6_IO33	-	142N	BK6_IO21		88N	BK6_IO21	-	76N
B18	BK6_IO34	-	143P	BK6_IO22		89P	NC	-	-
-	GND (Bank 6)	-	-	-	-	-	-	-	-
C17	BK6_IO35	-	143N	BK6_IO23		89N	NC	-	-
B17	BK6_IO36	-	144P	NC	-	-	NC	-	-
A17	BK6_IO37	-	144N	NC	-	-	NC	-	-
D16	BK6_IO38	-	145P	NC	-	-	NC	-	-
C16	BK6_IO39	-	145N	NC	-	-	NC	-	-
B16	BK6_IO40	-	146P	BK6_IO24	-	90P	NC	-	-
A16	BK6_IO41	-	146N	BK6_IO25	-	90N	NC	-	-
-	GND (Bank 6)	-	-	GND (Bank 6)	-	-	-	-	-
-	GND (Bank 7)	-	-	GND (Bank 7)	-	-	-	-	-
A15	BK7_IO0	-	147P	BK7_IO0	-	91P	BK7_IO0	-	77P
B15	BK7_IO1	-	147N	BK7_IO1	-	91N	BK7_IO1	-	77N
C15	BK7_IO2	-	148P	BK7_IO2	-	92P	BK7_IO2	-	78P
-	-	-	-	-	-	-	GND (Bank 7)	-	-
D15	BK7_IO3	-	148N	BK7_IO3	-	92N	BK7_IO3	-	78N
A14	BK7_IO4	-	149P	BK7_IO4	-	93P	BK7_IO4	-	79P
B14	BK7_IO5	-	149N	BK7_IO5	-	93N	BK7_IO5	-	79N
C14	BK7_IO6	-	150P	BK7_IO6	-	94P	NC	-	-
-	GND (Bank 7)	-	-	GND (Bank 7)	-	-	-	-	-
A13	BK7_IO7	-	150N	BK7_IO7	-	94N	NC	-	-
B13	BK7_IO8	-	151P	BK7_IO8	-	95P	NC	-	-
C13	BK7_IO9	-	151N	BK7_IO9	-	95N	NC	-	-
D13	BK7_IO10	-	152P	BK7_IO10	-	96P	BK7_IO6	-	80P
B12	BK7_IO11	-	152N	BK7_IO11	-	96N	BK7_IO7	-	80N
C12	BK7_IO12	-	153P	BK7_IO12	-	97P	BK7_IO8	-	81P
-	-	-	-	-	-	-	GND (Bank 7)	-	-
A12	BK7_IO13	-	153N	BK7_IO13		97N	BK7_IO9	-	81N
A11	BK7_IO14	-	154P	BK7_IO14	-	98P	BK7_IO10	-	82P
-	GND (Bank 7)	-	-	GND (Bank 7)	-	-	-	-	-
B11	BK7_IO15	-	154N	BK7_IO15	-	98N	BK7_IO11	-	82N
C11	BK7_IO16	-	155P	NC	-	-	NC	-	-
D11	BK7_IO17	-	155N	NC	-	-	NC	-	-

ispXPGA Logic Signal Connections: 680-Ball fpBGA

LFX1200			
680-Ball fpBGA	**Signal Name**	**Second Function**	**LVDS Pair/sysHSI Reserved[1]**
C4	BK0_IO0	-	0P
B4	BK0_IO1	-	0N
E6	BK0_IO2	-	1P
-	GND (Bank 0)	-	-
D6	BK0_IO3	-	1N
A4	BK0_IO4	-	2P
E8	BK0_IO5	-	2N
C5	BK0_IO6	HSI0A_SOUTP	3P
C6	BK0_IO7	HSI0A_SOUTN	3N
A6	BK0_IO8	-	4P
A5	BK0_IO9	-	4N
B6	BK0_IO10	HSI0A_SINP	5P/HSI0
-	GND (Bank 0)	-	-
B5	BK0_IO11	HSI0A_SINN	5N/HSI0
B7	BK0_IO12	VREF0	6P/HSI0
A7	BK0_IO13	-	6N/HSI0
D8	BK0_IO14	HSI0B_SOUTP	7P/HSI0
D7	BK0_IO15	HSI0B_SOUTN	7N/HSI0
D9	BK0_IO16	-	8P/HSI0
E10	BK0_IO17	-	8N/HSI0
C8	BK0_IO18	HSI0B_SINP	9P/HSI0
-	GND (Bank 0)	-	-
C7	BK0_IO19	HSI0B_SINN	9N/HSI0
A8	BK0_IO20	-	10P/HSI0
A9	BK0_IO21	-	10N/HSI0
C9	BK0_IO22	HSI1A_SOUTP	11P/HSI0
B8	BK0_IO23	HSI1A_SOUTN	11N/HSI0
B9	BK0_IO24	-	12P/HSI0
B10	BK0_IO25	-	12N/HSI0
D11	BK0_IO26	HSI1A_SINP	13P/HSI1
-	GND (Bank 0)	-	-
D10	BK0_IO27	HSI1A_SINN	13N/HSI1
A10	BK0_IO28	-	14P/HSI1
C12	BK0_IO29	-	14N/HSI1
D12	BK0_IO30	HSI1B_SOUTP	15P/HSI1
C11	BK0_IO31	HSI1B_SOUTN	15N/HSI1
A12	BK0_IO32	-	16P/HSI1
A13	BK0_IO33	-	16N/HSI1
B13	BK0_IO34	HSI1B_SINP	17P/HSI1
-	GND (Bank 0)	-	-
B12	BK0_IO35	HSI1B_SINN	17N/HSI1
E14	BK0_IO36	-	18P/HSI1

ispXPGA Logic Signal Connections: 680-Ball fpBGA (Cont.)

LFX1200			
680-Ball fpBGA	**Signal Name**	**Second Function**	**LVDS Pair/sysHSI Reserved[1]**
A33	BK1_IO45	-	53N/HSI4
C33	BK1_IO46	HSI4A_SINP	54P/HSI4
B33	BK1_IO47	HSI4A_SINN	54N/HSI4
A34	BK1_IO48	-	55P/HSI4
A35	BK1_IO49	VREF1	55N/HSI4
D32	BK1_IO50	HSI4B_SOUTP	56P/HSI4
-	GND (Bank 1)	-	-
D33	BK1_IO51	HSI4B_SOUTN	56N/HSI4
E32	BK1_IO52	-	57P
C34	BK1_IO53	-	57N
B34	BK1_IO54	HSI4B_SINP	58P
B35	BK1_IO55	HSI4B_SINN	58N
A36	BK1_IO56	-	59P
D34	BK1_IO57	-	59N
C35	BK1_IO58	-	60P
-	GND (Bank 1)	-	-
E34	BK1_IO59	-	60N
B36	BK1_IO60	-	61P
C36	BK1_IO61	-	61N
D39	TCK	-	-
D37	TMS	-	-
D38	TOE	-	-
E37	BK2_IO0	-	62P
F35	BK2_IO1	-	62N
E39	BK2_IO2	-	63P
-	GND (Bank 2)	-	-
F39	BK2_IO3	-	63N
F36	BK2_IO4	-	64P
E38	BK2_IO5	-	64N
G38	BK2_IO6	-	65P
F37	BK2_IO7	-	65N
G36	BK2_IO8	-	66P
G39	BK2_IO9	-	66N
H35	BK2_IO10	-	67P
-	GND (Bank 2)	-	-
F38	BK2_IO11	-	67N
J37	BK2_IO12	VREF2	68P
H36	BK2_IO13	-	68N
G37	BK2_IO14	-	69P
H37	BK2_IO15	-	69N
H39	BK2_IO16	-	70P
K35	BK2_IO17	-	70N
J36	BK2_IO18	-	71P

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
-	-	-	-	GND (Bank 1)	-	-
T1	BK1_IO1	CLK_OUT3	31N	BK1_IO1	CLK_OUT3	21N
U2	BK1_IO2	SS_CLKOUT0P	32P	BK1_IO2	SS_CLKOUT0P	22P
-	GND (Bank 1)	-	-	-	-	-
U1	BK1_IO3	SS_CLKOUT0N	32N	BK1_IO3	SS_CLKOUT0N	22N
U3	BK1_IO4	PLL_FBK2	33P	BK1_IO4	PLL_FBK2	23P
U4	BK1_IO5	PLL_FBK3	33N	BK1_IO5	PLL_FBK3	23N
V1	BK1_IO6	SS_CLKIN0P	34P	BK1_IO10	SS_CLKIN0P	26P
V2	BK1_IO7	SS_CLKIN0N	34N	BK1_IO11	SS_CLKIN0N	26N
U5	BK1_IO8	-	35P	BK1_IO12	-	27P
U6	BK1_IO9	-	35N	BK1_IO13	-	27N
V4	BK1_IO10	-	36P	BK1_IO6	-	24P
-	GND (Bank 1)	-	-	GND (Bank 1)	-	-
V3	BK1_IO11	-	36N	BK1_IO7	-	24N
V6	BK1_IO12	PLL_RST2	37P	BK1_IO20	PLL_RST2	31P
V7	BK1_IO13	PLL_RST3	37N	BK1_IO21	PLL_RST3	31N
W1	BK1_IO14	-	38P	BK1_IO8	-	25P
W2	BK1_IO15	-	38N	BK1_IO9	-	25N
W3	BK1_IO16	-	39P	BK1_IO14	-	28P
-	-	-	-	GND (Bank 1)	-	-
W4	BK1_IO17	-	39N	BK1_IO15	-	28N
W5	BK1_IO18	-	40P	BK1_IO16	-	29P
-	GND (Bank 1)	-	-	-	-	-
W6	BK1_IO19	-	40N	BK1_IO17	-	29N
Y6	BK1_IO20	-	41P/HSI3	NC	-	-
Y5	BK1_IO21	-	41N/HSI3	NC	-	-
Y4	BK1_IO22	-	42P/HSI3	NC	-	-
Y3	BK1_IO23	-	42N/HSI3	NC	-	-
AA5	BK1_IO24	-	43P/HSI3	NC	-	-
AA4	BK1_IO25	-	43N/HSI3	NC	-	-
Y2	BK1_IO26	HSI3A_SOUTP	44P/HSI3	BK1_IO18	HSI2A_SOUTP	30P
-	GND (Bank 1)	-	-	-	-	-
Y1	BK1_IO27	HSI3A_SOUTN	44N/HSI3	BK1_IO19	HSI2A_SOUTN	30N
AB7	BK1_IO28	-	45P/HSI3	NC	-	-
AB6	BK1_IO29	-	45N/HSI3	NC	-	-
AA2	BK1_IO30	HSI3A_SINP	46P/HSI3	BK1_IO22	HSI2A_SINP	32P
-	-	-	-	GND (Bank 1)	-	-
AA1	BK1_IO31	HSI3A_SINN	46N/HSI3	BK1_IO23	HSI2A_SINN	32N
AB5	BK1_IO32	-	47P/HSI3	NC	-	-
AB4	BK1_IO33	-	47N/HSI3	NC	-	-
AB2	BK1_IO34	HSI3B_SOUTP	48P/HSI3	NC	-	-
-	GND (Bank 1)	-	-	-	-	-

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
AC27	BK4_IO21	-	134N/HSI5	NC	-	-
AD29	BK4_IO22	HSI6A_SINP	135P/HSI5	NC	-	-
AD30	BK4_IO23	HSI6A_SINN	135N/HSI5	NC	-	-
AB24	BK4_IO24	-	136P/HSI5	NC	-	-
AB25	BK4_IO25	-	136N/HSI5	NC	-	-
AC29	BK4_IO26	HSI6A_SOUTP	137P/HSI6	NC	-	-
-	GND (Bank 4)	-	-	-	-	-
AC30	BK4_IO27	HSI6A_SOUTN	137N/HSI6	NC	-	-
AB27	BK4_IO28	-	138P/HSI6	NC	-	-
AB26	BK4_IO29	-	138N/HSI6	NC	-	-
AB30	BK4_IO30	HSI6B_SINP	139P/HSI6	BK4_IO18	HSI3B_SINP	93P
-	-	-	-	GND (Bank 4)	-	-
AB29	BK4_IO31	HSI6B_SINN	139N/HSI6	BK4_IO19	HSI3B_SINN	93N
AA26	BK4_IO32	-	140P/HSI6	NC	-	-
AA27	BK4_IO33	-	140N/HSI6	NC	-	-
AA30	BK4_IO34	HSI6B_SOUTP	141P/HSI6	BK4_IO22	HSI3B_SOUTP	95P
-	GND (Bank 4)	-	-	-	-	-
AA29	BK4_IO35	HSI6B_SOUTN	141N/HSI6	BK4_IO23	HSI3B_SOUTN	95N
Y25	BK4_IO36	-	142P/HSI6	NC	-	-
Y26	BK4_IO37	-	142N/HSI6	NC	-	-
Y28	BK4_IO38	-	143P/HSI6	NC	-	-
Y27	BK4_IO39	-	143N/HSI6	NC	-	-
W25	BK4_IO40	-	144P/HSI6	NC	-	-
W26	BK4_IO41	-	144N/HSI6	NC	-	-
W27	BK4_IO42	-	145P	BK4_IO24	-	96P
-	GND (Bank 4)	-	-	-	-	-
W28	BK4_IO43	-	145N	BK4_IO25	-	96N
V24	BK4_IO44	-	146P	BK4_IO26	-	97P
-	-	-	-	GND (Bank 4)	-	-
V25	BK4_IO45	-	146N	BK4_IO27	-	97N
Y29	BK4_IO46	-	147P	BK4_IO32	-	100P
Y30	BK4_IO47	-	147N	BK4_IO33	-	100N
V27	BK4_IO48	PLL_RST4	148P	BK4_IO20	PLL_RST4	94P
V28	BK4_IO49	PLL_RST5	148N	BK4_IO21	PLL_RST5	94N
W29	BK4_IO50	-	149P	BK4_IO34	-	101P
-	GND (Bank 4)	-	-	GND (Bank 4)	-	-
W30	BK4_IO51	-	149N	BK4_IO35	-	101N
U25	BK4_IO52	-	150P	BK4_IO28	-	98P
U26	BK4_IO53	-	150N	BK4_IO29	-	98N
V29	BK4_IO54	SS_CLKIN1P	151P	BK4_IO30	SS_CLKIN1P	99P
V30	BK4_IO55	SS_CLKIN1N	151N	BK4_IO31	SS_CLKIN1N	99N
U28	BK4_IO56	PLL_FBK4	152P	BK4_IO36	PLL_FBK4	102P

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
K30	BK5_IO22	HSI7B_SOUTP	166P/HSI8	BK5_IO22	HSI4B_SOUTP	116P/HSI4
-	-	-	-	GND (Bank 5)	-	-
K29	BK5_IO23	HSI7B_SOUTN	166N/HSI8	BK5_IO23	HSI4B_SOUTN	116N/HSI4
L28	BK5_IO24	-	167P/HSI8	BK5_IO24	-	117P/HSI5
L27	BK5_IO25	-	167N/HSI8	BK5_IO25	-	117N/HSI5
L26	BK5_IO26	HSI8A_SINP	168P/HSI8	BK5_IO26	HSI5A_SINP	118P/HSI5
-	GND (Bank 5)	-	-	-	-	-
L25	BK5_IO27	HSI8A_SINN	168N/HSI8	BK5_IO27	HSI5A_SINN	118N/HSI5
K27	BK5_IO28	-	169P/HSI8	BK5_IO28	-	119P/HSI5
K26	BK5_IO29	-	169N/HSI8	BK5_IO29	-	119N/HSI5
J30	BK5_IO30	HSI8A_SOUTP	170P/HSI8	BK5_IO30	HSI5A_SOUTP	120P/HSI5
-	-	-	-	GND (Bank 5)	-	-
J29	BK5_IO31	HSI8A_SOUTN	170N/HSI8	BK5_IO31	HSI5A_SOUTN	120N/HSI5
J26	BK5_IO32	-	171P/HSI8	NC	-	-
J27	BK5_IO33	-	171N/HSI8	NC	-	-
H30	BK5_IO34	HSI8B_SINP	172P/HSI8	NC	-	-
-	GND (Bank 5)	-	-	-	-	-
H29	BK5_IO35	HSI8B_SINN	172N/HSI8	NC	-	-
J25	BK5_IO36	-	173P/HSI9	NC	-	-
J24	BK5_IO37	-	173N/HSI9	NC	-	-
G30	BK5_IO38	HSI8B_SOUTP	174P/HSI9	NC	-	-
G29	BK5_IO39	HSI8B_SOUTN	174N/HSI9	NC	-	-
H27	BK5_IO40	-	175P/HSI9	NC	-	-
H28	BK5_IO41	-	175N/HSI9	NC	-	-
F30	BK5_IO42	HSI9A_SINP	176P/HSI9	NC	-	-
-	GND (Bank 5)	-	-	-	-	-
F29	BK5_IO43	HSI9A_SINN	176N/HSI9	NC	-	-
G27	BK5_IO44	-	177P/HSI9	NC	-	-
G28	BK5_IO45	-	177N/HSI9	NC	-	-
E30	BK5_IO46	HSI9A_SOUTP	178P/HSI9	NC	-	-
E29	BK5_IO47	HSI9A_SOUTN	178N/HSI9	NC	-	-
H26	BK5_IO48	-	179P/HSI9	BK5_IO33	-	121N/HSI5
H25	BK5_IO49	VREF5	179N/HSI9	BK5_IO32	VREF5	121P/HSI5
D30	BK5_IO50	HSI9B_SINP	180P/HSI9	BK5_IO34	HSI5B_SINP	122P/HSI5
-	GND (Bank 5)	-	-	-	-	-
D29	BK5_IO51	HSI9B_SINN	180N/HSI9	BK5_IO35	HSI5B_SINN	122N/HSI5
F28	BK5_IO52	-	181P	BK5_IO36	-	123P/HSI5
F27	BK5_IO53	-	181N	BK5_IO37	-	123N/HSI5
C30	BK5_IO54	HSI9B_SOUTP	182P	BK5_IO38	HSI5B_SOUTP	124P/HSI5
-	-	-	-	GND (Bank 5)	-	-
C29	BK5_IO55	HSI9B_SOUTN	182N	BK5_IO39	HSI5B_SOUTN	124N/HSI5
G26	BK5_IO56	-	183P	NC	-	-

"E-Series" Commercial

Part Number	Gates	Voltage	Speed Grade	Package	Balls
LFX125EB-05F256C	139K	2.5/3.3	-5	fpBGA	256
LFX125EB-04F256C	139K	2.5/3.3	-4	fpBGA	256
LFX125EB-03F256C	139K	2.5/3.3	-3	fpBGA	256
LFX125EC-04F256C	139K	1.8	-4	fpBGA	256
LFX125EC-03F256C	139K	1.8	-3	fpBGA	256
LFX125EB-05F516C	139K	2.5/3.3	-5	fpBGA	516
LFX125EB-04F516C	139K	2.5/3.3	-4	fpBGA	516
LFX125EB-03F516C	139K	2.5/3.3	-3	fpBGA	516
LFX125EC-04F516C	139K	1.8	-4	fpBGA	516
LFX125EC-03F516C	139K	1.8	-3	fpBGA	516
LFX125EB-05FH516C[1]	139K	2.5/3.3	-5	fpBGA	516
LFX125EB-04FH516C[1]	139K	2.5/3.3	-4	fpBGA	516
LFX125EB-03FH516C[1]	139K	2.5/3.3	-3	fpBGA	516
LFX125EC-04FH516C[1]	139K	1.8	-4	fpBGA	516
LFX125EC-03FH516C[1]	139K	1.8	-3	fpBGA	516
LFX200EB-05F256C	210K	2.5/3.3	-5	fpBGA	256
LFX200EB-04F256C	210K	2.5/3.3	-4	fpBGA	256
LFX200EB-03F256C	210K	2.5/3.3	-3	fpBGA	256
LFX200EC-04F256C	210K	1.8	-4	fpBGA	256
LFX200EC-03F256C	210K	1.8	-3	fpBGA	256
LFX200EB-05F516C	210K	2.5/3.3	-5	fpBGA	516
LFX200EB-04F516C	210K	2.5/3.3	-4	fpBGA	516
LFX200EB-03F516C	210K	2.5/3.3	-3	fpBGA	516
LFX200EC-04F516C	210K	1.8	-4	fpBGA	516
LFX200EC-03F516C	210K	1.8	-3	fpBGA	516
LFX200EB-05FH516C[1]	210K	2.5/3.3	-5	fpBGA	516
LFX200EB-04FH516C[1]	210K	2.5/3.3	-4	fpBGA	516
LFX200EB-03FH516C[1]	210K	2.5/3.3	-3	fpBGA	516
LFX200EC-04FH516C[1]	210K	1.8	-4	fpBGA	516
LFX200EC-03FH516C[1]	210K	1.8	-3	fpBGA	516
LFX500EB-05F516C	476K	2.5/3.3	-5	fpBGA	516
LFX500EB-04F516C	476K	2.5/3.3	-4	fpBGA	516
LFX500EB-03F516C	476K	2.5/3.3	-3	fpBGA	516
LFX500EC-04F516C	476K	1.8	-4	fpBGA	516
LFX500EC-03F516C	476K	1.8	-3	fpBGA	516
LFX500EB-05FH516C[1]	476K	2.5/3.3	-5	fpBGA	516
LFX500EB-04FH516C[1]	476K	2.5/3.3	-4	fpBGA	516
LFX500EB-03FH516C[1]	476K	2.5/3.3	-3	fpBGA	516
LFX500EC-04FH516C[1]	476K	1.8	-4	fpBGA	516
LFX500EC-03FH516C[1]	476K	1.8	-3	fpBGA	516
LFX500EB-05F900C	476K	2.5/3.3	-5	fpBGA	900
LFX500EB-04F900C	476K	2.5/3.3	-4	fpBGA	900
LFX500EB-03F900C	476K	2.5/3.3	-3	fpBGA	900
LFX500EC-04F900C	476K	1.8	-4	fpBGA	900