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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	2704
Total RAM Bits	113664
Number of I/O	336
Number of Gates	476000
Voltage - Supply	2.3V ~ 3.6V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 105°C (TJ)
Package / Case	516-BBGA
Supplier Device Package	516-FPBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/lfx500eb-04f516i

Product Line	Ordering Part Number	Product Status	Reference PCN
LFX500B	LFX500B-03F516C	**Discontinued**	PCN#09-10
	LFX500B-04F516C		
	LFX500B-05F516C		
	LFX500B-03F900C		
	LFX500B-03FN900C		
	LFX500B-04F900C		
	LFX500B-04FN900C		
	LFX500B-05F900C		
	LFX500B-05FN900C		
LFX500C	LFX500C-03F516C	**Discontinued**	PCN#09-10
	LFX500C-04F516C		
	LFX500C-03F900C		
	LFX500C-03FN900C		
	LFX500C-04F900C		
	LFX500C-04FN900C		
LFX1200B	LFX1200B-03FE680C	**Discontinued**	PCN#03A-10
	LFX1200B-04FE680C		
	LFX1200B-05FE680C		
	LFX1200B-03F900C		
	LFX1200B-04F900C		
	LFX1200B-05F900C		
LFX1200C	LFX1200C-03FE680C	**Discontinued**	PCN#03A-10
	LFX1200C-04FE680C		
	LFX1200C-03F900C		
	LFX1200C-04F900C		
LFX125EB	LFX125EB-03F256C	Active / Orderable	
	LFX125EB-03FN256C		
	LFX125EB-04F256C		
	LFX125EB-04FN256C		
	LFX125EB-05F256C		
	LFX125EB-05FN256C		
	LFX125EB-03F256I		
	LFX125EB-03FN256I		
	LFX125EB-04F256I		
	LFX125EB-04FN256I		
	LFX125EB-03F516C	**Discontinued**	PCN#09-10
	LFX125EB-04F516C		
	LFX125EB-05F516C		
	LFX125EB-03F516I		
	LFX125EB-04F516I		
LFX125EC	LFX125EC-03F256C	**Discontinued**	PCN#09-10
	LFX125EC-03FN256C		
	LFX125EC-04F256C		
	LFX125EC-04FN256C		
	LFX125EC-03F256I		
	LFX125EC-03FN256I		

ispXPGA® Family

Includes High-Performance, Low-Cost "E-Series"

February 2010 Data Sheet DS1026

SELECT DEVICES DISCONTINUED

Non-volatile, Infinitely Reconfigurable
- Instant-on - Powers up in microseconds via on-chip E^2CMOS® based memory
- No external configuration memory
- Excellent design security, no bit stream to intercept
- Reconfigure SRAM based logic in milliseconds

High Logic Density for System-level Integration
- 139K to 1.25M functional gates
- 160 to 496 I/O
- 1.8V, 2.5V, and 3.3V V_{CC} operation
- Up to 414Kb sysMEM™ embedded memory

High Performance Programmable Function Unit (PFU)
- Four LUT-4 per PFU supports wide and narrow functions
- Dual flip-flops per LUT-4 for extensive pipelining
- Dedicated logic for adders, multipliers, multiplexers, and counters

Flexible Memory Resources
- Multiple sysMEM Embedded RAM Blocks
  - Single port, Dual port, and FIFO operation
- 64-bit distributed memory in each PFU
  - Single port, Double port, FIFO, and Shift Register operation

Flexible Programming, Reconfiguration, and Testing
- Supports IEEE 1532 and 1149.1
- Microprocessor configuration interface
- Program E^2CMOS while operating from SRAM

Eight sysCLOCK™ Phase Locked Loops (PLLs) for Clock Management
- True PLL technology
- 10MHz to 320MHz operation
- Clock multiplication and division
- Phase adjustment
- Shift clocks in 250ps steps

sysIO™ for High System Performance
- High speed memory support through SSTL and HSTL
- Advanced buses supported through PCI, GTL+, LVDS, BLVDS, and LVPECL
- Standard logic supported through LVTTL, LVCMOS 3.3, 2.5 and 1.8
- 5V tolerant I/O for LVCMOS 3.3 and LVTTL interfaces
- Programmable drive strength for series termination
- Programmable bus maintenance

Two Options Available
- High-performance sysHSI (standard part number)
- Low-cost, no sysHSI ("E-Series")

sysHSI™ Capability for Ultra Fast Serial Communications
- Up to 800Mbps performance
- Up to 20 channels per device
- Built in Clock Data Recovery (CDR) and Serialization and De-serialization (SERDES)

Table 1. ispXPGA Family Selection Guide

	ispXPGA 125/E	ispXPGA 200/E	ispXPGA 500/E	ispXPGA 1200/E[3]
Functional Gates	139K	210K	476K	1.25M
PFUs	484	676	1764	3844
LUT-4s	1936	2704	7056	15376
Logic FFs	3.8K	5.4K	14.1K	30.7K
sysMEM Memory	92K	111K	184K	414K
Distributed Memory	30K	43K	112K	246K
EBR	20	24	40	90
sysHSI Channels[1]	4	8	12	20
User I/O	160/176	160/208	336	496
Packaging	256 fpBGA 516 fpBGA[2]	256 fpBGA 516 fpBGA[2]	516 fpBGA[2] 900 fpBGA	680 fpSBGA 900 fpBGA

1. "E-Series" does not support sysHSI.
2. FH516 package was converted to F516 via PCN #09A-08.
3. Discontinued via PCN #03A-10.

Architecture Overview

The ispXPGA architecture is a symmetrical architecture consisting of an array of Programmable Function Units (PFUs) enclosed by Input Output Groups (PICs) with columns of sysMEM Embedded Block RAMs (EBRs) distributed throughout the array. Figure 1 illustrates the ispXPGA architecture. Each PIC has two corresponding sysIO blocks, each of which includes one input and output buffer. On two sides of the device, between the PICs and the sysIO blocks, there are sysHSI High-Speed Interface blocks. The symmetrical architecture allows designers to easily implement their designs, since any logic function can be placed in any section of the device.

The PFUs contain the basic building blocks to create logic, memory, arithmetic, and register functions. They are optimized for speed and flexibility allowing complex designs to be implemented quickly and efficiently.

The PICs interface the PFUs and EBRs to the external pins of the device. They allow the signals to be registered quickly to minimize setup times for high-speed designs. They also allow connections directly to the different logic elements for fast access to combinatorial functions.

The sysMEM EBRs are large, fast memory elements that can be configured as RAM, ROM, FIFO, and other storage types. They are designed to facilitate both single and dual-port memory for high-speed applications.

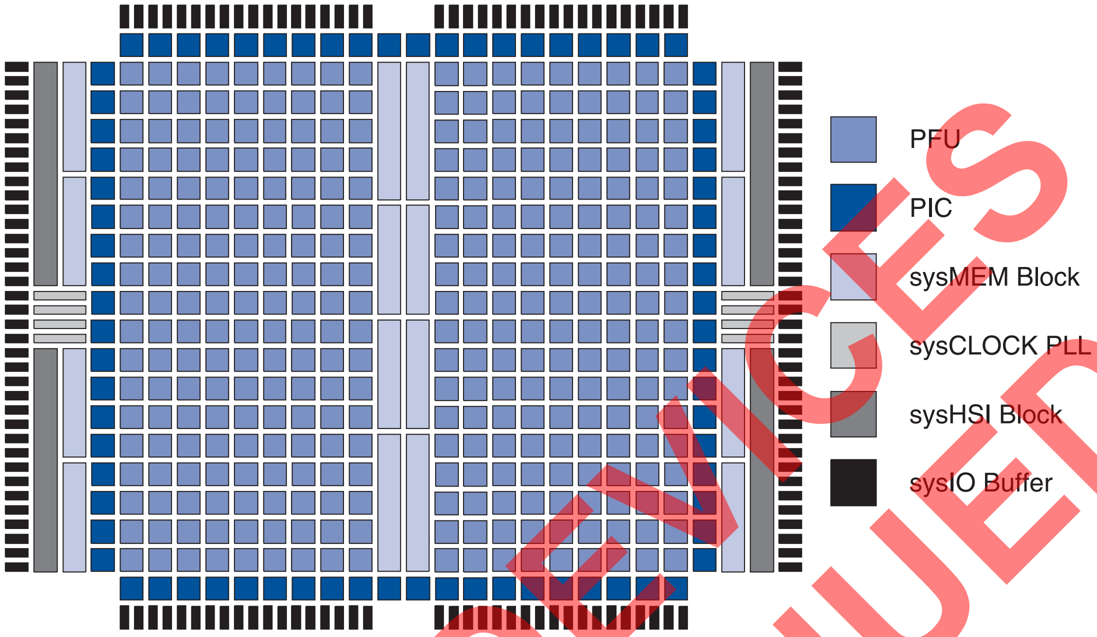
These three components of the architecture are interconnected via a high-speed, flexible routing array. The routing array consists of Variable Length Interconnect (VLI) lines between the PICs, PFUs, and EBRs. There is additional routing available to the PFU for feedback and direct routing of signals to adjacent PFUs or PICs.

The sysIO blocks consist of configurable input and output buffers connected directly to the PICs. These buffers can be configured to interface with 16 different I/O standards. This allows the ispXPGA to interface with other devices without the need for external transceivers.

The sysHSI blocks provide the necessary components to allow the ispXPGA device to transfer data at up to 800Mbps using the LVDS standard. These components include serializing, de-serializing, and clock data recovery (CDR) logic.

The sysCLOCK blocks provide clock multiplication/division, clock distribution, delay compensation, and increased performance through the use of PLL circuitry that manipulates the global clocks. There is one sysCLOCK block for each global clock tree in the device.

Figure 1. ispXPGA Block Diagram



Programmable Function Unit

The Programmable Function Unit (PFU) is the basic building block of the ispXPGA architecture. The PFUs are arranged in rows and columns in the device with PFU (1,1) referring to (row 1, column 1). Each PFU consists of four Configurable Logic Elements (CLEs), four Configurable Sequential Elements (CSEs), and a Wide Logic Generator (WLG). By utilizing these components, the PFU can implement a variety of functions. Table 3 lists some of the function capabilities of the PFU.

There are 57 inputs to each PFU and nine outputs. The PFU uses 20 inputs for logic, and 37 inputs drive the control logic from which six control signals are derived for the PFU.

Table 3. Function Capability of ispXPGA PFU

Function	Capability
Look-up table	LUT-4, LUT-5, LUT-6
Wide logic functions	Up to 20 input logic functions
Multiplexing	2:1, 4:1, 8:1
Arithmetic logic	Dedicated carry chain and booth multiplication logic
Single-port RAM	16X1, 16X2, 16X4, 32X1, 32X2, 64X1
Double-port RAM	16X1, 16X2, 32X1
Shift register	8-bit shift registers (up to 32-bit shift capability)

Configurable Logic Element

The CLE is made up of a four-input Look-up Table (LUT-4), a Carry Chain Generator (CCG), and a two-input AND gate. The LUT-4 creates various combinatorial and memory elements, the CCG creates a single one-bit full adder, and the two-input AND gate can expand the CCG to incorporate Booth Multiplier capability by feeding the output of the AND gate to one of the inputs of the CCG.

Of the five inputs that feed each CLE, two are dedicated inputs into each LUT-4 and the remaining three take on varying functionality. The third and fourth inputs can be used as either inputs to the LUT-4 or as a Feed-Thru to the CSE via the WLG. The fifth input can be a data port when the LUT is configured as Distributed Memory, a select line for multiplexer operation, or a Feed-Thru directly to the CSE via the WLG (Figure 2).

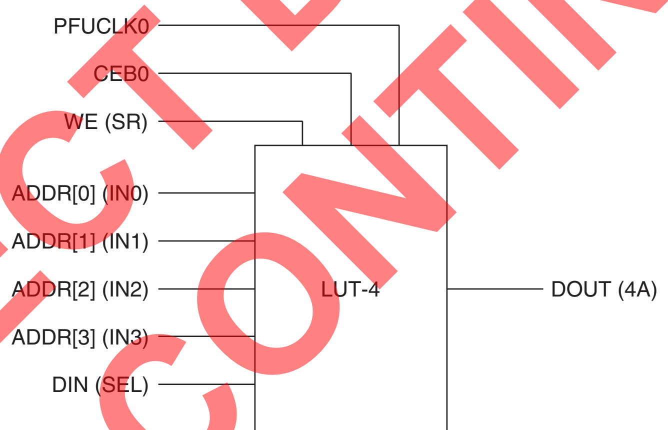
Look-Up Table – Combinatorial Mode

In combinatorial mode, the LUT-4 can implement any logic function up to four inputs. By using the carry chain and the WLG, each LUT-4 can be combined to form the enhanced functions listed in Table 3.

Look-Up Table – Distributed Memory Mode

In the distributed memory mode, the LUT functions as a memory element. The inputs to the LUT function as Address and Data. Each PFU is capable of implementing up to 64 SRAM bits. Both single and double port RAM can be performed in the PFU (Table 3). Furthermore, the distributed memory can be configured as either synchronous or asynchronous memory. Figure 3 illustrates the LUT while in distributed memory mode. When using any LUT in the PFU in memory mode, the Set/Reset signal will be used for Write Enable (WE(SR)) and the CLK0 signal will be used as the clock for synchronous read and write.

Figure 3. LUT in Distributed Memory Mode



Look-Up Table – Shift Register Mode

In the shift register mode, the LUT functions as a 1-bit to 8-bit shift register. This means that each PFU can implement up to four 8-bit shift registers or any cascaded combination. Figure 4 illustrates the LUT when configured in shift register mode.

Set/Reset signal controls all the registers for each PFU. This common Set/Reset signal is composed of the logical OR term of the Global Set/Reset signal (GSR) and the selected signal from routing. The polarity of this signal is not controllable inside the PFU. The polarity of the Global Set/Reset signal (GSR) is programmable. Figure 9 shows the Clock Enable and Output Enable selection for each PFU.

Figure 7. Clock Selection per PFU

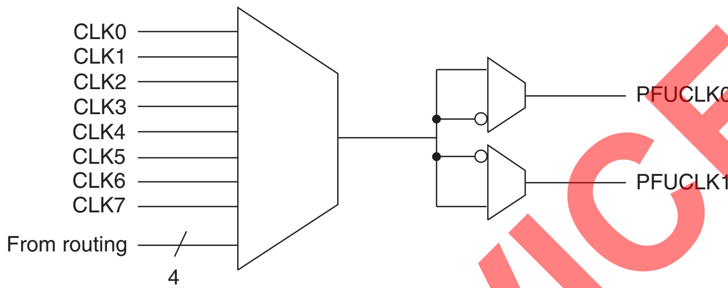


Figure 8. Set/Reset Selection per PFU

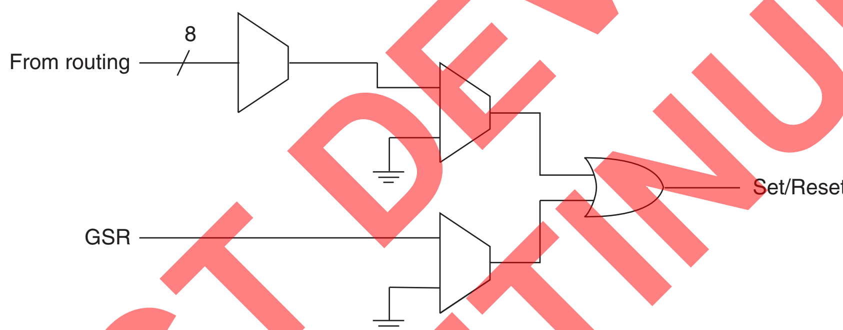
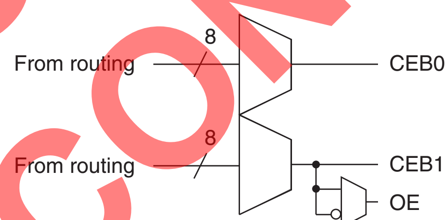


Figure 9. Clock Enable and Output Enable Selection per PFU



Programmable Input/Output Cell

The Programmable Input/Output Cell (PIC) is an essential part of the symmetrical architecture of the ispXPGA Family. The PICs interface the PFUs and EBRs to the sysIO and sysHSI blocks of the device.

Each PIC contains two Programmable Input/Outputs (PIOs) with a total of 21 inputs and 10 outputs. There are 18 inputs from routing, two inputs from the sysIO buffers, and the Global Set/Reset signal. Four outputs of the PIC connect to routing and two outputs are available as Output Enables for the tri-statable Long Lines. The remaining four outputs feed the sysIO buffers directly (one output enable and one output to each). Each PIC associated with a sysHSI block has four additional inputs and six additional outputs to support the sysHSI blocks. The four additional inputs come from the sysHSI block associated with the PIC. The four of the six additional outputs come from the PIC outputs and feed the sysHSI block, while the remaining two outputs feed routing. Figure 10 shows the block diagram of the PIC with the sysHSI block inputs and outputs.

The second type of interface implemented is the terminated, single-ended interface standard. This group of interfaces includes different versions of SSTL and HSTL interfaces along with CTT, and GTL+. Usage of these particular I/O interfaces requires an additional V_{REF} signal. At the system level a termination voltage, V_{TT}, is also required. Typically an output will be terminated to V_{TT} at the receiving end of the transmission line it is driving.

The third type of interface standards are the differential standards LVDS, BLVDS, and LVPECL. The differential standards require two I/O pins to create the differential pair. The logic level is determined by the difference in the two signals. Table 6 lists how these interface standards are implemented in the ispXPGA devices.

For more information on sysIO capability, refer to TN1000, sysIO Usage Guidelines for Lattice Devices.

Figure 19. sysIO Banks per Device

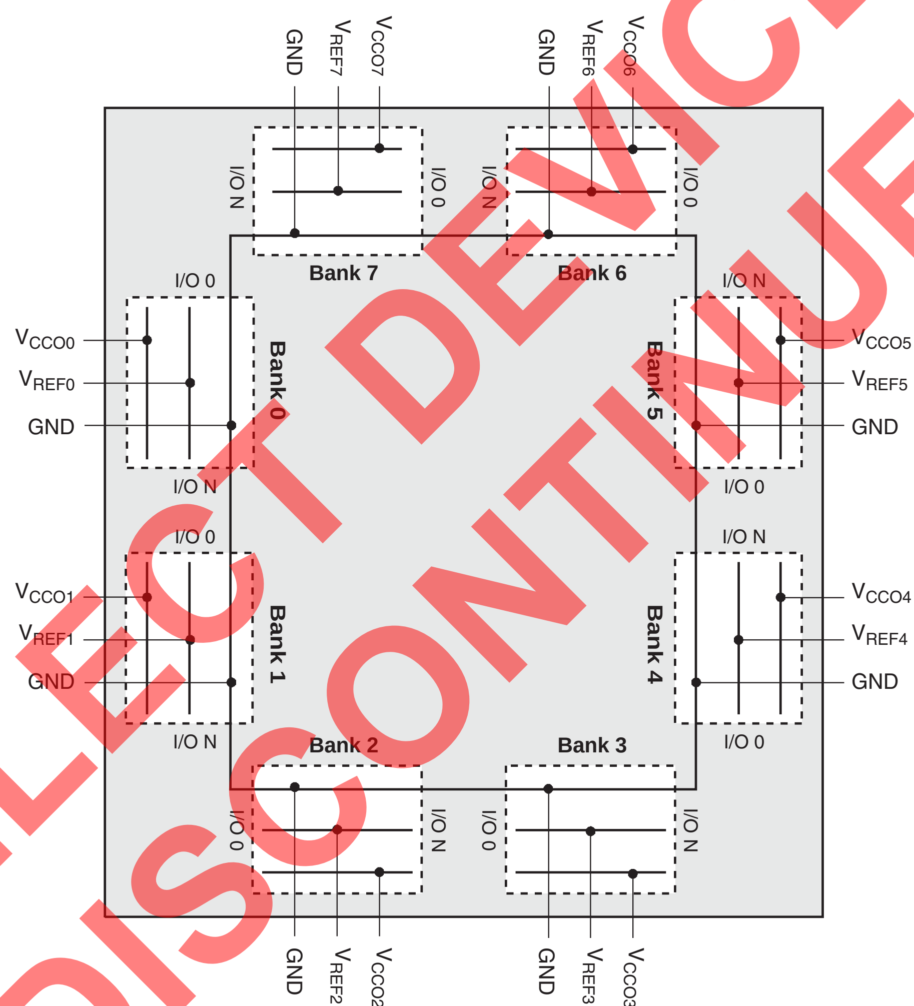


Table 4. Number of I/Os per Bank

Device	Max. Number of I/Os per Bank (N)
XPGA 1200	62
XPGA 500	42
XPGA 200	26
XPGA 125	22

DC Electrical Characteristics

Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{IL}, I_{IH}[1]	Input or I/O Low Leakage	0 ð V_{IN} < (V_{CCO} - 0.2V)	—	—	10	µA
		(V_{CCO} - 0.2V) ð V_{IN} ð 3.6V	—	—	300	µA
I_{IH}[2]	Input High Leakage Current	3.6V < V_{IN} ð 5.5V and 3.0V ð V_{CCO} ð 3.6V	—	—	3	mA
I_{PU}	I/O Active Pull-up Current	0 ð V_{IN} ð 0.7 V_{CCO}	-30	—	-150	µA
I_{PD}	I/O Active Pull-down Current	V_{IL} (MAX) ð V_{IN} ð V_{IH} (MAX)	30	—	150	µA
I_{BHLS}	Bus Hold Low Sustaining Current	V_{IN} = V_{IL} (MAX)	30	—	—	µA
I_{BHHS}	Bus Hold High Sustaining Current	V_{IN} = 0.7 V_{CCO}	-30	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive Current	0 ð V_{IN} ð V_{IH} (MAX)	—	—	150	µA
I_{BHHO}	Bus Hold High Overdrive Current	0 ð V_{IN} ð V_{IH} (MAX)	—	—	-150	µA
V_{BHT}	Bus Hold Trip Points		V_{CCO} * 0.35	—	V_{CCO} * 0.65	V
C_1	I/O Capacitance[3]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	8	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—	
C_2	Clock Capacitance[3]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	8	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—	
C_3	Global Input Capacitance[3]	V_{CCO} = 3.3V, 2.5V, 1.8V	—	6	—	pf
		V_{CC} = 1.8V, V_{IO} = 0 to V_{IH} (MAX)	—		—	

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. 5V tolerant inputs and I/Os should be placed in banks where 3.0V ð V_{CCO} ð 3.6V. The JTAG and sysCONFIG ports are not included for the 5V tolerant interface.
3. T_A = 25°C, f = 1.0MHz.

ispXPGA 500B/C & ispXPGA 500EB/EC EBR Timing Parameters

Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Synchronous Write								
t_{EBSWAD_S}	Address Setup Delay	0.59	—	0.61	—	0.70	—	ns
t_{EBSWAD_H}	Address Hold Delay	-0.40	—	-0.39	—	-0.33	—	ns
$t_{EBSWCPW}$	Clock Pulse Width	3.16	—	3.40	—	3.91	—	ns
t_{EBSWWE_S}	Write Enable Setup Time	-0.12	—	-0.12	—	-0.10	—	ns
t_{EBSWWE_H}	Write Enable Hold Time	0.16	—	0.16	—	0.18	—	ns
t_{EBSWD_S}	Data Setup Time	0.27	—	0.28	—	0.32	—	ns
t_{EBSWD_H}	Data Hold Time	-0.27	—	-0.26	—	-0.22	—	ns
Synchronous Read								
t_{EBSR_CO}	Clock to Data Delay	—	2.04	—	2.19	—	2.52	ns
t_{EBSRAD_S}	Address Setup Delay	0.10	—	0.10	—	0.12	—	ns
t_{EBSRAD_H}	Address Hold Delay	-0.07	—	-0.07	—	-0.06	—	ns
$t_{EBSRCPW}$	Clock Pulse Width	3.16	—	3.40	—	3.91	—	ns
t_{EBSRCE_S}	Clock Enable Setup Time	-1.76	—	-1.71	—	-1.45	—	ns
t_{EBSRCE_H}	Clock Enable Hold Time	1.64	—	1.69	—	1.94	—	ns
t_{EBSRWE_S}	Write Enable Setup Time	-0.18	—	-0.17	—	-0.14	—	ns
t_{EBSRWE_H}	Write Enable Hold Time	0.12	—	0.12	—	0.14	—	ns
$t_{EBSRWEEN}$	Write Enable to Data Enable Time	—	1.02	—	1.05	—	1.21	ns
$t_{EBSRWEDIS}$	Write Enable to Data Disable Time	—	0.99	—	1.02	—	1.17	ns
t_{EBSREN}	Output Enable to Data Enable Time	—	1.02	—	1.05	—	1.21	ns
$t_{EBSRDIS}$	Output Enable to Data Disable Time	—	0.83	—	0.86	—	0.99	ns
Asynchronous Read								
$t_{EBARADO}$	Address to New Valid Data Delay	—	2.39	—	2.46	—	2.83	ns
t_{EBARAD_H}	Address to Previous Valid Data Delay	—	2.10	—	2.17	—	2.50	ns
$t_{EBARWEEN}$	Write Enable to Data Enable Time	—	1.01	—	1.04	—	1.20	ns
$t_{EBARWEDIS}$	Write Enable to Data Disable Time	—	0.98	—	1.01	—	1.16	ns
t_{EBAREN}	Output Enable to Data Enable Time	—	1.02	—	1.05	—	1.21	ns
$t_{EBARDIS}$	Output Enable to Data Disable Time	—	0.83	—	0.86	—	0.99	ns

1. Only available for ispXPGA 500B and ispXPGA 500EB (2.5V/3.3V) devices.

Timing v.0.3

ispXPGA 1200B/C & ispXPGA 1200EB/EC External Switching Characteristics

Over Recommended Operating Conditions

Parameter	Description	Conditions	-5[1]		-4		-3		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{CO}	Global Clock Input to Output	PIO Output Register	—	6.6	—	7.1	—	8.2	ns
t_S	Global Clock Input Setup	PIO Input Register without input delay	-2.7	—	-2.7	—	-2.3	—	ns
t_H	Global Clock Input Hold	PIO Input Register without input delay	4.5	—	4.6	—	5.3	—	ns
t_{SINDLY}	Global Clock Input Setup	PIO Input Register with input delay	3.8	—	3.8	—	4.4	—	ns
t_{HINDLY}	Global Clock Input Hold	PIO Input Register with input delay	0.0	—	0.0	—	0.0	—	
t_{COPLL}	Global Clock Input to Output	PIO Output Register using PLL without delay	—	3.1	—	3.3	—	3.8	ns
t_{SPLL}	Global Clock Input Setup	PIO Input Register without input delay using PLL without delay	0.5	—	0.5	—	0.6	—	ns
t_{HPLL}	Global Clock Input Hold	PIO Input Register without input delay using PLL without delay	0.8	—	0.8	—	1.0	—	ns
$t_{SINDLYPLL}$	Global Clock Input Setup	PIO Input Register with input delay using PLL without delay	7.6	—	7.6	—	8.8	—	ns
$t_{HINDLYPLL}$	Global Clock Input Hold	PIO Input Register with input delay using PLL without delay	-4.1	—	-4.0	—	-3.4	—	ns

1. Only available for ispXPGA 1200B and ispXPGA 1200EB (2.5V/3.3V) devices.

Timing v.0.2

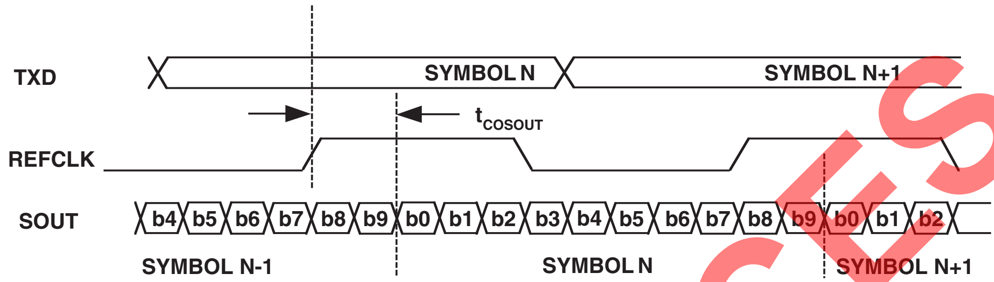
ispXPGA 1200B/C & ispXPGA 1200EB/EC PFU Timing Parameters

Over Recommended Operating Conditions

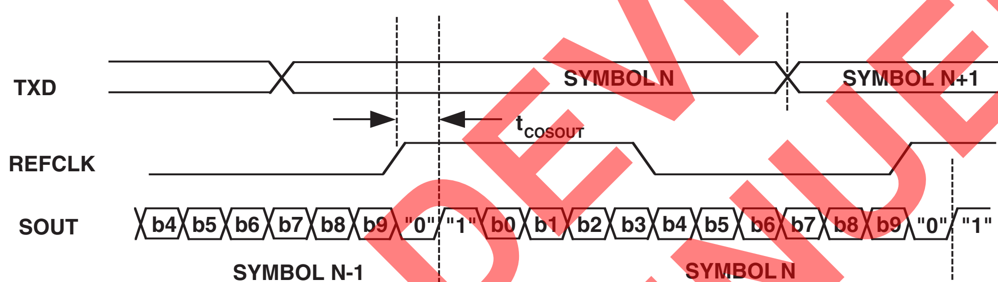
Parameter	Description	-5[1]		-4		-3		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Functional Delays								
LUTs								
t_{LUT4}	4-Input LUT Delay	—	0.41	—	0.44	—	0.51	ns
t_{LUT5}	5-Input LUT Delay	—	0.73	—	0.79	—	0.91	ns
t_{LUT6}	6-Input LUT Delay	—	0.86	—	0.93	—	1.07	ns
Shift Register (LUT)								
t_{LSR_S}	Shift Register Setup Time	-0.64	—	-0.62	—	-0.53	—	ns
t_{LSR_H}	Shift Register Hold Time	0.61	—	0.63	—	0.72	—	ns
t_{LSR_CO}	Shift Register Clock to Output Delay	—	0.70	—	0.75	—	0.86	ns
Arithmetic Functions								
$t_{LCTHRUR}$	MC (Macro Cell) Carry In to MC Carry Out Delay (Ripple)	—	0.08	—	0.09	—	0.10	ns
$t_{LCTHRUL}$[2]	MC Carry In to MC Carry Out Delay (Look Ahead)	—	0.05	—	0.05	—	0.06	ns
t_{LSTHRU}	MC Sum In to MC Sum Out Delay	—	0.42	—	0.45	—	0.52	ns
$t_{LSINCOUT}$	MC Sum In to MC Carry Out Delay	—	0.29	—	0.31	—	0.36	ns
$t_{LCINSOUTR}$	MC Carry In to MC Sum Out Delay (Ripple)	—	0.36	—	0.39	—	0.45	ns
$t_{LCINSOUTL}$	MC Carry In to MC Sum Out Delay (Look Ahead)	—	0.26	—	0.28	—	0.32	ns
Feed-thru								
t_{LFT}	PFU Feed-Thru Delay	—	0.15	—	0.16	—	0.18	ns
Distributed RAM								
t_{LRAM_CO}	Clock to RAM Output	—	1.24	—	1.33	—	1.53	ns
t_{LRAMAD_S}	Address Setup Time	-0.41	—	-0.40	—	-0.34	—	ns
t_{LRAMD_S}	Data Setup Time	0.21	—	0.22	—	0.25	—	ns
t_{LRAMWE_S}	Write Enable Setup Time	0.45	—	0.46	—	0.53	—	ns
t_{LRAMAD_H}	Address Hold Time	0.58	—	0.60	—	0.69	—	ns
t_{LRAMD_H}	Data Hold Time	0.11	—	0.11	—	0.13	—	ns
t_{LRAMWE_H}	Write Enable Hold Time	0.12	—	0.12	—	0.14	—	ns
$t_{LRAMCPW}$	Clock Pulse Width (High or Low)	2.91	—	3.00	—	3.45	—	ns
$t_{LRAMADO}$	Address to Output Delay	—	0.86	—	0.93	—	1.07	ns
Register/Latch Delays								
Registers								
t_{L_CO}	Register Clock to Output Delay	—	0.58	—	0.62	—	0.71	ns
t_{L_S}	Register Setup Time (Data before Clock)	0.14	—	0.14	—	0.16	—	ns
t_{L_H}	Register Hold Time (Data after Clock)	-0.12	—	-0.12	—	-0.10	—	ns
t_{LCE_S}	Register Clock Enable Setup Time	-0.11	—	-0.11	—	-0.09	—	ns
t_{LCE_H}	Register Clock Enable Hold Time	0.11	—	0.11	—	0.13	—	ns
Latches								
t_{L_GO}	Latch Gate to Output Delay	—	0.09	—	0.10	—	0.12	ns
t_{LL_S}	Latch Setup Time	0.14	—	0.14	—	0.16	—	ns
t_{LL_H}	Latch Hold Time	-0.12	—	-0.12	—	-0.10	—	ns
t_{LLPD}	Latch Propagation Delay (Transparent Mode)	—	0.09	—	0.10	—	0.12	ns

Serializer Timing

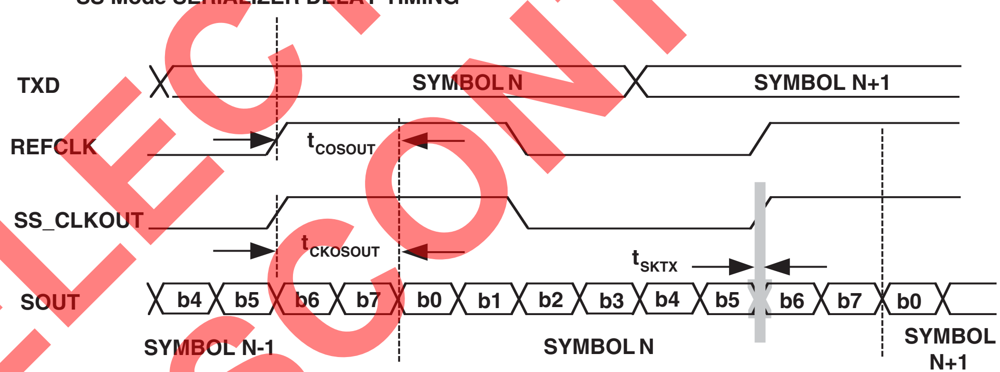
8B/10B SERIALIZER DELAY TIMING



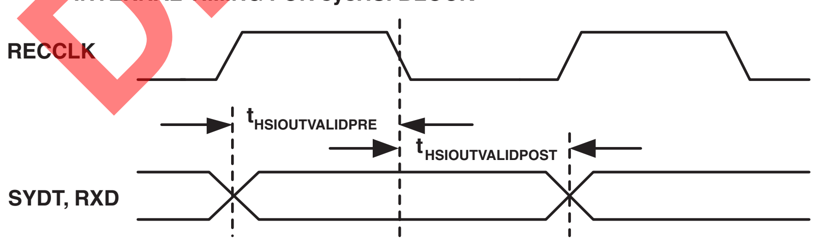
10B/12B SERIALIZER DELAY TIMING



SS Mode SERIALIZER DELAY TIMING



INTERNAL TIMING FOR sysHSI BLOCK



Signal Descriptions[1]

Signal Name	Signal Type	Description
General Purpose		
BK*y*_IO*x*[1,2]	Input/Output	General purpose I/O number x in I/O Bank y
GCLK*n*/I*n*[7]	Input	Global clock/input[8]
GSR	Input	Global Set/Reset
NC	—	No Connect
GND	GND	Ground
V_{CC}	VCC	Core logic power supply
V_{CCJ}	VCC	IEEE 1149.1 TAP power supply
V_{CCOy}[2]	VCC	I/O Bank y power supply
V_{REFy}[2]	Input	I/O Bank y reference voltage
D_{XN}, D_{XP}	Output	Temperature Sensing Diodes, provide a differential voltage, which corresponds to the temperature of the device.
Test and Program/Configuration		
TMS	Input	Test Mode Select
TCK	Input	Test Clock
TDI	Input	Test Data In
TDO	Output	Test Data Out
TOE	Input	Test Output Enable tri-states all I/O pins when driven low
CFG0	Input	Selects the SRAM memory configuration type (Peripheral or E^2CMOS Refresh)
PROGRAMb	Input	Initiates download from E^2CMOS or the peripheral port to SRAM memory (active low)
DONE	Bi-directional	Indicates when configuration is complete
INITb	Bi-directional	Indicates the device is ready for programming (active low)
READ	Input	Selects the READ operation when in sysCONFIG mode
CCLK	Input	sysCONFIG Configuration Clock
CSb	Input	sysCONFIG Chip Select (active low)
DATA[0:7]	Bi-directional	sysCONFIG Peripheral Port Data I/O
sysCLOCK PLL[3]		
PLL_FBK*z*	Input	Optional external feedback
PLL_RST*z*	Input	Optional external M divider reset
CLK_OUT*z*	Internal Signal	Clock output (routable to any I/O)
PLL_LOCK*z*	Internal Signal	Lock output (routable to any I/O)
GND_{P0}	GND	Left side PLL Ground
GND_{P1}	GND	Right side PLL Ground
V_{CCP0}	VCC	Left side PLL power supply
V_{CCP1}	VCC	Right side PLL power supply
sysHSI Block[4, 5]		
HSI*m*A_SINP, HSI*m*B_SINP	Input	P-side of differential serial data input
HSI*m*A_SINN, HSI*m*B_SINN	Input	N-side of differential serial data input
HSI*m*A_SOUTP, HSI*m*B_SOUTP	Output	P-side of differential serial data output
HSI*m*A_SOUTN, HSI*m*B_SOUTN	Output	N-side of differential serial data output
HSI*m*A_SYDT, HSI*m*B_SYDT	Internal Signal	Symbol alignment detect
HSI*m*A_RECCLK, HSI*m*B_RECCLK	Internal Signal	Recovered clock

ispXPGA Power Supply and NC Connections[1] (Continued)

Signal	680-Ball fpBGA[3]	900-Ball fpBGA[3]
V_{CC}	AE35, AE5, AL5, AR15, AR25, AR31, AR35, AR5, AT36, AT4, AU3, AU37, C3, C37, D36, D4, E15, E25, E35, E5, E9, J35, R35, R5	L11, L20, M12, M13, M14, M17, M18, M19, N12, N19, P12, P19, U12, U19, V12, V19, W12, W13, W14, W17, W18, W19, Y11, Y20
V_{CCO0}	E11, E12, E13, E17, E18, E7	K3, L10, M11, N11, N5, P11, R11, R12
V_{CCO1}	E22, E23, E27, E29, E31, E33	AA3, T11, T12, U11, V11, V5, W11, Y10
V_{CCO2}	G35, L35, M35, N35, U35, V35	AA11, AF13, AH10, W15, Y12, Y13, Y14, Y15
V_{CCO3}	AB35, AC35, AG35, AJ35, AL35, AN35	AA20, AF18, AH21, W16, Y16, Y17, Y18, Y19
V_{CCO4}	AR22, AR23, AR27, AR28, AR29, AR33	AA28, T19, T20, U20, V20, V26, W20, Y21
V_{CCO5}	AR11, AR13, AR17, AR18, AR7, AR9	K28, L21, M20, N20, N26, P20, R19, R20
V_{CCO6}	AB5, AC5, AG5, AH5, AJ5, AN5	C21, E18, K20, L16, L17, L18, L19, M16
V_{CCO7}	G5, J5, L5, N5, U5, V5	C10, E13, K11, L12, L13, L14, L15, M15
V_{CCP}	E20, AW22	R5, T26
V_{CCJ}	D3	B3
GND	A1, A2, A20, A38, A39, AE3, AE37, AK3, AK37, AR36, AR4, AT20, AT35, AT5, AU10, AU14, AU20, AU26, AU30, AV1, AV2, AV20, AV38, AV39, AW1, AW2, AW20, AW38, AW39, B1, B2, B20, B38, B39, C10, C14, C20, C26, C30, D20, D35, D5, E36, E4, K3, K37, P37, R3, Y1, Y2, Y3, Y36, Y37, Y38, Y39, Y4	A1, A2, A29, A30, AB28, AB3, AG27, AG4, AH22, AH28, AH3, AH9, AJ1, AJ2, AJ29, AJ30, AK1, AK2, AK29, AK30, B1, B2, B29, B30, C22, C28, C3, C9, D27, D4, J28, J3, N13, N14, N15, N16, N17, N18, P13, P14, P15, P16, P17, P18, R13, R14, R15, R16, R17, R18, T13, T14, T15, T16, T17, T18, U13, U14, U15, U16, U17, U18, V13, V14, V15, V16, V17, V18
GND_P	AR20, A21	R28, T3

ispXPGA Logic Signal Connections: 256-Ball fpBGA (Cont.)

256-fpBGA Ball	LFX200 Signal Name	LFX200 Second Function	LFX200 LVDS Pair/ sysHSI Reserved[2]	LFX125 Signal Name	LFX125 Second Function	LFX125 LVDS Pair/ sysHSI Reserved[2]
-	GND (Bank 2)	-	-	GND (Bank 2)	-	-
R8	BK2_IO19	-	35N	BK2_IO19	-	31N
N8	BK2_IO20	-	36P	BK2_IO20	-	32P
P8	BK2_IO21	-	36N	BK2_IO21	-	32N
-	GND (Bank 2)	-	-	-	-	-
-	GND (Bank 3)	-	-	-	-	-
T8	BK3_IO0	-	39P	BK3_IO0	-	33P
T9	BK3_IO1	-	39N	BK3_IO1	-	33N
R9	BK3_IO2	-	40P	BK3_IO2	-	34P
-	-	-	-	GND (Bank 3)	-	-
R10	BK3_IO3	-	40N	BK3_IO3	-	34N
P9	BK3_IO4	-	41P	BK3_IO4	-	35P
N9	BK3_IO5	-	41N	BK3_IO5	-	35N
T10	BK3_IO6	-	42P	BK3_IO6	-	36P
-	GND (Bank 3)	-	-	-	-	-
T11	BK3_IO7	-	42N	BK3_IO7	-	36N
P10	BK3_IO8	-	43P	BK3_IO8	-	37P
-	-	-	-	GND (Bank 3)	-	-
N10	BK3_IO9	-	43N	BK3_IO9	-	37N
R11	BK3_IO14	-	46P	BK3_IO10	-	38P
-	GND (Bank 3)	-	-	-	-	-
R12	BK3_IO15	-	46N	BK3_IO11	-	38N
P11	BK3_IO16	VREF3	47P	BK3_IO12	VREF3	39P
N11	BK3_IO17	-	47N	BK3_IO13	-	39N
T12	BK3_IO18	-	48P	BK3_IO14	-	40P
T13	BK3_IO19	-	48N	BK3_IO15	-	40N
R13	BK3_IO20	-	49P	BK3_IO16	-	41P
-	-	-	-	GND (Bank 3)	-	-
R14	BK3_IO21	-	49N	BK3_IO17	-	41N
P12	BK3_IO22	-	50P	BK3_IO18	-	42P
-	GND (Bank 3)	-	-	-	-	-
N12	BK3_IO23	-	50N	BK3_IO19	-	42N
T14	GSR	-	-	GSR	-	-
T15	DXP	-	-	DXP	-	-
P13	DXN	-	-	DXN	-	-
P15	BK4_IO0	-	52P/HSI2	BK4_IO0	-	44P
N14	BK4_IO1	-	52N/HSI2	BK4_IO1	-	44N
R16	BK4_IO2	HSI2A_SINP	53P/HSI2	BK4_IO2	-	45P
-	GND (Bank 4)	-	-	-	-	-
P16	BK4_IO3	HSI2A_SINN	53N/HSI2	BK4_IO3	-	45N
N15	BK4_IO4	-	54P/HSI2	BK4_IO4	-	46P
-	-	-	-	GND (Bank 4)	-	-

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
L2	BK0_IO35	HSI1B_SINN	17N/HSI1	BK0_IO15	HSI0B_SINN	7N/HSI0
L6	BK0_IO36	-	18P/HSI1	BK0_IO16	-	8P/HSI0
L5	BK0_IO37	-	18N/HSI1	BK0_IO17	-	8N/HSI0
M1	BK0_IO38	HSI2A_SOUTP	19P/HSI1	BK0_IO18	HSI1A_SOUTP	9P/HSI1
-	-	-	-	GND (Bank 0)	-	-
M2	BK0_IO39	HSI2A_SOUTN	19N/HSI1	BK0_IO19	HSI1A_SOUTN	9N/HSI1
L3	BK0_IO40	-	20P/HSI1	BK0_IO20	-	10P/HSI1
L4	BK0_IO41	-	20N/HSI1	BK0_IO21	-	10N/HSI1
M6	BK0_IO42	HSI2A_SINP	21P/HSI2	BK0_IO22	HSI1A_SINP	11P/HSI1
-	GND (Bank 0)	-	-	-	-	-
M5	BK0_IO43	HSI2A_SINN	21N/HSI2	BK0_IO23	HSI1A_SINN	11N/HSI1
M4	BK0_IO44	-	22P/HSI2	BK0_IO24	-	12P/HSI1
M3	BK0_IO45	-	22N/HSI2	BK0_IO25	-	12N/HSI1
N1	BK0_IO46	HSI2B_SOUTP	23P/HSI2	BK0_IO26	HSI1B_SOUTP	13P/HSI1
-	-	-	-	GND (Bank 0)	-	-
N2	BK0_IO47	HSI2B_SOUTN	23N/HSI2	BK0_IO27	HSI1B_SOUTN	13N/HSI1
N7	BK0_IO48	-	24P/HSI2	BK0_IO28	-	14P/HSI1
N6	BK0_IO49	-	24N/HSI2	BK0_IO29	-	14N/HSI1
P1	BK0_IO50	HSI2B_SINP	25P/HSI2	BK0_IO30	HSI1B_SINP	15P/HSI1
-	GND (Bank 0)	-	-	-	-	-
P2	BK0_IO51	HSI2B_SINN	25N/HSI2	BK0_IO31	HSI1B_SINN	15N/HSI1
N3	BK0_IO52	-	26P/HSI2	BK0_IO32	-	16P/HSI1
N4	BK0_IO53	-	26N/HSI2	BK0_IO33	-	16N/HSI1
P6	BK0_IO54	PLL_RST0	27P/HSI2	BK0_IO38	PLL_RST0	19P
P5	BK0_IO55	PLL_RST1	27N/HSI2	BK0_IO35	PLL_RST1	17N
P3	BK0_IO56	-	28P/HSI2	BK0_IO36	-	18P
P4	BK0_IO57	-	28N/HSI2	BK0_IO39	-	19N
R7	BK0_IO58	PLL_FBK0	29P	BK0_IO34	PLL_FBK0	17P
-	GND (Bank 0)	-	-	GND (Bank 0)	-	-
R6	BK0_IO59	PLL_FBK1	29N	BK0_IO37	PLL_FBK1	18N
R1	BK0_IO60	CLK_OUT0	30P	BK0_IO40	CLK_OUT0	20P
-	-	-	-	GND (Bank 0)	-	-
R2	BK0_IO61	CLK_OUT1	30N	BK0_IO41	CLK_OUT1	20N
-	GND (Bank 0)	-	-	-	-	-
R3	GCLK0	-	LVDS Pair0P	GCLK0	-	LVDS Pair0P
R4	GCLK1	-	LVDS Pair0N	GCLK1	-	LVDS Pair0N
R5	VCCP0	-	-	VCCP0	-	-
T3	GNDP0	-	-	GNDP0	-	-
T4	GCLK2	-	LVDS Pair1P	GCLK2	-	LVDS Pair1P
T5	GCLK3	-	LVDS Pair1N	GCLK3	-	LVDS Pair1N
-	GND (Bank 1)	-	-	-	-	-
T2	BK1_IO0	CLK_OUT2	31P	BK1_IO0	CLK_OUT2	21P

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
AJ12	BK2_IO43	-	83N	BK2_IO23	-	53N
AD13	BK2_IO44	-	84P	BK2_IO24	-	54P
AE13	BK2_IO45	-	84N	BK2_IO25	-	54N
AK13	BK2_IO46	-	85P	BK2_IO26	-	55P
-	-	-	-	GND (Bank 2)	-	-
AJ13	BK2_IO47	-	85N	BK2_IO27	-	55N
AG13	BK2_IO48	-	86P	BK2_IO28	-	56P
AH13	BK2_IO49	-	86N	BK2_IO29	-	56N
AE14	BK2_IO50	-	87P	BK2_IO30	-	57P
-	GND (Bank 2)	-	-	-	-	-
AF14	BK2_IO51	-	87N	BK2_IO31	-	57N
AG14	BK2_IO52	-	88P	BK2_IO32	-	58P
AH14	BK2_IO53	-	88N	BK2_IO33	-	58N
AJ14	BK2_IO54	-	89P	BK2_IO34	-	59P
-	-	-	-	GND (Bank 2)	-	-
AK14	BK2_IO55	-	89N	BK2_IO35	-	59N
AE15	BK2_IO56	-	90P	BK2_IO36	-	60P
AF15	BK2_IO57	-	90N	BK2_IO37	-	60N
AG15	BK2_IO58	-	91P	BK2_IO38	-	61P
-	GND (Bank 2)	-	-	-	-	-
AH15	BK2_IO59	-	91N	BK2_IO39	-	61N
AJ15	BK2_IO60	-	92P	BK2_IO40	-	62P
AK15	BK2_IO61	-	92N	BK2_IO41	-	62N
-	GND (Bank 2)	-	-	GND (Bank 2)	-	-
-	GND (Bank 3)	-	-	GND (Bank 3)	-	-
AK16	BK3_IO0	-	93P	BK3_IO0	-	63P
AJ16	BK3_IO1	-	93N	BK3_IO1	-	63N
AH16	BK3_IO2	-	94P	BK3_IO2	-	64P
-	GND (Bank 3)	-	-	-	-	-
AG16	BK3_IO3	-	94N	BK3_IO3	-	64N
AF16	BK3_IO4	-	95P	BK3_IO4	-	65P
AE16	BK3_IO5	-	95N	BK3_IO5	-	65N
AK17	BK3_IO6	-	96P	BK3_IO6	-	66P
-	-	-	-	GND (Bank 3)	-	-
AJ17	BK3_IO7	-	96N	BK3_IO7	-	66N
AH17	BK3_IO8	-	97P	BK3_IO8	-	67P
AG17	BK3_IO9	-	97N	BK3_IO9	-	67N
AF17	BK3_IO10	-	98P	BK3_IO10	-	68P
-	GND (Bank 3)	-	-	-	-	-
AE17	BK3_IO11	-	98N	BK3_IO11	-	68N
AH18	BK3_IO12	-	99P	BK3_IO12	-	69P
AG18	BK3_IO13	-	99N	BK3_IO13	-	69N

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
AC27	BK4_IO21	-	134N/HSI5	NC	-	-
AD29	BK4_IO22	HSI6A_SINP	135P/HSI5	NC	-	-
AD30	BK4_IO23	HSI6A_SINN	135N/HSI5	NC	-	-
AB24	BK4_IO24	-	136P/HSI5	NC	-	-
AB25	BK4_IO25	-	136N/HSI5	NC	-	-
AC29	BK4_IO26	HSI6A_SOUTP	137P/HSI6	NC	-	-
-	GND (Bank 4)	-	-	-	-	-
AC30	BK4_IO27	HSI6A_SOUTN	137N/HSI6	NC	-	-
AB27	BK4_IO28	-	138P/HSI6	NC	-	-
AB26	BK4_IO29	-	138N/HSI6	NC	-	-
AB30	BK4_IO30	HSI6B_SINP	139P/HSI6	BK4_IO18	HSI3B_SINP	93P
-	-	-	-	GND (Bank 4)	-	-
AB29	BK4_IO31	HSI6B_SINN	139N/HSI6	BK4_IO19	HSI3B_SINN	93N
AA26	BK4_IO32	-	140P/HSI6	NC	-	-
AA27	BK4_IO33	-	140N/HSI6	NC	-	-
AA30	BK4_IO34	HSI6B_SOUTP	141P/HSI6	BK4_IO22	HSI3B_SOUTP	95P
-	GND (Bank 4)	-	-	-	-	-
AA29	BK4_IO35	HSI6B_SOUTN	141N/HSI6	BK4_IO23	HSI3B_SOUTN	95N
Y25	BK4_IO36	-	142P/HSI6	NC	-	-
Y26	BK4_IO37	-	142N/HSI6	NC	-	-
Y28	BK4_IO38	-	143P/HSI6	NC	-	-
Y27	BK4_IO39	-	143N/HSI6	NC	-	-
W25	BK4_IO40	-	144P/HSI6	NC	-	-
W26	BK4_IO41	-	144N/HSI6	NC	-	-
W27	BK4_IO42	-	145P	BK4_IO24	-	96P
-	GND (Bank 4)	-	-	-	-	-
W28	BK4_IO43	-	145N	BK4_IO25	-	96N
V24	BK4_IO44	-	146P	BK4_IO26	-	97P
-	-	-	-	GND (Bank 4)	-	-
V25	BK4_IO45	-	146N	BK4_IO27	-	97N
Y29	BK4_IO46	-	147P	BK4_IO32	-	100P
Y30	BK4_IO47	-	147N	BK4_IO33	-	100N
V27	BK4_IO48	PLL_RST4	148P	BK4_IO20	PLL_RST4	94P
V28	BK4_IO49	PLL_RST5	148N	BK4_IO21	PLL_RST5	94N
W29	BK4_IO50	-	149P	BK4_IO34	-	101P
-	GND (Bank 4)	-	-	GND (Bank 4)	-	-
W30	BK4_IO51	-	149N	BK4_IO35	-	101N
U25	BK4_IO52	-	150P	BK4_IO28	-	98P
U26	BK4_IO53	-	150N	BK4_IO29	-	98N
V29	BK4_IO54	SS_CLKIN1P	151P	BK4_IO30	SS_CLKIN1P	99P
V30	BK4_IO55	SS_CLKIN1N	151N	BK4_IO31	SS_CLKIN1N	99N
U28	BK4_IO56	PLL_FBK4	152P	BK4_IO36	PLL_FBK4	102P

ispXPGA Logic Signal Connections: 900-Ball fpBGA (Cont.)

900 fpBGA Ball	LFX1200			LFX500		
	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]	Signal Name	Second Function	LVDS Pair/ sysHSI Reserved[1]
K30	BK5_IO22	HSI7B_SOUTP	166P/HSI8	BK5_IO22	HSI4B_SOUTP	116P/HSI4
-	-	-	-	GND (Bank 5)	-	-
K29	BK5_IO23	HSI7B_SOUTN	166N/HSI8	BK5_IO23	HSI4B_SOUTN	116N/HSI4
L28	BK5_IO24	-	167P/HSI8	BK5_IO24	-	117P/HSI5
L27	BK5_IO25	-	167N/HSI8	BK5_IO25	-	117N/HSI5
L26	BK5_IO26	HSI8A_SINP	168P/HSI8	BK5_IO26	HSI5A_SINP	118P/HSI5
-	GND (Bank 5)	-	-	-	-	-
L25	BK5_IO27	HSI8A_SINN	168N/HSI8	BK5_IO27	HSI5A_SINN	118N/HSI5
K27	BK5_IO28	-	169P/HSI8	BK5_IO28	-	119P/HSI5
K26	BK5_IO29	-	169N/HSI8	BK5_IO29	-	119N/HSI5
J30	BK5_IO30	HSI8A_SOUTP	170P/HSI8	BK5_IO30	HSI5A_SOUTP	120P/HSI5
-	-	-	-	GND (Bank 5)	-	-
J29	BK5_IO31	HSI8A_SOUTN	170N/HSI8	BK5_IO31	HSI5A_SOUTN	120N/HSI5
J26	BK5_IO32	-	171P/HSI8	NC	-	-
J27	BK5_IO33	-	171N/HSI8	NC	-	-
H30	BK5_IO34	HSI8B_SINP	172P/HSI8	NC	-	-
-	GND (Bank 5)	-	-	-	-	-
H29	BK5_IO35	HSI8B_SINN	172N/HSI8	NC	-	-
J25	BK5_IO36	-	173P/HSI9	NC	-	-
J24	BK5_IO37	-	173N/HSI9	NC	-	-
G30	BK5_IO38	HSI8B_SOUTP	174P/HSI9	NC	-	-
G29	BK5_IO39	HSI8B_SOUTN	174N/HSI9	NC	-	-
H27	BK5_IO40	-	175P/HSI9	NC	-	-
H28	BK5_IO41	-	175N/HSI9	NC	-	-
F30	BK5_IO42	HSI9A_SINP	176P/HSI9	NC	-	-
-	GND (Bank 5)	-	-	-	-	-
F29	BK5_IO43	HSI9A_SINN	176N/HSI9	NC	-	-
G27	BK5_IO44	-	177P/HSI9	NC	-	-
G28	BK5_IO45	-	177N/HSI9	NC	-	-
E30	BK5_IO46	HSI9A_SOUTP	178P/HSI9	NC	-	-
E29	BK5_IO47	HSI9A_SOUTN	178N/HSI9	NC	-	-
H26	BK5_IO48	-	179P/HSI9	BK5_IO33	-	121N/HSI5
H25	BK5_IO49	VREF5	179N/HSI9	BK5_IO32	VREF5	121P/HSI5
D30	BK5_IO50	HSI9B_SINP	180P/HSI9	BK5_IO34	HSI5B_SINP	122P/HSI5
-	GND (Bank 5)	-	-	-	-	-
D29	BK5_IO51	HSI9B_SINN	180N/HSI9	BK5_IO35	HSI5B_SINN	122N/HSI5
F28	BK5_IO52	-	181P	BK5_IO36	-	123P/HSI5
F27	BK5_IO53	-	181N	BK5_IO37	-	123N/HSI5
C30	BK5_IO54	HSI9B_SOUTP	182P	BK5_IO38	HSI5B_SOUTP	124P/HSI5
-	-	-	-	GND (Bank 5)	-	-
C29	BK5_IO55	HSI9B_SOUTN	182N	BK5_IO39	HSI5B_SOUTN	124N/HSI5
G26	BK5_IO56	-	183P	NC	-	-

"E-Series" Commercial

Part Number	Gates	Voltage	Speed Grade	Package	Balls
LFX125EB-05F256C	139K	2.5/3.3	-5	fpBGA	256
LFX125EB-04F256C	139K	2.5/3.3	-4	fpBGA	256
LFX125EB-03F256C	139K	2.5/3.3	-3	fpBGA	256
LFX125EC-04F256C	139K	1.8	-4	fpBGA	256
LFX125EC-03F256C	139K	1.8	-3	fpBGA	256
LFX125EB-05F516C	139K	2.5/3.3	-5	fpBGA	516
LFX125EB-04F516C	139K	2.5/3.3	-4	fpBGA	516
LFX125EB-03F516C	139K	2.5/3.3	-3	fpBGA	516
LFX125EC-04F516C	139K	1.8	-4	fpBGA	516
LFX125EC-03F516C	139K	1.8	-3	fpBGA	516
LFX125EB-05FH516C[1]	139K	2.5/3.3	-5	fpBGA	516
LFX125EB-04FH516C[1]	139K	2.5/3.3	-4	fpBGA	516
LFX125EB-03FH516C[1]	139K	2.5/3.3	-3	fpBGA	516
LFX125EC-04FH516C[1]	139K	1.8	-4	fpBGA	516
LFX125EC-03FH516C[1]	139K	1.8	-3	fpBGA	516
LFX200EB-05F256C	210K	2.5/3.3	-5	fpBGA	256
LFX200EB-04F256C	210K	2.5/3.3	-4	fpBGA	256
LFX200EB-03F256C	210K	2.5/3.3	-3	fpBGA	256
LFX200EC-04F256C	210K	1.8	-4	fpBGA	256
LFX200EC-03F256C	210K	1.8	-3	fpBGA	256
LFX200EB-05F516C	210K	2.5/3.3	-5	fpBGA	516
LFX200EB-04F516C	210K	2.5/3.3	-4	fpBGA	516
LFX200EB-03F516C	210K	2.5/3.3	-3	fpBGA	516
LFX200EC-04F516C	210K	1.8	-4	fpBGA	516
LFX200EC-03F516C	210K	1.8	-3	fpBGA	516
LFX200EB-05FH516C[1]	210K	2.5/3.3	-5	fpBGA	516
LFX200EB-04FH516C[1]	210K	2.5/3.3	-4	fpBGA	516
LFX200EB-03FH516C[1]	210K	2.5/3.3	-3	fpBGA	516
LFX200EC-04FH516C[1]	210K	1.8	-4	fpBGA	516
LFX200EC-03FH516C[1]	210K	1.8	-3	fpBGA	516
LFX500EB-05F516C	476K	2.5/3.3	-5	fpBGA	516
LFX500EB-04F516C	476K	2.5/3.3	-4	fpBGA	516
LFX500EB-03F516C	476K	2.5/3.3	-3	fpBGA	516
LFX500EC-04F516C	476K	1.8	-4	fpBGA	516
LFX500EC-03F516C	476K	1.8	-3	fpBGA	516
LFX500EB-05FH516C[1]	476K	2.5/3.3	-5	fpBGA	516
LFX500EB-04FH516C[1]	476K	2.5/3.3	-4	fpBGA	516
LFX500EB-03FH516C[1]	476K	2.5/3.3	-3	fpBGA	516
LFX500EC-04FH516C[1]	476K	1.8	-4	fpBGA	516
LFX500EC-03FH516C[1]	476K	1.8	-3	fpBGA	516
LFX500EB-05F900C	476K	2.5/3.3	-5	fpBGA	900
LFX500EB-04F900C	476K	2.5/3.3	-4	fpBGA	900
LFX500EB-03F900C	476K	2.5/3.3	-3	fpBGA	900
LFX500EC-04F900C	476K	1.8	-4	fpBGA	900