Infineon Technologies - XC167CI32F40FBBAFXQMA1 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Last Time Buy
Core Processor	C166SV2
Core Size	16-Bit
Speed	40MHz
Connectivity	CANbus, EBI/EMI, I²C, SPI, UART/USART
Peripherals	PWM, WDT
Number of I/O	103
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 2.7V
Data Converters	A/D 16x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc167ci32f40fbbafxqma1

XC167CI-32F

16-Bit Single-Chip Microcontroller with C166SV2 Core

Microcontrollers

Never stop thinking

XC167
Revision History: V1.1, 2006-08

Previous Version(s):
V1.0, 2005-06

Page	Subjects (major changes since last revision)
13	Description of the $\overline{\text{TRST}}$ signal modified.
19	Footnote added about pins XTAL1/XTAL3 belonging to V_{DDI} power domain.
53	Instructions Set Summary improved.
60	Footnote added about amplitude at XTAL1 pin.
85	Green package added.
85	Thermal Resistance: R_{THA} replaced by $R_{\Theta JC}$ and $R_{\Theta JL}$ because R_{THA} strongly depends on the external system (PCB, environment). P_{DISS} removed, because no static parameter, but derived from thermal resistance.
	Title at the Cover Page corrected XC167CS to XC167CI.

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Table 2 Pin Definitions and Functions

Sym-bol	Pin Num.	Input Outp.	Function
P20.12	3	IO	For details, please refer to the description of **P20**.
NMI	4	I	Non-Maskable Interrupt Input. A high to low transition at this pin causes the CPU to vector to the NMI trap routine. When the PWRDN (power down) instruction is executed, the NMI pin must be low in order to force the XC167 into power down mode. If NMI is high, when PWRDN is executed, the part will continue to run in normal mode. If not used, pin NMI should be pulled high externally.
P6		IO	Port 6 is an 8-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output (configurable as push/pull or open drain driver). The input threshold of Port 6 is selectable (standard or special). The Port 6 pins also serve for alternate functions:
P6.0	7	O	CS0 Chip Select 0 Output,
		IO	CC0IO CAPCOM1: CC0 Capture Inp./Compare Output
P6.1	8	O	CS1 Chip Select 1 Output,
		IO	CC1IO CAPCOM1: CC1 Capture Inp./Compare Output
P6.2	9	O	CS2 Chip Select 2 Output,
		IO	CC2IO CAPCOM1: CC2 Capture Inp./Compare Output
P6.3	10	O	CS3 Chip Select 3 Output,
		IO	CC3IO CAPCOM1: CC3 Capture Inp./Compare Output
P6.4	11	O	CS4 Chip Select 4 Output,
		IO	CC4IO CAPCOM1: CC4 Capture Inp./Compare Output
P6.5	12	I	HOLD External Master Hold Request Input,
		IO	CC5IO CAPCOM1: CC5 Capture Inp./Compare Output
P6.6	13	I/O	HLDA Hold Acknowledge Output (master mode) or Input (slave mode),
		IO	CC6IO CAPCOM1: CC6 Capture Inp./Compare Output
P6.7	14	O	BREQ Bus Request Output,
		IO	CC7IO CAPCOM1: CC7 Capture Inp./Compare Output

Table 2 Pin Definitions and Functions (cont'd)

Sym-bol	Pin Num.	Input Outp.	Function
P7		IO	Port 7 is a 4-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output (configurable as push/pull or open drain driver). The input threshold of Port 7 is selectable (standard or special). Port 7 pins provide inputs/outputs for CAPCOM2 and serial interface lines.[1)]
P7.4	15	I/O I I	CC28IO CAPCOM2: CC28 Capture Inp./Compare Outp., CAN2_RxD CAN Node 2 Receive Data Input, EX7IN Fast External Interrupt 7 Input (alternate pin B)
P7.5	16	I/O O I	CC29IO CAPCOM2: CC29 Capture Inp./Compare Outp., CAN2_TxD CAN Node 2 Transmit Data Output, EX6IN Fast External Interrupt 6 Input (alternate pin B)
P7.6	17	I/O I I	CC30IO CAPCOM2: CC30 Capture Inp./Compare Outp., CAN1_RxD CAN Node 1 Receive Data Input, EX7IN Fast External Interrupt 7 Input (alternate pin A)
P7.7	18	I/O O I	CC31IO CAPCOM2: CC31 Capture Inp./Compare Outp., CAN1_TxD CAN Node 1 Transmit Data Output, EX6IN Fast External Interrupt 6 Input (alternate pin A)

Table 2 Pin Definitions and Functions (cont'd)

Sym-bol	Pin Num.	Input Outp.	Function	
P3		IO	Port 3 is a 15-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output (configurable as push/pull or open drain driver). The input threshold of Port 3 is selectable (standard or special). The following Port 3 pins also serve for alternate functions:	
P3.0	59	I	T0IN	CAPCOM1 Timer T0 Count Input,
		O	TxD1	ASC1 Clock/Data Output (Async./Sync),
		I	EX1IN	Fast External Interrupt 1 Input (alternate pin B)
P3.1	60	O	T6OUT	GPT2 Timer T6 Toggle Latch Output,
		I/O	RxD1	ASC1 Data Input (Async.) or Inp./Outp. (Sync.),
		I	EX1IN	Fast External Interrupt 1 Input (alternate pin A)
P3.2	61	I	CAPIN	GPT2 Register CAPREL Capture Input
P3.3	62	O	T3OUT	GPT1 Timer T3 Toggle Latch Output
P3.4	63	I	T3EUD	GPT1 Timer T3 External Up/Down Control Input
P3.5	64	I	T4IN	GPT1 Timer T4 Count/Gate/Reload/Capture Inp
P3.6	65	I	T3IN	GPT1 Timer T3 Count/Gate Input
P3.7	66	I	T2IN	GPT1 Timer T2 Count/Gate/Reload/Capture Inp
P3.8	67	I/O	MRST0	SSC0 Master-Receive/Slave-Transmit In/Out.
P3.9	68	I/O	MTSR0	SSC0 Master-Transmit/Slave-Receive Out/In.
P3.10	69	O	TxD0	ASC0 Clock/Data Output (Async./Sync.),
		I	EX2IN	Fast External Interrupt 2 Input (alternate pin B)
P3.11	70	I/O	RxD0	ASC0 Data Input (Async.) or Inp./Outp. (Sync.),
		I	EX2IN	Fast External Interrupt 2 Input (alternate pin A)
P3.12	75	O	$\overline{\text{BHE}}$	External Memory High Byte Enable Signal,
		O	$\overline{\text{WRH}}$	External Memory High Byte Write Strobe,
		I	EX3IN	Fast External Interrupt 3 Input (alternate pin B)
P3.13	76	I/O	SCLK0	SSC0 Master Clock Output/Slave Clock Input,
		I	EX3IN	Fast External Interrupt 3 Input (alternate pin A)
P3.15	77	O	CLKOUT	Master Clock Output,
		O	FOUT	Programmable Frequency Output
TCK	71	I	Debug System: JTAG Clock Input	
TDI	72	I	Debug System: JTAG Data In	
TDO	73	O	Debug System: JTAG Data Out	
TMS	74	I	Debug System: JTAG Test Mode Selection	

Table 2 Pin Definitions and Functions (cont'd)

Sym-bol	Pin Num.	Input Outp.	Function
P4		IO	Port 4 is an 8-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output (configurable as push/pull or open drain driver). The input threshold of Port 4 is selectable (standard or special). Port 4 can be used to output the segment address lines, the optional chip select lines, and for serial interface lines:[1)]
P4.0	80	O	A16 Least Significant Segment Address Line
P4.1	81	O	A17 Segment Address Line
P4.2	82	O	A18 Segment Address Line
P4.3	83	O	A19 Segment Address Line
P4.4	84	O	A20 Segment Address Line,
		I	CAN2_RxD CAN Node 2 Receive Data Input,
		I	EX5IN Fast External Interrupt 5 Input (alternate pin B)
P4.5	85	O	A21 Segment Address Line,
		I	CAN1_RxD CAN Node 1 Receive Data Input,
		I	EX4IN Fast External Interrupt 4 Input (alternate pin B)
P4.6	86	O	A22 Segment Address Line,
		O	CAN1_TxD CAN Node 1 Transmit Data Output,
		I	EX5IN Fast External Interrupt 5 Input (alternate pin A)
P4.7	87	O	A23 Most Significant Segment Address Line,
		I	CAN1_RxD CAN Node 1 Receive Data Input,
		O	CAN2_TxD CAN Node 2 Transmit Data Output,
		I	EX4IN Fast External Interrupt 4 Input (alternate pin A)

Table 2 Pin Definitions and Functions (cont'd)

Sym-bol	Pin Num.	Input Outp.	Function	
PORT1		IO	PORT1 consists of the two 8-bit bidirectional I/O ports P1L and P1H. Each pin can be programmed for input (output driver in high-impedance state) or output. PORT1 is used as the 16-bit address bus (A) in demultiplexed bus modes (also after switching from a demultiplexed to a multiplexed bus mode). The following PORT1 pins also serve for alt. functions:	
P1L.0	117	I/O	CC60	CAPCOM6: Input / Output of Channel 0
P1L.1	118	O	COUT60	CAPCOM6: Output of Channel 0
P1L.2	119	I/O	CC61	CAPCOM6: Input / Output of Channel 1
P1L.3	120	O	COUT61	CAPCOM6: Output of Channel 1
P1L.4	121	I/O	CC62	CAPCOM6: Input / Output of Channel 2
P1L.5	122	O	COUT62	CAPCOM6: Output of Channel 2
P1L.6	123	O	$\overline{\text{COUT63}}$	Output of 10-bit Compare Channel
P1L.7	124	I	$\overline{\text{CTRAP}}$	$\overline{\text{CAPCOM2}}$: CC22 Capture Inp./Compare Outp. $\overline{\text{CTRAP}}$ is an input pin with an internal pullup resistor. A low level on this pin switches the CAPCOM6 compare outputs to the logic level defined by software (if enabled).
		I/O	$\overline{\text{CC22IO}}$	CAPCOM2: CC22 Capture Inp./Compare Outp.
P1H.0	127	I	$\overline{\text{CC6POS0}}$	CAPCOM6: Position 0 Input,
		I	EX0IN	Fast External Interrupt 0 Input (alternate pin B),
		I/O	$\overline{\text{CC23IO}}$	CAPCOM2: CC23 Capture Inp./Compare Outp.
P1H.1	128	I	$\overline{\text{CC6POS1}}$	CAPCOM6: Position 1 Input,
		I/O	$\overline{\text{MRST1}}$	SSC1 Master-Receive/Slave-Transmit In/Out.
P1H.2	129	I	$\overline{\text{CC6POS2}}$	CAPCOM6: Position 2 Input,
		I/O	MTSR1	SSC1 Master-Transmit/Slave-Receive Out/Inp.
P1H.3	130	I/O	SCLK1	SSC1 Master Clock Output / Slave Clock Input,
		I	EX0IN	Fast External Interrupt 0 Input (alternate pin A)
P1H.4	131	I/O	CC24IO	CAPCOM2: CC24 Capture Inp./Compare Outp.
P1H.5	132	I/O	CC25IO	CAPCOM2: CC25 Capture Inp./Compare Outp.
P1H.6	133	I/O	CC26IO	CAPCOM2: CC26 Capture Inp./Compare Outp.
P1H.7	134	I/O	CC27IO	CAPCOM2: CC27 Capture Inp./Compare Outp.

Table 4 XC167 Interrupt Nodes (cont'd)

Source of Interrupt or PEC Service Request	Control Register	Vector Location[1)]	Trap Number
ASC1 Autobaud	ASC1_ABIC	xx'0108$_H$	42$_H$ / 66$_D$
End of PEC Subchannel	EOPIC	xx'0130$_H$	4C$_H$ / 76$_D$
CAPCOM6 Timer T12	CCU6_T12IC	xx'0134$_H$	4D$_H$ / 77$_D$
CAPCOM6 Timer T13	CCU6_T13IC	xx'0138$_H$	4E$_H$ / 78$_D$
CAPCOM6 Emergency	CCU6_EIC	xx'013C$_H$	4F$_H$ / 79$_D$
CAPCOM6	CAPCOM6	xx'0140$_H$	50$_H$ / 80$_D$
SSC1 Transmit	SSC1_TIC	xx'0144$_H$	51$_H$ / 81$_D$
SSC1 Receive	SSC1_RIC	xx'0148$_H$	52$_H$ / 82$_D$
SSC1 Error	SSC1_EIC	xx'014C$_H$	53$_H$ / 83$_D$
CAN0	CAN_0IC	xx'0150$_H$	54$_H$ / 84$_D$
CAN1	CAN_1IC	xx'0154$_H$	55$_H$ / 85$_D$
CAN2	CAN_2IC	xx'0158$_H$	56$_H$ / 86$_D$
CAN3	CAN_3IC	xx'015C$_H$	57$_H$ / 87$_D$
CAN4	CAN_4IC	xx'0164$_H$	59$_H$ / 89$_D$
CAN5	CAN_5IC	xx'0168$_H$	5A$_H$ / 90$_D$
CAN6	CAN_6IC	xx'016C$_H$	5B$_H$ / 91$_D$
CAN7	CAN_7IC	xx'0170$_H$	5C$_H$ / 92$_D$
RTC	RTC_IC	xx'0174$_H$	5D$_H$ / 93$_D$
Unassigned node	–	xx'012C$_H$	3F$_H$ / 63$_D$
Unassigned node	–	xx'00FC$_H$	3F$_H$ / 63$_D$
Unassigned node	–	xx'0160$_H$	58$_H$ / 88$_D$

1) Register VECSEG defines the segment where the vector table is located to.
Bitfield VECSC in register CPUCON1 defines the distance between two adjacent vectors. This table represents the default setting, with a distance of 4 (two words) between two vectors.

3.5 On-Chip Debug Support (OCDS)

The On-Chip Debug Support system provides a broad range of debug and emulation features built into the XC167. The user software running on the XC167 can thus be debugged within the target system environment.

The OCDS is controlled by an external debugging device via the debug interface, consisting of the IEEE-1149-conforming JTAG port and a break interface. The debugger controls the OCDS via a set of dedicated registers accessible via the JTAG interface. Additionally, the OCDS system can be controlled by the CPU, e.g. by a monitor program. An injection interface allows the execution of OCDS-generated instructions by the CPU.

Multiple breakpoints can be triggered by on-chip hardware, by software, or by an external trigger input. Single stepping is supported as well as the injection of arbitrary instructions and read/write access to the complete internal address space. A breakpoint trigger can be answered with a CPU-halt, a monitor call, a data transfer, or/and the activation of an external signal.

Tracing data can be obtained via the JTAG interface or via the external bus interface for increased performance.

The debug interface uses a set of 6 interface signals (4 JTAG lines, 2 break lines) to communicate with external circuitry. These interface signals use dedicated pins.

Complete system emulation is supported by the New Emulation Technology (NET) interface.

3.7 The Capture/Compare Unit CAPCOM6

The CAPCOM6 unit supports generation and control of timing sequences on up to three 16-bit capture/compare channels plus one independent 10-bit compare channel.
In compare mode the CAPCOM6 unit provides two output signals per channel which have inverted polarity and non-overlapping pulse transitions (deadtime control). The compare channel can generate a single PWM output signal and is further used to modulate the capture/compare output signals.
In capture mode the contents of compare timer T12 is stored in the capture registers upon a signal transition at pins CCx.

Compare timers T12 (16-bit) and T13 (10-bit) are free running timers which are clocked by the prescaled system clock.

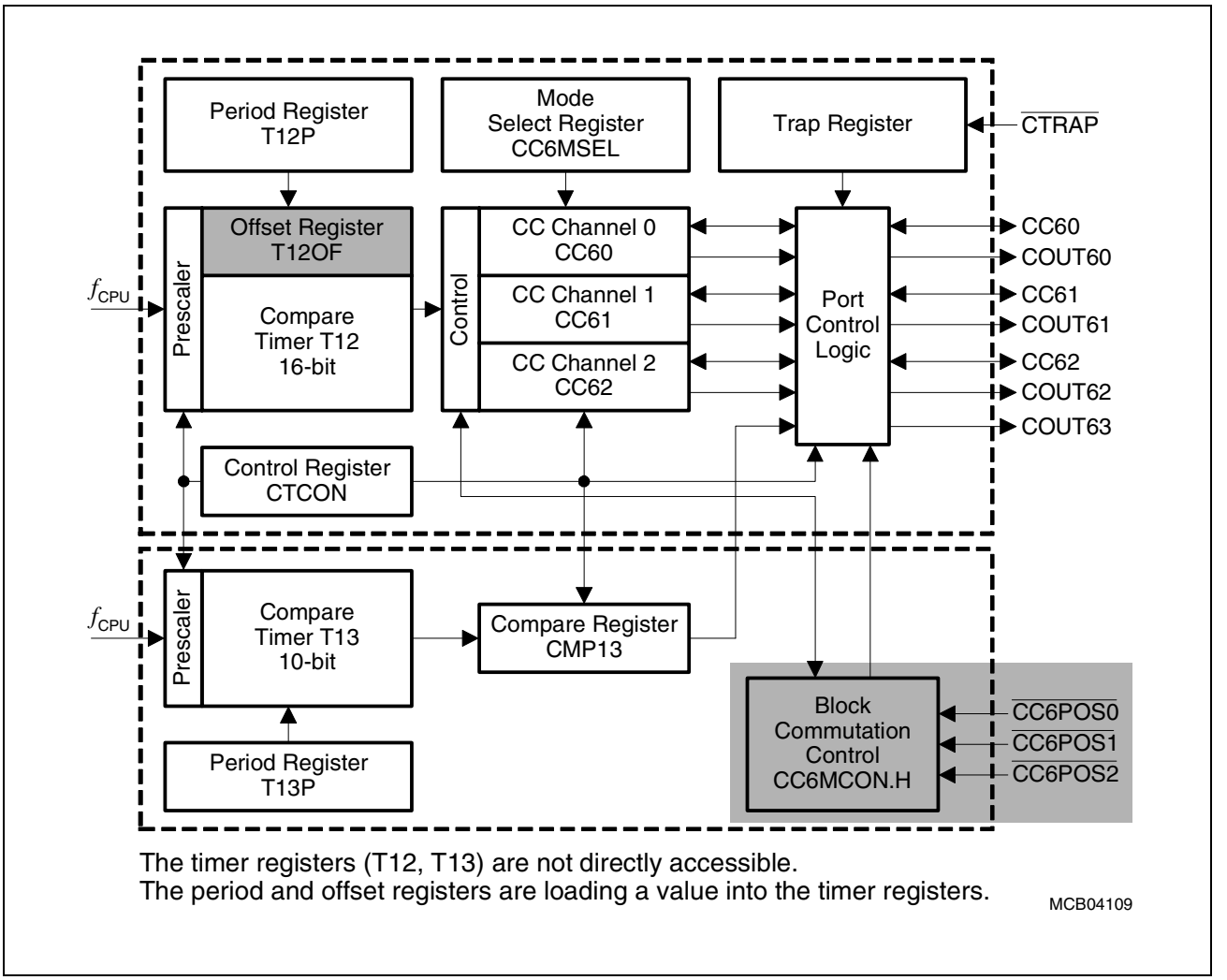


Figure 6 CAPCOM6 Block Diagram

For motor control applications both subunits may generate versatile multichannel PWM signals which are basically either controlled by compare timer T12 or by a typical hall sensor pattern at the interrupt inputs (block commutation).

3.11 Asynchronous/Synchronous Serial Interfaces (ASC0/ASC1)

The Asynchronous/Synchronous Serial Interfaces ASC0/ASC1 (USARTs) provide serial communication with other microcontrollers, processors, terminals or external peripheral components. They are upward compatible with the serial ports of the Infineon 8-bit microcontroller families and support full-duplex asynchronous communication and half-duplex synchronous communication. A dedicated baud rate generator with a fractional divider precisely generates all standard baud rates without oscillator tuning. For transmission, reception, error handling, and baudrate detection 5 separate interrupt vectors are provided.

In asynchronous mode, 8- or 9-bit data frames (with optional parity bit) are transmitted or received, preceded by a start bit and terminated by one or two stop bits. For multiprocessor communication, a mechanism to distinguish address from data bytes has been included (8-bit data plus wake-up bit mode). IrDA data transmissions up to 115.2 kbit/s with fixed or programmable IrDA pulse width are supported.

In synchronous mode, bytes (8 bits) are transmitted or received synchronously to a shift clock which is generated by the ASC0/1. The LSB is always shifted first.

In both modes, transmission and reception of data is FIFO-buffered. An autobaud detection unit allows to detect asynchronous data frames with its baudrate and mode with automatic initialization of the baudrate generator and the mode control bits.

A number of optional hardware error detection capabilities has been included to increase the reliability of data transfers. A parity bit can automatically be generated on transmission or be checked on reception. Framing error detection allows to recognize data frames with missing stop bits. An overrun error will be generated, if the last character received has not been read out of the receive buffer register at the time the reception of a new character is complete.

Summary of Features

- Full-duplex asynchronous operating modes
  - 8- or 9-bit data frames, LSB first, one or two stop bits, parity generation/checking
  - Baudrate from 2.5 Mbit/s to 0.6 bit/s (@ 40 MHz)
  - Multiprocessor mode for automatic address/data byte detection
  - Support for IrDA data transmission/reception up to max. 115.2 kbit/s (@ 40 MHz)
  - Loop-back capability
  - Auto baudrate detection
- Half-duplex 8-bit synchronous operating mode at 5 Mbit/s to 406.9 bit/s (@ 40 MHz)
- Buffered transmitter/receiver with FIFO support (8 entries per direction)
- Loop-back option available for testing purposes
- Interrupt generation on transmitter buffer empty condition, last bit transmitted condition, receive buffer full condition, error condition (frame, parity, overrun error), start and end of an autobaud detection

3.19 Instruction Set Summary

Table 8 lists the instructions of the XC167 in a condensed way.
The various addressing modes that can be used with a specific instruction, the operation of the instructions, parameters for conditional execution of instructions, and the opcodes for each instruction can be found in the **"Instruction Set Manual"**.

This document also provides a detailed description of each instruction.

Table 8 Instruction Set Summary

Mnemonic	Description	Bytes
ADD(B)	Add word (byte) operands	2 / 4
ADDC(B)	Add word (byte) operands with Carry	2 / 4
SUB(B)	Subtract word (byte) operands	2 / 4
SUBC(B)	Subtract word (byte) operands with Carry	2 / 4
MUL(U)	(Un)Signed multiply direct GPR by direct GPR (16- × 16-bit)	2
DIV(U)	(Un)Signed divide register MDL by direct GPR (16-/16-bit)	2
DIVL(U)	(Un)Signed long divide reg. MD by direct GPR (32-/16-bit)	2
CPL(B)	Complement direct word (byte) GPR	2
NEG(B)	Negate direct word (byte) GPR	2
AND(B)	Bitwise AND, (word/byte operands)	2 / 4
OR(B)	Bitwise OR, (word/byte operands)	2 / 4
XOR(B)	Bitwise exclusive OR, (word/byte operands)	2 / 4
BCLR/BSET	Clear/Set direct bit	2
BMOV(N)	Move (negated) direct bit to direct bit	4
BAND/BOR/BXOR	AND/OR/XOR direct bit with direct bit	4
BCMP	Compare direct bit to direct bit	4
BFLDH/BFLDL	Bitwise modify masked high/low byte of bit-addressable direct word memory with immediate data	4
CMP(B)	Compare word (byte) operands	2 / 4
CMPD1/2	Compare word data to GPR and decrement GPR by 1/2	2 / 4
CMPI1/2	Compare word data to GPR and increment GPR by 1/2	2 / 4
PRIOR	Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR	2
SHL/SHR	Shift left/right direct word GPR	2

Operating Conditions

The following operating conditions must not be exceeded to ensure correct operation of the XC167. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

Table 10 Operating Condition Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Digital supply voltage for the core	V_{DDI}	2.35	2.7	V	Active mode, $f_{CPU} = f_{CPUmax}$ 1)2)
Digital supply voltage for IO pads	V_{DDP}	4.4	5.5	V	Active mode 2)
Supply Voltage Difference	ΔV_{DD}	-0.5	–	V	V_{DDP} - V_{DDI} 3)
Digital ground voltage	V_{SS}	0		V	Reference voltage
Overload current	I_{OV}	-5	5	mA	Per IO pin 4)5)
		-2	5	mA	Per analog input pin 4)5)
Overload current coupling factor for analog inputs 6)	K_{OVA}	–	1.0×10^{-4}	–	$I_{OV} > 0$
		–	1.5×10^{-3}	–	$I_{OV} < 0$
Overload current coupling factor for digital I/O pins 6)	K_{OVD}	–	5.0×10^{-3}	–	$I_{OV} > 0$
		–	1.0×10^{-2}	–	$I_{OV} < 0$
Absolute sum of overload currents	$\Sigma\|I_{OV}\|$	–	50	mA	5)
External Load Capacitance	C_L	–	50	pF	Pin drivers in **default** mode 7)
Ambient temperature	T_A	0	70	°C	SAB-XC167…
		-40	85	°C	SAF-XC167…
		-40	125	°C	SAK-XC167…

1) f_{CPUmax} = 40 MHz for devices marked … 40F, f_{CPUmax} = 20 MHz for devices marked … 20F.

2) External circuitry must guarantee low level at the $\overline{\text{RSTIN}}$ pin at least until both power supply voltages have reached their operating range.

3) This limitation must be fulfilled under all operating conditions including power-ramp-up, power-ramp-down, and power-save modes.

4.2 DC Parameters

Table 11 DC Characteristics (Operating Conditions apply)[1)]

Parameter	Symbol		Limit Values		Unit	Test Condition
			Min.	Max.		
Input low voltage TTL (all except XTAL1, XTAL3)	V_{IL}	SR	-0.5	$0.2 \times V_{DDP}$ - 0.1	V	–
Input low voltage for XTAL1, XTAL3[2)3)]	V_{ILC}	SR	-0.5	$0.3 \times V_{DDI}$	V	–
Input low voltage (Special Threshold)	V_{ILS}	SR	-0.5	$0.45 \times V_{DDP}$	V	[4)]
Input high voltage TTL (all except XTAL1, XTAL3)	V_{IH}	SR	$0.2 \times V_{DDP}$ + 0.9	V_{DDP} + 0.5	V	–
Input high voltage XTAL1, XTAL3[2)3)]	V_{IHC}	SR	$0.7 \times V_{DDI}$	V_{DDI} + 0.5	V	–
Input high voltage (Special Threshold)	V_{IHS}	SR	$0.8 \times V_{DDP}$ - 0.2	V_{DDP} + 0.5	V	[4)]
Input Hysteresis (Special Threshold)	HYS		$0.04 \times V_{DDP}$	–	V	V_{DDP} in [V], Series resistance = 0 Ω[4)]
Output low voltage	V_{OL}	CC	–	1.0	V	$I_{OL} \le I_{OLmax}$[5)]
			–	0.45	V	$I_{OL} \le I_{OLnom}$[5)6)]
Output high voltage[7)]	V_{OH}	CC	V_{DDP} - 1.0	–	V	$I_{OH} \ge I_{OHmax}$[5)]
			V_{DDP} - 0.45	–	V	$I_{OH} \ge I_{OHnom}$[5)6)]
Input leakage current (Port 5)[8)]	I_{OZ1}	CC	–	±300	nA	$0\ V < V_{IN} < V_{DDP}$, $T_A \le 125$ °C
				±200	nA	$0\ V < V_{IN} < V_{DDP}$, $T_A \le 85$ °C[15)]
Input leakage current (all other[9)])[8)]	I_{OZ2}	CC	–	±500	nA	$0.45\ V < V_{IN} < V_{DDP}$
Configuration pull-up current[10)]	I_{CPUH}[11)]		–	-10	µA	$V_{IN} = V_{IHmin}$
	I_{CPUL}[12)]		-100	–	µA	$V_{IN} = V_{ILmax}$

Table 11 DC Characteristics (Operating Conditions apply)[1] (cont'd)

Parameter	Symbol		Limit Values		Unit	Test Condition
			Min.	Max.		
Configuration pull-down current[13]	I_{CPDL}[11]		–	10	µA	$V_{IN} = V_{ILmax}$
	I_{CPDH}[12]		120	–	µA	$V_{IN} = V_{IHmin}$
Level inactive hold current[14]	I_{LHI}[11]		–	-10	µA	$V_{OUT} = 0.5 \times V_{DDP}$
Level active hold current[14]	I_{LHA}[12]		-100	–	µA	V_{OUT} = 0.45 V
XTAL1, XTAL3 input current	I_{IL}	CC	–	±20	µA	0 V < V_{IN} < V_{DDI}
Pin capacitance[15] (digital inputs/outputs)	C_{IO}	CC	–	10	pF	–

1) Keeping signal levels within the limits specified in this table, ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current I_{OV}.

2) If XTAL1 is driven by a crystal, reaching an amplitude (peak to peak) of 0.4 × V_{DDI} is sufficient.

3) If XTAL3 is driven by a crystal, reaching an amplitude (peak to peak) of 0.25 × V_{DDI} is sufficient.

4) This parameter is tested for P2, P3, P4, P6, P7, P9.

5) The maximum deliverable output current of a port driver depends on the selected output driver mode, see **Table 12, Current Limits for Port Output Drivers**. The limit for pin groups must be respected.

6) As a rule, with decreasing output current the output levels approach the respective supply level ($V_{OL} \rightarrow V_{SS}$, $V_{OH} \rightarrow V_{DDP}$). However, only the levels for nominal output currents are guaranteed.

7) This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage results from the external circuitry.

8) An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin. Please refer to the definition of the overload coupling factor K_{OV}.

9) The driver of P3.15 is designed for faster switching, because this pin can deliver the reference clock for the bus interface (CLKOUT). The maximum leakage current for P3.15 is, therefore, increased to 1 µA.

10) This specification is valid during Reset for configuration on $\overline{RD}$, $\overline{WR}$, $\overline{EA}$, PORT0.
The pull-ups on $\overline{RD}$ and $\overline{WR}$ ($\overline{WRL}$/$\overline{WRH}$) are also active during bus hold.

11) The maximum current may be drawn while the respective signal line remains inactive.

12) The minimum current must be drawn to drive the respective signal line active.

13) This specification is valid during Reset for configuration on ALE.
The pull-down on ALE is also active during bus hold.

14) This specification is valid during Reset for pins P6.4-0, which can act as $\overline{CS}$ outputs.
The pull-ups on $\overline{CS}$ outputs are also active during bus hold.
The pull-up on pin $\overline{HLDA}$ is active when arbitration is enabled and the EBC operates in slave mode.

15) Not subject to production test - verified by design/characterization.

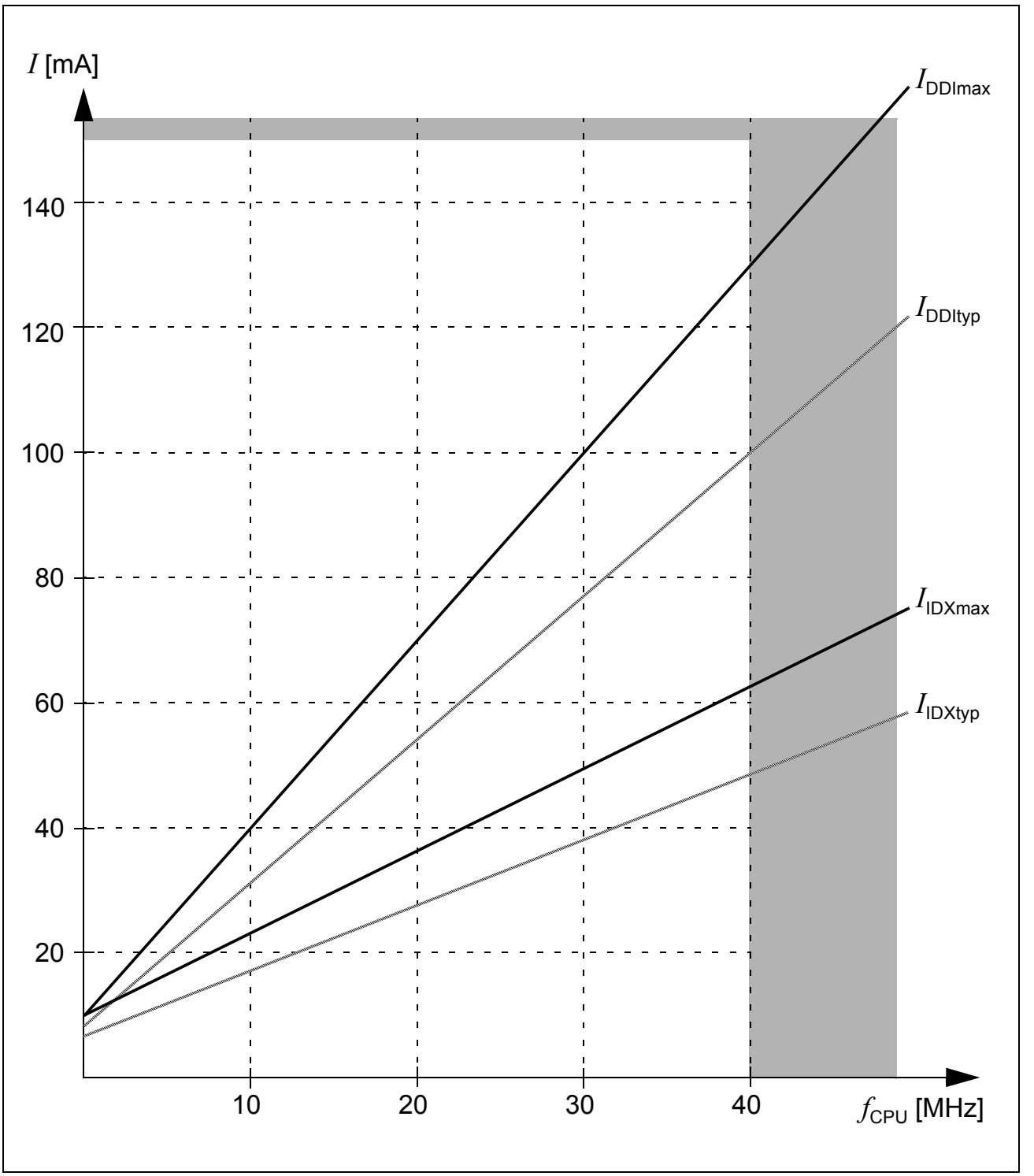


Figure 11 Supply/Idle Current as a Function of Operating Frequency

4.4 AC Parameters

4.4.1 Definition of Internal Timing

The internal operation of the XC167 is controlled by the internal master clock f_{MC}.

The master clock signal f_{MC} can be generated from the oscillator clock signal f_{OSC} via different mechanisms. The duration of master clock periods (TCMs) and their variation (and also the derived external timing) depend on the used mechanism to generate f_{MC}. This influence must be regarded when calculating the timings for the XC167.

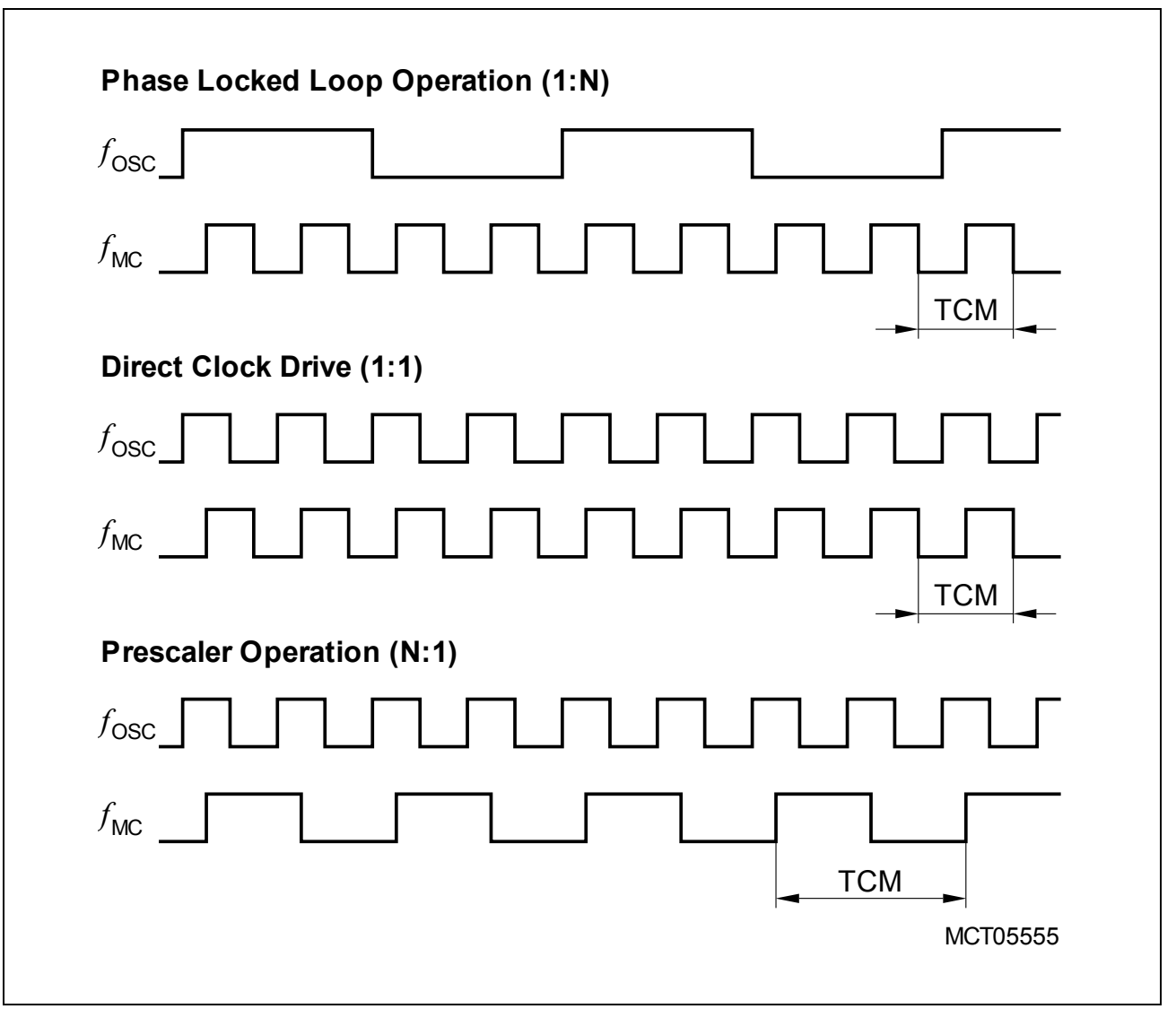


Figure 15 Generation Mechanisms for the Master Clock

*Note: The example for PLL operation shown in **Figure 15** refers to a PLL factor of 1:4, the example for prescaler operation refers to a divider factor of 2:1.*

The used mechanism to generate the master clock is selected by register PLLCON.

generation or measurement, lower baudrates, etc.) the deviation caused by the PLL jitter is negligible.

The value of the accumulated PLL jitter depends on the number of consecutive VCO output cycles within the respective timeframe. The VCO output clock is divided by the output prescaler (K = PLLODIV+1) to generate the master clock signal f_{MC}. Therefore, the number of VCO cycles can be represented as K × **N**, where **N** is the number of consecutive f_{MC} cycles (TCM).

For a period of **N** × TCM the accumulated PLL jitter is defined by the deviation D_N:

D_N [ns] = ±(1.5 + 6.32 × **N** / f_{MC}); f_{MC} in [MHz], **N** = number of consecutive TCMs.

So, for a period of 3 TCMs @ 20 MHz and K = 12: D_3 = ±(1.5 + 6.32 × **3** / 20) = 2.448 ns.

This formula is applicable for K × **N** < 95. For longer periods the K × **N** = 95 value can be used. This steady value can be approximated by: D_{Nmax} [ns] = ±(1.5 + 600 / (K × f_{MC})).

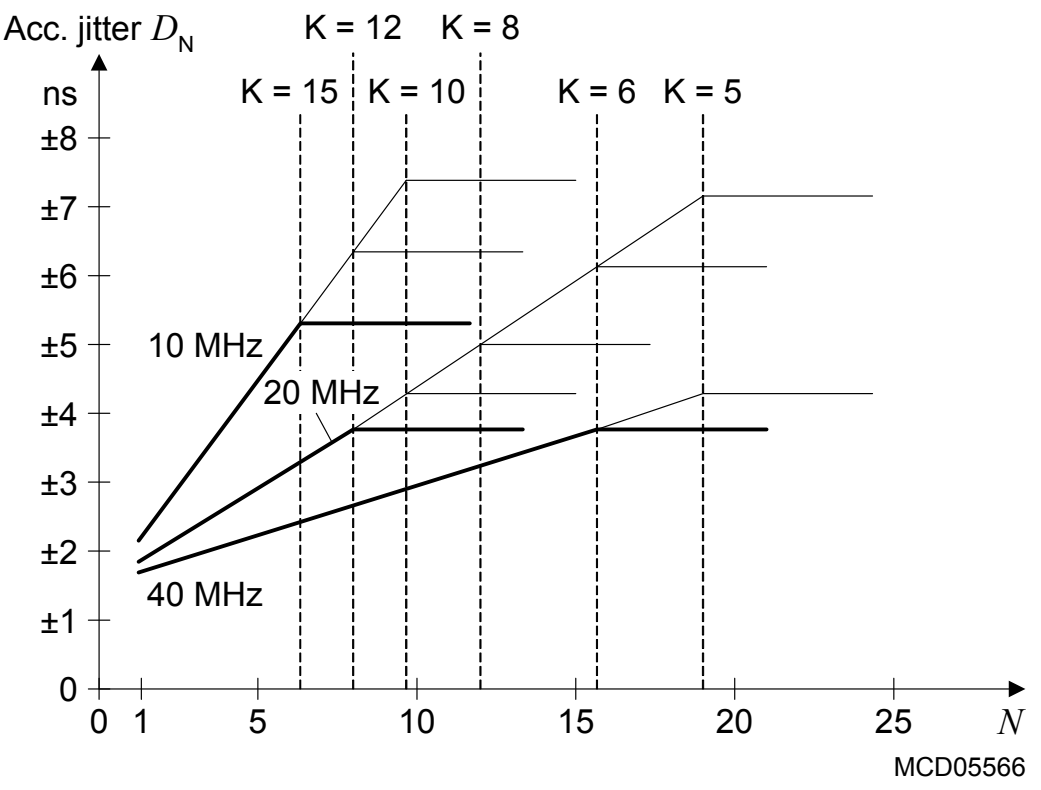
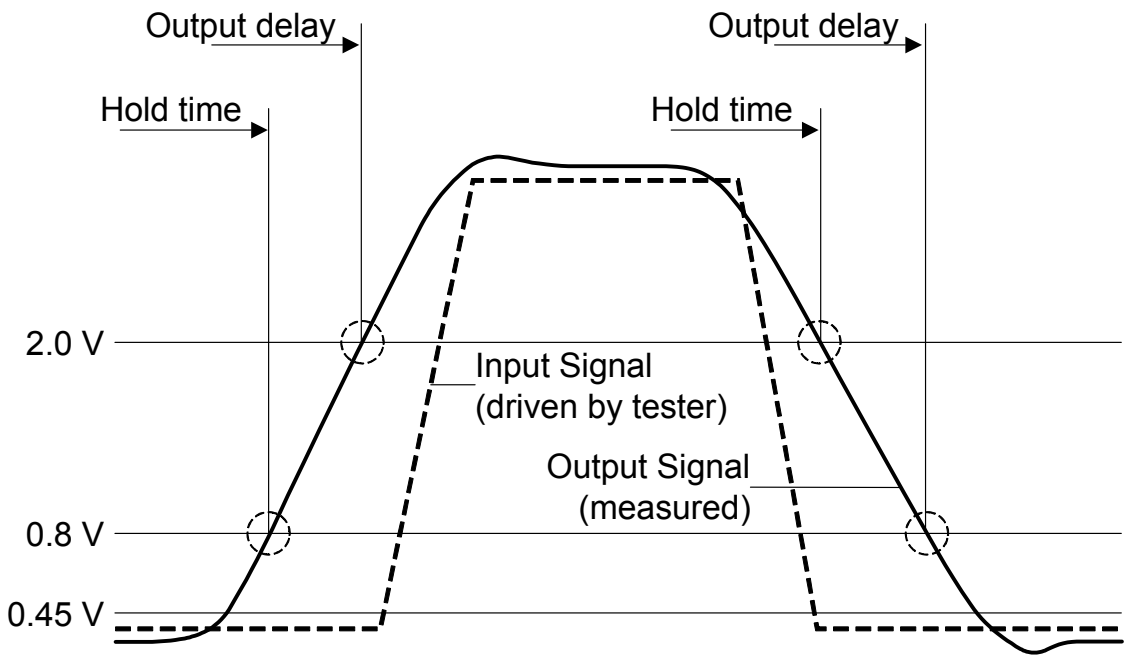


Figure 16 Approximated Accumulated PLL Jitter

Note: The bold lines indicate the minimum accumulated jitter which can be achieved by selecting the maximum possible output prescaler factor K.

Different frequency bands can be selected for the VCO, so the operation of the PLL can be adjusted to a wide range of input and output frequencies:

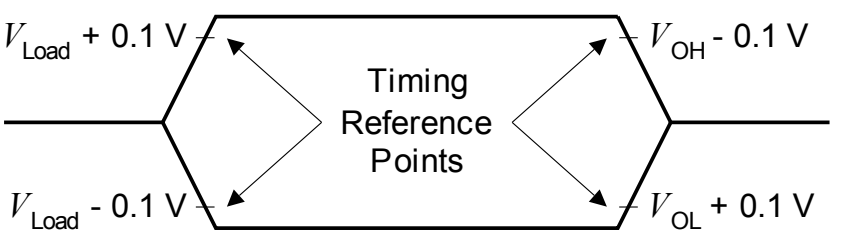
4.4.4 Testing Waveforms



Output timings refer to the rising edge of CLKOUT.
Input timings are calculated from the time, when the input signal reaches V_{IH} or V_{IL}, respectively.

MCD05556

Figure 18 Input Output Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, but begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs (I_{OH}/I_{OL} = 20 mA).

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Figure 19 Float Waveforms

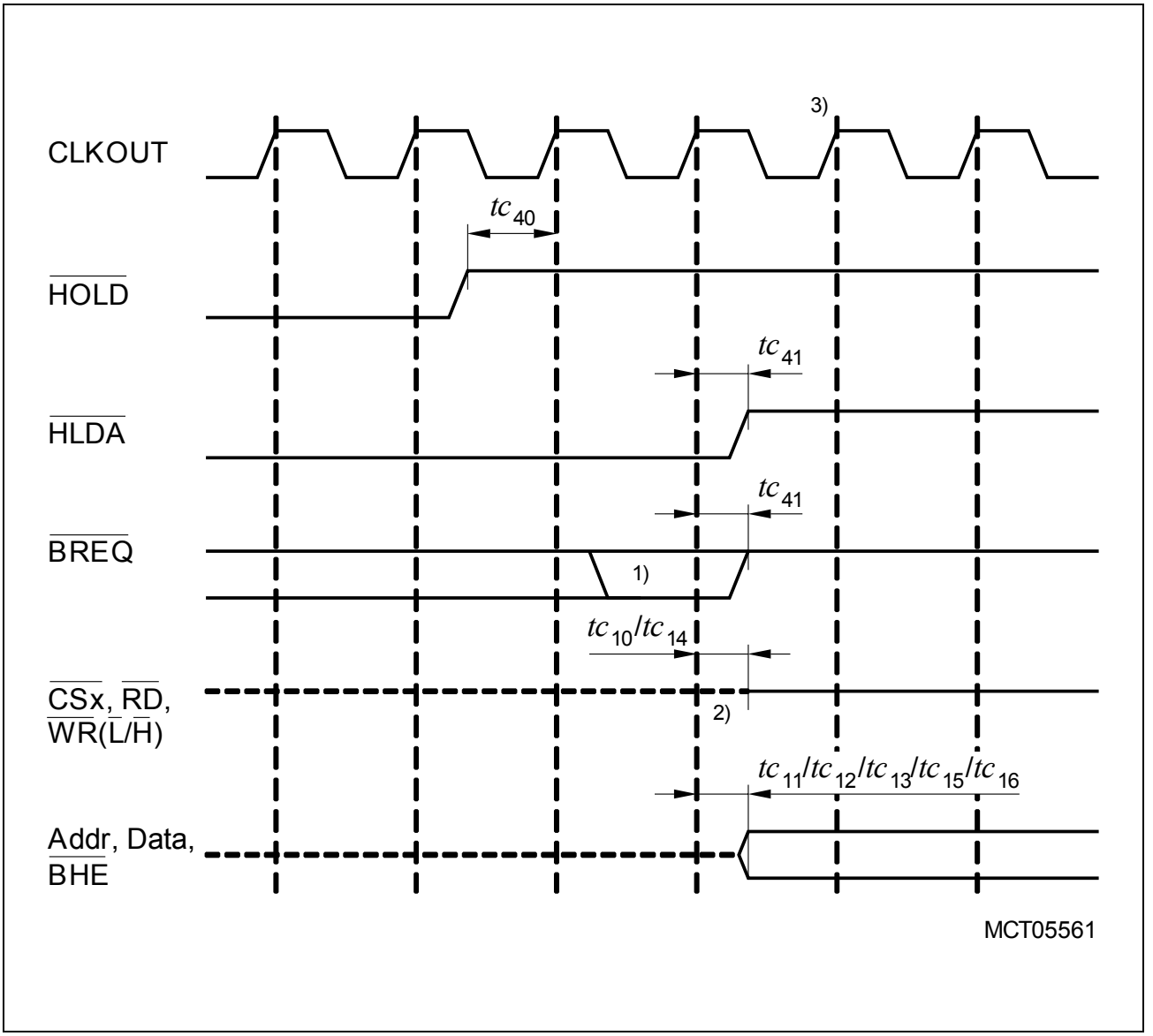

Figure 25 External Bus Arbitration, Regaining the Bus

Notes

1. *This is the last chance for $\overline{BREQ}$ to trigger the indicated regain-sequence. Even if $\overline{BREQ}$ is activated earlier, the regain-sequence is initiated by $\overline{HOLD}$ going high. Please note that $\overline{HOLD}$ may also be deactivated without the XC167 requesting the bus.*
2. *The control outputs will be resistive high (pull-up) before being driven inactive (ALE will be low).*
3. *The next XC167 driven bus cycle may start here.*