Infineon Technologies - XC167CI32F40FBBAFXUMA1 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Last Time Buy
Core Processor	C166SV2
Core Size	16-Bit
Speed	40MHz
Connectivity	CANbus, EBI/EMI, I²C, SPI, UART/USART
Peripherals	PWM, WDT
Number of I/O	103
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 2.7V
Data Converters	A/D 16x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	PG-TQFP-144-7
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc167ci32f40fbbafxuma1

XC167CI-32F

16-Bit Single-Chip Microcontroller with C166SV2 Core

Microcontrollers

Never stop thinking

Table of Contents

1 Summary of Features

- High Performance 16-bit CPU with 5-Stage Pipeline
  - 25 ns Instruction Cycle Time at 40 MHz CPU Clock (Single-Cycle Execution)
  - 1-Cycle Multiplication (16 × 16 bit), Background Division (32 / 16 bit) in 21 Cycles
  - 1-Cycle Multiply-and-Accumulate (MAC) Instructions
  - Enhanced Boolean Bit Manipulation Facilities
  - Zero-Cycle Jump Execution
  - Additional Instructions to Support HLL and Operating Systems
  - Register-Based Design with Multiple Variable Register Banks
  - Fast Context Switching Support with Two Additional Local Register Banks
  - 16 Mbytes Total Linear Address Space for Code and Data
  - 1024 bytes On-Chip Special Function Register Area (C166 Family Compatible)
- 16-Priority-Level Interrupt System with 77 Sources, Sample-Rate down to 50 ns
- 8-Channel Interrupt-Driven Single-Cycle Data Transfer Facilities via Peripheral Event Controller (PEC), 24-Bit Pointers Cover Total Address Space
- Clock Generation via on-chip PLL (factors 1:0.15 … 1:10), or via Prescaler (factors 1:1 … 60:1)
- On-Chip Memory Modules
  - 2 Kbytes On-Chip Dual-Port RAM (DPRAM)
  - 4 Kbytes On-Chip Data SRAM (DSRAM)
  - 6 Kbytes On-Chip Program/Data SRAM (PSRAM)
  - 256 Kbytes On-Chip Program Memory (Flash Memory)
- On-Chip Peripheral Modules
  - 16-Channel A/D Converter with Programmable Resolution (10-bit or 8-bit) and Conversion Time (down to 2.55 µs or 2.15 µs)
  - Two 16-Channel General Purpose Capture/Compare Units (32 Input/Output Pins)
  - Capture/Compare Unit for flexible PWM Signal Generation (CAPCOM6) (3/6 Capture/Compare Channels and 1 Compare Channel)
  - Multi-Functional General Purpose Timer Unit with 5 Timers
  - Two Synchronous/Asynchronous Serial Channels (USARTs)
  - Two High-Speed-Synchronous Serial Channels
  - On-Chip TwinCAN Interface (Rev. 2.0B active) with 32 Message Objects (Full CAN/Basic CAN) on Two CAN Nodes, and Gateway Functionality
  - IIC Bus Interface (10-bit addressing, 400 kbit/s) with 3 Channels (multiplexed)
  - On-Chip Real Time Clock, Driven by Dedicated Oscillator
- Idle, Sleep, and Power Down Modes with Flexible Power Management
- Programmable Watchdog Timer and Oscillator Watchdog

Table 2 Pin Definitions and Functions

Sym-bol	Pin Num.	Input Outp.	Function
P20.12	3	IO	For details, please refer to the description of **P20**.
NMI	4	I	Non-Maskable Interrupt Input. A high to low transition at this pin causes the CPU to vector to the NMI trap routine. When the PWRDN (power down) instruction is executed, the NMI pin must be low in order to force the XC167 into power down mode. If NMI is high, when PWRDN is executed, the part will continue to run in normal mode. If not used, pin NMI should be pulled high externally.
P6		IO	Port 6 is an 8-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output (configurable as push/pull or open drain driver). The input threshold of Port 6 is selectable (standard or special). The Port 6 pins also serve for alternate functions:
P6.0	7	O	CS0 Chip Select 0 Output,
		IO	CC0IO CAPCOM1: CC0 Capture Inp./Compare Output
P6.1	8	O	CS1 Chip Select 1 Output,
		IO	CC1IO CAPCOM1: CC1 Capture Inp./Compare Output
P6.2	9	O	CS2 Chip Select 2 Output,
		IO	CC2IO CAPCOM1: CC2 Capture Inp./Compare Output
P6.3	10	O	CS3 Chip Select 3 Output,
		IO	CC3IO CAPCOM1: CC3 Capture Inp./Compare Output
P6.4	11	O	CS4 Chip Select 4 Output,
		IO	CC4IO CAPCOM1: CC4 Capture Inp./Compare Output
P6.5	12	I	HOLD External Master Hold Request Input,
		IO	CC5IO CAPCOM1: CC5 Capture Inp./Compare Output
P6.6	13	I/O	HLDA Hold Acknowledge Output (master mode) or Input (slave mode),
		IO	CC6IO CAPCOM1: CC6 Capture Inp./Compare Output
P6.7	14	O	BREQ Bus Request Output,
		IO	CC7IO CAPCOM1: CC7 Capture Inp./Compare Output

Table 2 Pin Definitions and Functions (cont'd)

Sym-bol	Pin Num.	Input Outp.	Function
PORT0 P0L.0 - P0L.7, P0H.0, P0H.1, P0H.2 - P0H.7	 95 - 102, 105, 106, 111 - 116	IO	PORT0 consists of the two 8-bit bidirectional I/O ports P0L and P0H. Each pin can be programmed for input (output driver in high-impedance state) or output. In case of an external bus configuration, PORT0 serves as the address (A) and address/data (AD) bus in multiplexed bus modes and as the data (D) bus in demultiplexed bus modes. **Demultiplexed bus modes:** 8-bit data bus: P0H = I/O, P0L = D7 - D0 16-bit data bus: P0H = D15 - D8, P0L = D7 - D0 **Multiplexed bus modes:** 8-bit data bus: P0H = A15 - A8, P0L = AD7 - AD0 16-bit data bus: P0H = AD15 - AD8, P0L = AD7 - AD0 *Note: At the end of an external reset ($\overline{EA}$ = 0) PORT0 also may input configuration values.*

Table 4 XC167 Interrupt Nodes (cont'd)

Source of Interrupt or PEC Service Request	Control Register	Vector Location[1)]	Trap Number
ASC1 Autobaud	ASC1_ABIC	xx'0108$_H$	42$_H$ / 66$_D$
End of PEC Subchannel	EOPIC	xx'0130$_H$	4C$_H$ / 76$_D$
CAPCOM6 Timer T12	CCU6_T12IC	xx'0134$_H$	4D$_H$ / 77$_D$
CAPCOM6 Timer T13	CCU6_T13IC	xx'0138$_H$	4E$_H$ / 78$_D$
CAPCOM6 Emergency	CCU6_EIC	xx'013C$_H$	4F$_H$ / 79$_D$
CAPCOM6	CAPCOM6	xx'0140$_H$	50$_H$ / 80$_D$
SSC1 Transmit	SSC1_TIC	xx'0144$_H$	51$_H$ / 81$_D$
SSC1 Receive	SSC1_RIC	xx'0148$_H$	52$_H$ / 82$_D$
SSC1 Error	SSC1_EIC	xx'014C$_H$	53$_H$ / 83$_D$
CAN0	CAN_0IC	xx'0150$_H$	54$_H$ / 84$_D$
CAN1	CAN_1IC	xx'0154$_H$	55$_H$ / 85$_D$
CAN2	CAN_2IC	xx'0158$_H$	56$_H$ / 86$_D$
CAN3	CAN_3IC	xx'015C$_H$	57$_H$ / 87$_D$
CAN4	CAN_4IC	xx'0164$_H$	59$_H$ / 89$_D$
CAN5	CAN_5IC	xx'0168$_H$	5A$_H$ / 90$_D$
CAN6	CAN_6IC	xx'016C$_H$	5B$_H$ / 91$_D$
CAN7	CAN_7IC	xx'0170$_H$	5C$_H$ / 92$_D$
RTC	RTC_IC	xx'0174$_H$	5D$_H$ / 93$_D$
Unassigned node	–	xx'012C$_H$	3F$_H$ / 63$_D$
Unassigned node	–	xx'00FC$_H$	3F$_H$ / 63$_D$
Unassigned node	–	xx'0160$_H$	58$_H$ / 88$_D$

1) Register VECSEG defines the segment where the vector table is located to.
Bitfield VECSC in register CPUCON1 defines the distance between two adjacent vectors. This table represents the default setting, with a distance of 4 (two words) between two vectors.

The XC167 also provides an excellent mechanism to identify and to process exceptions or error conditions that arise during run-time, so-called ‘Hardware Traps’. Hardware traps cause immediate non-maskable system reaction which is similar to a standard interrupt service (branching to a dedicated vector table location). The occurrence of a hardware trap is additionally signified by an individual bit in the trap flag register (TFR). Except when another higher prioritized trap service is in progress, a hardware trap will interrupt any actual program execution. In turn, hardware trap services can normally not be interrupted by standard or PEC interrupts.

Table 5 shows all of the possible exceptions or error conditions that can arise during run-time:

Table 5 Hardware Trap Summary

Exception Condition	Trap Flag	Trap Vector	Vector Location[1)]	Trap Number	Trap Priority
Reset Functions:	–				
• Hardware Reset		RESET	xx’0000$_H$	00$_H$	III
• Software Reset		RESET	xx’0000$_H$	00$_H$	III
• Watchdog Timer Overflow		RESET	xx’0000$_H$	00$_H$	III
Class A Hardware Traps:					
• Non-Maskable Interrupt	NMI	NMITRAP	xx’0008$_H$	02$_H$	II
• Stack Overflow	STKOF	STOTRAP	xx’0010$_H$	04$_H$	II
• Stack Underflow	STKUF	STUTRAP	xx’0018$_H$	06$_H$	II
• Software Break	SOFTBRK	SBRKTRAP	xx’0020$_H$	08$_H$	II
Class B Hardware Traps:					
• Undefined Opcode	UNDOPC	BTRAP	xx’0028$_H$	0A$_H$	I
• PMI Access Error	PACER	BTRAP	xx’0028$_H$	0A$_H$	I
• Protected Instruction Fault	PRTFLT	BTRAP	xx’0028$_H$	0A$_H$	I
• Illegal Word Operand Access	ILLOPA	BTRAP	xx’0028$_H$	0A$_H$	I
Reserved	–	–	[2C$_H$ - 3C$_H$]	[0B$_H$ - 0F$_H$]	–
Software Traps • TRAP Instruction	–	–	Any [xx’0000$_H$ - xx’01FC$_H$] in steps of 4$_H$	Any [00$_H$ - 7F$_H$]	Current CPU Priority

1) Register VECSEG defines the segment where the vector table is located to.

3.5 On-Chip Debug Support (OCDS)

The On-Chip Debug Support system provides a broad range of debug and emulation features built into the XC167. The user software running on the XC167 can thus be debugged within the target system environment.

The OCDS is controlled by an external debugging device via the debug interface, consisting of the IEEE-1149-conforming JTAG port and a break interface. The debugger controls the OCDS via a set of dedicated registers accessible via the JTAG interface. Additionally, the OCDS system can be controlled by the CPU, e.g. by a monitor program. An injection interface allows the execution of OCDS-generated instructions by the CPU.

Multiple breakpoints can be triggered by on-chip hardware, by software, or by an external trigger input. Single stepping is supported as well as the injection of arbitrary instructions and read/write access to the complete internal address space. A breakpoint trigger can be answered with a CPU-halt, a monitor call, a data transfer, or/and the activation of an external signal.

Tracing data can be obtained via the JTAG interface or via the external bus interface for increased performance.

The debug interface uses a set of 6 interface signals (4 JTAG lines, 2 break lines) to communicate with external circuitry. These interface signals use dedicated pins.

Complete system emulation is supported by the New Emulation Technology (NET) interface.

3.7 The Capture/Compare Unit CAPCOM6

The CAPCOM6 unit supports generation and control of timing sequences on up to three 16-bit capture/compare channels plus one independent 10-bit compare channel.
In compare mode the CAPCOM6 unit provides two output signals per channel which have inverted polarity and non-overlapping pulse transitions (deadtime control). The compare channel can generate a single PWM output signal and is further used to modulate the capture/compare output signals.
In capture mode the contents of compare timer T12 is stored in the capture registers upon a signal transition at pins CCx.

Compare timers T12 (16-bit) and T13 (10-bit) are free running timers which are clocked by the prescaled system clock.

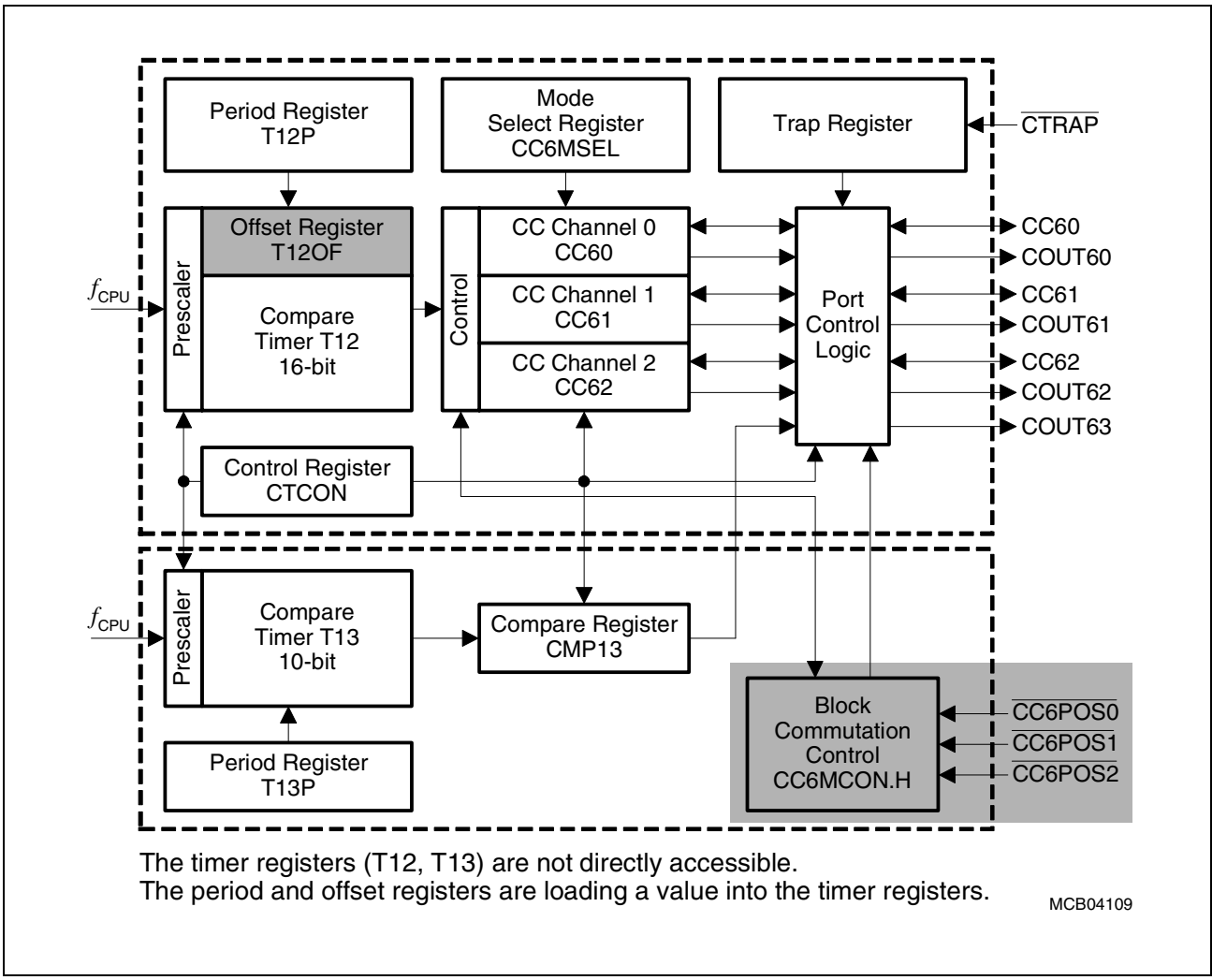

Figure 6 CAPCOM6 Block Diagram

For motor control applications both subunits may generate versatile multichannel PWM signals which are basically either controlled by compare timer T12 or by a typical hall sensor pattern at the interrupt inputs (block commutation).

3.12 High Speed Synchronous Serial Channels (SSC0/SSC1)

The High Speed Synchronous Serial Channels SSC0/SSC1 support full-duplex and half-duplex synchronous communication. It may be configured so it interfaces with serially linked peripheral components, full SPI functionality is supported.

A dedicated baud rate generator allows to set up all standard baud rates without oscillator tuning. For transmission, reception and error handling three separate interrupt vectors are provided.

The SSC transmits or receives characters of 2 … 16 bits length synchronously to a shift clock which can be generated by the SSC (master mode) or by an external master (slave mode). The SSC can start shifting with the LSB or with the MSB and allows the selection of shifting and latching clock edges as well as the clock polarity.

A number of optional hardware error detection capabilities has been included to increase the reliability of data transfers. Transmit error and receive error supervise the correct handling of the data buffer. Phase error and baudrate error detect incorrect serial data.

Summary of Features

- Master or Slave mode operation
- Full-duplex or Half-duplex transfers
- Baudrate generation from 20 Mbit/s to 305.18 bit/s (@ 40 MHz)
- Flexible data format
  - Programmable number of data bits: 2 to 16 bits
  - Programmable shift direction: LSB-first or MSB-first
  - Programmable clock polarity: idle low or idle high
  - Programmable clock/data phase: data shift with leading or trailing clock edge
- Loop back option available for testing purposes
- Interrupt generation on transmitter buffer empty condition, receive buffer full condition, error condition (receive, phase, baudrate, transmit error)
- Three pin interface with flexible SSC pin configuration

Summary of Features

- CAN functionality according to CAN specification V2.0 B active
- Data transfer rate up to 1 Mbit/s
- Flexible and powerful message transfer control and error handling capabilities
- Full-CAN functionality and Basic CAN functionality for each message object
- 32 flexible message objects
  - Assignment to one of the two CAN nodes
  - Configuration as transmit object or receive object
  - Concatenation to a 2-, 4-, 8-, 16-, or 32-message buffer with FIFO algorithm
  - Handling of frames with 11-bit or 29-bit identifiers
  - Individual programmable acceptance mask register for filtering for each object
  - Monitoring via a frame counter
  - Configuration for Remote Monitoring Mode
- Up to eight individually programmable interrupt nodes can be used
- CAN Analyzer Mode for bus monitoring is implemented

Note: When a CAN node has the interface lines assigned to Port 4, the segment address output on Port 4 must be limited. $\overline{CS}$ lines can be used to increase the total amount of addressable external memory.

3.14 IIC Bus Module

The integrated IIC Bus Module handles the transmission and reception of frames over the two-line IIC bus in accordance with the IIC Bus specification. The IIC Module can operate in slave mode, in master mode or in multi-master mode. It can receive and transmit data using 7-bit or 10-bit addressing. Up to 4 send/receive data bytes can be stored in the extended buffers.

Several physical interfaces (port pins) can be established under software control. Data can be transferred at speeds up to 400 kbit/s.

Two interrupt nodes dedicated to the IIC module allow efficient interrupt service and also support operation via PEC transfers.

Note: The port pins associated with the IIC interfaces must be switched to open drain mode, as required by the IIC specification.

3.19 Instruction Set Summary

Table 8 lists the instructions of the XC167 in a condensed way.
The various addressing modes that can be used with a specific instruction, the operation of the instructions, parameters for conditional execution of instructions, and the opcodes for each instruction can be found in the **"Instruction Set Manual"**.

This document also provides a detailed description of each instruction.

Table 8 Instruction Set Summary

Mnemonic	Description	Bytes
ADD(B)	Add word (byte) operands	2 / 4
ADDC(B)	Add word (byte) operands with Carry	2 / 4
SUB(B)	Subtract word (byte) operands	2 / 4
SUBC(B)	Subtract word (byte) operands with Carry	2 / 4
MUL(U)	(Un)Signed multiply direct GPR by direct GPR (16- × 16-bit)	2
DIV(U)	(Un)Signed divide register MDL by direct GPR (16-/16-bit)	2
DIVL(U)	(Un)Signed long divide reg. MD by direct GPR (32-/16-bit)	2
CPL(B)	Complement direct word (byte) GPR	2
NEG(B)	Negate direct word (byte) GPR	2
AND(B)	Bitwise AND, (word/byte operands)	2 / 4
OR(B)	Bitwise OR, (word/byte operands)	2 / 4
XOR(B)	Bitwise exclusive OR, (word/byte operands)	2 / 4
BCLR/BSET	Clear/Set direct bit	2
BMOV(N)	Move (negated) direct bit to direct bit	4
BAND/BOR/BXOR	AND/OR/XOR direct bit with direct bit	4
BCMP	Compare direct bit to direct bit	4
BFLDH/BFLDL	Bitwise modify masked high/low byte of bit-addressable direct word memory with immediate data	4
CMP(B)	Compare word (byte) operands	2 / 4
CMPD1/2	Compare word data to GPR and decrement GPR by 1/2	2 / 4
CMPI1/2	Compare word data to GPR and increment GPR by 1/2	2 / 4
PRIOR	Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR	2
SHL/SHR	Shift left/right direct word GPR	2

Table 8 Instruction Set Summary (cont'd)

Mnemonic	Description	Bytes
NOP	Null operation	2
CoMUL/CoMAC	Multiply (and accumulate)	4
CoADD/CoSUB	Add/Subtract	4
Co(A)SHR	(Arithmetic) Shift right	4
CoSHL	Shift left	4
CoLOAD/STORE	Load accumulator/Store MAC register	4
CoCMP	Compare	4
CoMAX/MIN	Maximum/Minimum	4
CoABS/CoRND	Absolute value/Round accumulator	4
CoMOV	Data move	4
CoNEG/NOP	Negate accumulator/Null operation	4

3) The limit values for f_{BC} must not be exceeded when selecting the peripheral frequency and the ADCTC setting.
4) This parameter includes the sample time t_S, the time for determining the digital result and the time to load the result register with the conversion result (t_{SYS} = 1/f_{SYS}).
Values for the basic clock t_{BC} depend on programming and can be taken from **Table 15**.
When the post-calibration is switched off, the conversion time is reduced by 12 × t_{BC}.
5) The actual duration of the reset calibration depends on the noise on the reference signal. Conversions executed during the reset calibration increase the calibration time. The TUE for those conversions may be increased.
6) Not subject to production test - verified by design/characterization.
The given parameter values cover the complete operating range. Under relaxed operating conditions (temperature, supply voltage) reduced values can be used for calculations. At room temperature and nominal supply voltage the following typical values can be used:
$C_{AINTtyp}$ = 12 pF, $C_{AINStyp}$ = 7 pF, R_{AINtyp} = 1.5 kΩ, $C_{AREFTtyp}$ = 15 pF, $C_{AREFStyp}$ = 13 pF, $R_{AREFtyp}$ = 0.7 kΩ.

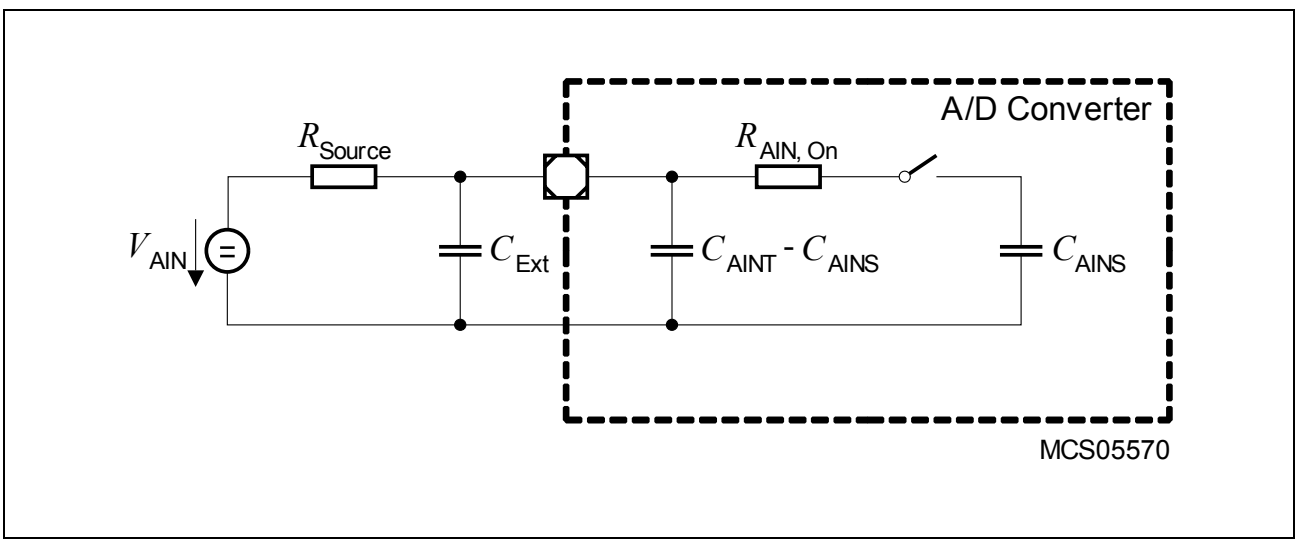

Figure 14 Equivalent Circuitry for Analog Inputs

CPU and EBC are clocked with the CPU clock signal f_{CPU}. The CPU clock can have the same frequency as the master clock ($f_{CPU} = f_{MC}$) or can be the master clock divided by two: $f_{CPU} = f_{MC} / 2$. This factor is selected by bit CPSYS in register SYSCON1.

The specification of the external timing (AC Characteristics) depends on the period of the CPU clock, called “TCP”.

The other peripherals are supplied with the system clock signal f_{SYS} which has the same frequency as the CPU clock signal f_{CPU}.

Bypass Operation

When bypass operation is configured (PLLCTRL = $0x_B$) the master clock is derived from the internal oscillator (input clock signal XTAL1) through the input- and output-prescalers:

$f_{MC} = f_{OSC} / ((PLLIDIV + 1) \times (PLLODIV + 1))$.

If both divider factors are selected as ‘1’ (PLLIDIV = PLLODIV = ‘0’) the frequency of f_{MC} directly follows the frequency of f_{OSC} so the high and low time of f_{MC} is defined by the duty cycle of the input clock f_{OSC}.

The lowest master clock frequency is achieved by selecting the maximum values for both divider factors:

$f_{MC} = f_{OSC} / ((3 + 1) \times (14 + 1)) = f_{OSC} / 60$.

Phase Locked Loop (PLL)

When PLL operation is configured (PLLCTRL = 11_B) the on-chip phase locked loop is enabled and provides the master clock. The PLL multiplies the input frequency by the factor **F** ($f_{MC} = f_{OSC} \times$ **F**) which results from the input divider, the multiplication factor, and the output divider (**F** = PLLMUL+1 / (PLLIDIV+1 $\times$ PLLODIV+1)). The PLL circuit synchronizes the master clock to the input clock. This synchronization is done smoothly, i.e. the master clock frequency does not change abruptly.

Due to this adaptation to the input clock the frequency of f_{MC} is constantly adjusted so it is locked to f_{OSC}. The slight variation causes a jitter of f_{MC} which also affects the duration of individual TCMs.

The timing listed in the AC Characteristics refers to TCPs. Because f_{CPU} is derived from f_{MC}, the timing must be calculated using the minimum TCP possible under the respective circumstances.
The actual minimum value for TCP depends on the jitter of the PLL. As the PLL is constantly adjusting its output frequency so it corresponds to the applied input frequency (crystal or oscillator) the relative deviation for periods of more than one TCP is lower than for one single TCP (see formula and **Figure 16**).

This is especially important for bus cycles using waitstates and e.g. for the operation of timers, serial interfaces, etc. For all slower operations and longer periods (e.g. pulse train

4.4.3 External Clock Drive XTAL1

Table 19 External Clock Drive Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit
			Min.	Max.	
Oscillator period	t_{OSC}	SR	25	250[1)]	ns
High time[2)]	t_1	SR	6	–	ns
Low time[2)]	t_2	SR	6	–	ns
Rise time[2)]	t_3	SR	–	8	ns
Fall time[2)]	t_4	SR	–	8	ns

1) The maximum limit is only relevant for PLL operation to ensure the minimum input frequency for the PLL.

2) The clock input signal must reach the defined levels V_{ILC} and V_{IHC}.

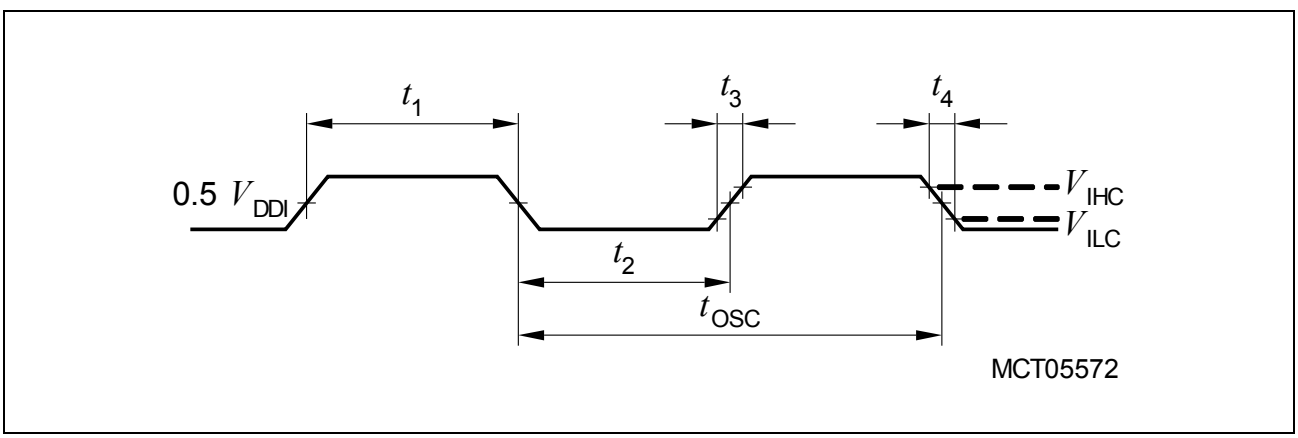

Figure 17 External Clock Drive XTAL1

Note: If the on-chip oscillator is used together with a crystal or a ceramic resonator, the oscillator frequency is limited to a range of 4 MHz to 16 MHz.
It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimum parameters for the oscillator operation. Please refer to the limits specified by the crystal supplier.
When driven by an external clock signal it will accept the specified frequency range. Operation at lower input frequencies is possible but is verified by design only (not subject to production test).

4.4.5 External Bus Timing

Table 20 CLKOUT Reference Signal

Parameter	Symbol		Limits		Unit
			Min.	Max.	
CLKOUT cycle time	tc_5	CC	40/30/25[1]		ns
CLKOUT high time	tc_6	CC	8	–	ns
CLKOUT low time	tc_7	CC	6	–	ns
CLKOUT rise time	tc_8	CC	–	4	ns
CLKOUT fall time	tc_9	CC	–	4	ns

1) The CLKOUT cycle time is influenced by the PLL jitter (given values apply to f_{CPU} = 25/33/40 MHz). For longer periods the relative deviation decreases (see PLL deviation formula).

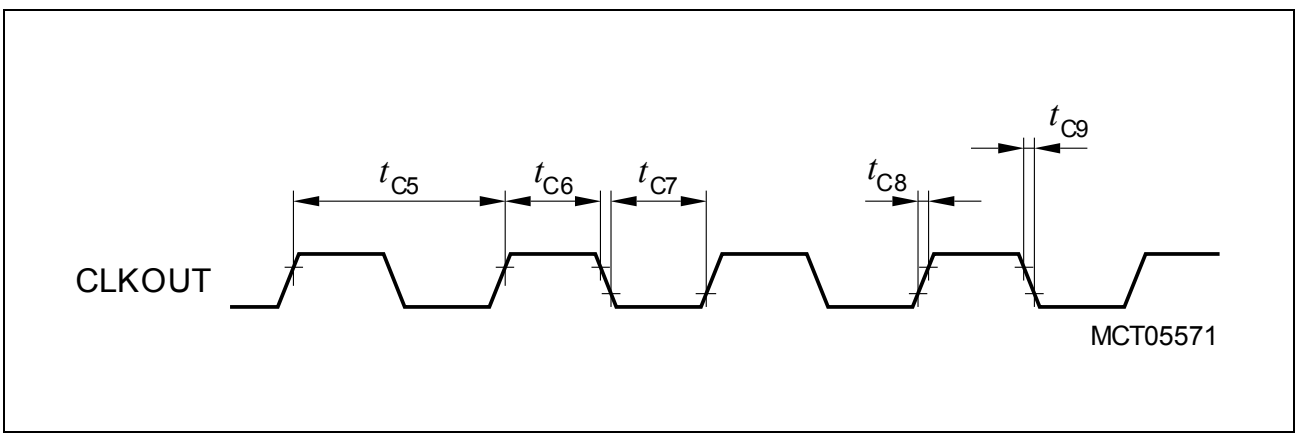

Figure 20 CLKOUT Signal Timing

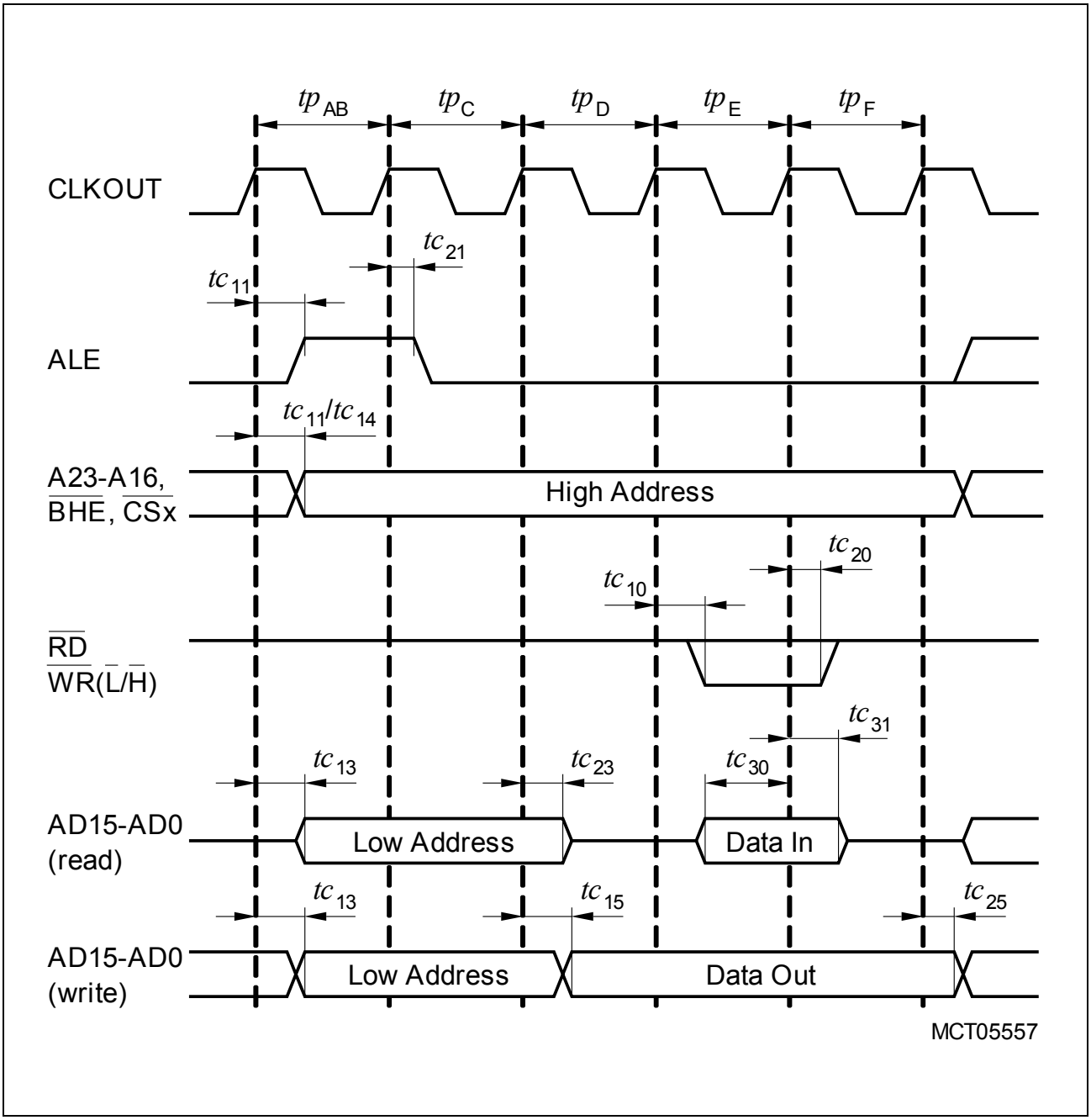

Figure 21 Multiplexed Bus Cycle

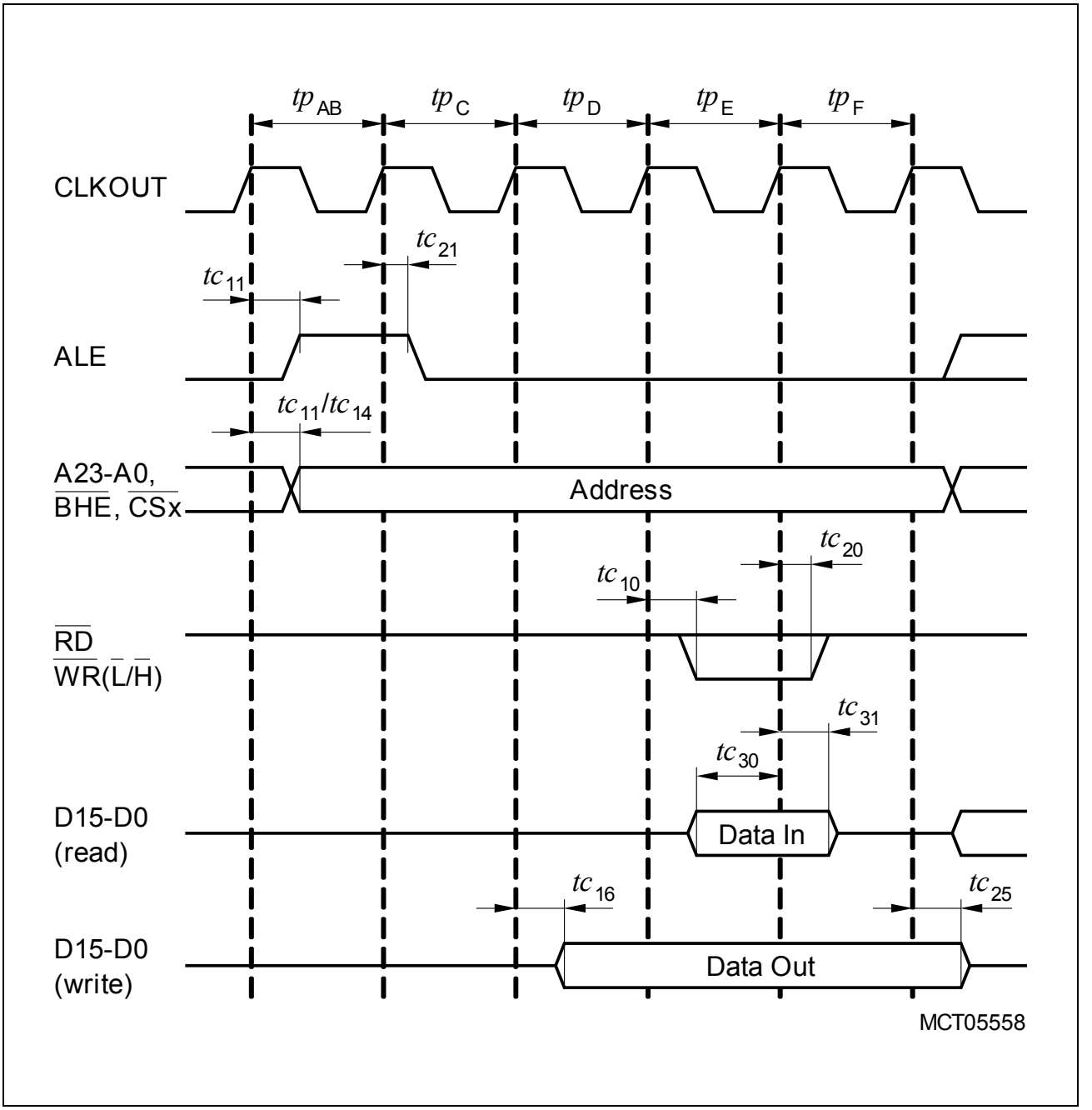

Figure 22 Demultiplexed Bus Cycle

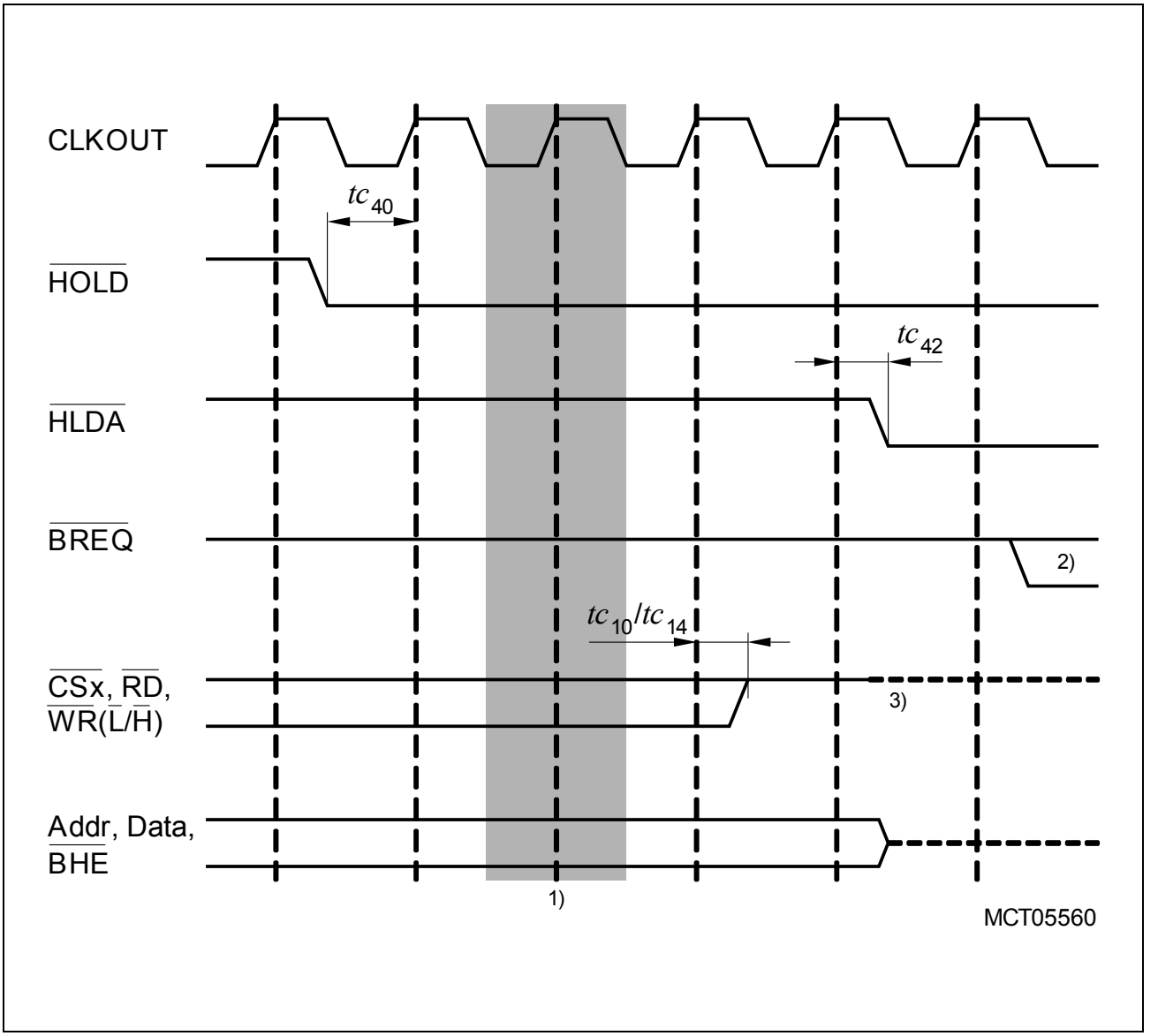

Figure 24 External Bus Arbitration, Releasing the Bus

Notes

1. *The XC167 will complete the currently running bus cycle before granting bus access.*
2. *This is the first possibility for BREQ to get active.*
3. *The control outputs will be resistive high (pull-up) after being driven inactive (ALE will be low).*