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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Last Time Buy
Core Processor	C166SV2
Core Size	16-Bit
Speed	40MHz
Connectivity	CANbus, EBI/EMI, I²C, SPI, UART/USART
Peripherals	PWM, WDT
Number of I/O	103
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	12K x 8
Voltage - Supply (Vcc/Vdd)	2.35V ~ 2.7V
Data Converters	A/D 16x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	PG-TQFP-144-7
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc167ci32f40fbbakxuma1

2.2 Pin Configuration and Definition

The pins of the XC167 are described in detail in **Table 2**, including all their alternate functions. **Figure 2** summarizes all pins in a condensed way, showing their location on the 4 sides of the package. E*) and C*) mark pins to be used as alternate external interrupt inputs, C*) marks pins that can have CAN interface lines assigned to them.

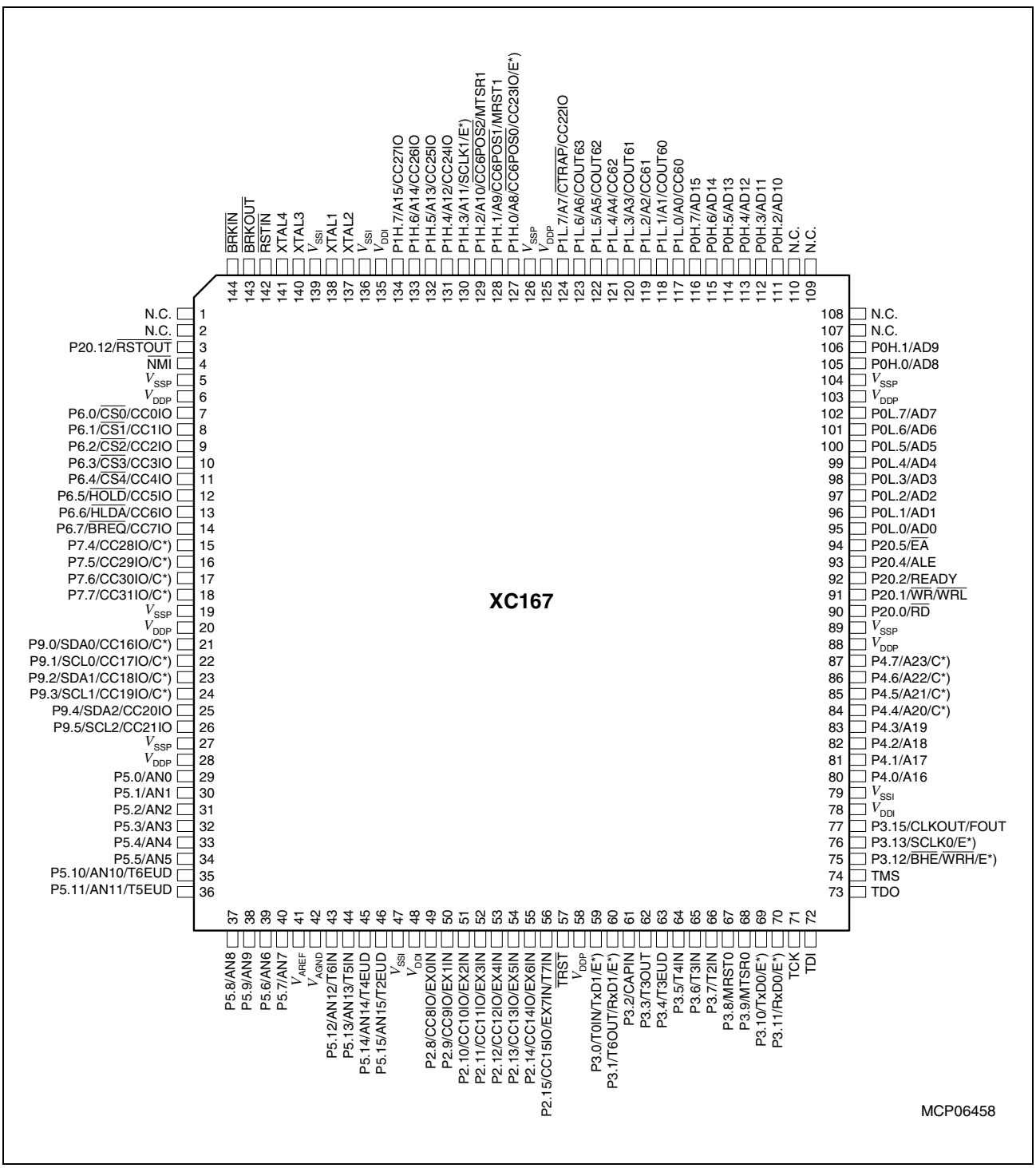

Figure 2 Pin Configuration (top view)

Table 2 Pin Definitions and Functions (cont'd)

Sym-bol	Pin Num.	Input Outp.	Function
P7		IO	Port 7 is a 4-bit bidirectional I/O port. Each pin can be programmed for input (output driver in high-impedance state) or output (configurable as push/pull or open drain driver). The input threshold of Port 7 is selectable (standard or special). Port 7 pins provide inputs/outputs for CAPCOM2 and serial interface lines.[1)]
P7.4	15	I/O I I	CC28IO CAPCOM2: CC28 Capture Inp./Compare Outp., CAN2_RxD CAN Node 2 Receive Data Input, EX7IN Fast External Interrupt 7 Input (alternate pin B)
P7.5	16	I/O O I	CC29IO CAPCOM2: CC29 Capture Inp./Compare Outp., CAN2_TxD CAN Node 2 Transmit Data Output, EX6IN Fast External Interrupt 6 Input (alternate pin B)
P7.6	17	I/O I I	CC30IO CAPCOM2: CC30 Capture Inp./Compare Outp., CAN1_RxD CAN Node 1 Receive Data Input, EX7IN Fast External Interrupt 7 Input (alternate pin A)
P7.7	18	I/O O I	CC31IO CAPCOM2: CC31 Capture Inp./Compare Outp., CAN1_TxD CAN Node 1 Transmit Data Output, EX6IN Fast External Interrupt 6 Input (alternate pin A)

Table 2 Pin Definitions and Functions (cont'd)

Sym-bol	Pin Num.	Input Outp.	Function		
P5		I	Port 5 is a 16-bit input-only port. The pins of Port 5 also serve as analog input channels for the A/D converter, or they serve as timer inputs:		
P5.0	29	I	AN0		
P5.1	30	I	AN1		
P5.2	31	I	AN2		
P5.3	32	I	AN3		
P5.4	33	I	AN4		
P5.5	34	I	AN5		
P5.10	35	I	AN10,	T6EUD	GPT1 Timer T4 Ext. Up/Down Ctrl. Inp.
P5.11	36	I	AN11,	T5EUD	GPT1 Timer T2 Ext. Up/Down Ctrl. Inp.
P5.8	37	I	AN8		
P5.9	38	I	AN9		
P5.6	39	I	AN6		
P5.7	40	I	AN7		
P5.12	43	I	AN12,	T6IN	GPT2 Timer T6 Count/Gate Input
P5.13	44	I	AN13,	T5IN	GPT2 Timer T5 Count/Gate Input
P5.14	45	I	AN14,	T4EUD	GPT1 Timer T4 Ext. Up/Down Ctrl. Inp.
P5.15	46	I	AN15,	T2EUD	GPT1 Timer T2 Ext. Up/Down Ctrl. Inp.

Table 2 Pin Definitions and Functions (cont'd)

Sym-bol	Pin Num.	Input Outp.	Function	
PORT1		IO	PORT1 consists of the two 8-bit bidirectional I/O ports P1L and P1H. Each pin can be programmed for input (output driver in high-impedance state) or output. PORT1 is used as the 16-bit address bus (A) in demultiplexed bus modes (also after switching from a demultiplexed to a multiplexed bus mode). The following PORT1 pins also serve for alt. functions:	
P1L.0	117	I/O	CC60	CAPCOM6: Input / Output of Channel 0
P1L.1	118	O	COUT60	CAPCOM6: Output of Channel 0
P1L.2	119	I/O	CC61	CAPCOM6: Input / Output of Channel 1
P1L.3	120	O	COUT61	CAPCOM6: Output of Channel 1
P1L.4	121	I/O	CC62	CAPCOM6: Input / Output of Channel 2
P1L.5	122	O	COUT62	CAPCOM6: Output of Channel 2
P1L.6	123	O	$\overline{\text{COUT63}}$	Output of 10-bit Compare Channel
P1L.7	124	I	$\overline{\text{CTRAP}}$	$\overline{\text{CAPCOM2}}$: CC22 Capture Inp./Compare Outp. $\overline{\text{CTRAP}}$ is an input pin with an internal pullup resistor. A low level on this pin switches the CAPCOM6 compare outputs to the logic level defined by software (if enabled).
		I/O	$\overline{\text{CC22IO}}$	CAPCOM2: CC22 Capture Inp./Compare Outp.
P1H.0	127	I	$\overline{\text{CC6POS0}}$	CAPCOM6: Position 0 Input,
		I	EX0IN	Fast External Interrupt 0 Input (alternate pin B),
		I/O	$\overline{\text{CC23IO}}$	CAPCOM2: CC23 Capture Inp./Compare Outp.
P1H.1	128	I	$\overline{\text{CC6POS1}}$	CAPCOM6: Position 1 Input,
		I/O	$\overline{\text{MRST1}}$	SSC1 Master-Receive/Slave-Transmit In/Out.
P1H.2	129	I	$\overline{\text{CC6POS2}}$	CAPCOM6: Position 2 Input,
		I/O	MTSR1	SSC1 Master-Transmit/Slave-Receive Out/Inp.
P1H.3	130	I/O	SCLK1	SSC1 Master Clock Output / Slave Clock Input,
		I	EX0IN	Fast External Interrupt 0 Input (alternate pin A)
P1H.4	131	I/O	CC24IO	CAPCOM2: CC24 Capture Inp./Compare Outp.
P1H.5	132	I/O	CC25IO	CAPCOM2: CC25 Capture Inp./Compare Outp.
P1H.6	133	I/O	CC26IO	CAPCOM2: CC26 Capture Inp./Compare Outp.
P1H.7	134	I/O	CC27IO	CAPCOM2: CC27 Capture Inp./Compare Outp.

3.1 Memory Subsystem and Organization

The memory space of the XC167 is configured in a Von Neumann architecture, which means that all internal and external resources, such as code memory, data memory, registers and I/O ports, are organized within the same linear address space. This common memory space includes 16 Mbytes and is arranged as 256 segments of 64 Kbytes each, where each segment consists of four data pages of 16 Kbytes each. The entire memory space can be accessed bytewise or wordwise. Portions of the on-chip DPRAM and the register spaces (E/SFR) have additionally been made directly bitaddressable.

The internal data memory areas and the Special Function Register areas (SFR and ESFR) are mapped into segment 0, the system segment.

The Program Management Unit (PMU) handles all code fetches and, therefore, controls accesses to the program memories, such as Flash memory and PSRAM.

The Data Management Unit (DMU) handles all data transfers and, therefore, controls accesses to the DSRAM and the on-chip peripherals.

Both units (PMU and DMU) are connected via the high-speed system bus to exchange data. This is required if operands are read from program memory, code or data is written to the PSRAM, code is fetched from external memory, or data is read from or written to external resources, including peripherals on the LXBus (such as TwinCAN). The system bus allows concurrent two-way communication for maximum transfer performance.

256 Kbytes of on-chip Flash memory store code or constant data. The on-chip Flash memory is organized as four 8-Kbyte sectors, one 32-Kbyte sector, and three 64-Kbyte sectors. Each sector can be separately write protected[1)], erased and programmed (in blocks of 128 bytes). The complete Flash area can be read-protected. A password sequence temporarily unlocks protected areas. The Flash module combines very fast 64-bit one-cycle read accesses with protected and efficient writing algorithms for programming and erasing. Thus, program execution out of the internal Flash results in maximum performance. Dynamic error correction provides extremely high read data security for all read accesses.
For timing characteristics, please refer to **Section 4.4.2**.

6 Kbytes of on-chip Program SRAM (PSRAM) are provided to store user code or data. The PSRAM is accessed via the PMU and is therefore optimized for code fetches.

4 Kbytes of on-chip Data SRAM (DSRAM) are provided as a storage for general user data. The DSRAM is accessed via the DMU and is therefore optimized for data accesses.

2 Kbytes of on-chip Dual-Port RAM (DPRAM) are provided as a storage for user defined variables, for the system stack, and general purpose register banks. A register bank can consist of up to 16 wordwide (R0 to R15) and/or bytewide (RL0, RH0, …, RL7,

1) Each two 8-Kbyte sectors are combined for write-protection purposes.

Table 4 XC167 Interrupt Nodes (cont'd)

Source of Interrupt or PEC Service Request	Control Register	Vector Location[1)]	Trap Number
CAPCOM Register 29	CC2_CC29IC	xx'0110$_H$	44$_H$ / 68$_D$
CAPCOM Register 30	CC2_CC30IC	xx'0114$_H$	45$_H$ / 69$_D$
CAPCOM Register 31	CC2_CC31IC	xx'0118$_H$	46$_H$ / 70$_D$
CAPCOM Timer 0	CC1_T0IC	xx'0080$_H$	20$_H$ / 32$_D$
CAPCOM Timer 1	CC1_T1IC	xx'0084$_H$	21$_H$ / 33$_D$
CAPCOM Timer 7	CC2_T7IC	xx'00F4$_H$	3D$_H$ / 61$_D$
CAPCOM Timer 8	CC2_T8IC	xx'00F8$_H$	3E$_H$ / 62$_D$
GPT1 Timer 2	GPT12E_T2IC	xx'0088$_H$	22$_H$ / 34$_D$
GPT1 Timer 3	GPT12E_T3IC	xx'008C$_H$	23$_H$ / 35$_D$
GPT1 Timer 4	GPT12E_T4IC	xx'0090$_H$	24$_H$ / 36$_D$
GPT2 Timer 5	GPT12E_T5IC	xx'0094$_H$	25$_H$ / 37$_D$
GPT2 Timer 6	GPT12E_T6IC	xx'0098$_H$	26$_H$ / 38$_D$
GPT2 CAPREL Register	GPT12E_CRIC	xx'009C$_H$	27$_H$ / 39$_D$
A/D Conversion Complete	ADC_CIC	xx'00A0$_H$	28$_H$ / 40$_D$
A/D Overrun Error	ADC_EIC	xx'00A4$_H$	29$_H$ / 41$_D$
ASC0 Transmit	ASC0_TIC	xx'00A8$_H$	2A$_H$ / 42$_D$
ASC0 Transmit Buffer	ASC0_TBIC	xx'011C$_H$	47$_H$ / 71$_D$
ASC0 Receive	ASC0_RIC	xx'00AC$_H$	2B$_H$ / 43$_D$
ASC0 Error	ASC0_EIC	xx'00B0$_H$	2C$_H$ / 44$_D$
ASC0 Autobaud	ASC0_ABIC	xx'017C$_H$	5F$_H$ / 95$_D$
SSC0 Transmit	SSC0_TIC	xx'00B4$_H$	2D$_H$ / 45$_D$
SSC0 Receive	SSC0_RIC	xx'00B8$_H$	2E$_H$ / 46$_D$
SSC0 Error	SSC0_EIC	xx'00BC$_H$	2F$_H$ / 47$_D$
IIC Data Transfer Event	IIC_DTIC	xx'0100$_H$	40$_H$ / 64$_D$
IIC Protocol Event	IIC_PEIC	xx'0104$_H$	41$_H$ / 65$_D$
PLL/OWD	PLLIC	xx'010C$_H$	43$_H$ / 67$_D$
ASC1 Transmit	ASC1_TIC	xx'0120$_H$	48$_H$ / 72$_D$
ASC1 Transmit Buffer	ASC1_TBIC	xx'0178$_H$	5E$_H$ / 94$_D$
ASC1 Receive	ASC1_RIC	xx'0124$_H$	49$_H$ / 73$_D$
ASC1 Error	ASC1_EIC	xx'0128$_H$	4A$_H$ / 74$_D$

Table 4 XC167 Interrupt Nodes (cont'd)

Source of Interrupt or PEC Service Request	Control Register	Vector Location[1)]	Trap Number
ASC1 Autobaud	ASC1_ABIC	xx'0108$_H$	42$_H$ / 66$_D$
End of PEC Subchannel	EOPIC	xx'0130$_H$	4C$_H$ / 76$_D$
CAPCOM6 Timer T12	CCU6_T12IC	xx'0134$_H$	4D$_H$ / 77$_D$
CAPCOM6 Timer T13	CCU6_T13IC	xx'0138$_H$	4E$_H$ / 78$_D$
CAPCOM6 Emergency	CCU6_EIC	xx'013C$_H$	4F$_H$ / 79$_D$
CAPCOM6	CAPCOM6	xx'0140$_H$	50$_H$ / 80$_D$
SSC1 Transmit	SSC1_TIC	xx'0144$_H$	51$_H$ / 81$_D$
SSC1 Receive	SSC1_RIC	xx'0148$_H$	52$_H$ / 82$_D$
SSC1 Error	SSC1_EIC	xx'014C$_H$	53$_H$ / 83$_D$
CAN0	CAN_0IC	xx'0150$_H$	54$_H$ / 84$_D$
CAN1	CAN_1IC	xx'0154$_H$	55$_H$ / 85$_D$
CAN2	CAN_2IC	xx'0158$_H$	56$_H$ / 86$_D$
CAN3	CAN_3IC	xx'015C$_H$	57$_H$ / 87$_D$
CAN4	CAN_4IC	xx'0164$_H$	59$_H$ / 89$_D$
CAN5	CAN_5IC	xx'0168$_H$	5A$_H$ / 90$_D$
CAN6	CAN_6IC	xx'016C$_H$	5B$_H$ / 91$_D$
CAN7	CAN_7IC	xx'0170$_H$	5C$_H$ / 92$_D$
RTC	RTC_IC	xx'0174$_H$	5D$_H$ / 93$_D$
Unassigned node	–	xx'012C$_H$	3F$_H$ / 63$_D$
Unassigned node	–	xx'00FC$_H$	3F$_H$ / 63$_D$
Unassigned node	–	xx'0160$_H$	58$_H$ / 88$_D$

1) Register VECSEG defines the segment where the vector table is located to.
Bitfield VECSC in register CPUCON1 defines the distance between two adjacent vectors. This table represents the default setting, with a distance of 4 (two words) between two vectors.

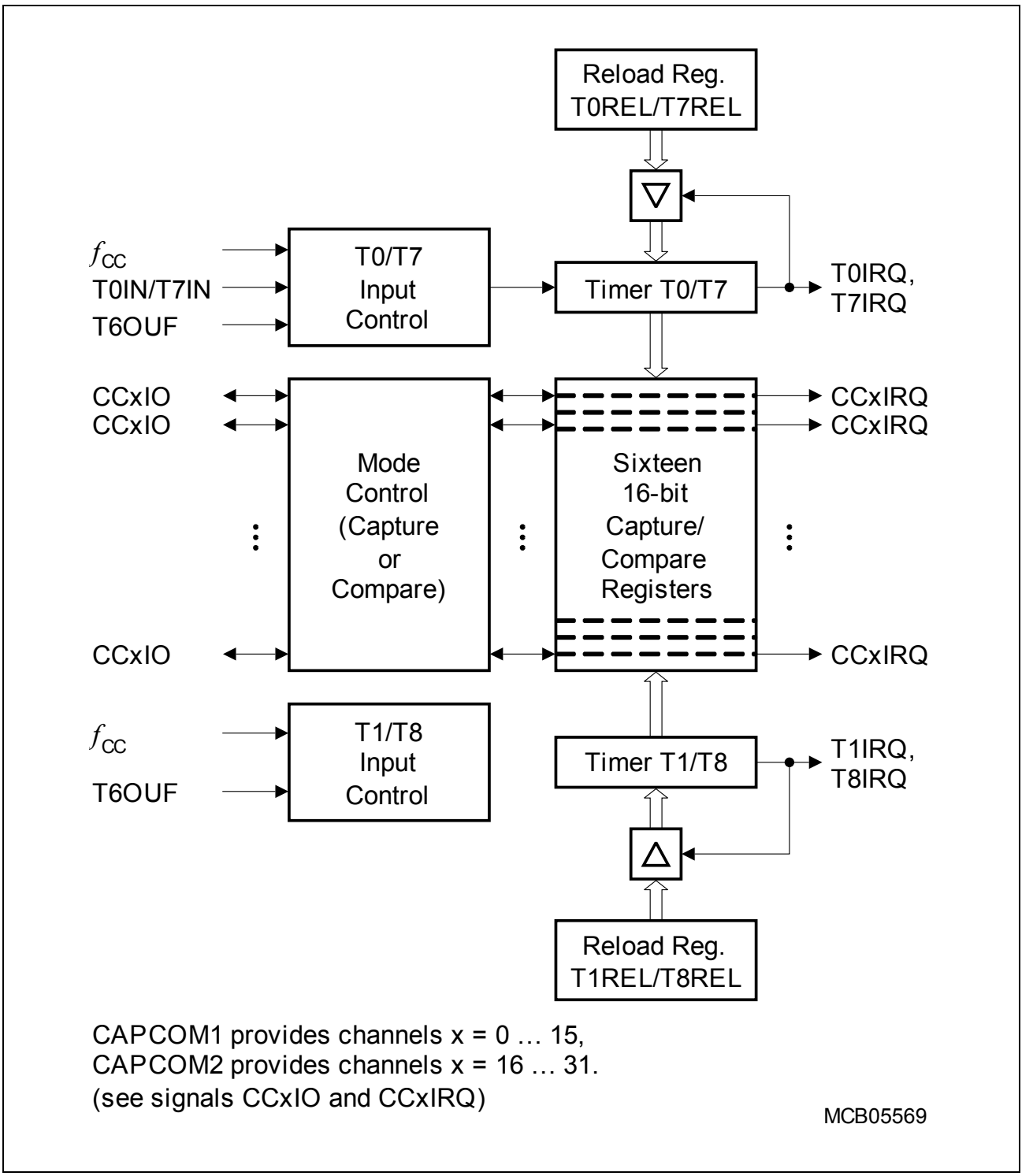

Figure 5 CAPCOM1/2 Unit Block Diagram

count direction (up/down) for each timer is programmable by software or may additionally be altered dynamically by an external signal on a port pin (TxEUD). Concatenation of the timers is supported via the output toggle latch (T6OTL) of timer T6, which changes its state on each timer overflow/underflow.

The state of this latch may be used to clock timer T5, and/or it may be output on pin T6OUT. The overflows/underflows of timer T6 can additionally be used to clock the CAPCOM1/2 timers, and to cause a reload from the CAPREL register.

The CAPREL register may capture the contents of timer T5 based on an external signal transition on the corresponding port pin (CAPIN), and timer T5 may optionally be cleared after the capture procedure. This allows the XC167 to measure absolute time differences or to perform pulse multiplication without software overhead.

The capture trigger (timer T5 to CAPREL) may also be generated upon transitions of GPT1 timer T3's inputs T3IN and/or T3EUD. This is especially advantageous when T3 operates in Incremental Interface Mode.

3.10 A/D Converter

For analog signal measurement, a 10-bit A/D converter with 16 multiplexed input channels and a sample and hold circuit has been integrated on-chip. It uses the method of successive approximation. The sample time (for loading the capacitors) and the conversion time is programmable (in two modes) and can thus be adjusted to the external circuitry. The A/D converter can also operate in 8-bit conversion mode, where the conversion time is further reduced.

Overrun error detection/protection is provided for the conversion result register (ADDAT): either an interrupt request will be generated when the result of a previous conversion has not been read from the result register at the time the next conversion is complete, or the next conversion is suspended in such a case until the previous result has been read.

For applications which require less analog input channels, the remaining channel inputs can be used as digital input port pins.

The A/D converter of the XC167 supports four different conversion modes. In the standard Single Channel conversion mode, the analog level on a specified channel is sampled once and converted to a digital result. In the Single Channel Continuous mode, the analog level on a specified channel is repeatedly sampled and converted without software intervention. In the Auto Scan mode, the analog levels on a prespecified number of channels are sequentially sampled and converted. In the Auto Scan Continuous mode, the prespecified channels are repeatedly sampled and converted. In addition, the conversion of a specific channel can be inserted (injected) into a running sequence without disturbing this sequence. This is called Channel Injection Mode.

The Peripheral Event Controller (PEC) may be used to automatically store the conversion results into a table in memory for later evaluation, without requiring the overhead of entering and exiting interrupt routines for each data transfer.

After each reset and also during normal operation the ADC automatically performs calibration cycles. This automatic self-calibration constantly adjusts the converter to changing operating conditions (e.g. temperature) and compensates process variations.

These calibration cycles are part of the conversion cycle, so they do not affect the normal operation of the A/D converter.

In order to decouple analog inputs from digital noise and to avoid input trigger noise those pins used for analog input can be disconnected from the digital IO or input stages under software control. This can be selected for each pin separately via register P5DIDIS (Port 5 Digital Input Disable).

The Auto-Power-Down feature of the A/D converter minimizes the power consumption when no conversion is in progress.

3.18 Power Management

The XC167 provides several means to control the power it consumes either at a given time or averaged over a certain timespan. Three mechanisms can be used (partly in parallel):

- **Power Saving Modes** switch the XC167 into a special operating mode (control via instructions).
  Idle Mode stops the CPU while the peripherals can continue to operate.
  Sleep Mode and Power Down Mode stop all clock signals and all operation (RTC may optionally continue running). Sleep Mode can be terminated by external interrupt signals.
- **Clock Generation Management** controls the distribution and the frequency of internal and external clock signals. While the clock signals for currently inactive parts of logic are disabled automatically, the user can reduce the XC167's CPU clock frequency which drastically reduces the consumed power.
  External circuitry can be controlled via the programmable frequency output FOUT.
- **Peripheral Management** permits temporary disabling of peripheral modules (control via register SYSCON3). Each peripheral can separately be disabled/enabled.

The on-chip RTC supports intermittent operation of the XC167 by generating cyclic wake-up signals. This offers full performance to quickly react on action requests while the intermittent sleep phases greatly reduce the average power consumption of the system.

3.19 Instruction Set Summary

Table 8 lists the instructions of the XC167 in a condensed way.
The various addressing modes that can be used with a specific instruction, the operation of the instructions, parameters for conditional execution of instructions, and the opcodes for each instruction can be found in the **"Instruction Set Manual"**.

This document also provides a detailed description of each instruction.

Table 8 Instruction Set Summary

Mnemonic	Description	Bytes
ADD(B)	Add word (byte) operands	2 / 4
ADDC(B)	Add word (byte) operands with Carry	2 / 4
SUB(B)	Subtract word (byte) operands	2 / 4
SUBC(B)	Subtract word (byte) operands with Carry	2 / 4
MUL(U)	(Un)Signed multiply direct GPR by direct GPR (16- × 16-bit)	2
DIV(U)	(Un)Signed divide register MDL by direct GPR (16-/16-bit)	2
DIVL(U)	(Un)Signed long divide reg. MD by direct GPR (32-/16-bit)	2
CPL(B)	Complement direct word (byte) GPR	2
NEG(B)	Negate direct word (byte) GPR	2
AND(B)	Bitwise AND, (word/byte operands)	2 / 4
OR(B)	Bitwise OR, (word/byte operands)	2 / 4
XOR(B)	Bitwise exclusive OR, (word/byte operands)	2 / 4
BCLR/BSET	Clear/Set direct bit	2
BMOV(N)	Move (negated) direct bit to direct bit	4
BAND/BOR/BXOR	AND/OR/XOR direct bit with direct bit	4
BCMP	Compare direct bit to direct bit	4
BFLDH/BFLDL	Bitwise modify masked high/low byte of bit-addressable direct word memory with immediate data	4
CMP(B)	Compare word (byte) operands	2 / 4
CMPD1/2	Compare word data to GPR and decrement GPR by 1/2	2 / 4
CMPI1/2	Compare word data to GPR and increment GPR by 1/2	2 / 4
PRIOR	Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR	2
SHL/SHR	Shift left/right direct word GPR	2

4 Electrical Parameters

4.1 General Parameters

Table 9 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Storage temperature	T_{ST}	-65	150	°C	1)
Junction temperature	T_J	-40	150	°C	under bias
Voltage on V_{DDI} pins with respect to ground (V_{SS})	V_{DDI}	-0.5	3.25	V	–
Voltage on V_{DDP} pins with respect to ground (V_{SS})	V_{DDP}	-0.5	6.2	V	–
Voltage on any pin with respect to ground (V_{SS})	V_{IN}	-0.5	V_{DDP} + 0.5	V	2)
Input current on any pin during overload condition	–	-10	10	mA	–
Absolute sum of all input currents during overload condition	–	–	|100|	mA	–

1) Moisture Sensitivity Level (MSL) 3, conforming to Jedec J-STD-020C for 260 °C for PG-TQFP-144-7, and 240 °C for P-TQFP-144-19.

2) Input pins XTAL1/XTAL3 belong to the core voltage domain. Therefore, input voltages must be within the range defined for V_{DDI}.

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
During absolute maximum rating overload conditions ($V_{IN} > V_{DDP}$ or $V_{IN} < V_{SS}$) the voltage on V_{DDP} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

Table 11 DC Characteristics (Operating Conditions apply)[1] (cont'd)

Parameter	Symbol		Limit Values		Unit	Test Condition
			Min.	Max.		
Configuration pull-down current[13]	I_{CPDL}[11]		–	10	µA	$V_{IN} = V_{ILmax}$
	I_{CPDH}[12]		120	–	µA	$V_{IN} = V_{IHmin}$
Level inactive hold current[14]	I_{LHI}[11]		–	-10	µA	$V_{OUT} = 0.5 \times V_{DDP}$
Level active hold current[14]	I_{LHA}[12]		-100	–	µA	V_{OUT} = 0.45 V
XTAL1, XTAL3 input current	I_{IL}	CC	–	±20	µA	0 V < V_{IN} < V_{DDI}
Pin capacitance[15] (digital inputs/outputs)	C_{IO}	CC	–	10	pF	–

1) Keeping signal levels within the limits specified in this table, ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current I_{OV}.

2) If XTAL1 is driven by a crystal, reaching an amplitude (peak to peak) of 0.4 × V_{DDI} is sufficient.

3) If XTAL3 is driven by a crystal, reaching an amplitude (peak to peak) of 0.25 × V_{DDI} is sufficient.

4) This parameter is tested for P2, P3, P4, P6, P7, P9.

5) The maximum deliverable output current of a port driver depends on the selected output driver mode, see **Table 12, Current Limits for Port Output Drivers**. The limit for pin groups must be respected.

6) As a rule, with decreasing output current the output levels approach the respective supply level ($V_{OL} \rightarrow V_{SS}$, $V_{OH} \rightarrow V_{DDP}$). However, only the levels for nominal output currents are guaranteed.

7) This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage results from the external circuitry.

8) An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin. Please refer to the definition of the overload coupling factor K_{OV}.

9) The driver of P3.15 is designed for faster switching, because this pin can deliver the reference clock for the bus interface (CLKOUT). The maximum leakage current for P3.15 is, therefore, increased to 1 µA.

10) This specification is valid during Reset for configuration on $\overline{RD}$, $\overline{WR}$, $\overline{EA}$, PORT0.
The pull-ups on $\overline{RD}$ and $\overline{WR}$ ($\overline{WRL}$/$\overline{WRH}$) are also active during bus hold.

11) The maximum current may be drawn while the respective signal line remains inactive.

12) The minimum current must be drawn to drive the respective signal line active.

13) This specification is valid during Reset for configuration on ALE.
The pull-down on ALE is also active during bus hold.

14) This specification is valid during Reset for pins P6.4-0, which can act as $\overline{CS}$ outputs.
The pull-ups on $\overline{CS}$ outputs are also active during bus hold.
The pull-up on pin $\overline{HLDA}$ is active when arbitration is enabled and the EBC operates in slave mode.

15) Not subject to production test - verified by design/characterization.

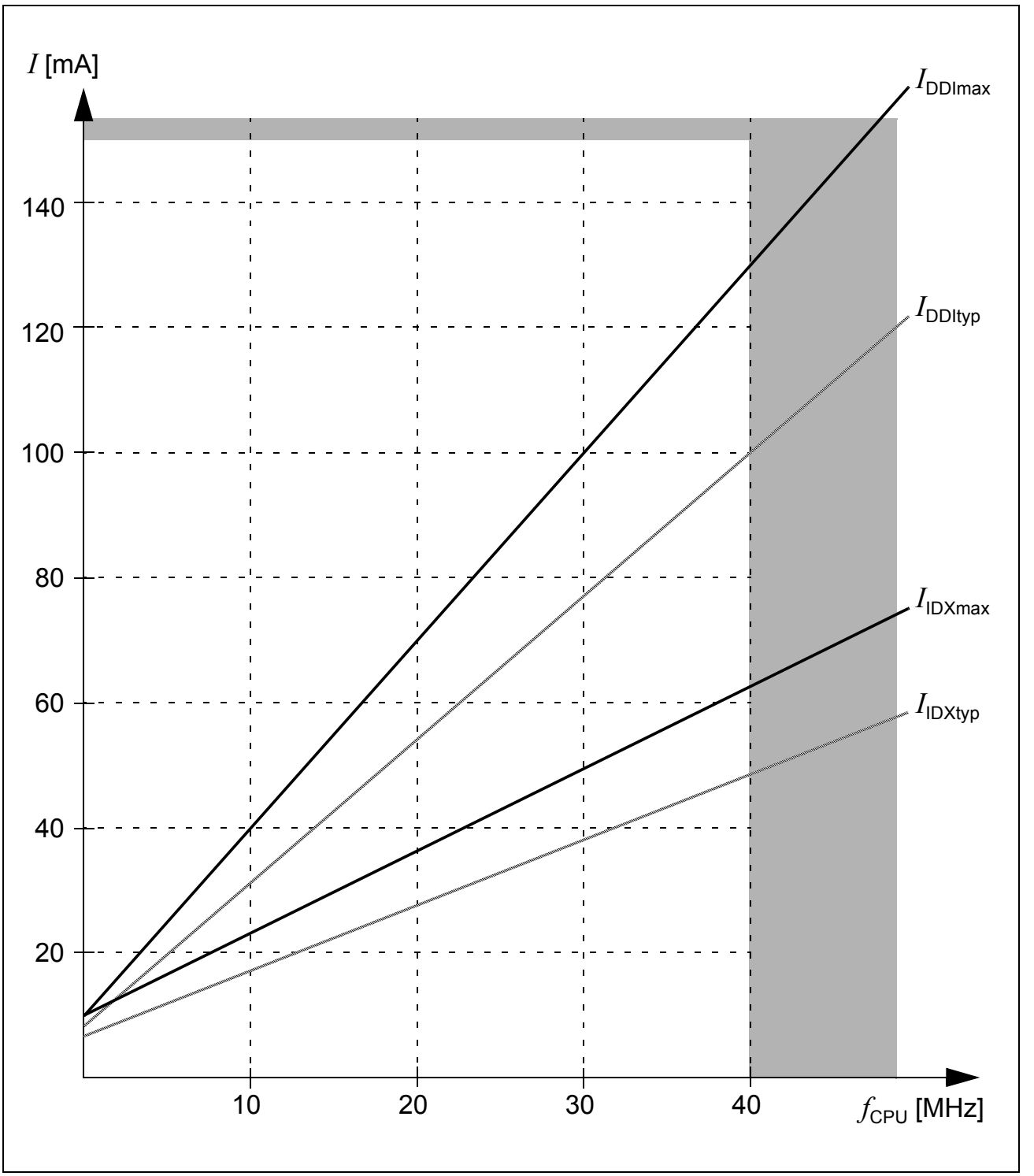

Figure 11 Supply/Idle Current as a Function of Operating Frequency

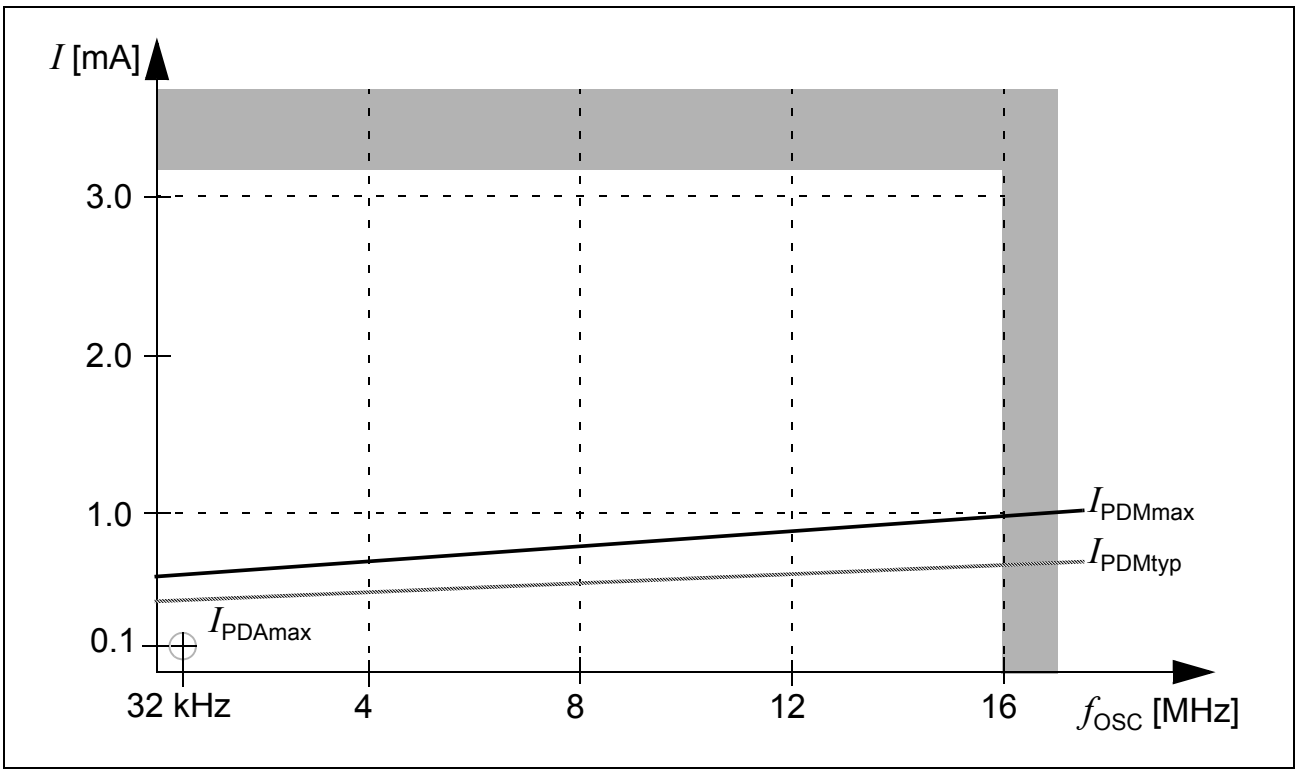

Figure 12 Sleep and Power Down Supply Current due to RTC and Oscillator Running, as a Function of Oscillator Frequency

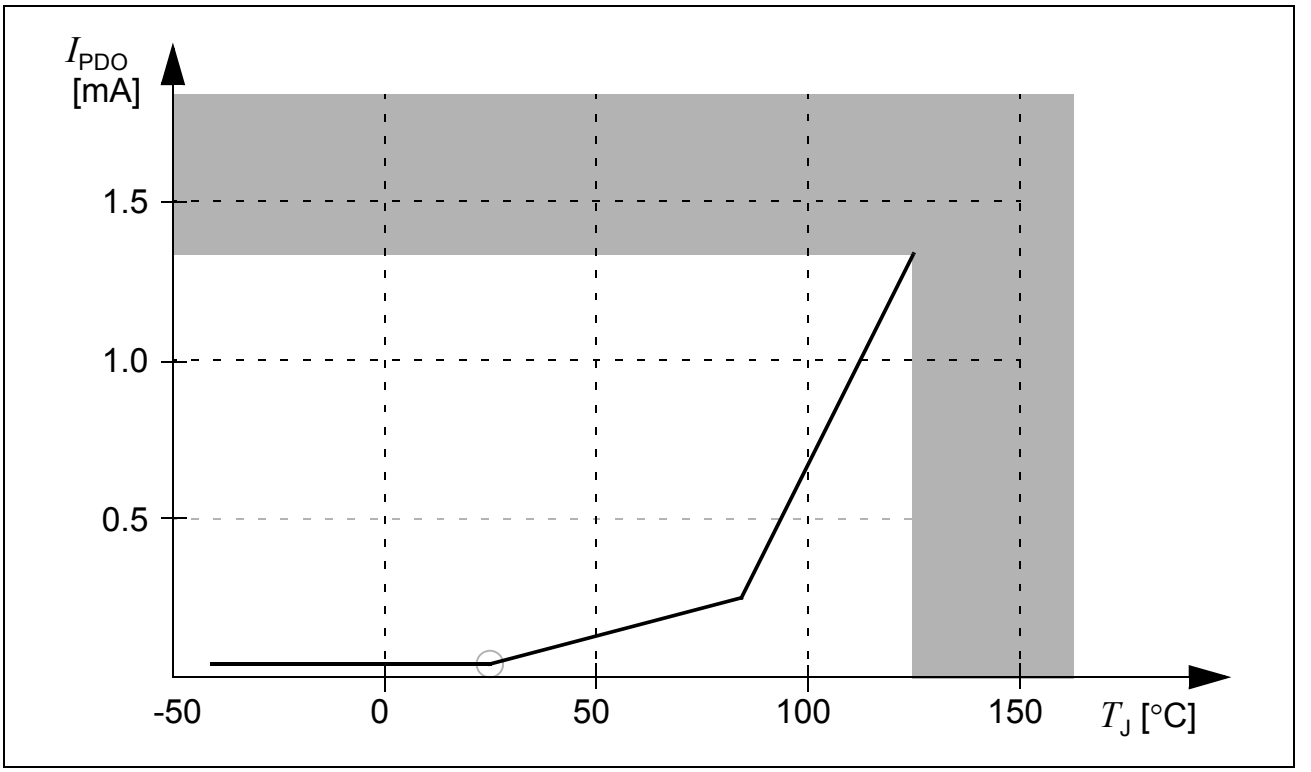

Figure 13 Sleep and Power Down Leakage Supply Current as a Function of Temperature

CPU and EBC are clocked with the CPU clock signal f_{CPU}. The CPU clock can have the same frequency as the master clock ($f_{CPU} = f_{MC}$) or can be the master clock divided by two: $f_{CPU} = f_{MC} / 2$. This factor is selected by bit CPSYS in register SYSCON1.

The specification of the external timing (AC Characteristics) depends on the period of the CPU clock, called “TCP”.

The other peripherals are supplied with the system clock signal f_{SYS} which has the same frequency as the CPU clock signal f_{CPU}.

Bypass Operation

When bypass operation is configured (PLLCTRL = $0x_B$) the master clock is derived from the internal oscillator (input clock signal XTAL1) through the input- and output-prescalers:

$f_{MC} = f_{OSC} / ((PLLIDIV + 1) \times (PLLODIV + 1))$.

If both divider factors are selected as ‘1’ (PLLIDIV = PLLODIV = ‘0’) the frequency of f_{MC} directly follows the frequency of f_{OSC} so the high and low time of f_{MC} is defined by the duty cycle of the input clock f_{OSC}.

The lowest master clock frequency is achieved by selecting the maximum values for both divider factors:

$f_{MC} = f_{OSC} / ((3 + 1) \times (14 + 1)) = f_{OSC} / 60$.

Phase Locked Loop (PLL)

When PLL operation is configured (PLLCTRL = 11_B) the on-chip phase locked loop is enabled and provides the master clock. The PLL multiplies the input frequency by the factor **F** ($f_{MC} = f_{OSC} \times$ **F**) which results from the input divider, the multiplication factor, and the output divider (**F** = PLLMUL+1 / (PLLIDIV+1 $\times$ PLLODIV+1)). The PLL circuit synchronizes the master clock to the input clock. This synchronization is done smoothly, i.e. the master clock frequency does not change abruptly.

Due to this adaptation to the input clock the frequency of f_{MC} is constantly adjusted so it is locked to f_{OSC}. The slight variation causes a jitter of f_{MC} which also affects the duration of individual TCMs.

The timing listed in the AC Characteristics refers to TCPs. Because f_{CPU} is derived from f_{MC}, the timing must be calculated using the minimum TCP possible under the respective circumstances.
The actual minimum value for TCP depends on the jitter of the PLL. As the PLL is constantly adjusting its output frequency so it corresponds to the applied input frequency (crystal or oscillator) the relative deviation for periods of more than one TCP is lower than for one single TCP (see formula and **Figure 16**).

This is especially important for bus cycles using waitstates and e.g. for the operation of timers, serial interfaces, etc. For all slower operations and longer periods (e.g. pulse train

Bus Cycle Control via READY Input

The duration of an external bus cycle can be controlled by the external circuitry via the READY input signal. The polarity of this input signal can be selected.

Synchronous READY permits the shortest possible bus cycle but requires the input signal to be synchronous to the reference signal CLKOUT.

Asynchronous READY puts no timing constraints on the input signal but incurs one waitstate minimum due to the additional synchronization stage. The minimum duration of an asynchronous READY signal to be safely synchronized must be one CLKOUT period plus the input setup time.

An active READY signal can be deactivated in response to the trailing (rising) edge of the corresponding command ($\overline{RD}$ or $\overline{WR}$).

If the next following bus cycle is READY-controlled, an active READY signal must be disabled before the first valid sample point for the next bus cycle. This sample point depends on the programmed phases of the next following cycle.

5 Package and Reliability

5.1 Packaging

Table 24 Package Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Green Package PG-TQFP-144-7					
Thermal resistance junction to case	$R_{\Theta JC}$	–	8	K/W	–
Thermal resistance junction to leads	$R_{\Theta JL}$	–	40	K/W	–
Standard Package P-TQFP-144-19					
Thermal resistance junction to case	$R_{\Theta JC}$	–	6	K/W	–
Thermal resistance junction to leads	$R_{\Theta JL}$	–	18	K/W	–

Package Outlines

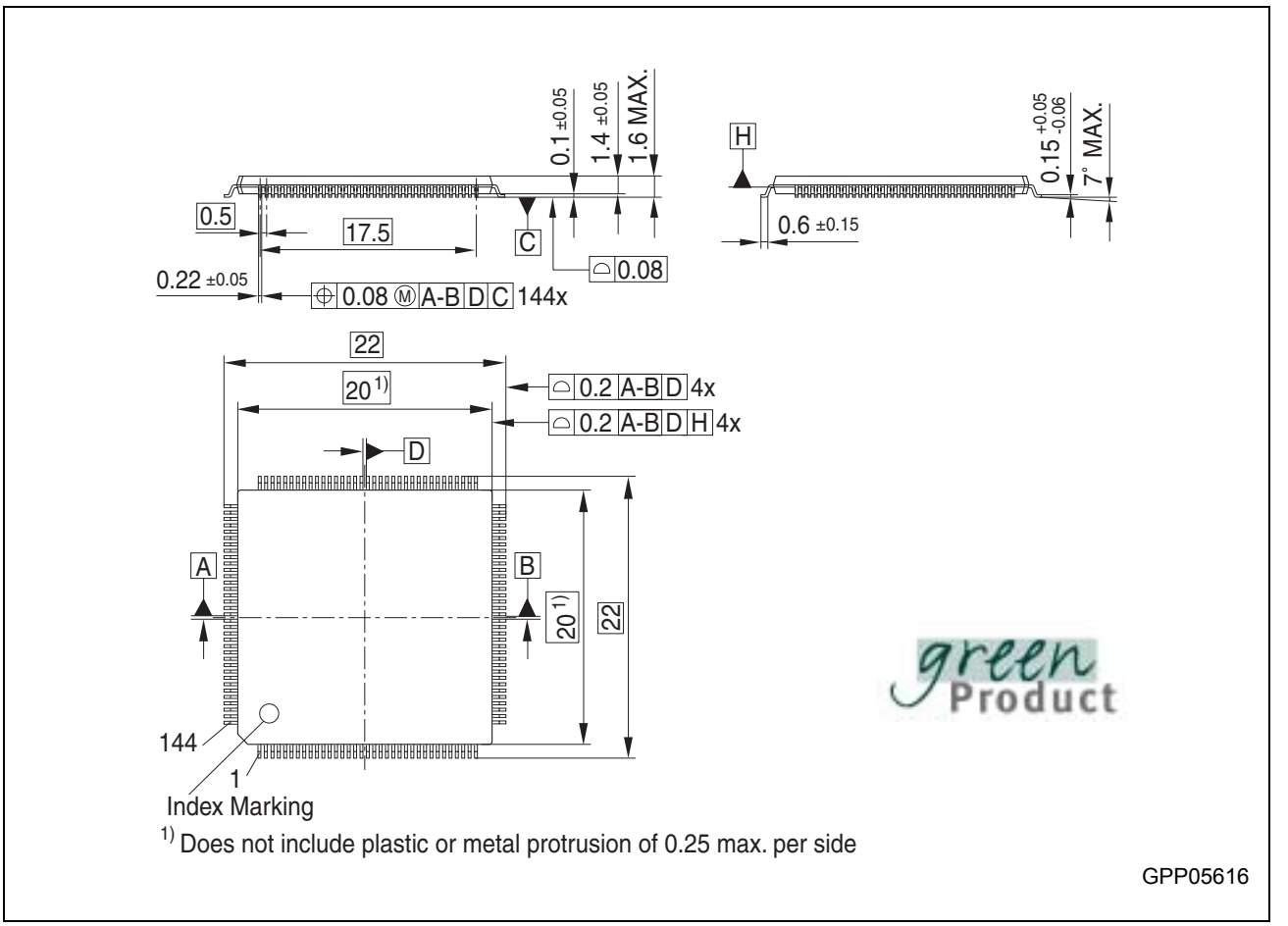

Figure 26 PG-TQFP-144-7 (Plastic Green Thin Quad Flat Package)

w w w . i n f i n e o n . c o m

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