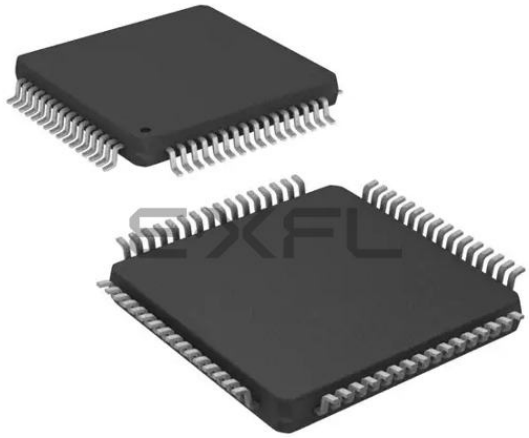


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

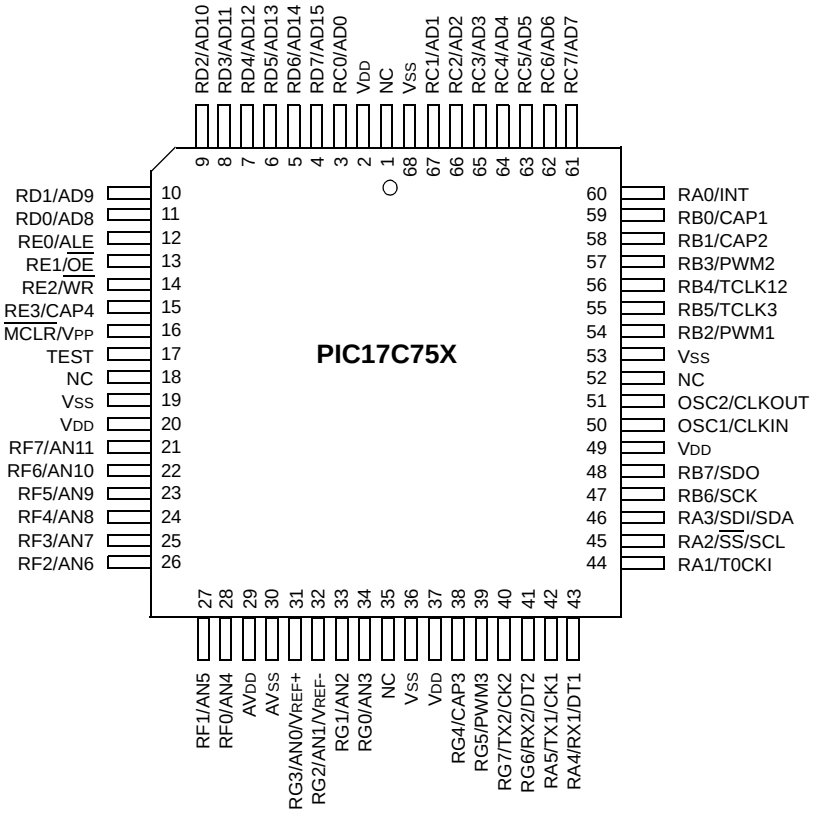
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	50
Program Memory Size	16KB (8K x 16)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	454 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic17c752-16i-pt

Pin Diagrams cont.'d

68-Pin PLCC



64-Pin TQFP

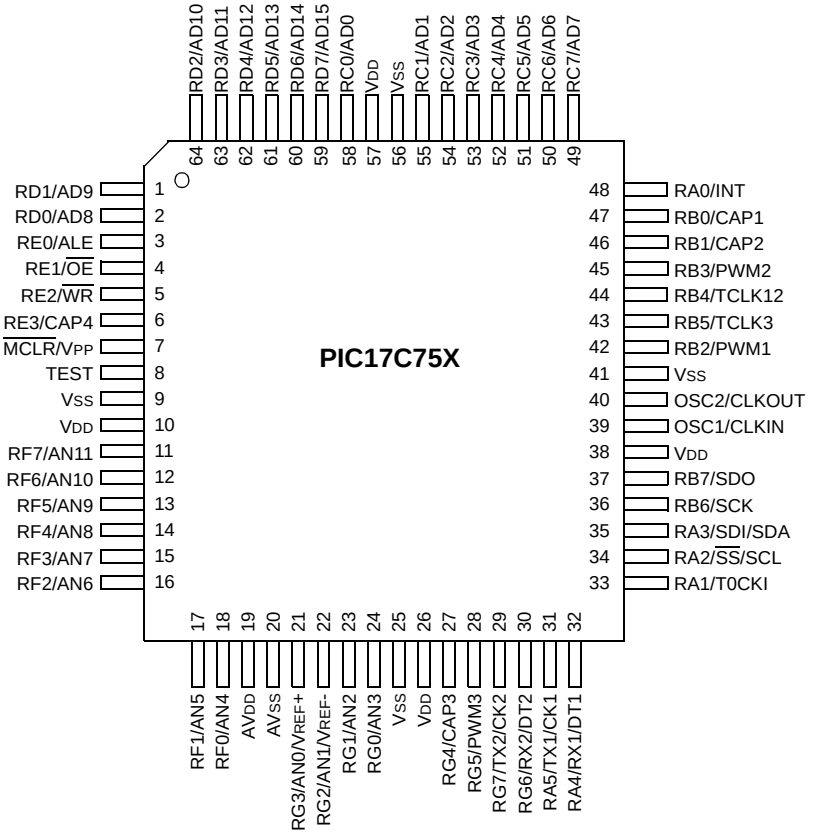


TABLE 3-1: PINOUT DESCRIPTIONS

Name	PIC17C75X			PIC17C76X		I/O/P Type	Buffer Type	Description
	DIP No.	PLCC No.	TQFP No.	PLCC No.	QFP No.			
OSC1/CLKIN	47	50	39	62	49	I	ST	Oscillator input in Crystal/Resonator or RC Oscillator mode. External clock input in External Clock mode.
OSC2/CLKOUT	48	51	40	63	50	O	—	Oscillator output. Connects to crystal or resonator in Crystal Oscillator mode. In RC Oscillator or External Clock modes, OSC2 pin outputs CLKOUT which has one fourth the frequency (FOSC/4) of OSC1 and denotes the instruction cycle rate.
$\overline{MCLR}$/VPP	15	16	7	20	9	I/P	ST	Master clear (RESET) input or Programming Voltage (VPP) input. This is the active low RESET input to the device.
								PORTA pins have individual differentiations that are listed in the following descriptions:
RA0/INT	56	60	48	72	58	I	ST	RA0 can also be selected as an external interrupt input. Interrupt can be configured to be on positive or negative edge. Input only pin.
RA1/T0CKI	41	44	33	56	43	I	ST	RA1 can also be selected as an external interrupt input and the interrupt can be configured to be on positive or negative edge. RA1 can also be selected to be the clock input to the Timer0 timer/counter. Input only pin.
RA2/$\overline{SS}$/SCL	42	45	34	57	44	I/O(2)	ST	RA2 can also be used as the slave select input for the SPI or the clock input for the I^2C bus. High voltage, high current, open drain port pin.
RA3/SDI/SDA	43	46	35	58	45	I/O(2)	ST	RA3 can also be used as the data input for the SPI or the data for the I^2C bus. High voltage, high current, open drain port pin.
RA4/RX1/DT1	40	43	32	51	38	I/O(1)	ST	RA4 can also be selected as the USART1 (SCI) Asynchronous Receive or USART1 (SCI) Synchronous Data. Output available from USART only.
RA5/TX1/CK1	39	42	31	50	37	I/O(1)	ST	RA5 can also be selected as the USART1 (SCI) Asynchronous Transmit or USART1 (SCI) Synchronous Clock. Output available from USART only.
								PORTB is a bi-directional I/O Port with software configurable weak pull-ups.
RB0/CAP1	55	59	47	71	57	I/O	ST	RB0 can also be the Capture1 input pin.
RB1/CAP2	54	58	46	70	56	I/O	ST	RB1 can also be the Capture2 input pin.
RB2/PWM1	50	54	42	66	52	I/O	ST	RB2 can also be the PWM1 output pin.
RB3/PWM2	53	57	45	69	55	I/O	ST	RB3 can also be the PWM2 output pin.
RB4/TCLK12	52	56	44	68	54	I/O	ST	RB4 can also be the external clock input to Timer1 and Timer2.
RB5/TCLK3	51	55	43	67	53	I/O	ST	RB5 can also be the external clock input to Timer3.
RB6/SCK	44	47	36	59	46	I/O	ST	RB6 can also be used as the master/slave clock for the SPI.
RB7/SDO	45	48	37	60	47	I/O	ST	RB7 can also be used as the data output for the SPI.

Legend: I = Input only; O = Output only; I/O = Input/Output;
P = Power; — = Not Used; TTL = TTL input; ST = Schmitt Trigger input

Note 1: The output is only available by the peripheral operation.
2: Open drain input/output pin. Pin forced to input upon any device RESET.

NOTES:

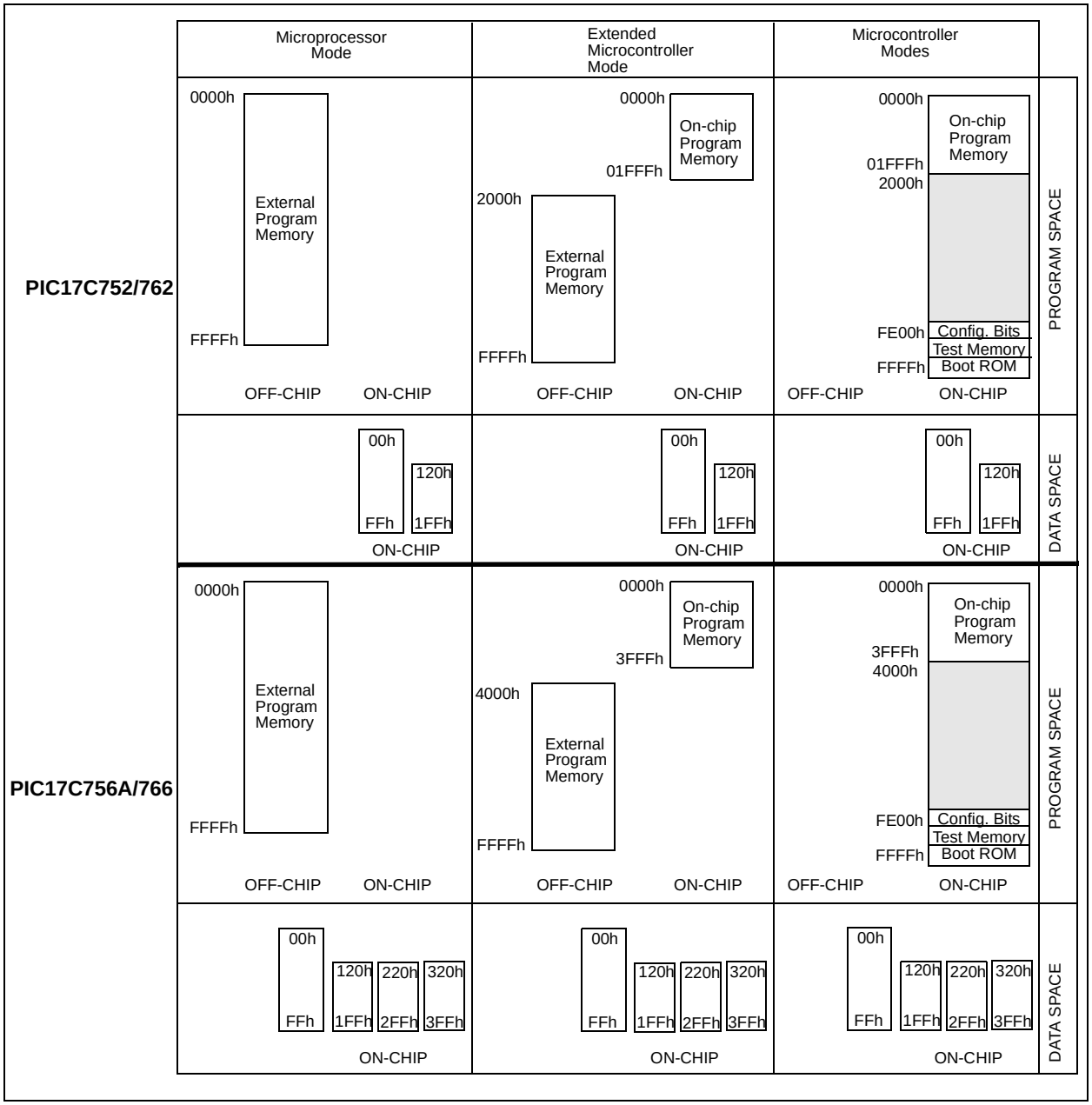
TABLE 7-1: MODE MEMORY ACCESS

Operating Mode	Internal Program Memory	Configuration Bits, Test Memory, Boot ROM
Microprocessor	No Access	No Access
Microcontroller	Access	Access
Extended Microcontroller	Access	No Access
Protected Microcontroller	Access	Access

The PIC17C7XX can operate in modes where the program memory is off-chip. They are the Microprocessor and Extended Microcontroller modes. The Microprocessor mode is the default for an unprogrammed device.

Regardless of the processor mode, data memory is always on-chip.

FIGURE 7-2: MEMORY MAP IN DIFFERENT MODES



7.2.2.1 ALU Status Register (ALUSTA)

The ALUSTA register contains the status bits of the Arithmetic and Logic Unit and the mode control bits for the indirect addressing register.

As with all the other registers, the ALUSTA register can be the destination for any instruction. If the ALUSTA register is the destination for an instruction that affects the Z, DC, C, or OV bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Therefore, the result of an instruction with the ALUSTA register as destination may be different than intended.

For example, the `CLRF ALUSTA, F` instruction will clear the upper four bits and set the Z bit. This leaves the ALUSTA register as `0000u1uu` (where `u` = unchanged).

It is recommended, therefore, that only `BCF`, `BSF`, `SWAPF` and `MOVWF` instructions be used to alter the ALUSTA register, because these instructions do not affect any status bits. To see how other instructions affect the status bits, see the "Instruction Set Summary."

Note 1: The C and DC bits operate as a $\overline{\text{borrow}}$ and digit $\overline{\text{borrow}}$ bit, respectively, in subtraction. See the `SUBLW` and `SUBWF` instructions for examples.

2: The overflow bit will be set if the 2's complement result exceeds +127, or is less than -128.

The Arithmetic and Logic Unit (ALU) is capable of carrying out arithmetic or logical operations on two operands, or a single operand. All single operand instructions operate either on the WREG register, or the given file register. For two operand instructions, one of the operands is the WREG register and the other is either a file register, or an 8-bit immediate constant.

REGISTER 7-1: ALUSTA REGISTER (ADDRESS: 04h, UNBANKED)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-x	R/W-x	R/W-x	R/W-x
FS3	FS2	FS1	FS0	OV	Z	DC	C
bit 7							bit 0

bit 7-6 **FS3:FS2**: FSR1 Mode Select bits
`00` = Post auto-decrement FSR1 value
`01` = Post auto-increment FSR1 value
`1x` = FSR1 value does not change

bit 5-4 **FS1:FS0**: FSR0 Mode Select bits
`00` = Post auto-decrement FSR0 value
`01` = Post auto-increment FSR0 value
`1x` = FSR0 value does not change

bit 3 **OV**: Overflow bit
This bit is used for signed arithmetic (2's complement). It indicates an overflow of the 7-bit magnitude, which causes the sign bit (bit7) to change state.
`1` = Overflow occurred for signed arithmetic (in this arithmetic operation)
`0` = No overflow occurred

bit 2 **Z**: Zero bit
`1` = The result of an arithmetic or logic operation is zero
`0` = The result of an arithmetic or logic operation is not zero

bit 1 **DC**: Digit carry/$\overline{\text{borrow}}$ bit
For `ADDWF` and `ADDLW` instructions.
`1` = A carry-out from the 4th low order bit of the result occurred
`0` = No carry-out from the 4th low order bit of the result

Note: For borrow, the polarity is reversed.

bit 0 **C**: Carry/$\overline{\text{borrow}}$ bit

For `ADDWF` and `ADDLW` instructions. Note that a subtraction is executed by adding the two's complement of the second operand.
For rotate (`RRCF`, `RLCF`) instructions, this bit is loaded with either the high or low order bit of the source register.
`1` = A carry-out from the Most Significant bit of the result occurred
`0` = No carry-out from the Most Significant bit of the result

Note: For borrow, the polarity is reversed.

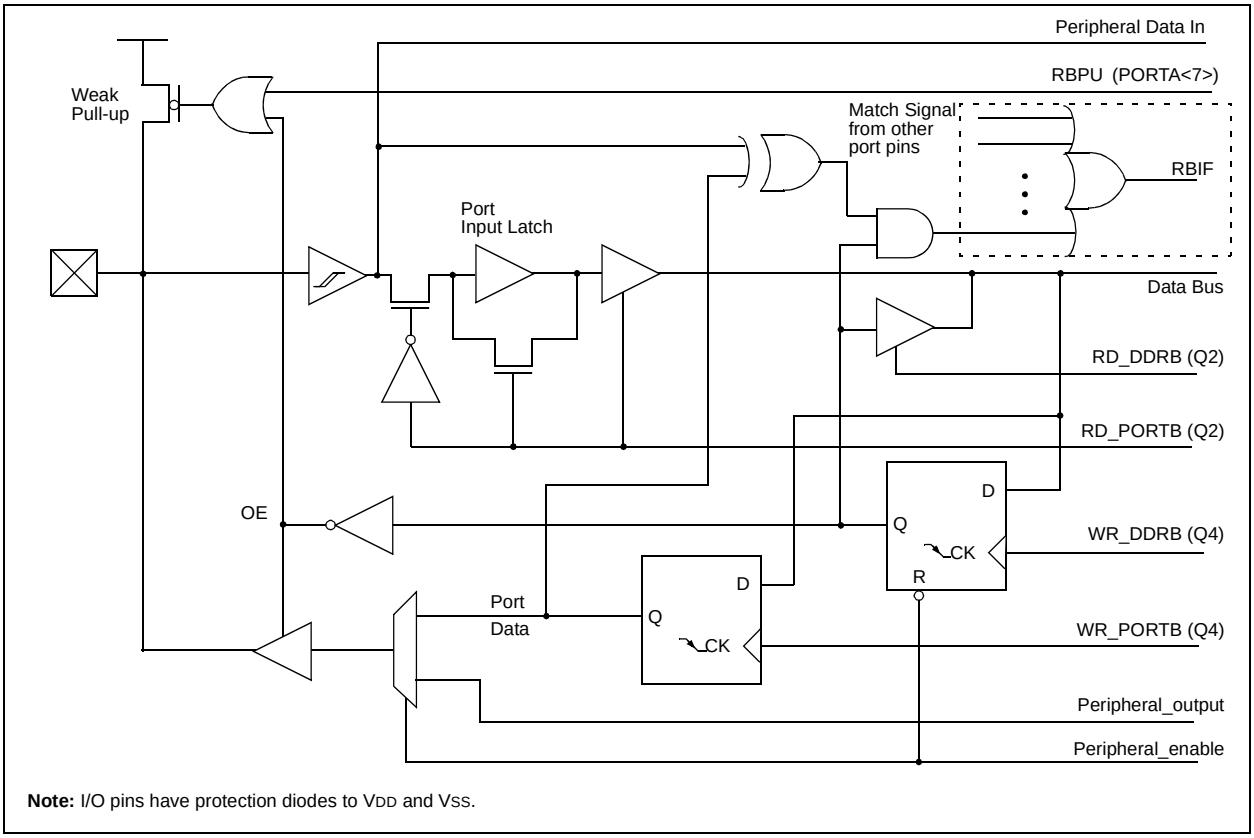
Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR Reset	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

Example 10-2 shows an instruction sequence to initialize PORTB. The Bank Select Register (BSR) must be selected to Bank 0 for the port to be initialized. The following example uses the MOVLB instruction to load the BSR register for bank selection.

EXAMPLE 10-2: INITIALIZING PORTB

```
MOVLB   0          ; Select Bank 0
CLRF    PORTB, F   ; Init PORTB by clearing
                   ;  output data latches
MOVLW   0xCF       ; Value used to initialize
                   ;  data direction
MOVWF   DDRB       ; Set RB<3:0> as inputs
                   ;   RB<5:4> as outputs
                   ;   RB<7:6> as inputs
```

FIGURE 10-6: BLOCK DIAGRAM OF RB3:RB2 PORT PINS



Note: I/O pins have protection diodes to VDD and VSS.

10.6 PORTF and DDRF Registers

PORTF is an 8-bit wide bi-directional port. The corresponding data direction register is DDRF. A '1' in DDRF configures the corresponding port pin as an input. A '0' in the DDRF register configures the corresponding port pin as an output. Reading PORTF reads the status of the pins, whereas writing to PORTF will write to the respective port latch.

All eight bits of PORTF are multiplexed with 8 channels of the 10-bit A/D converter.

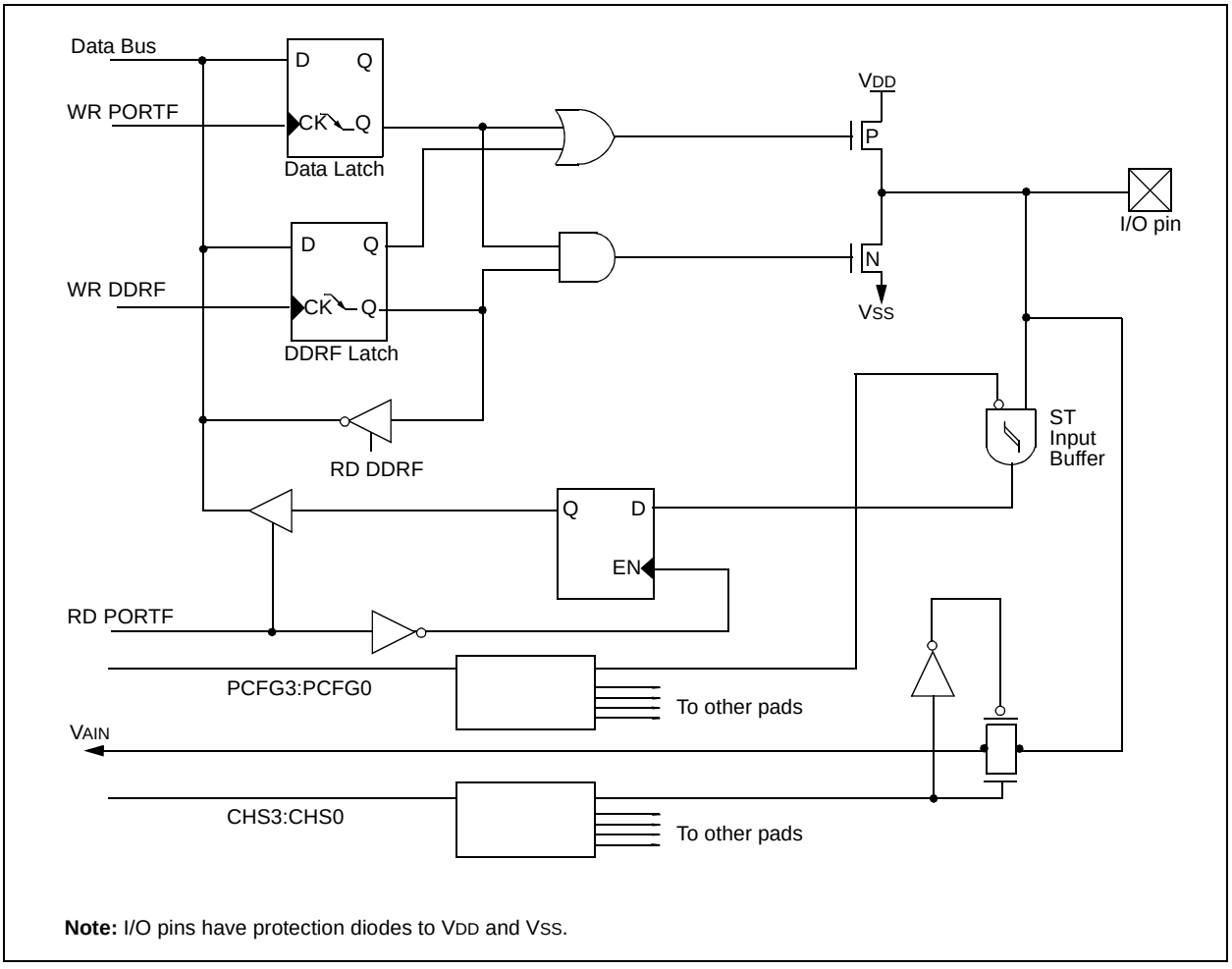
Upon RESET, the entire Port is automatically configured as analog inputs and must be configured in software to be a digital I/O.

Example 10-6 shows an instruction sequence to initialize PORTF. The Bank Select Register (BSR) must be selected to Bank 5 for the port to be initialized. The following example uses the `MOVLB` instruction to load the BSR register for bank selection.

EXAMPLE 10-6: INITIALIZING PORTF

```
MOVLB   5          ; Select Bank 5
MOVWF   0x0E       ; Configure PORTF as
MOVWF   ADCON1     ; Digital
CLRF    PORTF, F   ; Initialize PORTF data
                   ;   latches before
                   ;   the data direction
                   ;   register
MOVLW    0x03      ; Value used to init
                   ;   data direction
MOVWF    DDRF      ; Set RF<1:0> as inputs
                   ;   RF<7:2> as outputs
```

FIGURE 10-13: BLOCK DIAGRAM OF RF7:RF0



Note: I/O pins have protection diodes to V_{DD} and V_{SS}.

TABLE 10-11: PORTF FUNCTIONS

Name	Bit	Buffer Type	Function
RF0/AN4	bit0	ST	Input/output or analog input 4.
RF1/AN5	bit1	ST	Input/output or analog input 5.
RF2/AN6	bit2	ST	Input/output or analog input 6.
RF3/AN7	bit3	ST	Input/output or analog input 7.
RF4/AN8	bit4	ST	Input/output or analog input 8.
RF5/AN9	bit5	ST	Input/output or analog input 9.
RF6/AN10	bit6	ST	Input/output or analog input 10.
RF7/AN11	bit7	ST	Input/output or analog input 11.

Legend: ST = Schmitt Trigger input

TABLE 10-12: REGISTERS/BITS ASSOCIATED WITH PORTF

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	$\overline{\text{MCLR}}$, WDT
10h, Bank 5	DDRF	Data Direction Register for PORTF								1111 1111	1111 1111
11h, Bank 5	PORTF	RF7/ AN11	RF6/ AN10	RF5/ AN9	RF4/ AN8	RF3/ AN7	RF2/ AN6	RF1/ AN5	RF0/ AN4	0000 0000	0000 0000
15h, Bank 5	ADCON1	ADCS1	ADCS0	ADFM	—	PCFG3	PCFG2	PCFG1	PCFG0	000- 0000	000- 0000

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by PORTF.

The USART can be configured as a full duplex asynchronous system that can communicate with peripheral devices such as CRT terminals and personal computers, or it can be configured as a half duplex synchronous system that can communicate with peripheral devices such as A/D or D/A integrated circuits, Serial EEPROMs etc. The USART can be configured in the following modes:

- Asynchronous (full duplex)
- Synchronous - Master (half duplex)
- Synchronous - Slave (half duplex)

The SPEN (RCSTA<7>) bit has to be set in order to configure the I/O pins as the Serial Communication Interface (USART).

The USART module will control the direction of the RX/DT and TX/CK pins, depending on the states of the USART configuration bits in the RCSTA and TXSTA registers. The bits that control I/O direction are:

- SPEN
- TXEN
- SREN
- CREN
- CSRC

REGISTER 14-2: RCSTA1 REGISTER (ADDRESS: 13h, BANK 0)
RCSTA2 REGISTER (ADDRESS: 13h, BANK 4)

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R-0	R-0	R-x
SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D
bit 7							bit 0

bit 7 **SPEN**: Serial Port Enable bit
1 = Configures TX/CK and RX/DT pins as serial port pins
0 = Serial port disabled

bit 6 **RX9**: 9-bit Receive Select bit
1 = Selects 9-bit reception
0 = Selects 8-bit reception

bit 5 **SREN**: Single Receive Enable bit
This bit enables the reception of a single byte. After receiving the byte, this bit is automatically cleared.

Synchronous mode:
1 = Enable reception
0 = Disable reception

Note: This bit is ignored in synchronous slave reception.

Asynchronous mode:
Don't care

bit 4 **CREN**: Continuous Receive Enable bit
This bit enables the continuous reception of serial data.

Asynchronous mode:
1 = Enable continuous reception
0 = Disables continuous reception

Synchronous mode:
1 = Enables continuous reception until CREN is cleared (CREN overrides SREN)
0 = Disables continuous reception

bit 3 **Unimplemented**: Read as '0'

bit 2 **FERR**: Framing Error bit
1 = Framing error (updated by reading RCREG)
0 = No framing error

bit 1 bit **OERR**: Overrun Error bit
1 = Overrun (cleared by clearing CREN)
0 = No overrun error

bit 0 **RX9D**: 9th bit of Receive Data (can be the software calculated parity bit)

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR Reset	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

15.2.14 STOP CONDITION TIMING

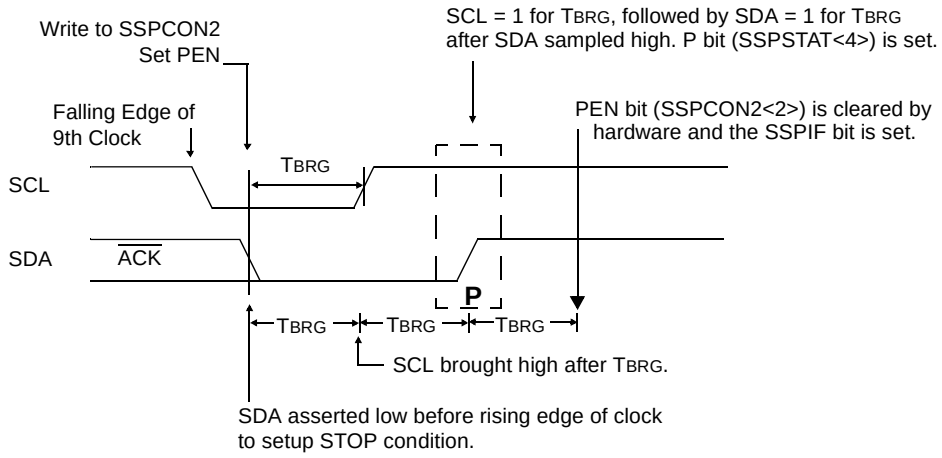
A STOP bit is asserted on the SDA pin at the end of a receive/transmit by setting the Stop Sequence Enable bit PEN (SSPCON2<2>). At the end of a receive/transmit the SCL line is held low after the falling edge of the ninth clock. When the PEN bit is set, the master will assert the SDA line low. When the SDA line is sampled low, the baud rate generator is reloaded and counts down to '0'. When the baud rate generator times out, the SCL pin will be brought high and one TBRG (baud rate generator rollover count) later, the SDA pin will be de-asserted. When the SDA pin is sampled high while SCL is high, the P bit (SSPSTAT<4>) is set. A TBRG later, the PEN bit is cleared and the SSPIF bit is set (Figure 15-31).

Whenever the firmware decides to take control of the bus, it will first determine if the bus is busy by checking the S and P bits in the SSPSTAT register. If the bus is busy, then the CPU can be interrupted (notified) when a STOP bit is detected (i.e., bus is free).

15.2.14.1 WCOL Status Flag

If the user writes the SSPBUF when a STOP sequence is in progress, then WCOL is set and the contents of the buffer are unchanged (the write doesn't occur).

FIGURE 15-31: STOP CONDITION RECEIVE OR TRANSMIT MODE



Note: TBRG = one baud rate generator period.

15.2.18.3 Bus Collision During a STOP Condition

Bus collision occurs during a STOP condition if:

a) After the SDA pin has been de-asserted and allowed to float high, SDA is sampled low after the BRG has timed out.

b) After the SCL pin is de-asserted, SCL is sampled low before SDA goes high.

The STOP condition begins with SDA asserted low. When SDA is sampled low, the SCL pin is allowed to float. When the pin is sampled high (clock arbitration), the baud rate generator is loaded with SSPADD<6:0> and counts down to ‘0’. After the BRG times out, SDA is sampled. If SDA is sampled low, a bus collision has occurred. This is due to another master attempting to drive a data '0'. If the SCL pin is sampled low before SDA is allowed to float high, a bus collision occurs. This is another case of another master attempting to drive a data '0' (Figure 15-40).

FIGURE 15-40: BUS COLLISION DURING A STOP CONDITION (CASE 1)

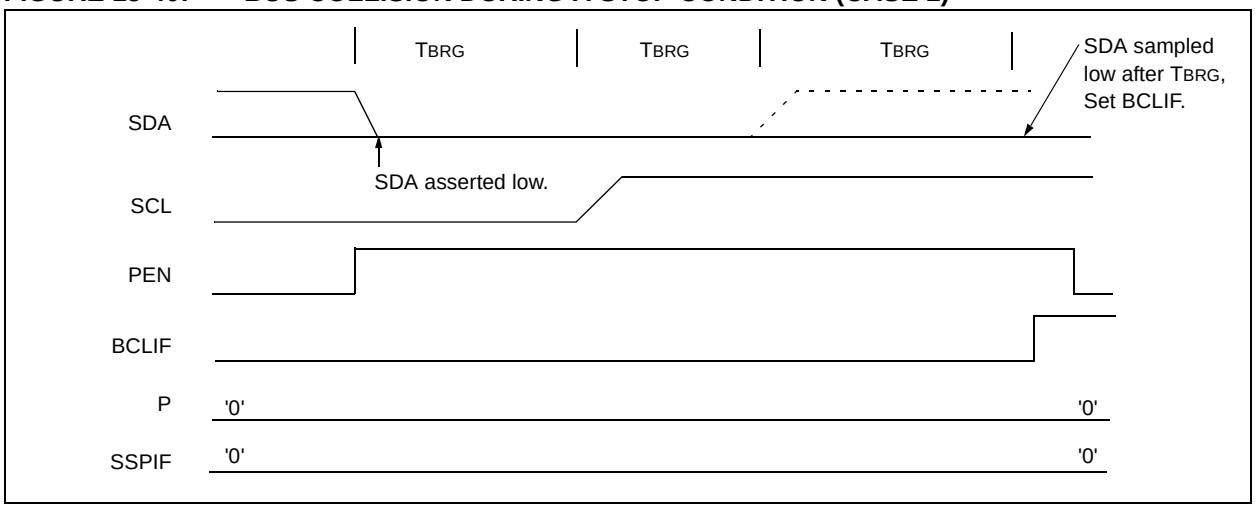
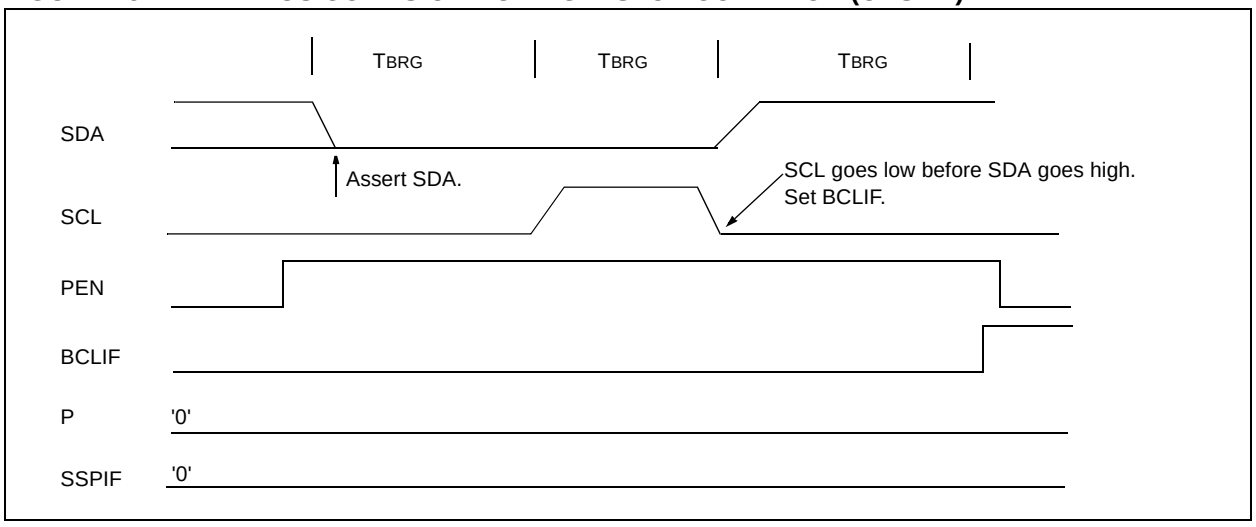


FIGURE 15-41: BUS COLLISION DURING A STOP CONDITION (CASE 2)



16.4.1 A/D RESULT REGISTERS

The ADRESH:ADRESL register pair is the location where the 10-bit A/D result is loaded at the completion of the A/D conversion. This register pair is 16-bits wide. The A/D module gives the flexibility to left or right justify the 10-bit result in the 16-bit result register. The A/D Format Select bit (ADFM) controls this justification. Figure 16-6 shows the operation of the A/D result justification. The extra bits are loaded with '0's'. When an A/D result will not overwrite these locations (A/D disable), these registers may be used as two general purpose 8-bit registers.

16.5 A/D Operation During SLEEP

The A/D module can operate during SLEEP mode. This requires that the A/D clock source be set to RC (ADCS1:ADCS0 = 11). When the RC clock source is selected, the A/D module waits one instruction cycle before starting the conversion. This allows the SLEEP instruction to be executed, which eliminates all digital switching noise from the conversion. When the conversion is completed, the GO/DONE bit will be cleared, and the result loaded into the ADRES register. If the A/D interrupt is enabled, the device will wake-up from SLEEP. If the A/D interrupt is not enabled, the A/D module will then be turned off, although the ADON bit will remain set.

When the A/D clock source is another clock option (not RC), a SLEEP instruction will cause the present conversion to be aborted and the A/D module to be turned off, though the ADON bit will remain set.

Turning off the A/D places the A/D module in its lowest current consumption state.

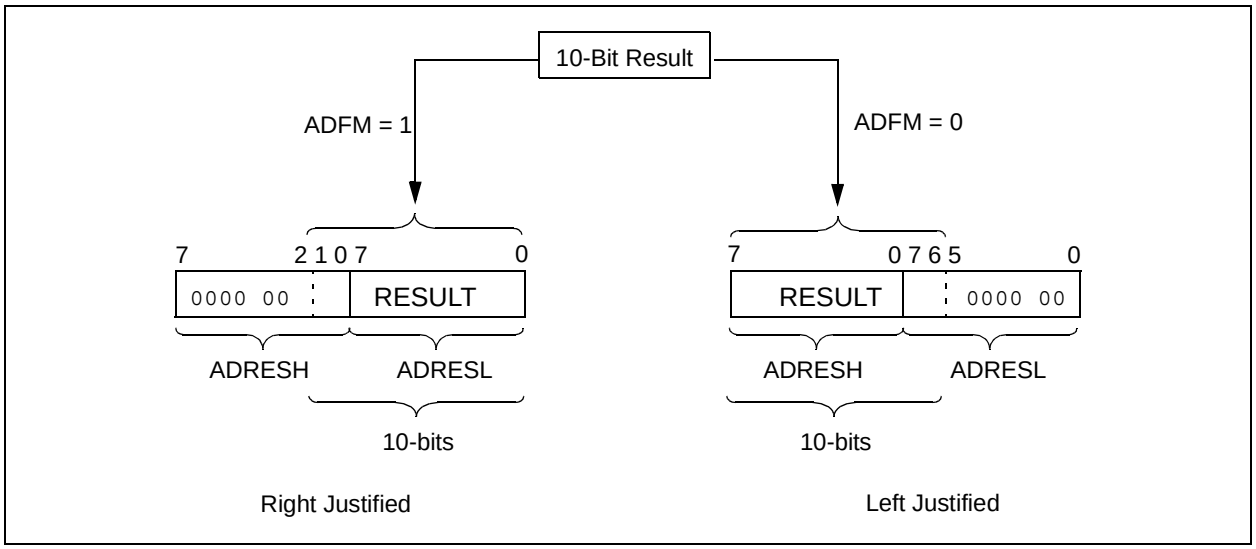
Note:	For the A/D module to operate in SLEEP, the A/D clock source must be set to RC (ADCS1:ADCS0 = 11). To allow the conversion to occur during SLEEP, ensure the SLEEP instruction immediately follows the instruction that sets the GO/DONE bit.

16.6 Effects of a RESET

A device RESET forces all registers to their RESET state. This forces the A/D module to be turned off, and any conversion is aborted.

The value that is in the ADRESH:ADRESL registers is not modified for a Power-on Reset. The ADRESH:ADRESL registers will contain unknown data after a Power-on Reset.

FIGURE 16-6: A/D RESULT JUSTIFICATION



18.2 Q Cycle Activity

Each instruction cycle (TCY) is comprised of four Q cycles (Q1-Q4). The Q cycle is the same as the device oscillator cycle (TOSC). The Q cycles provide the timing/ designation for the Decode, Read, Process Data, Write, etc., of each instruction cycle. The following diagram shows the relationship of the Q cycles to the instruction cycle.

The four Q cycles that make up an instruction cycle (TCY) can be generalized as:

Q1: Instruction Decode Cycle or forced No operation

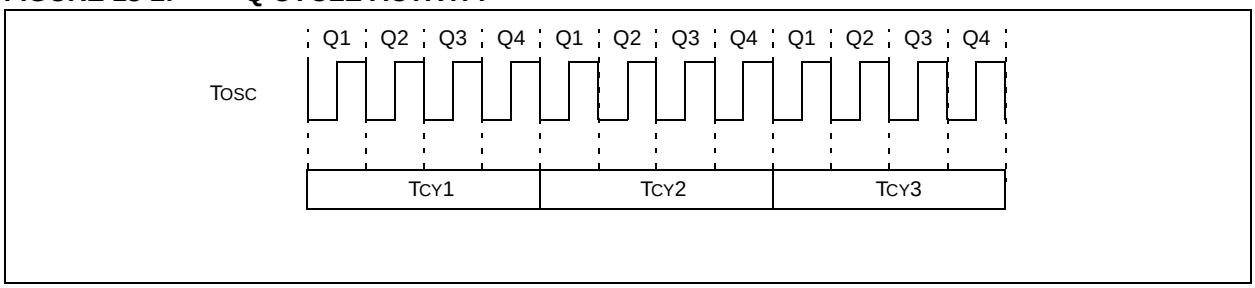
Q2: Instruction Read Cycle or No operation

Q3: Process the Data

Q4: Instruction Write Cycle or No operation

Each instruction will show the detailed Q cycle operation for the instruction.

FIGURE 18-2: Q CYCLE ACTIVITY



CPFSLT — **Compare f with WREG, skip if f < WREG**

Syntax: [*label*] CPFSLT f

Operands: $0 \le f \le 255$

Operation: (f) – (WREG), skip if (f) < (WREG) (unsigned comparison)

Status Affected: None

Encoding:

0011	0000	ffff	ffff

Description: Compares the contents of data memory location 'f' to the contents of WREG by performing an unsigned subtraction.
If the contents of 'f' are less than the contents of WREG, then the fetched instruction is discarded and a NOP is executed instead, making this a two-cycle instruction.

Words: 1

Cycles: 1 (2)

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	No operation

If skip:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation

Example:
```
HERE    CPFSLT REG
NLESS   :
LESS    :
```

Before Instruction
PC = Address (HERE)
W = ?

After Instruction
If REG < WREG;
PC = Address (LESS)
If REG ≥ WREG;
PC = Address (NLESS)

DAW — **Decimal Adjust WREG Register**

Syntax: [*label*] DAW f,s

Operands: $0 \le f \le 255$
$s \in [0,1]$

Operation:
If [[WREG<7:4> > 9].OR.[C = 1]].AND. [WREG<3:0> > 9]
then
WREG<7:4> + 7→ f<7:4>, s<7:4>;

If [WREG<7:4> > 9].OR.[C = 1]
then
WREG<7:4> + 6→ f<7:4>, s<7:4>;
else
WREG<7:4>→ f<7:4>, s<7:4>;

If [WREG<3:0> > 9].OR.[DC = 1]
then
WREG<3:0> + 6→ f<3:0>, s<3:0>;
else
WREG<3:0>→ f<3:0>, s<3:0>

Status Affected: C

Encoding:

0010	111s	ffff	ffff

Description: DAW adjusts the eight-bit value in WREG, resulting from the earlier addition of two variables (each in packed BCD format) and produces a correct packed BCD result.
s = 0: Result is placed in Data memory location 'f' and WREG.
s = 1: Result is placed in Data memory location 'f'.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write register 'f' and other specified register

Example:
```
DAW   REG1, 0
```

Before Instruction
WREG = 0xA5
REG1 = ??
C = 0
DC = 0

After Instruction
WREG = 0x05
REG1 = 0x05
C = 1
DC = 0

INCF **Increment f**

Syntax: [*label*] INCF f,d

Operands: $0 \le f \le 255$
$d \in [0,1]$

Operation: (f) + 1 → (dest)

Status Affected: OV, C, DC, Z

Encoding:

0001	010d	ffff	ffff

Description: The contents of register 'f' are incremented. If 'd' is 0, the result is placed in WREG. If 'd' is 1, the result is placed back in register 'f'.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

Example: `INCF CNT, 1`

Before Instruction
CNT = 0xFF
Z = 0
C = ?

After Instruction
CNT = 0x00
Z = 1
C = 1

INCFSZ **Increment f, skip if 0**

Syntax: [*label*] INCFSZ f,d

Operands: $0 \le f \le 255$
$d \in [0,1]$

Operation: (f) + 1 → (dest)
skip if result = 0

Status Affected: None

Encoding:

0001	111d	ffff	ffff

Description: The contents of register 'f' are incremented. If 'd' is 0, the result is placed in WREG. If 'd' is 1, the result is placed back in register 'f'.
If the result is 0, the next instruction, which is already fetched is discarded and a NOP is executed instead, making it a two-cycle instruction.

Words: 1

Cycles: 1(2)

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

If skip:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation

Example:
```
HERE    INCFSZ  CNT, 1
NZERO   :
ZERO    :
```

Before Instruction
PC = Address (HERE)

After Instruction
CNT = CNT + 1
If CNT = 0;
PC = Address (ZERO)
If CNT ≠ 0;
PC = Address (NZERO)

MOVLR — **Move Literal to high nibble in BSR**

Syntax: [*label*] MOVLR k

Operands: $0 \le k \le 15$

Operation: $k \rightarrow (BSR<7:4>)$

Status Affected: None

Encoding:

1011	101x	kkkk	uuuu

Description: The 4-bit literal 'k' is loaded into the most significant 4-bits of the Bank Select Register (BSR). Only the high 4-bits of the Bank Select Register are affected. The lower half of the BSR is unchanged. The assembler will encode the “u” fields as 0.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal 'k'	Process Data	Write literal 'k' to BSR<7:4>

Example: `MOVLR 5`

Before Instruction
BSR register = 0x22

After Instruction
BSR register = 0x52

MOVLW — **Move Literal to WREG**

Syntax: [*label*] MOVLW k

Operands: $0 \le k \le 255$

Operation: $k \rightarrow (WREG)$

Status Affected: None

Encoding:

1011	0000	kkkk	kkkk

Description: The eight-bit literal 'k' is loaded into WREG.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal 'k'	Process Data	Write to WREG

Example: `MOVLW 0x5A`

After Instruction
WREG = 0x5A

NOTES:

Param No.	Sym	Characteristic		Min	Max	Units	Conditions
110	Tbuf	Bus free time	100 kHz mode	4.7	—	ms	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	ms	
			1 MHz mode(1)	0.5	—	ms	
D102	Cb	Bus capacitive loading		—	400	pF	

Note 1: Maximum pin capacitance = 10 pF for all I^2C pins.

2: A fast mode (400 KHz) I^2C bus device can be used in a standard mode I^2C bus system, but the parameter # 107 ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line. Parameter #102 + #107 = 1000 + 250 = 1250 ns (for 100 kHz mode) before the SCL line is released.

3: C_b is specified to be from 10-400pF. The minimum specifications are characterized with C_b=10pF. The rise time spec (t_r) is characterized with R_p=R_p min. The minimum fall time specification (t_f) is characterized with C_b=10pF,and R_p=R_p max. These are only valid for fast mode operation (V_{DD}=4.5-5.5V) and where the SPM bit (SSPSTAT<7>) =1.)

4: Max specifications for these parameters are valid for falling edge only. Specs are characterized with R_p=R_p min and C_b=400pF for standard mode, 200pF for fast mode, and 10pF for 1MHz mode.

FIGURE 20-19: USART SYNCHRONOUS TRANSMISSION (MASTER/SLAVE) TIMING

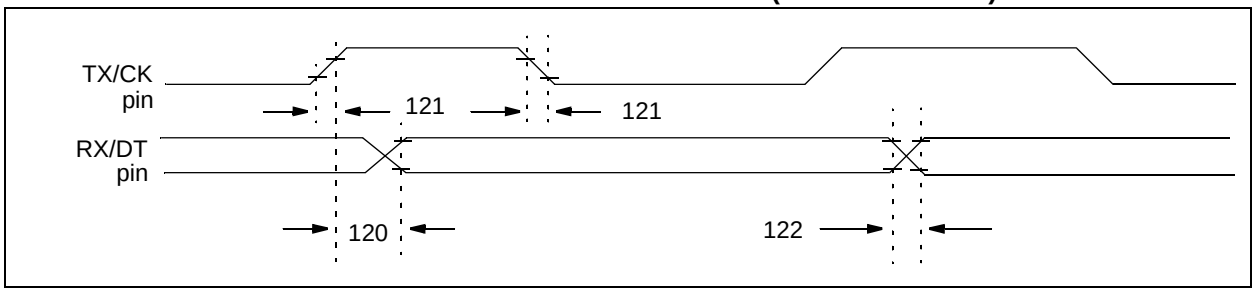


TABLE 20-14: USART SYNCHRONOUS TRANSMISSION REQUIREMENTS

Param No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
120	TckH2dtV	SYNC XMIT (MASTER & SLAVE) Clock high to data out valid	PIC17**C**XXX	—	—	50	ns	
			PIC17**LC**XXX	—	—	75	ns	
121	TckRF	Clock out rise time and fall time (Master mode)	PIC17**C**XXX	—	—	25	ns	
			PIC17**LC**XXX	—	—	40	ns	
122	TdtRF	Data out rise time and fall time	PIC17**C**XXX	—	—	25	ns	
			PIC17**LC**XXX	—	—	40	ns	

† Data in “Typ” column is at 5V, 25°C unless otherwise stated.

FIGURE 20-21: USART ASYNCHRONOUS MODE START BIT DETECT

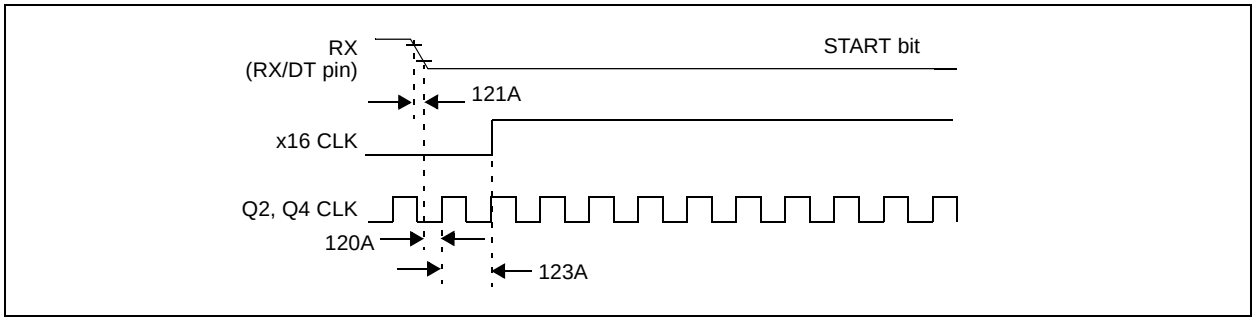


TABLE 20-16: USART ASYNCHRONOUS MODE START BIT DETECT REQUIREMENTS

Param No.	Sym	Characteristic		Min	Typ	Max	Units	Conditions
120A	TdtL2ckH	Time to ensure that the RX pin is sampled low		—	—	TCY	ns	
121A	TdtRF	Data rise time and fall time	Receive	—	—	**(Note 1)**	ns	
			Transmit	—	—	40	ns	
123A	TckH2bckL	Time from RX pin sampled low to first rising edge of x16 clock		—	—	TCY	ns	

Note 1: Schmitt trigger will determine logic level.

FIGURE 20-22: USART ASYNCHRONOUS RECEIVE SAMPLING WAVEFORM

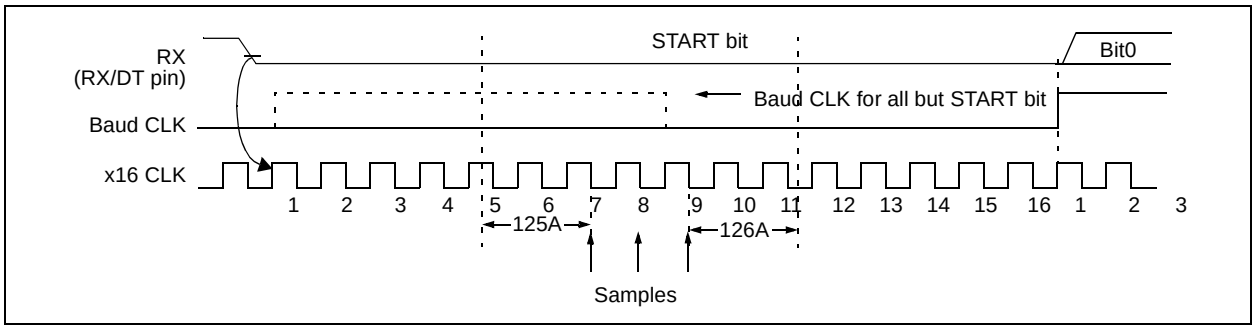


TABLE 20-17: USART ASYNCHRONOUS RECEIVE SAMPLING REQUIREMENTS

Param No.	Sym	Characteristic	Min	Typ	Max	Units	Conditions
125A	TdtL2ckH	Setup time of RX pin to first data sampled	TCY	—	—	ns	
126A	TdtL2ckH	Hold time of RX pin from last data sampled	TCY	—	—	ns	

APPENDIX A: MODIFICATIONS

The following is the list of modifications over the PIC16CXX microcontroller family:

1. Instruction word length is increased to 16-bit. This allows larger page sizes, both in program memory (8 Kwords verses 2 Kwords) and register file (256 bytes versus 128 bytes).
2. Four modes of operation: Microcontroller, Protected Microcontroller, Extended Microcontroller, and Microprocessor.
3. 22 new instructions.
   The MOVF, TRIS and OPTION instructions are no longer supported.
4. Four new instructions (TLRD, TLWT, TABLRD, TABLWT) for transferring data between data memory and program memory. They can be used to "self program" the EPROM program memory.
5. Single cycle data memory to data memory transfers possible (MOVPF and MOVFP instructions). These instructions do not affect the Working register (WREG).
6. W register (WREG) is now directly addressable.
7. A PC high latch register (PCLATH) is extended to 8-bits. The PCLATCH register is now both readable and writable.
8. Data memory paging is redefined slightly.
9. DDR registers replace function of TRIS registers.
10. Multiple Interrupt vectors added. This can decrease the latency for servicing interrupts.
11. Stack size is increased to 16 deep.
12. BSR register for data memory paging.
13. Wake-up from SLEEP operates slightly differently.
14. The Oscillator Start-Up Timer (OST) and Power-Up Timer (PWRT) operate in parallel and not in series.
15. PORTB interrupt-on-change feature works on all eight port pins.
16. TMR0 is 16-bit, plus 8-bit prescaler.
17. Second indirect addressing register added (FSR1 and FSR2). Control bits can select the FSR registers to auto-increment, auto-decrement, remain unchanged after an indirect address.
18. Hardware multiplier added (8 x 8 $\rightarrow$ 16-bit).
19. Peripheral modules operate slightly differently.
20. A/D has both V_{REF}+ and V_{REF}- inputs.
21. USARTs do not implement BRGH feature.
22. Oscillator modes slightly redefined.
23. Control/Status bits and registers have been placed in different registers and the control bit for globally enabling interrupts has inverse polarity.
24. In-circuit serial programming is implemented differently.

APPENDIX B: COMPATIBILITY

To convert code written for PIC16CXXX to PIC17CXXX, the user should take the following steps:

1. Remove any TRIS and OPTION instructions, and implement the equivalent code.
2. Separate the Interrupt Service Routine into its four vectors.
3. Replace:
   ```
   MOVF    REG1, W
   ```
   with:
   ```
   MOVFP   REG1, WREG
   ```
4. Replace:
   ```
   MOVF    REG1, W
   MOVWF   REG2
   ```
   with:
   ```
   MOVPF   REG1, REG2 ; Addr(REG1)<20h
   ```
   or
   ```
   MOVFP   REG1, REG2 ; Addr(REG2)<20h
   ```

   Note: If REG1 and REG2 are both at addresses greater then 20h, two instructions are required.
   ```
   MOVFP   REG1, WREG ;
   MOVPF   WREG, REG2 ;
   ```
5. Ensure that all bit names and register names are updated to new data memory map locations.
6. Verify data memory banking.
7. Verify mode of operation for indirect addressing.
8. Verify peripheral routines for compatibility.
9. Weak pull-ups are enabled on RESET.
10. WDT time-outs always reset the device (in run or SLEEP mode).

B.1 Upgrading from PIC17C42 Devices

To convert code from the PIC17C42 to all the other PIC17CXXX devices, the user should take the following steps.

1. If the hardware multiply is to be used, ensure that any variables at address 18h and 19h are moved to another address.
2. Ensure that the upper nibble of the BSR was not written with a non-zero value. This may cause unexpected operation since the RAM bank is no longer 0.
3. The disabling of global interrupts has been enhanced, so there is no additional testing of the GLINTD bit after a BSF CPUSTA, GLINTD instruction.