



Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	33MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	50
Program Memory Size	16KB (8K x 16)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	454 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	68-LCC (J-Lead)
Supplier Device Package	68-PLCC (24.23x24.23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic17c752-33-l

PIC17C7XX

TABLE 1-1: PIC17CXXX FAMILY OF DEVICES

Features		PIC17C42A	PIC17C43	PIC17C44	PIC17C752	PIC17C756A	PIC17C762	PIC17C766
Maximum Frequency of Operation		33 MHz	33 MHz	33 MHz	33 MHz	33 MHz	33 MHz	33 MHz
Operating Voltage Range		2.5 - 6.0V	2.5 - 6.0V	2.5 - 6.0V	3.0 - 5.5V	3.0 - 5.5V	3.0 - 5.5V	3.0 - 5.5V
Program Memory (x16)	(EPROM)	2 K	4 K	8 K	8 K	16 K	8 K	16 K
	(ROM)	—	—	—	—	—	—	—
Data Memory (bytes)		232	454	454	678	902	678	902
Hardware Multiplier (8 x 8)		Yes	Yes	Yes	Yes	Yes	Yes	Yes
Timer0 (16-bit + 8-bit postscaler)		Yes	Yes	Yes	Yes	Yes	Yes	Yes
Timer1 (8-bit)		Yes	Yes	Yes	Yes	Yes	Yes	Yes
Timer2 (8-bit)		Yes	Yes	Yes	Yes	Yes	Yes	Yes
Timer3 (16-bit)		Yes	Yes	Yes	Yes	Yes	Yes	Yes
Capture inputs (16-bit)		2	2	2	4	4	4	4
PWM outputs (up to 10-bit)		2	2	2	3	3	3	3
USART/SCI		1	1	1	2	2	2	2
A/D channels (10-bit)		—	—	—	12	12	16	16
SSP (SPI/I ² C w/Master mode)		—	—	—	Yes	Yes	Yes	Yes
Power-on Reset		Yes	Yes	Yes	Yes	Yes	Yes	Yes
Watchdog Timer		Yes	Yes	Yes	Yes	Yes	Yes	Yes
External Interrupts		Yes	Yes	Yes	Yes	Yes	Yes	Yes
Interrupt Sources		11	11	11	18	18	18	18
Code Protect		Yes	Yes	Yes	Yes	Yes	Yes	Yes
Brown-out Reset		—	—	—	Yes	Yes	Yes	Yes
In-Circuit Serial Programming		—	—	—	Yes	Yes	Yes	Yes
I/O Pins		33	33	33	50	50	66	66
I/O High Current Capability	Source	25 mA	25 mA	25 mA	25 mA	25 mA	25 mA	25 mA
	Sink	25 mA ⁽¹⁾	25 mA ⁽¹⁾	25 mA ⁽¹⁾	25 mA ⁽¹⁾	25 mA ⁽¹⁾	25 mA ⁽¹⁾	25 mA ⁽¹⁾
Package Types		40-pin DIP 44-pin PLCC 44-pin MQFP 44-pin TQFP	40-pin DIP 44-pin PLCC 44-pin MQFP 44-pin TQFP	40-pin DIP 44-pin PLCC 44-pin MQFP 44-pin TQFP	64-pin TQFP 68-pin PLCC	64-pin TQFP 68-pin PLCC	80-pin TQFP 84-pin PLCC	80-pin TQFP 84-pin PLCC

Note 1: Pins RA2 and RA3 can sink up to 60 mA.

PIC17C7XX

5.1 Power-on Reset (POR), Power-up Timer (PWRT), Oscillator Start-up Timer (OST) and Brown-out Reset (BOR)

5.1.1 POWER-ON RESET (POR)

The Power-on Reset circuit holds the device in RESET until VDD is above the trip point (in the range of 1.4V - 2.3V). The devices produce an internal RESET for both rising and falling VDD. To take advantage of the POR, just tie the MCLR/VPP pin directly (or through a resistor) to VDD. This will eliminate external RC components usually needed to create Power-on Reset. A minimum rise time for VDD is required. See Electrical Specifications for details.

Figure 5-2 and Figure 5-3 show two possible POR circuits.

FIGURE 5-2: USING ON-CHIP POR

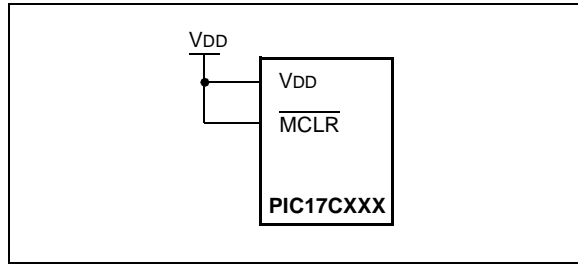
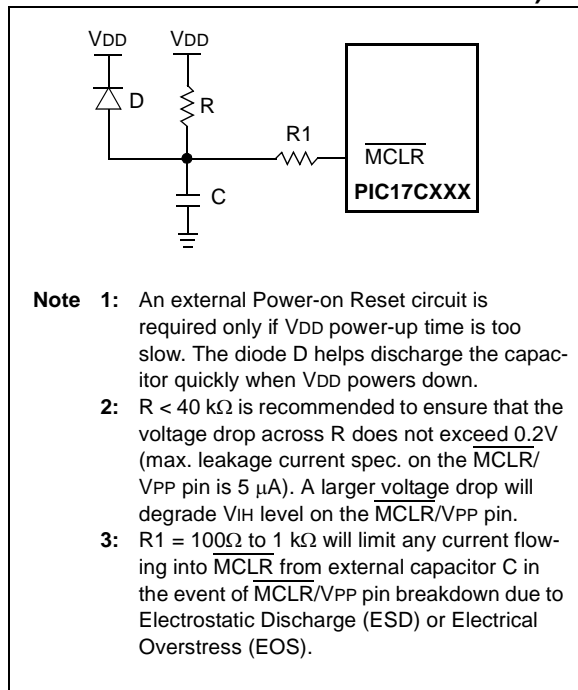


FIGURE 5-3: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)



5.1.2 POWER-UP TIMER (PWRT)

The Power-up Timer provides a fixed 96 ms time-out (nominal) on power-up. This occurs from the rising edge of the internal POR signal if VDD and MCLR are tied, or after the first rising edge of MCLR (detected high). The Power-up Timer operates on an internal RC oscillator. The chip is kept in RESET as long as the PWRT is active. In most cases, the PWRT delay allows VDD to rise to an acceptable level.

The power-up time delay will vary from chip to chip and with VDD and temperature. See DC parameters for details.

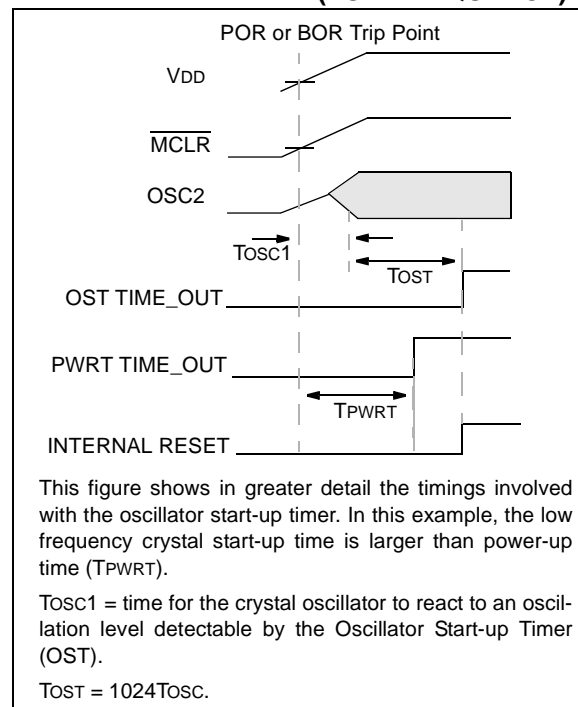
5.1.3 OSCILLATOR START-UP TIMER (OST)

The Oscillator Start-up Timer (OST) provides a 1024 oscillator cycle (1024Tosc) delay whenever the PWRT is invoked, or a wake-up from SLEEP event occurs in XT or LF mode. The PWRT and OST operate in parallel.

The OST counts the oscillator pulses on the OSC1/CLKIN pin. The counter only starts incrementing after the amplitude of the signal reaches the oscillator input thresholds. This delay allows the crystal oscillator or resonator to stabilize before the device exits RESET. The length of the time-out is a function of the crystal/resonator frequency.

Figure 5-4 shows the operation of the OST circuit. In this figure, the oscillator is of such a low frequency that although enabled simultaneously, the OST does not time-out until after the Power-up Timer time-out.

FIGURE 5-4: OSCILLATOR START-UP TIME (LOW FREQUENCY)



PIC17C7XX

In Figure 5-5, Figure 5-6 and Figure 5-7, the TPWRT timer time-out is greater then the TOST timer time-out, as would be the case in higher frequency crystals. For lower frequency crystals (i.e., 32 kHz), TOST may be greater.

FIGURE 5-5: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ TIED TO V_{DD})

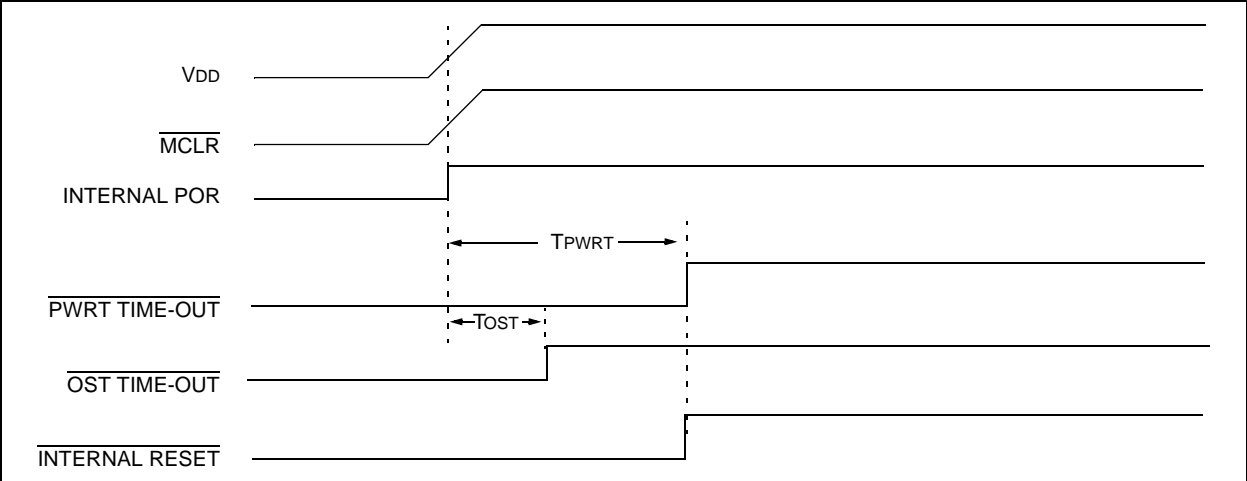


FIGURE 5-6: TIME-OUT SEQUENCE ON POWER-UP ($\overline{\text{MCLR}}$ NOT TIED TO V_{DD})

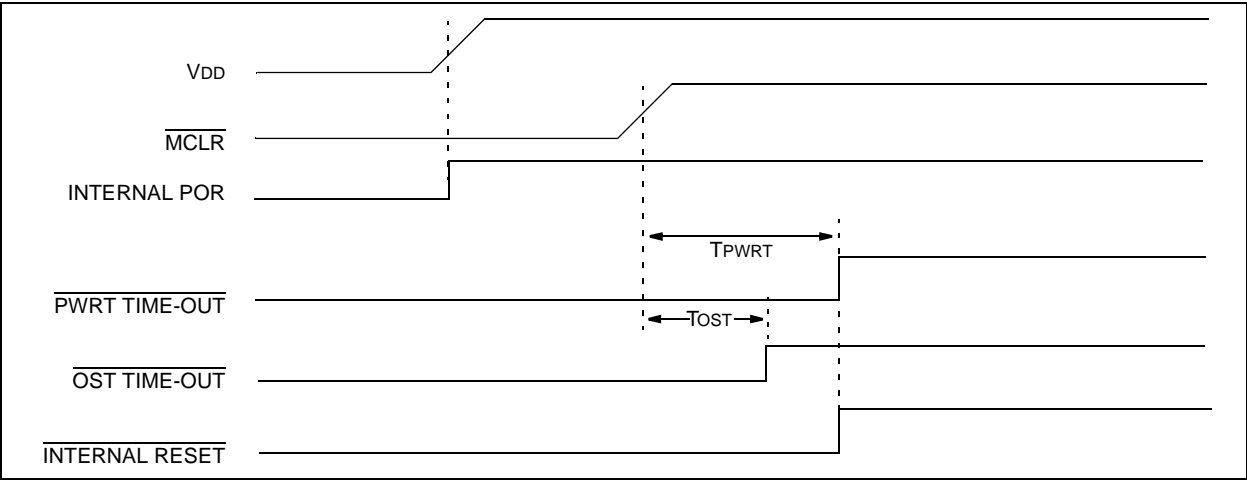
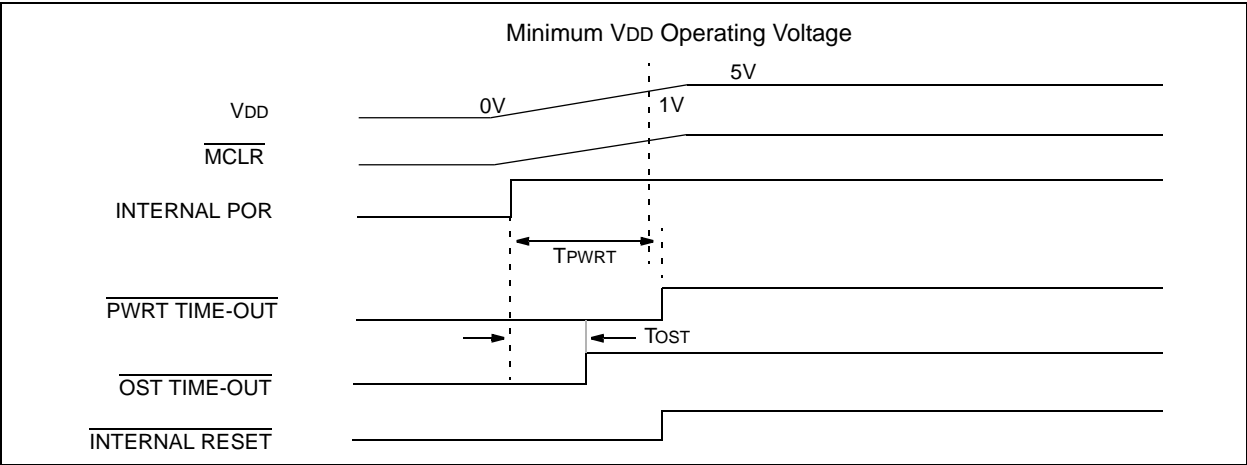


FIGURE 5-7: SLOW RISE TIME ($\overline{\text{MCLR}}$ TIED TO V_{DD})



EXAMPLE 6-1: SAVING STATUS AND WREG IN RAM (SIMPLE)

```

; The addresses that are used to store the CPUSTA and WREG values must be in the data memory
; address range of 1Ah - 1Fh. Up to 6 locations can be saved and restored using the MOVFP
; instruction. This instruction neither affects the status bits, nor corrupts the WREG register.
;
UNBANK1      EQU    0x01A      ; Address for 1st location to save
UNBANK2      EQU    0x01B      ; Address for 2nd location to save
UNBANK3      EQU    0x01C      ; Address for 3rd location to save
UNBANK4      EQU    0x01D      ; Address for 4th location to save
UNBANK5      EQU    0x01E      ; Address for 5th location to save
;                               ; (Label Not used in program)
UNBANK6      EQU    0x01F      ; Address for 6th location to save
;                               ; (Label Not used in program)
;
;                               ; At Interrupt Vector Address
PUSH         :               ; Push ALUSTA value
             MOVFP    ALUSTA, UNBANK1
             MOVFP    BSR, UNBANK2      ; Push BSR value
             MOVFP    WREG, UNBANK3     ; Push WREG value
             MOVFP    PCLATH, UNBANK4   ; Push PCLATH value
;
;                               ; Interrupt Service Routine (ISR) code
;
POP          :               ; Restore PCLATH value
             MOVFP    UNBANK4, PCLATH
             MOVFP    UNBANK3, WREG     ; Restore WREG value
             MOVFP    UNBANK2, BSR      ; Restore BSR value
             MOVFP    UNBANK1, ALUSTA   ; Restore ALUSTA value
;
             RETFIE                  ; Return from interrupt (enable interrupts)

```

7.8 Bank Select Register (BSR)

The BSR is used to switch between banks in the data memory area (Figure 7-9). In the PIC17C7XX devices, the entire byte is implemented. The lower nibble is used to select the peripheral register bank. The upper nibble is used to select the general purpose memory bank.

All the Special Function Registers (SFRs) are mapped into the data memory space. In order to accommodate the large number of registers, a banking scheme has been used. A segment of the SFRs, from address 10h to address 17h, is banked. The lower nibble of the bank select register (BSR) selects the currently active "peripheral bank." Effort has been made to group the peripheral registers of related functionality in one bank. However, it will still be necessary to switch from bank to

bank in order to address all peripherals related to a single task. To assist this, a `MOVLB` bank instruction has been included in the instruction set.

The need for a large general purpose memory space dictated a general purpose RAM banking scheme. The upper nibble of the BSR selects the currently active general purpose RAM bank. To assist this, a `MOVLB` bank instruction has been provided in the instruction set.

If the currently selected bank is not implemented (such as Bank 13), any read will read all '0's. Any write is completed to the bit bucket and the ALU status bits will be set/cleared as appropriate.

Note: Registers in Bank 15 in the Special Function Register area, are reserved for Microchip use. Reading of registers in this bank may cause random values to be read.

FIGURE 7-9: BSR OPERATION

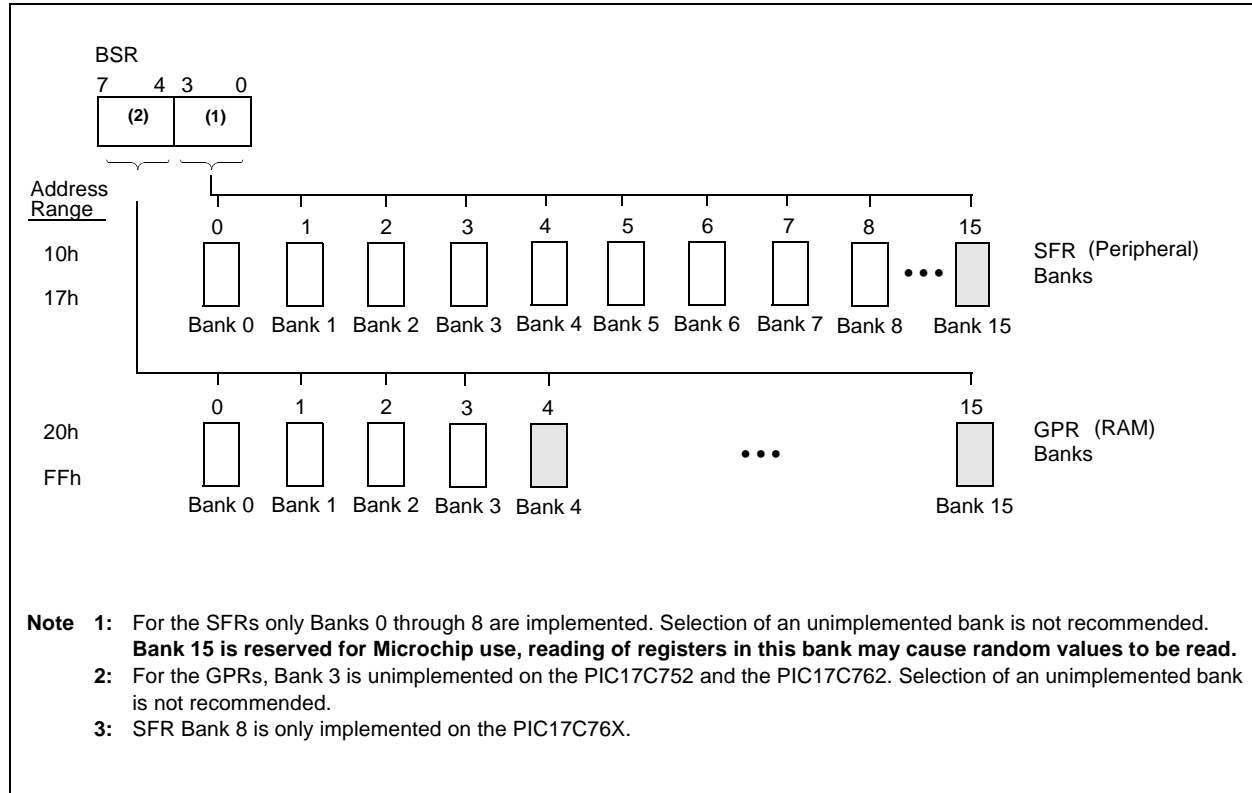


TABLE 10-11: PORTF FUNCTIONS

Name	Bit	Buffer Type	Function
RF0/AN4	bit0	ST	Input/output or analog input 4.
RF1/AN5	bit1	ST	Input/output or analog input 5.
RF2/AN6	bit2	ST	Input/output or analog input 6.
RF3/AN7	bit3	ST	Input/output or analog input 7.
RF4/AN8	bit4	ST	Input/output or analog input 8.
RF5/AN9	bit5	ST	Input/output or analog input 9.
RF6/AN10	bit6	ST	Input/output or analog input 10.
RF7/AN11	bit7	ST	Input/output or analog input 11.

Legend: ST = Schmitt Trigger input

TABLE 10-12: REGISTERS/BITS ASSOCIATED WITH PORTF

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	MCLR, WDT
10h, Bank 5	DDRF	Data Direction Register for PORTF								1111 1111	1111 1111
11h, Bank 5	PORTF	RF7/ AN11	RF6/ AN10	RF5/ AN9	RF4/ AN8	RF3/ AN7	RF2/ AN6	RF1/ AN5	RF0/ AN4	0000 0000	0000 0000
15h, Bank 5	ADCON1	ADCS1	ADCS0	ADFM	—	PCFG3	PCFG2	PCFG1	PCFG0	000- 0000	000- 0000

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by PORTF.

PIC17C7XX

TABLE 10-17: PORTJ FUNCTIONS

Name	Bit	Buffer Type	Function
RJ0	bit0	ST	Input/output
RJ1	bit1	ST	Input/output
RJ2	bit2	ST	Input/output
RJ3	bit3	ST	Input/output
RJ4	bit4	ST	Input/output
RJ5	bit5	ST	Input/output
RJ6	bit6	ST	Input/output
RJ7	bit7	ST	Input/output

Legend: ST = Schmitt Trigger input

TABLE 10-18: REGISTERS/BITS ASSOCIATED WITH PORTJ

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on, POR, BOR	$\overline{\text{MCLR}}$, WDT
12h, Bank 8	DDRJ	Data Direction Register for PORTJ								1111 1111	1111 1111
13h, Bank 8	PORTJ	RJ7	RJ6	RJ5	RJ4	RJ3	RJ2	RJ1	RJ0	xxxx xxxx	uuuu uuuu

Legend: x = unknown, u = unchanged

13.2.3 READING THE CAPTURE REGISTERS

The Capture overflow status flag bits are double buffered. The master bit is set if one captured word is already residing in the Capture register and another “event” has occurred on the CAPx pin. The new event will not transfer the TMR3 value to the capture register, protecting the previous unread capture value. When the user reads both the high and the low bytes (in any

order) of the Capture register, the master overflow bit is transferred to the slave overflow bit (CAxOVF) and then the master bit is reset. The user can then read TCONx to determine the value of CAxOVF.

An example of an instruction sequence to read capture registers and capture overflow flag bits is shown in Example 13-1. Depending on the capture source, different registers will need to be read.

EXAMPLE 13-1: SEQUENCE TO READ CAPTURE REGISTERS

```
MOVLB 3           ; Select Bank 3
MOVFPF CA2L, LO_BYTE ; Read Capture2 low byte, store in LO_BYTE
MOVFPF CA2H, HI_BYTE ; Read Capture2 high byte, store in HI_BYTE
MOVFPF TCON2, STAT_VAL ; Read TCON2 into file STAT_VAL
```

TABLE 13-6: REGISTERS ASSOCIATED WITH CAPTURE

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	MCLR, WDT
16h, Bank 3	TCON1	CA2ED1	CA2ED0	CA1ED1	CA1ED0	T16	TMR3CS	TMR2CS	TMR1CS	0000 0000	0000 0000
17h, Bank 3	TCON2	CA2OVF	CA1OVF	PWM2ON	PWM1ON	CA1/PR3	TMR3ON	TMR2ON	TMR1ON	0000 0000	0000 0000
16h, Bank 7	TCON3	—	CA4OVF	CA3OVF	CA4ED1	CA4ED0	CA3ED1	CA3ED0	PWM3ON	-000 0000	-000 0000
12h, Bank 2	TMR3L	Holding Register for the Low Byte of the 16-bit TMR3 Register								xxxx xxxx	uuuu uuuu
13h, Bank 2	TMR3H	Holding Register for the High Byte of the 16-bit TMR3 Register								xxxx xxxx	uuuu uuuu
16h, Bank 1	PIR1	RBIF	TMR3IF	TMR2IF	TMR1IF	CA2IF	CA1IF	TX1IF	RC1IF	x000 0010	u000 0010
17h, Bank 1	PIE1	RBIE	TMR3IE	TMR2IE	TMR1IE	CA2IE	CA1IE	TX1IE	RC1IE	0000 0000	0000 0000
10h, Bank 4	PIR2	SSPIF	BCLIF	ADIF	—	CA4IF	CA3IF	TX2IF	RC2IF	000- 0010	000- 0010
11h, Bank 4	PIE2	SSPIE	BCLIE	ADIE	—	CA4IE	CA3IE	TX2IE	RC2IE	000- 0000	000- 0000
07h, Unbanked	INTSTA	PEIF	T0CKIF	T0IF	INTF	PEIE	T0CKIE	T0IE	INTE	0000 0000	0000 0000
06h, Unbanked	CPUSTA	—	—	STKAV	GLINTD	\overline{TO}	\overline{PD}	\overline{POR}	\overline{BOR}	--11 11qq	--11 qquu
16h, Bank 2	PR3L/CA1L	Timer3 Period Register, Low Byte/Capture1 Register, Low Byte								xxxx xxxx	uuuu uuuu
17h, Bank 2	PR3H/CA1H	Timer3 Period Register, High Byte/Capture1 Register, High Byte								xxxx xxxx	uuuu uuuu
14h, Bank 3	CA2L	Capture2 Low Byte								xxxx xxxx	uuuu uuuu
15h, Bank 3	CA2H	Capture2 High Byte								xxxx xxxx	uuuu uuuu
12h, Bank 7	CA3L	Capture3 Low Byte								xxxx xxxx	uuuu uuuu
13h, Bank 7	CA3H	Capture3 High Byte								xxxx xxxx	uuuu uuuu
14h, Bank 7	CA4L	Capture4 Low Byte								xxxx xxxx	uuuu uuuu
15h, Bank 7	CA4H	Capture4 High Byte								xxxx xxxx	uuuu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0', q = value depends on condition.
Shaded cells are not used by Capture.

PIC17C7XX

Steps to follow when setting up an Asynchronous Reception:

1. Initialize the SPBRG register for the appropriate baud rate.
2. Enable the asynchronous serial port by clearing the SYNC bit and setting the SPEN bit.
3. If interrupts are desired, then set the RCIE bit.
4. If 9-bit reception is desired, then set the RX9 bit.
5. Enable the reception by setting the CREN bit.
6. The RCIF bit will be set when reception completes and an interrupt will be generated if the RCIE bit was set.

7. Read RCSTA to get the ninth bit (if enabled) and FERR bit to determine if any error occurred during reception.
8. Read RCREG for the 8-bit received data.
9. If an overrun error occurred, clear the error by clearing the OERR bit.

Note: To terminate a reception, either clear the SREN and CREN bits, or the SPEN bit. This will reset the receive logic, so that it will be in the proper state when receive is re-enabled.

FIGURE 14-7: ASYNCHRONOUS RECEPTION

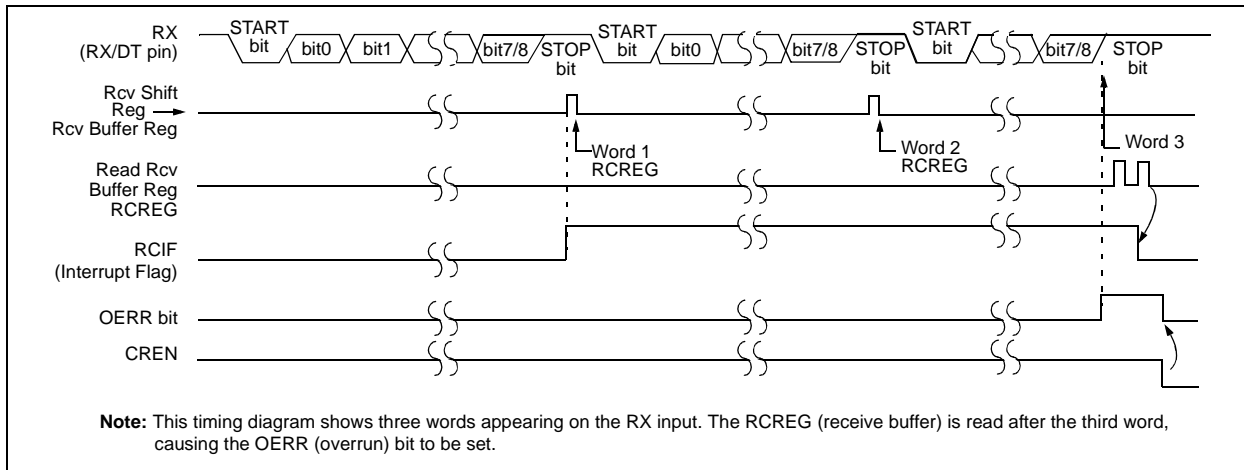


TABLE 14-7: REGISTERS ASSOCIATED WITH ASYNCHRONOUS RECEPTION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	MCLR, WDT
16h, Bank 1	PIR1	RBIF	TMR3IF	TMR2IF	TMR1IF	CA2IF	CA1IF	TX1IF	RC1IF	x000 0010	u000 0010
17h, Bank 1	PIE1	RBIE	TMR3IE	TMR2IE	TMR1IE	CA2IE	CA1IE	TX1IE	RC1IE	0000 0000	0000 0000
13h, Bank 0	RCSTA1	SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D	0000 -00x	0000 -00u
14h, Bank 0	RCREG1	RX7	RX6	RX5	RX4	RX3	RX2	RX1	RX0	xxxx xxxx	uuuu uuuu
15h, Bank 0	TXSTA1	CSRC	TX9	TXEN	SYNC	—	—	TRMT	TX9D	0000 --1x	0000 --1u
17h, Bank 0	SPBRG1	Baud Rate Generator Register								0000 0000	0000 0000
10h, Bank 4	PIR2	SSPIF	BCLIF	ADIF	—	CA4IF	CA3IF	TX2IF	RC2IF	000- 0010	000- 0010
11h, Bank 4	PIE2	SSPIE	BCLIE	ADIE	—	CA4IE	CA3IE	TX2IE	RC2IE	000- 0000	000- 0000
13h, Bank 4	RCSTA2	SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D	0000 -00x	0000 -00u
14h, Bank 4	RCREG2	RX7	RX6	RX5	RX4	RX3	RX2	RX1	RX0	xxxx xxxx	uuuu uuuu
15h, Bank 4	TXSTA2	CSRC	TX9	TXEN	SYNC	—	—	TRMT	TX9D	0000 --1x	0000 --1u
17h, Bank 4	SPBRG2	Baud Rate Generator Register								0000 0000	0000 0000

Legend: x = unknown, u = unchanged, - = unimplemented, read as a '0'. Shaded cells are not used for asynchronous reception.

14.3.2 USART SYNCHRONOUS MASTER RECEPTION

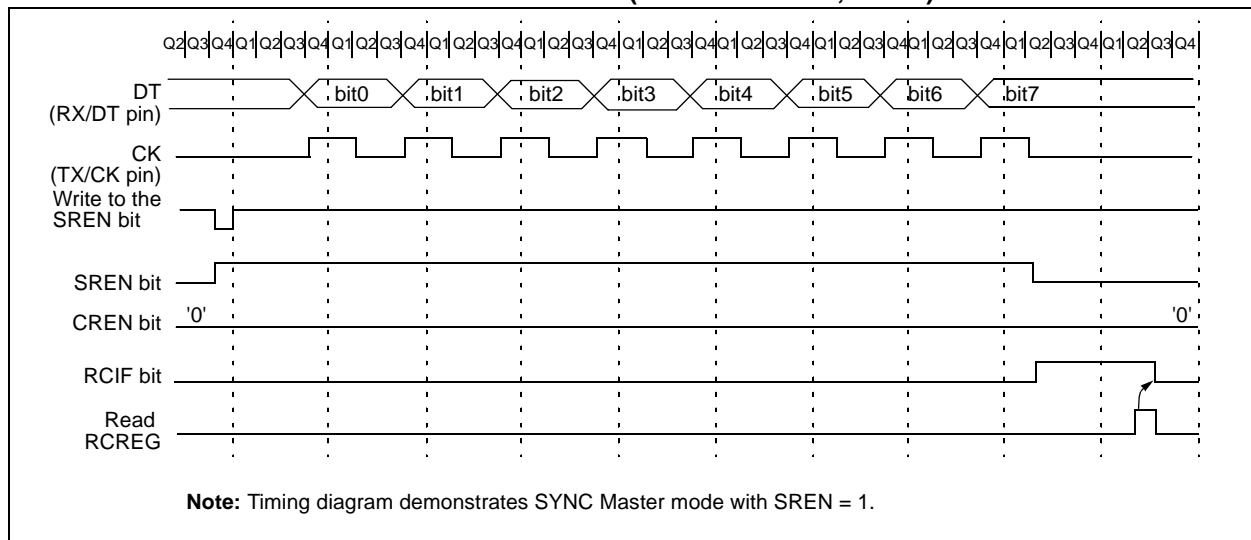
Once Synchronous mode is selected, reception is enabled by setting either the SREN (RCSTA<5>) bit or the CREN (RCSTA<4>) bit. Data is sampled on the RX/DT pin on the falling edge of the clock. If SREN is set, then only a single word is received. If CREN is set, the reception is continuous until CREN is reset. If both bits are set, then CREN takes precedence. After clocking the last bit, the received data in the Receive Shift Register (RSR) is transferred to RCREG (if it is empty). If the transfer is complete, the interrupt bit RCIF is set. The actual interrupt can be enabled/disabled by setting/clearing the RCIE bit. RCIF is a read only bit which is reset by the hardware. In this case, it is reset when RCREG has been read and is empty. RCREG is a double buffered register; i.e., it is a two deep FIFO. It is possible for two bytes of data to be received and transferred to the RCREG FIFO and a third byte to begin shifting into the RSR. On the clocking of the last bit of the third byte, if RCREG is still full, then the overrun error bit OERR (RCSTA<1>) is set. The word in the RSR will be lost. RCREG can be read twice to retrieve the two bytes in the FIFO. The OERR bit has to be cleared in software. This is done by clearing the CREN bit. If OERR is set, transfers from RSR to RCREG are inhibited, so it is essential to clear the OERR bit if it is set. The 9th receive bit is buffered the same way as the receive data. Reading the RCREG register will allow the RX9D and FERR bits to be loaded with values for the next received data; therefore, it is essential for the user to read the RCSTA register before reading RCREG in order not to lose the old FERR and RX9D information.

Steps to follow when setting up a Synchronous Master Reception:

1. Initialize the SPBRG register for the appropriate baud rate. See Section 14.1 for details.
2. Enable the synchronous master serial port by setting bits SYNC, SPEN, and CSRC.
3. If interrupts are desired, then set the RCIE bit.
4. If 9-bit reception is desired, then set the RX9 bit.
5. If a single reception is required, set bit SREN. For continuous reception set bit CREN.
6. The RCIF bit will be set when reception is complete and an interrupt will be generated if the RCIE bit was set.
7. Read RCSTA to get the ninth bit (if enabled) and determine if any error occurred during reception.
8. Read the 8-bit received data by reading RCREG.
9. If any error occurred, clear the error by clearing CREN.

Note: To terminate a reception, either clear the SREN and CREN bits, or the SPEN bit. This will reset the receive logic so that it will be in the proper state when receive is re-enabled.

FIGURE 14-10: SYNCHRONOUS RECEPTION (MASTER MODE, SREN)



PIC17C7XX

The SSPSTAT register gives the status of the data transfer. This information includes detection of a START or STOP bit, specifies if the received byte was data or address if the next byte is the completion of 10-bit address and if this will be a read or write data transfer.

The SSPBUF is the register to which transfer data is written to or read from. The SSPSR register shifts the data in or out of the device. In receive operations, the SSPBUF and SSPSR create a doubled buffered receiver. This allows reception of the next byte to begin before reading the last byte of received data. When the complete byte is received, it is transferred to the SSPBUF register and flag bit SSPIF is set. If another complete byte is received before the SSPBUF register is read, a receiver overflow has occurred and bit SSPOV (SSPCON1<6>) is set and the byte in the SSPSR is lost.

The SSPADD register holds the slave address. In 10-bit mode, the user needs to write the high byte of the address (1111 0 A9 A8 0). Following the high byte address match, the low byte of the address needs to be loaded (A7:A0).

15.2.1 SLAVE MODE

In Slave mode, the SCL and SDA pins must be configured as inputs. The MSSP module will override the input state with the output data when required (slave-transmitter).

When an address is matched or the data transfer after an address match is received, the hardware automatically will generate the acknowledge ($\overline{\text{ACK}}$) pulse and then load the SSPBUF register with the received value currently in the SSPSR register.

There are certain conditions that will cause the MSSP module not to give this $\overline{\text{ACK}}$ pulse. These are if either (or both):

- a) The buffer full bit BF (SSPSTAT<0>) was set before the transfer was received.
- b) The overflow bit SSPOV (SSPCON1<6>) was set before the transfer was received.

If the BF bit is set, the SSPSR register value is not loaded into the SSPBUF, but bit SSPIF and SSPOV are set. Table 15-2 shows what happens when a data transfer byte is received, given the status of bits BF and SSPOV. The shaded cells show the condition where user software did not properly clear the overflow condition. Flag bit BF is cleared by reading the SSPBUF register, while bit SSPOV is cleared through software.

The SCL clock input must have a minimum high and low time for proper operation. The high and low times of the I²C specification, as well as the requirement of the MSSP module, are shown in timing parameter #100 and parameter #101 of the Electrical Specifications.

15.2.1.1 Addressing

Once the MSSP module has been enabled, it waits for a START condition to occur. Following the START condition, the 8-bits are shifted into the SSPSR register. All incoming bits are sampled with the rising edge of the clock (SCL) line. The value of register SSPSR<7:1> is compared to the value of the SSPADD register. The address is compared on the falling edge of the eighth clock (SCL) pulse. If the addresses match and the BF and SSPOV bits are clear, the following events occur:

- The SSPSR register value is loaded into the SSPBUF register on the falling edge of the 8th SCL pulse.
- The buffer full bit, BF, is set on the falling edge of the 8th SCL pulse.
- An $\overline{\text{ACK}}$ pulse is generated.
- SSP interrupt flag bit, SSPIF (PIR2<7>), is set (interrupt is generated if enabled) - on the falling edge of the 9th SCL pulse.

In 10-bit address mode, two address bytes need to be received by the slave. The five Most Significant bits (MSBs) of the first address byte specify if this is a 10-bit address. Bit R/W (SSPSTAT<2>) must specify a write so the slave device will receive the second address byte. For a 10-bit address, the first byte would equal '1111 0 A9 A8 0', where A9 and A8 are the two MSBs of the address. The sequence of events for a 10-bit address is as follows, with steps 7- 9 for slave-transmitter:

- Receive first (high) byte of Address (bits SSPIF, BF and bit UA (SSPSTAT<1>) are set).
- Update the SSPADD register with second (low) byte of Address (clears bit UA and releases the SCL line).
- Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.
- Receive second (low) byte of Address (bits SSPIF, BF and UA are set).

- Update the SSPADD register with the first (high) byte of Address. This will clear bit UA and release the SCL line.
- Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.
- Receive Repeated Start condition.
- Receive first (high) byte of Address (bits SSPIF and BF are set).
- Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.

Note: Following the Repeated Start condition (step 7) in 10-bit mode, the user only needs to match the first 7-bit address. The user does not update the SSPADD for the second half of the address.

15.2.1.2 Slave Reception

When the R/W bit of the address byte is clear and an address match occurs, the R/W bit of the SSPSTAT register is cleared. The received address is loaded into the SSPBUF register.

When the address byte overflow condition exists, then no acknowledge (ACK) pulse is given. An overflow condition is defined as either bit BF (SSPSTAT<0>) is set, or bit SSPOV (SSPCON1<6>) is set.

An SSP interrupt is generated for each data transfer byte. Flag bit SSPIF (PIR2<7>) must be cleared in software. The SSPSTAT register is used to determine the status of the received byte.

Note: The SSPBUF will be loaded if the SSPOV bit is set and the BF flag is cleared. If a read of the SSPBUF was performed, but the user did not clear the state of the SSPOV bit before the next receive occurred, the $\overline{\text{ACK}}$ is not sent and the SSPBUF is updated.

TABLE 15-2: DATA TRANSFER RECEIVED BYTE ACTIONS

Status Bits as Data Transfer is Received		SSPSR → SSPBUF	Generate $\overline{\text{ACK}}$ Pulse	Set bit SSPIF (SSP Interrupt occurs if enabled)
BF	SSPOV			
0	0	Yes	Yes	Yes
1	0	No	No	Yes
1	1	No	No	Yes
0	1	Yes	No	Yes

Note 1: Shaded cells show the conditions where the user software did not properly clear the overflow condition.

PIC17C7XX

15.2.3 SLEEP OPERATION

While in SLEEP mode, the I²C module can receive addresses or data and when an address match or complete byte transfer occurs, wake the processor from SLEEP (if the SSP interrupt is enabled).

15.2.4 EFFECTS OF A RESET

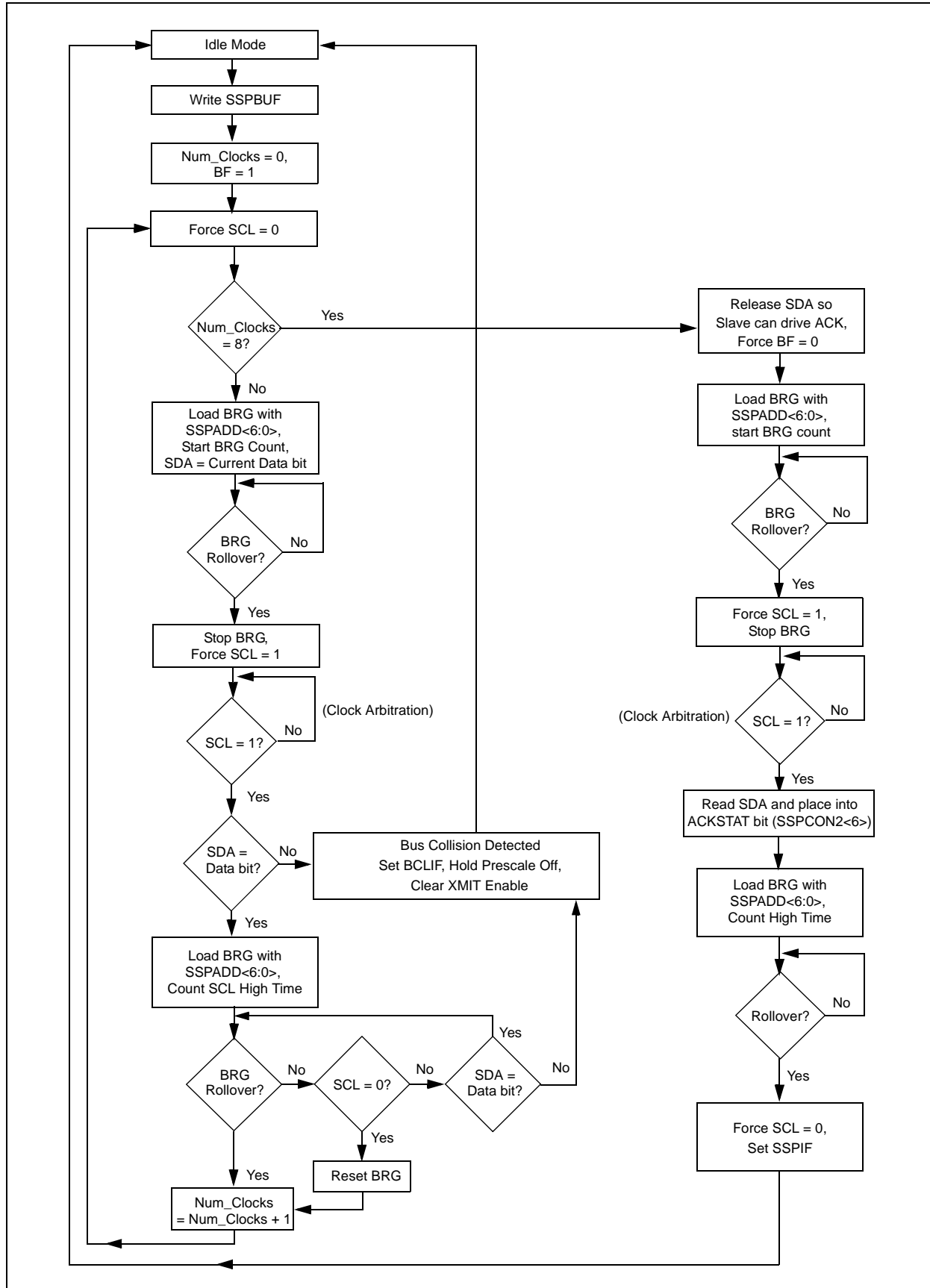
A RESET disables the SSP module and terminates the current transfer.

TABLE 15-3: REGISTERS ASSOCIATED WITH I²C OPERATION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR, BOR	MCLR, WDT
07h, Unbanked	INTSTA	PEIF	T0CKIF	T0IF	INTF	PEIE	T0CKIE	T0IE	INTE	0000 0000	0000 0000
10h, Bank 4	PIR2	SSPIF	BCLIF	ADIF	—	CA4IF	CA3IF	TX2IF	RC2IF	000- 0000	000- 0000
11h, Bank 4	PIE2	SSPIE	BCLIE	ADIE	—	CA4IE	CA3IE	TX2IE	RC2IE	000- 0000	000- 0000
10h, Bank 6	SSPADD	Synchronous Serial Port (I ² C mode) Address Register								0000 0000	0000 0000
14h, Bank 6	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register								xxxx xxxx	uuuu uuuu
11h, Bank 6	SSPCON1	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
12h, Bank 6	SSPCON2	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	0000 0000	0000 0000
13h, Bank 6	SSPSTAT	SMP	CKE	D/ \bar{A}	P	S	R/ \bar{W}	UA	BF	0000 0000	0000 0000

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by the SSP in I²C mode.

FIGURE 15-25: MASTER TRANSMIT FLOW CHART



18.2 Q Cycle Activity

Each instruction cycle (Tcy) is comprised of four Q cycles (Q1-Q4). The Q cycle is the same as the device oscillator cycle (Tosc). The Q cycles provide the timing/designation for the Decode, Read, Process Data, Write, etc., of each instruction cycle. The following diagram shows the relationship of the Q cycles to the instruction cycle.

The four Q cycles that make up an instruction cycle (Tcy) can be generalized as:

Q1: Instruction Decode Cycle or forced No operation

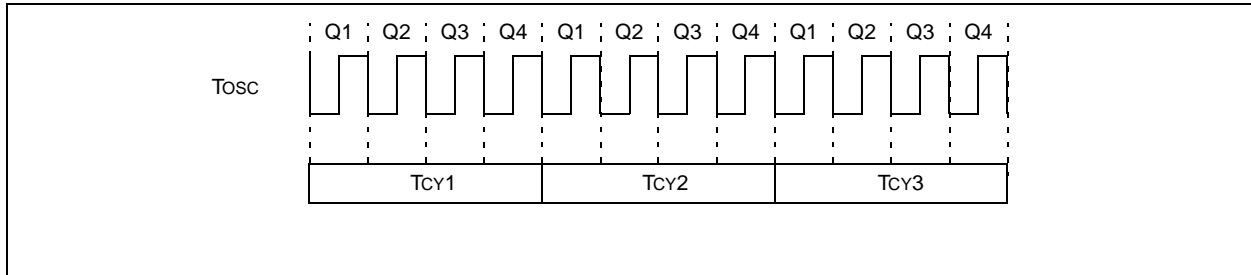
Q2: Instruction Read Cycle or No operation

Q3: Process the Data

Q4: Instruction Write Cycle or No operation

Each instruction will show the detailed Q cycle operation for the instruction.

FIGURE 18-2: Q CYCLE ACTIVITY



PIC17C7XX

TABLE 18-2: PIC17CXXX INSTRUCTION SET

Mnemonic, Operands	Description	Cycles	16-bit Opcode				Status Affected	Notes	
			MSb		LSb				
BYTE-ORIENTED FILE REGISTER OPERATIONS									
ADDWF f,d	ADD WREG to f	1	0000	111d	ffff	ffff	OV,C,DC,Z		
ADDWFC f,d	ADD WREG and Carry bit to f	1	0001	000d	ffff	ffff	OV,C,DC,Z		
ANDWF f,d	AND WREG with f	1	0000	101d	ffff	ffff	Z		
CLRF f,s	Clear f, or Clear f and Clear WREG	1	0010	100s	ffff	ffff	None	3	
COMF f,d	Complement f	1	0001	001d	ffff	ffff	Z		
CPFSEQ f	Compare f with WREG, skip if f = WREG	1 (2)	0011	0001	ffff	ffff	None	6,8	
CPFSGT f	Compare f with WREG, skip if f > WREG	1 (2)	0011	0010	ffff	ffff	None	2,6,8	
CPFSLT f	Compare f with WREG, skip if f < WREG	1 (2)	0011	0000	ffff	ffff	None	2,6,8	
DAW f,s	Decimal Adjust WREG Register	1	0010	111s	ffff	ffff	C	3	
DECf f,d	Decrement f	1	0000	011d	ffff	ffff	OV,C,DC,Z		
DECFSZ f,d	Decrement f, skip if 0	1 (2)	0001	011d	ffff	ffff	None	6,8	
DCFSNZ f,d	Decrement f, skip if not 0	1 (2)	0010	011d	ffff	ffff	None	6,8	
INCF f,d	Increment f	1	0001	010d	ffff	ffff	OV,C,DC,Z		
INCFSZ f,d	Increment f, skip if 0	1 (2)	0001	111d	ffff	ffff	None	6,8	
INFSNZ f,d	Increment f, skip if not 0	1 (2)	0010	010d	ffff	ffff	None	6,8	
IORWF f,d	Inclusive OR WREG with f	1	0000	100d	ffff	ffff	Z		
MOVFP f,p	Move f to p	1	011p	pppp	ffff	ffff	None		
MOVPF p,f	Move p to f	1	010p	pppp	ffff	ffff	Z		
MOVWF f	Move WREG to f	1	0000	0001	ffff	ffff	None		
MULWF f	Multiply WREG with f	1	0011	0100	ffff	ffff	None		
NEGf f,s	Negate WREG	1	0010	110s	ffff	ffff	OV,C,DC,Z	1,3	
NOP —	No Operation	1	0000	0000	0000	0000	None		
RLCF f,d	Rotate left f through Carry	1	0001	101d	ffff	ffff	C		
RLNCF f,d	Rotate left f (no carry)	1	0010	001d	ffff	ffff	None		
RRCF f,d	Rotate right f through Carry	1	0001	100d	ffff	ffff	C		
RRNCF f,d	Rotate right f (no carry)	1	0010	000d	ffff	ffff	None		
SETf f,s	Set f	1	0010	101s	ffff	ffff	None	3	
SUBWF f,d	Subtract WREG from f	1	0000	010d	ffff	ffff	OV,C,DC,Z	1	
SUBWFB f,d	Subtract WREG from f with Borrow	1	0000	001d	ffff	ffff	OV,C,DC,Z	1	
SWAPf f,d	Swap f	1	0001	110d	ffff	ffff	None		
TABLRD t,i,f	Table Read	2 (3)	1010	10ti	ffff	ffff	None	7	
TABLWT t,i,f	Table Write	2	1010	11ti	ffff	ffff	None	5	
TLRD t,f	Table Latch Read	1	1010	00tx	ffff	ffff	None		
TLWT t,f	Table Latch Write	1	1010	01tx	ffff	ffff	None		

Legend: Refer to Table 18-1 for opcode field descriptions.

Note 1: 2's Complement method.

2: Unsigned arithmetic.

3: If s = '1', only the file is affected: If s = '0', both the WREG register and the file are affected; If only the Working register (WREG) is required to be affected, then f = WREG must be specified.

4: During an LCALL, the contents of PCLATH are loaded into the MSB of the PC and kkkk kkkk is loaded into the LSB of the PC (PCL).

5: Multiple cycle instruction for EPROM programming when table pointer selects internal EPROM. The instruction is terminated by an interrupt event. When writing to external program memory, it is a two-cycle instruction.

6: Two-cycle instruction when condition is true, else single cycle instruction.

7: Two-cycle instruction except for TABLRD to PCL (program counter low byte), in which case it takes 3 cycles.

8: A "skip" means that instruction fetched during execution of current instruction is not executed, instead a NOP is executed.

21.0 PIC17C7XX DC AND AC CHARACTERISTICS

The graphs and tables provided in this section are for design guidance and are not tested nor guaranteed. In some graphs or tables the data presented is outside specified operating range (e.g., outside specified V_{DD} range). This is for information only and devices are ensured to operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time.

- **Typ** or **Typical** represents the mean of the distribution at 25°C.
- **Max** or **Maximum** represents (mean + 3 σ) over the temperature range of -40°C to 85°C.
- **Min** or **Minimum** represents (mean - 3 σ) over the temperature range of -40°C to 85°C.

Note: Standard deviation is denoted by sigma (σ).

TABLE 21-1: PIN CAPACITANCE PER PACKAGE TYPE

Pin Name	Typical Capacitance (pF)	
	68-pin PLCC	64-pin TQFP
All pins, except \overline{MCLR} , V_{DD} , and V_{SS}	10	10
\overline{MCLR} pin	20	20

FIGURE 21-1: TYPICAL RC OSCILLATOR FREQUENCY vs. TEMPERATURE

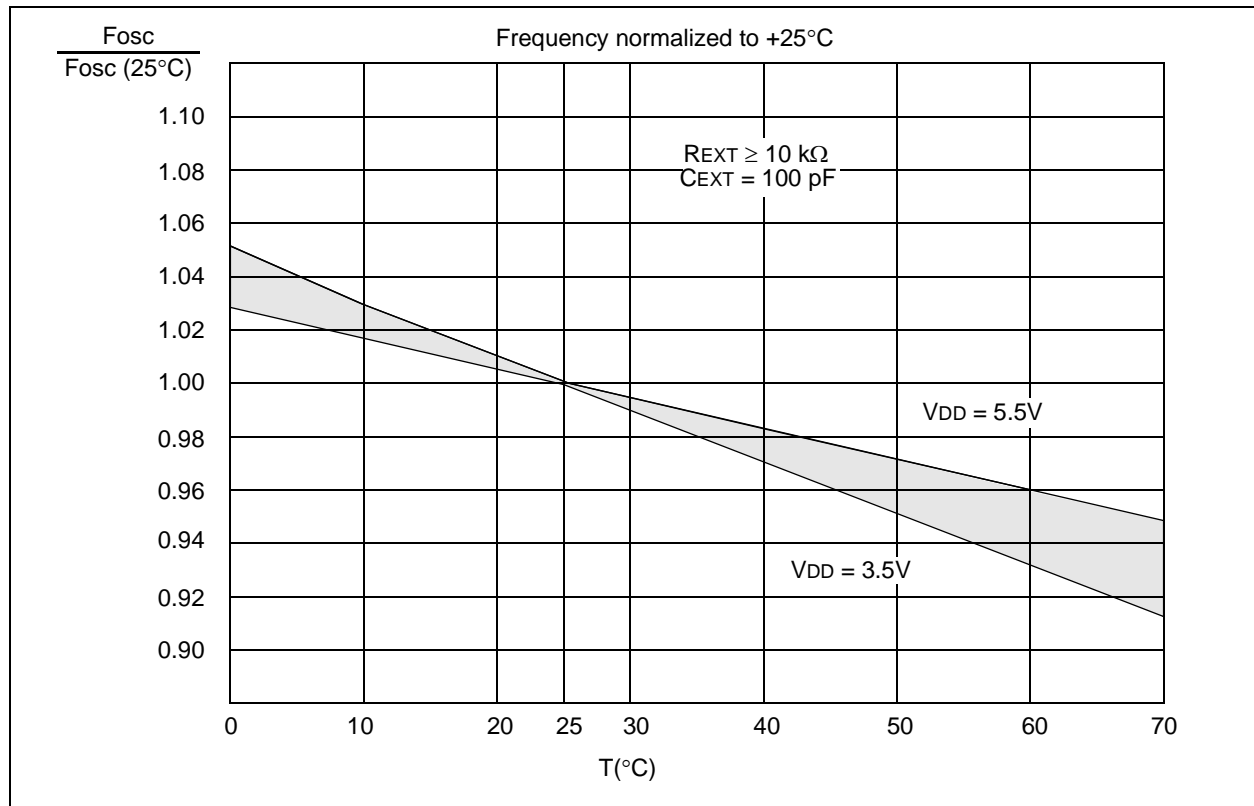


FIGURE 21-4: TYPICAL RC OSCILLATOR FREQUENCY vs. V_{DD}

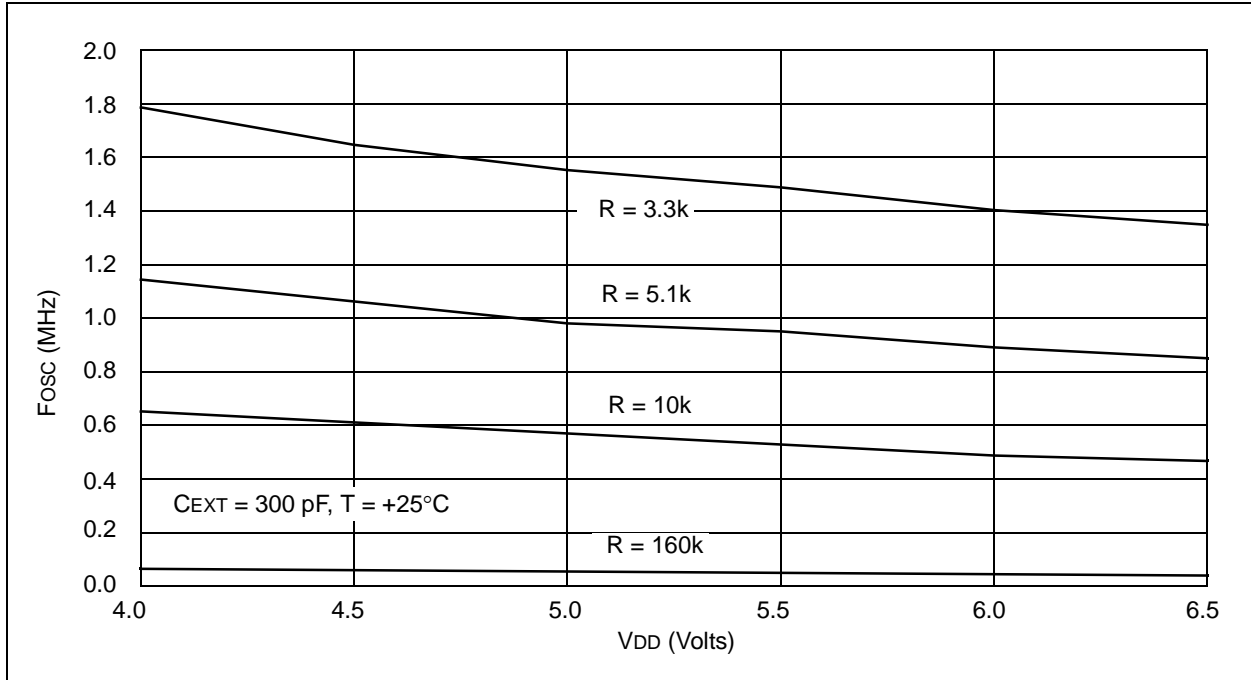


TABLE 21-2: RC OSCILLATOR FREQUENCIES

C _{EXT}	R _{EXT}	Average F _{osc} @ 5V, +25°C	
22 pF	10k	3.33 MHz	± 12%
	100k	353 kHz	± 13%
100 pF	3.3k	3.54 MHz	± 10%
	5.1k	2.43 MHz	± 14%
	10k	1.30 MHz	± 17%
	100k	129 kHz	± 10%
300 pF	3.3k	1.54 MHz	± 14%
	5.1k	980 kHz	± 12%
	10k	564 kHz	± 16%
	160k	35 kHz	± 18%

PIC17C7XX

FIGURE 21-5: TRANSCONDUCTANCE (gm) OF LF OSCILLATOR vs. VDD

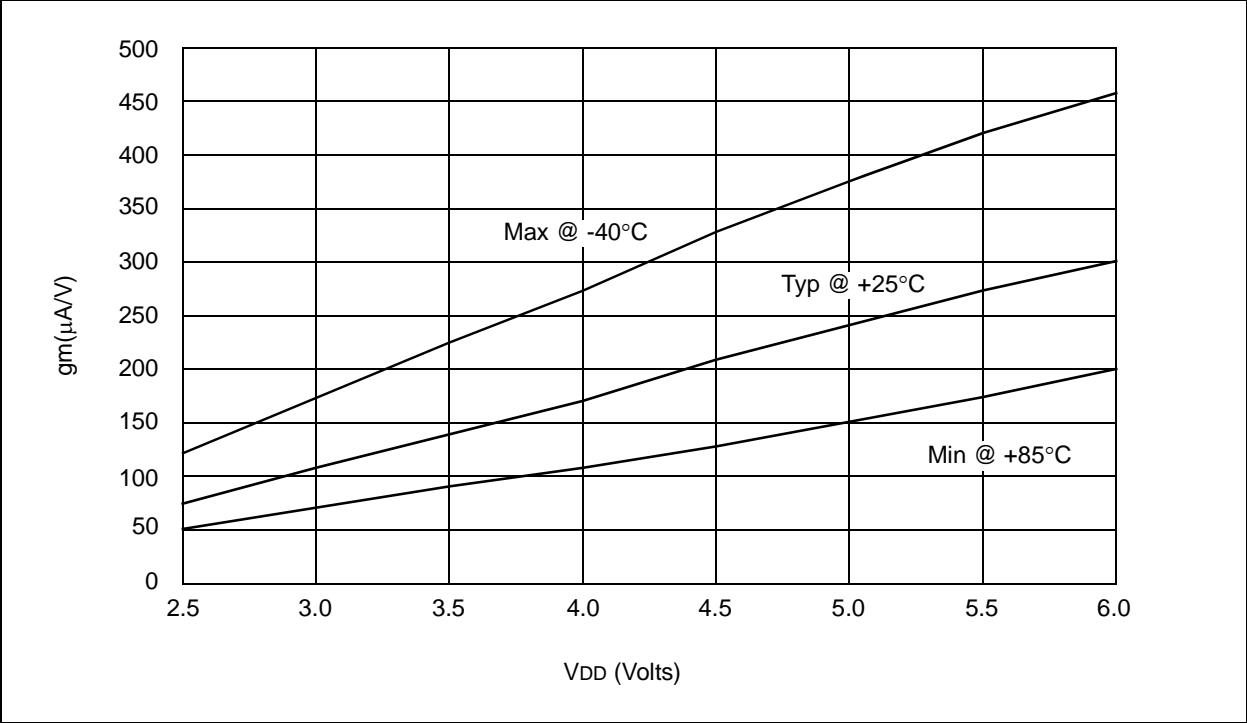


FIGURE 21-6: TRANSCONDUCTANCE (gm) OF XT OSCILLATOR vs. VDD

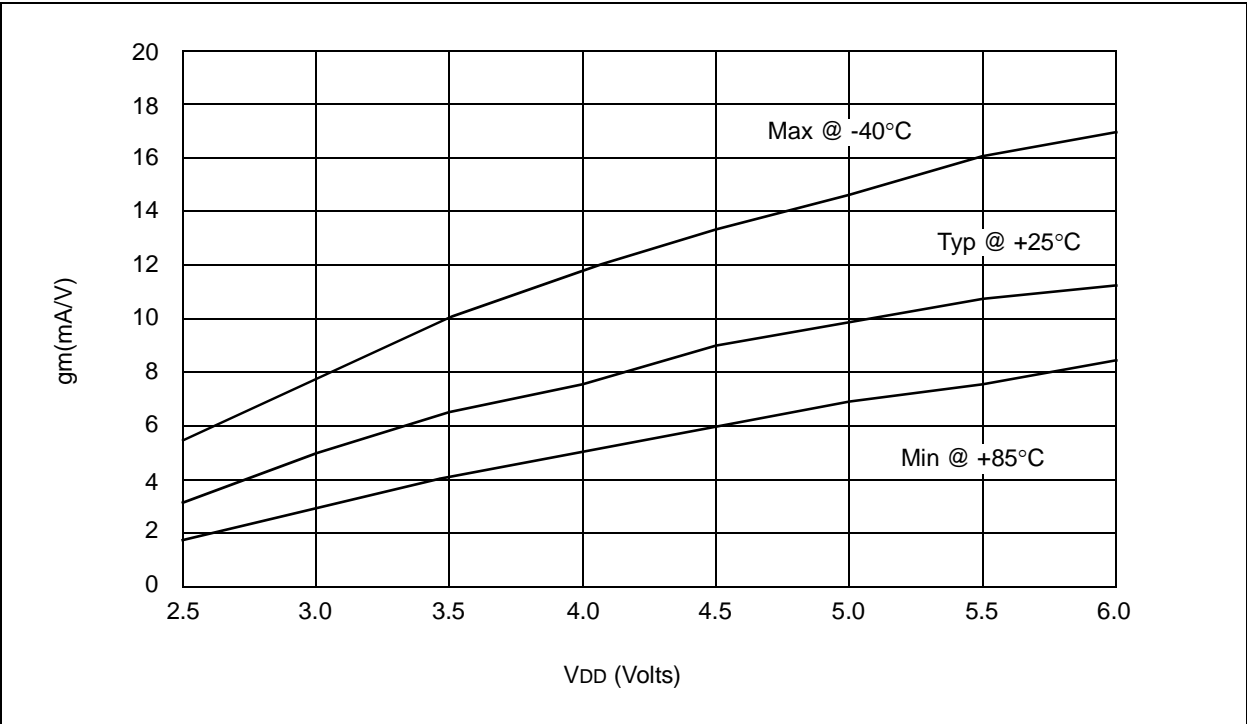


FIGURE 21-7: TYPICAL I_{DD} vs. F_{osc} OVER V_{DD} (LF MODE)

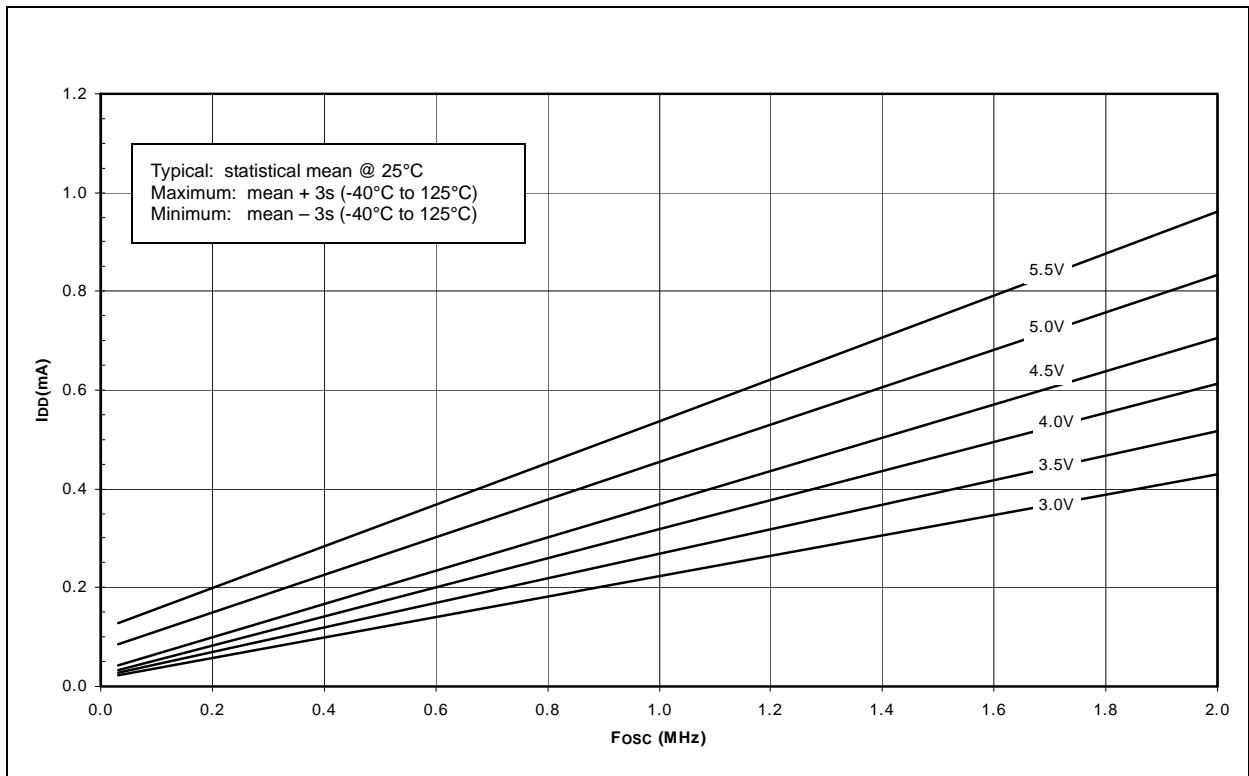


FIGURE 21-8: MAXIMUM I_{DD} vs. F_{osc} OVER V_{DD} (LF MODE)

