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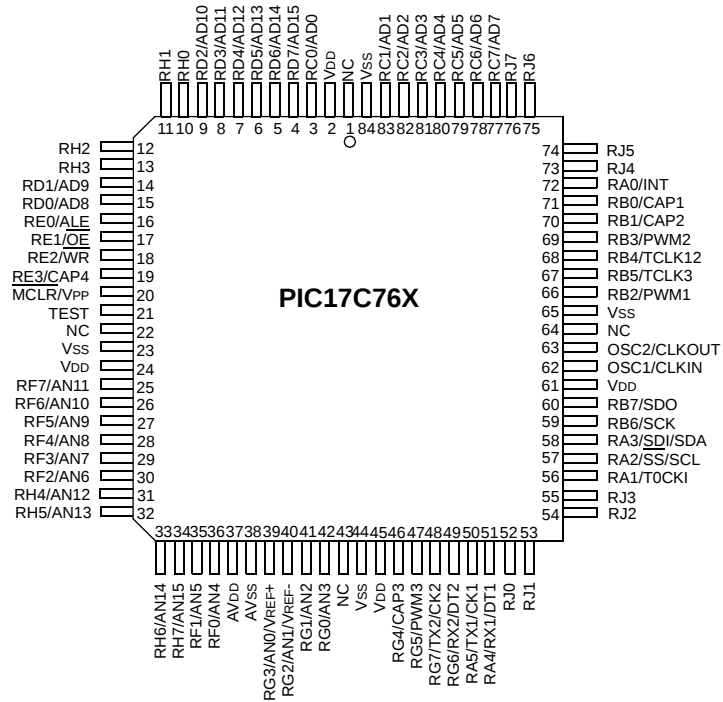
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Details

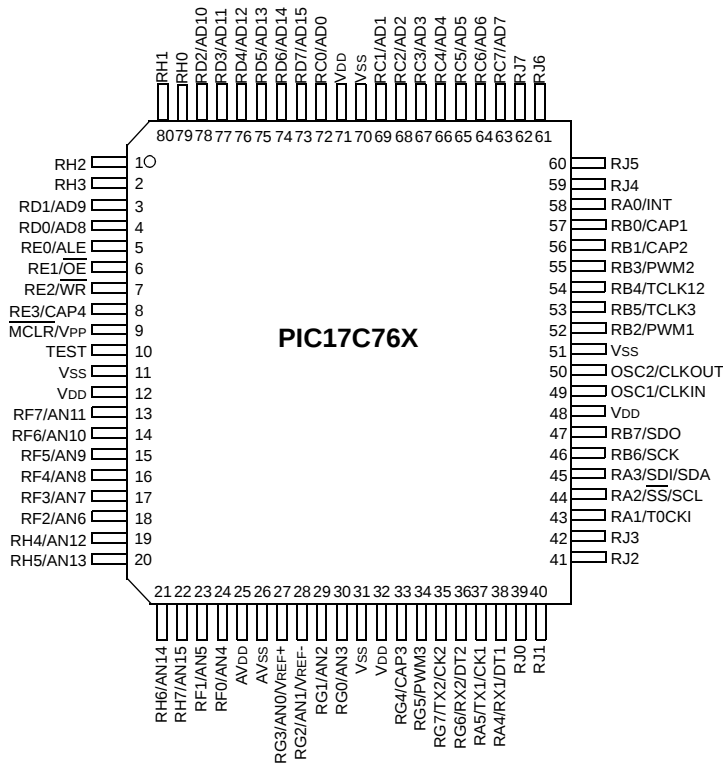
Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	16MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	50
Program Memory Size	16KB (8K x 16)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	454 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	68-LCC (J-Lead)
Supplier Device Package	68-PLCC (24.23x24.23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic17c752t-16-l

Pin Diagrams cont.'d

84-pin PLCC



80-Pin TQFP

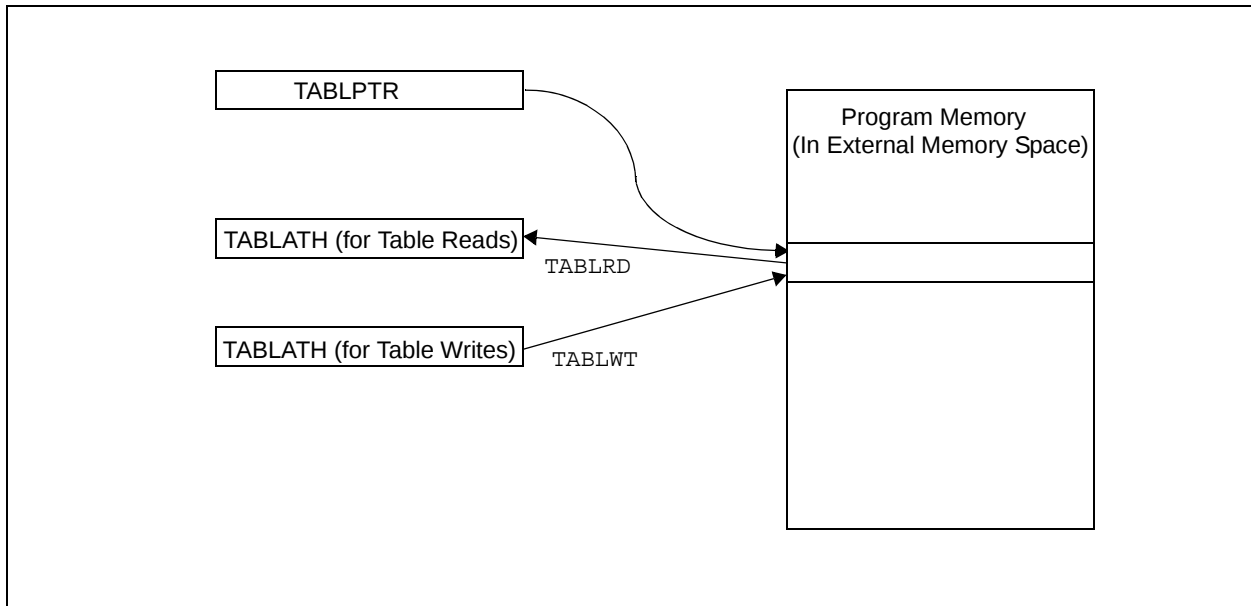


8.4 Operation with External Memory Interface

When the table reads/writes are accessing external memory (via the external system interface bus), the table latch for the table reads is different from the table latch for the table writes (see Figure 8-9).

This means that you cannot do a `TABLWD` instruction, and use the values that were loaded into the table latches for a `TABLWT` instruction. Any table write sequence should use both the `TLWT` and then the `TABLWT` instructions.

FIGURE 8-9: ACCESSING EXTERNAL MEMORY WITH `TABLWD` AND `TABLWT` INSTRUCTIONS



Example 10-2 shows an instruction sequence to initialize PORTB. The Bank Select Register (BSR) must be selected to Bank 0 for the port to be initialized. The following example uses the MOVLB instruction to load the BSR register for bank selection.

EXAMPLE 10-2: INITIALIZING PORTB

```
MOVLB  0      ; Select Bank 0
CLRF   PORTB, F ; Init PORTB by clearing
                ; output data latches
MOVLW  0xCF    ; Value used to initialize
                ; data direction
MOVWF  DDRB    ; Set RB<3:0> as inputs
                ; RB<5:4> as outputs
                ; RB<7:6> as inputs
```

FIGURE 10-6: BLOCK DIAGRAM OF RB3:RB2 PORT PINS

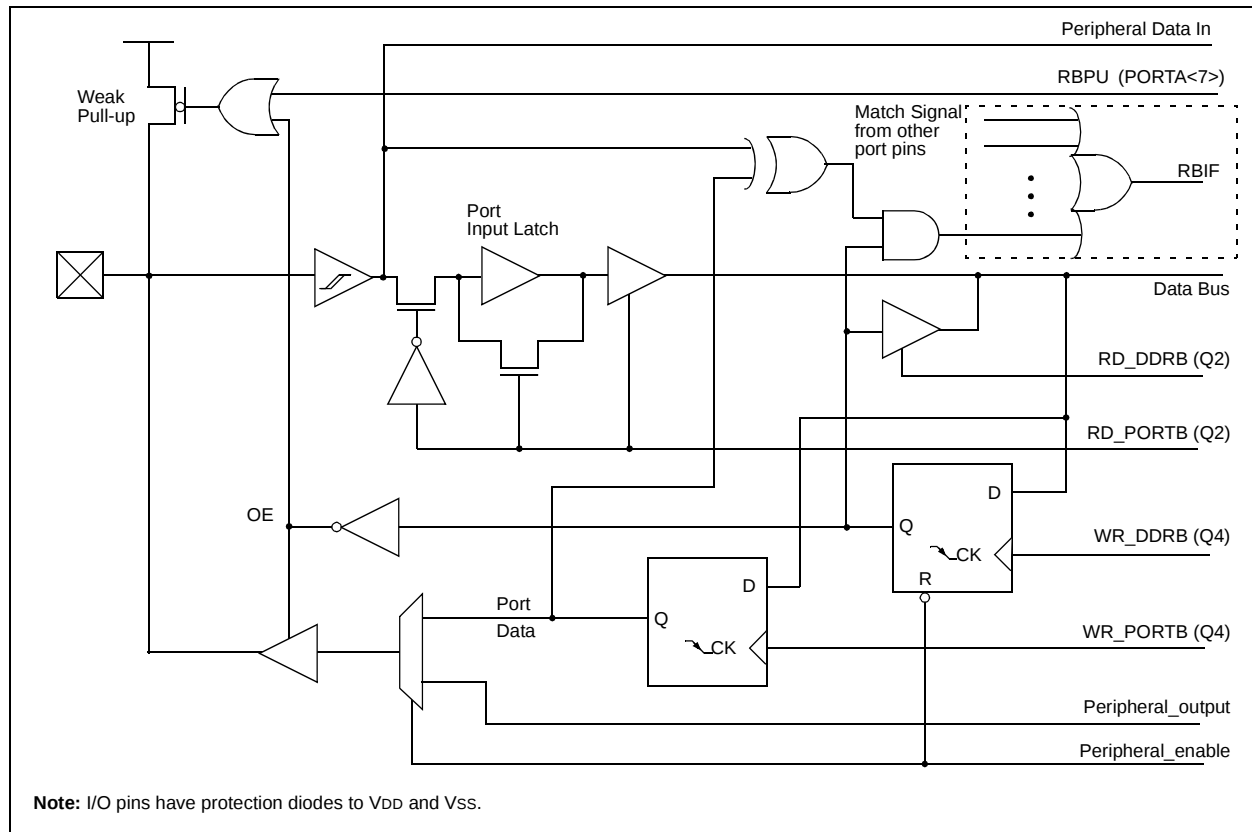


TABLE 10-5: PORTC FUNCTIONS

Name	Bit	Buffer Type	Function
RC0/AD0	bit0	TTL	Input/output or system bus address/data pin.
RC1/AD1	bit1	TTL	Input/output or system bus address/data pin.
RC2/AD2	bit2	TTL	Input/output or system bus address/data pin.
RC3/AD3	bit3	TTL	Input/output or system bus address/data pin.
RC4/AD4	bit4	TTL	Input/output or system bus address/data pin.
RC5/AD5	bit5	TTL	Input/output or system bus address/data pin.
RC6/AD6	bit6	TTL	Input/output or system bus address/data pin.
RC7/AD7	bit7	TTL	Input/output or system bus address/data pin.

Legend: TTL = TTL input

TABLE 10-6: REGISTERS/BITS ASSOCIATED WITH PORTC

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	MCLR, WDT
11h, Bank 1	PORTC	RC7/ AD7	RC6/ AD6	RC5/ AD5	RC4/ AD4	RC3/ AD3	RC2/ AD2	RC1/ AD1	RC0/ AD0	xxxx xxxx	uuuu uuuu
10h, Bank 1	DDRC	Data Direction Register for PORTC								1111 1111	1111 1111

Legend: x = unknown, u = unchanged

TABLE 10-7: PORTD FUNCTIONS

Name	Bit	Buffer Type	Function
RD0/AD8	bit0	TTL	Input/output or system bus address/data pin.
RD1/AD9	bit1	TTL	Input/output or system bus address/data pin.
RD2/AD10	bit2	TTL	Input/output or system bus address/data pin.
RD3/AD11	bit3	TTL	Input/output or system bus address/data pin.
RD4/AD12	bit4	TTL	Input/output or system bus address/data pin.
RD5/AD13	bit5	TTL	Input/output or system bus address/data pin.
RD6/AD14	bit6	TTL	Input/output or system bus address/data pin.
RD7/AD15	bit7	TTL	Input/output or system bus address/data pin.

Legend: TTL = TTL input

TABLE 10-8: REGISTERS/BITS ASSOCIATED WITH PORTD

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	MCLR, WDT
13h, Bank 1	PORTD	RD7/ AD15	RD6/ AD14	RD5/ AD13	RD4/ AD12	RD3/ AD11	RD2/ AD10	RD1/ AD9	RD0/ AD8	xxxx xxxx	uuuu uuuu
12h, Bank 1	DDRD	Data Direction Register for PORTD								1111 1111	1111 1111

Legend: x = unknown, u = unchanged

TABLE 10-11: PORTF FUNCTIONS

Name	Bit	Buffer Type	Function
RF0/AN4	bit0	ST	Input/output or analog input 4.
RF1/AN5	bit1	ST	Input/output or analog input 5.
RF2/AN6	bit2	ST	Input/output or analog input 6.
RF3/AN7	bit3	ST	Input/output or analog input 7.
RF4/AN8	bit4	ST	Input/output or analog input 8.
RF5/AN9	bit5	ST	Input/output or analog input 9.
RF6/AN10	bit6	ST	Input/output or analog input 10.
RF7/AN11	bit7	ST	Input/output or analog input 11.

Legend: ST = Schmitt Trigger input

TABLE 10-12: REGISTERS/BITS ASSOCIATED WITH PORTF

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	MCLR, WDT
10h, Bank 5	DDRF	Data Direction Register for PORTF								1111 1111	1111 1111
11h, Bank 5	PORTF	RF7/ AN11	RF6/ AN10	RF5/ AN9	RF4/ AN8	RF3/ AN7	RF2/ AN6	RF1/ AN5	RF0/ AN4	0000 0000	0000 0000
15h, Bank 5	ADCON1	ADCS1	ADCS0	ADFM	—	PCFG3	PCFG2	PCFG1	PCFG0	000- 0000	000- 0000

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by PORTF.

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FIGURE 12-4: TMR0 READ/WRITE IN TIMER MODE

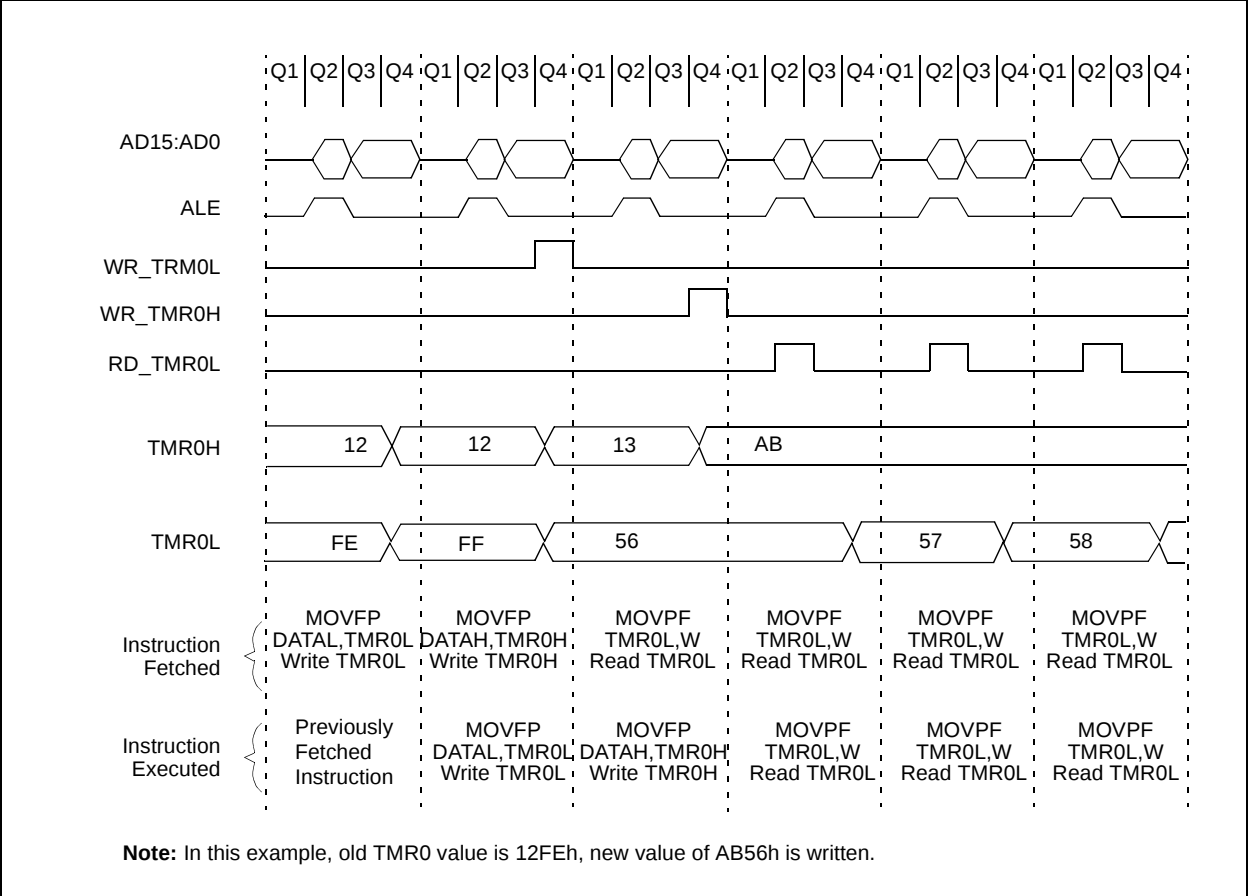


TABLE 12-1: REGISTERS/BITS ASSOCIATED WITH TIMER0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	MCLR, WDT
05h, Unbanked	T0STA	INTEDG	T0SE	T0CS	T0PS3	T0PS2	T0PS1	T0PS0	—	0000 000—	0000 000—
06h, Unbanked	CPUSTA	—	—	STKAV	GLINTD	T0	PD	POR	BOR	--11 11qq	--11 qquu
07h, Unbanked	INTSTA	PEIF	T0CKIF	T0IF	INTF	PEIE	T0CKIE	T0IE	INTE	0000 0000	0000 0000
0Bh, Unbanked	TMR0L	TMR0 Register; Low Byte								xxxx xxxx	uuuu uuuu
0Ch, Unbanked	TMR0H	TMR0 Register; High Byte								xxxx xxxx	uuuu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented, read as a '0', q = value depends on condition. Shaded cells are not used by Timer0.

13.0 TIMER1, TIMER2, TIMER3, PWMS AND CAPTURES

The PIC17C7XX has a wealth of timers and time based functions to ease the implementation of control applications. These time base functions include three PWM outputs and four Capture inputs.

Timer1 and Timer2 are two 8-bit incrementing timers, each with an 8-bit period register (PR1 and PR2, respectively) and separate overflow interrupt flags. Timer1 and Timer2 can operate either as timers (increment on internal $F_{osc}/4$ clock), or as counters (increment on falling edge of external clock on pin RB4/TCLK12). They are also software configurable to operate as a single 16-bit timer/counter. These timers are also used as the time base for the PWM (Pulse Width Modulation) modules.

Timer3 is a 16-bit timer/counter which uses the TMR3H and TMR3L registers. Timer3 also has two additional registers (PR3H/CA1H:PR3L/CA1L) that are configurable as a 16-bit period register or a 16-bit capture register. TMR3 can be software configured to increment from the internal system clock ($F_{osc}/4$), or from an external signal on the RB5/TCLK3 pin. Timer3 is the time base for all of the 16-bit captures.

Six other registers comprise the Capture2, Capture3, and Capture4 registers (CA2H:CA2L, CA3H:CA3L, and CA4H:CA4L).

Figure 13-1, Figure 13-2 and Figure 13-3 are the control registers for the operation of Timer1, Timer2 and Timer3, as well as PWM1, PWM2, PWM3, Capture1, Capture2, Capture3 and Capture4.

Table 13-1 shows the Timer resource requirements for these time base functions. Each timer is an open resource so that multiple functions may operate with it.

TABLE 13-1: TIME-BASE FUNCTION/ RESOURCE REQUIREMENTS

Time Base Function	Timer Resource
PWM1	Timer1
PWM2	Timer1 or Timer2
PWM3	Timer1 or Timer2
Capture1	Timer3
Capture2	Timer3
Capture3	Timer3
Capture4	Timer3

REGISTER 13-1: TCON1 REGISTER (ADDRESS: 16h, BANK 3)

	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	CA2ED1	CA2ED0	CA1ED1	CA1ED0	T16	TMR3CS	TMR2CS	TMR1CS
	bit 7							bit 0
bit 7-6	CA2ED1:CA2ED0: Capture2 Mode Select bits 00 = Capture on every falling edge 01 = Capture on every rising edge 10 = Capture on every 4th rising edge 11 = Capture on every 16th rising edge							
bit 5-4	CA1ED1:CA1ED0: Capture1 Mode Select bits 00 = Capture on every falling edge 01 = Capture on every rising edge 10 = Capture on every 4th rising edge 11 = Capture on every 16th rising edge							
bit 3	T16: Timer2:Timer1 Mode Select bit 1 = Timer2 and Timer1 form a 16-bit timer 0 = Timer2 and Timer1 are two 8-bit timers							
bit 2	TMR3CS: Timer3 Clock Source Select bit 1 = TMR3 increments off the falling edge of the RB5/TCLK3 pin 0 = TMR3 increments off the internal clock							
bit 1	TMR2CS: Timer2 Clock Source Select bit 1 = TMR2 increments off the falling edge of the RB4/TCLK12 pin 0 = TMR2 increments off the internal clock							
bit 0	TMR1CS: Timer1 Clock Source Select bit 1 = TMR1 increments off the falling edge of the RB4/TCLK12 pin 0 = TMR1 increments off the internal clock							

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR Reset	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

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13.2 Timer3

Timer3 is a 16-bit timer consisting of the TMR3H and TMR3L registers. TMR3H is the high byte of the timer and TMR3L is the low byte. This timer has an associated 16-bit period register (PR3H/CA1H:PR3L/CA1L). This period register can be software configured to be another 16-bit capture register.

When the TMR3CS bit (TCON1<2>) is clear, the timer increments every instruction cycle ($F_{osc}/4$). When TMR3CS is set, the counter increments on every falling edge of the RB5/TCLK3 pin. In either mode, the TMR3ON bit must be set for the timer/counter to increment. When TMR3ON is clear, the timer will not increment or set flag bit TMR3IF.

Timer3 has two modes of operation, depending on the CA1/PR3 bit (TCON2<3>). These modes are:

- Three capture and one period register mode
- Four capture register mode

The PIC17C7XX has up to four 16-bit capture registers that capture the 16-bit value of TMR3 when events are detected on capture pins. There are four capture pins

(RB0/CAP1, RB1/CAP2, RG4/CAP3, and RE3/CAP4), one for each capture register pair. The capture pins are multiplexed with the I/O pins. An event can be:

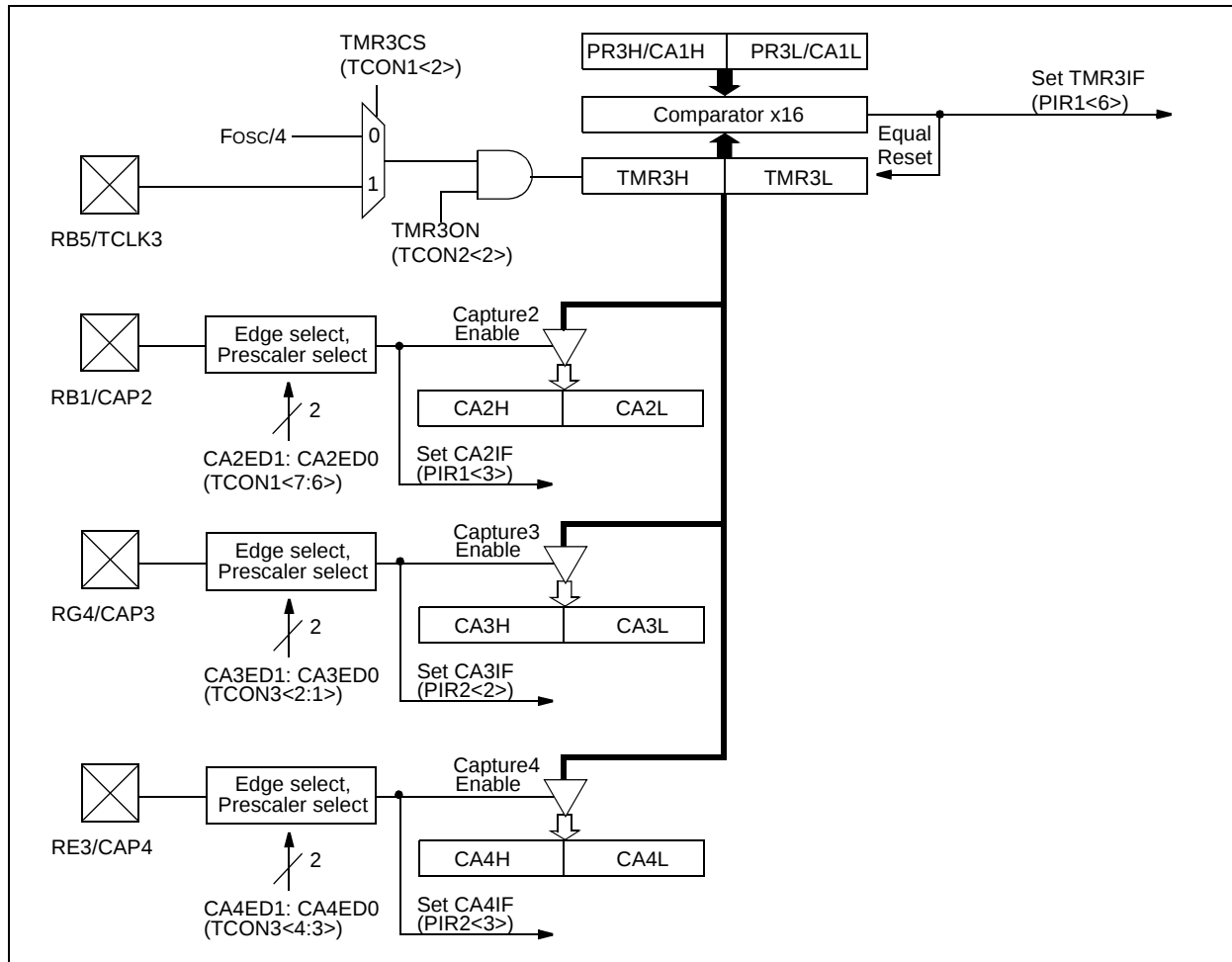
- A rising edge
- A falling edge
- Every 4th rising edge
- Every 16th rising edge

Each 16-bit capture register has an interrupt flag associated with it. The flag is set when a capture is made. The capture modules are truly part of the Timer3 block. Figure 13-5 and Figure 13-6 show the block diagrams for the two modes of operation.

13.2.1 THREE CAPTURE AND ONE PERIOD REGISTER MODE

In this mode, registers PR3H/CA1H and PR3L/CA1L constitute a 16-bit period register. A block diagram is shown in Figure 13-5. The timer increments until it equals the period register and then resets to 0000h on the next timer clock. TMR3 Interrupt Flag bit (TMR3IF) is set at this point. This interrupt can be disabled by clearing the TMR3 Interrupt Enable bit (TMR3IE). TMR3IF must be cleared in software.

FIGURE 13-5: TIMER3 WITH THREE CAPTURE AND ONE PERIOD REGISTER BLOCK DIAGRAM



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NOTES:

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TABLE 14-5: BAUD RATES FOR ASYNCHRONOUS MODE

BAUD RATE (K)	FOSC = 33 MHz			FOSC = 25 MHz			FOSC = 20 MHz			FOSC = 16 MHz		
	KBAUD	%ERROR	SPBRG VALUE (DECIMAL)	KBAUD	%ERROR	SPBRG VALUE (DECIMAL)	KBAUD	%ERROR	SPBRG VALUE (DECIMAL)	KBAUD	%ERROR	SPBRG VALUE (DECIMAL)
0.3	NA	—	—	NA	—	—	NA	—	—	NA	—	—
1.2	NA	—	—	NA	—	—	1.221	+1.73	255	1.202	+0.16	207
2.4	2.398	-0.07	214	2.396	0.14	162	2.404	+0.16	129	2.404	+0.16	103
9.6	9.548	-0.54	53	9.53	-0.76	40	9.469	-1.36	32	9.615	+0.16	25
19.2	19.09	-0.54	26	19.53	+1.73	19	19.53	+1.73	15	19.23	+0.16	12
76.8	73.66	-4.09	6	78.13	+1.73	4	78.13	+1.73	3	83.33	+8.51	2
96	103.12	+7.42	4	97.65	+1.73	3	104.2	+8.51	2	NA	—	—
300	257.81	-14.06	1	390.63	+30.21	0	312.5	+4.17	0	NA	—	—
500	515.62	+3.13	0	NA	—	—	NA	—	—	NA	—	—
HIGH	515.62	—	0	—	—	0	312.5	—	0	250	—	0
LOW	2.014	—	255	1.53	—	255	1.221	—	255	0.977	—	255

BAUD RATE (K)	FOSC = 10 MHz			FOSC = 7.159 MHz			FOSC = 5.068 MHz		
	KBAUD	%ERROR	SPBRG VALUE (DECIMAL)	KBAUD	%ERROR	SPBRG VALUE (DECIMAL)	KBAUD	%ERROR	SPBRG VALUE (DECIMAL)
0.3	NA	—	—	NA	—	—	0.31	+3.13	255
1.2	1.202	+0.16	129	1.203	-0.23	92	1.2	0	65
2.4	2.404	+0.16	64	2.380	-0.83	46	2.4	0	32
9.6	9.766	+1.73	15	9.322	-2.90	11	9.9	-3.13	7
19.2	19.53	+1.73	7	18.64	-2.90	5	19.8	+3.13	3
76.8	78.13	+1.73	1	NA	—	—	79.2	+3.13	0
96	NA	—	—	NA	—	—	NA	—	—
300	NA	—	—	NA	—	—	NA	—	—
500	NA	—	—	NA	—	—	NA	—	—
HIGH	156.3	—	0	111.9	—	0	79.2	—	0
LOW	0.610	—	255	0.437	—	255	0.309	—	255

BAUD RATE (K)	FOSC = 3.579 MHz			FOSC = 1 MHz			FOSC = 32.768 kHz		
	KBAUD	%ERROR	SPBRG VALUE (DECIMAL)	KBAUD	%ERROR	SPBRG VALUE (DECIMAL)	KBAUD	%ERROR	SPBRG VALUE (DECIMAL)
0.3	0.301	+0.23	185	0.300	+0.16	51	0.256	-14.67	1
1.2	1.190	-0.83	46	1.202	+0.16	12	NA	—	—
2.4	2.432	+1.32	22	2.232	-6.99	6	NA	—	—
9.6	9.322	-2.90	5	NA	—	—	NA	—	—
19.2	18.64	-2.90	2	NA	—	—	NA	—	—
76.8	NA	—	—	NA	—	—	NA	—	—
96	NA	—	—	NA	—	—	NA	—	—
300	NA	—	—	NA	—	—	NA	—	—
500	NA	—	—	NA	—	—	NA	—	—
HIGH	55.93	—	0	15.63	—	0	0.512	—	0
LOW	0.218	—	255	0.061	—	255	0.002	—	255

15.2.15 CLOCK ARBITRATION

Clock arbitration occurs when the master, during any receive, transmit, or Repeated Start/Stop condition, deasserts the SCL pin (SCL allowed to float high). When the SCL pin is allowed to float high, the baud rate generator (BRG) is suspended from counting until the SCL pin is actually sampled high. When the SCL pin is sampled high, the baud rate generator is reloaded with the contents of SSPADD<6:0> and begins counting. This ensures that the SCL high time will always be at least one BRG rollover count, in the event that the clock is held low by an external device (Figure 15-33).

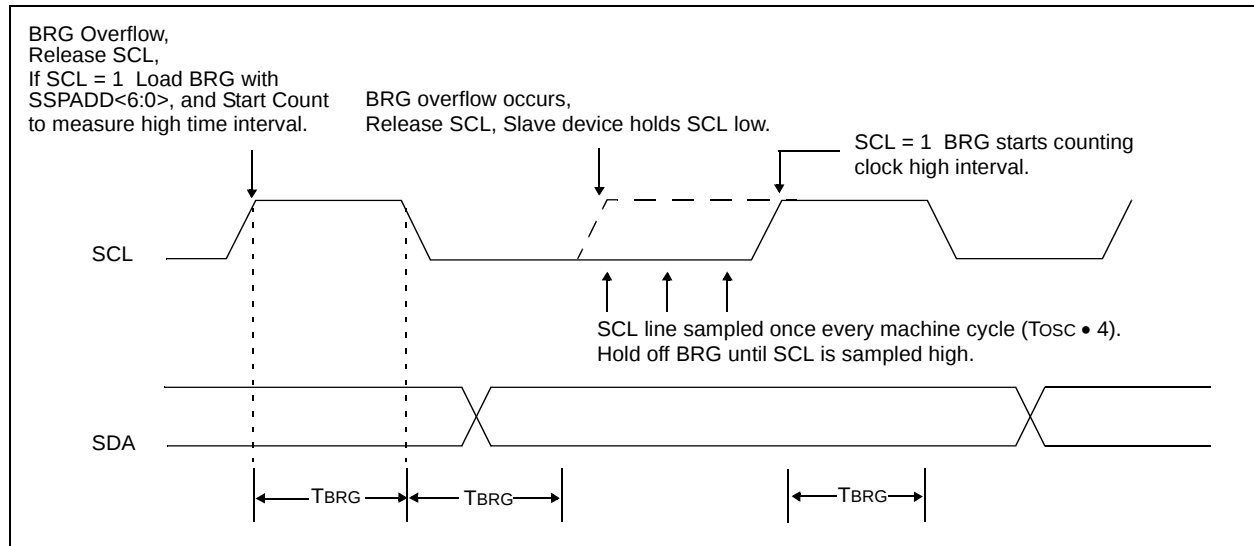
15.2.16 SLEEP OPERATION

While in SLEEP mode, the I²C module can receive addresses or data and when an address match or complete byte transfer occurs, wake the processor from SLEEP (if the SSP interrupt is enabled).

15.2.17 EFFECTS OF A RESET

A RESET disables the SSP module and terminates the current transfer.

FIGURE 15-33: CLOCK ARBITRATION TIMING IN MASTER TRANSMIT MODE



EXAMPLE 15-2: INTERFACING TO A 24LC01B SERIAL EEPROM (USING MPLAB C17)

```
// Writes the byte data to 24LC01B at the specified address
void ByteWrite(static unsigned char address, static unsigned char data)
{
    StartI2C();                // Send start bit
    IdleI2C();                 // Wait for idle condition
    WriteI2C(CONTROL);         // Send control byte
    IdleI2C();                 // Wait for idle condition
    if (!SSPCON2bits.ACKSTAT)   // If 24LC01B ACKs
    {
        WriteI2C(address);     // Send control byte
        IdleI2C();             // Wait for idle condition

        if (!SSPCON2bits.ACKSTAT) // If 24LC01B ACKs
            WriteI2C(data);     // Send data
    }
    IdleI2C();                 // Wait for idle condition
    StopI2C();                 // Send stop bit
    IdleI2C();                 // Wait for idle condition
    return;
}

// Reads a byte of data from 24LC01B at the specified address
unsigned char ByteRead(static unsigned char address)
{
    StartI2C();                // Send start bit
    IdleI2C();                 // Wait for idle condition
    WriteI2C(CONTROL);         // Send control byte
    IdleI2C();                 // Wait for idle condition
    if (!SSPCON2bits.ACKSTAT)   // If the 24LC01B ACKs
    {
        WriteI2C(address);     // Send address
        IdleI2C();             // Wait for idle condition
        if (!SSPCON2bits.ACKSTAT) // If the 24LC01B ACKs
        {
            RestartI2C();       // Send restart
            IdleI2C();           // Wait for idle condition
            WriteI2C(CONTROL+1); // Send control byte with R/W set
            IdleI2C();           // Wait for idle condition
            if (!SSPCON2bits.ACKSTAT) // If the 24LC01B ACKs
            {
                getcI2C();       // Read a byte of data from 24LC01B
                IdleI2C();       // Wait for idle condition
                NotAckI2C();     // Send a NACK to 24LC01B
                IdleI2C();       // Wait for idle condition
                StopI2C();       // Send stop bit
                IdleI2C();       // Wait for idle condition
            }
        }
    }
    return(SSPBUF);
}
```

16.7 A/D Accuracy/Error

In systems where the device frequency is low, use of the A/D RC clock is preferred. At moderate to high frequencies, T_{AD} should be derived from the device oscillator.

The absolute accuracy specified for the A/D converter includes the sum of all contributions for quantization error, integral error, differential error, full scale error, offset error, and monotonicity. It is defined as the maximum deviation from an actual transition versus an ideal transition for any code. The absolute error of the A/D converter is specified at $< \pm 1$ LSB for $V_{DD} = V_{REF}$ (over the device's specified operating range). However, the accuracy of the A/D converter will degrade as V_{REF} diverges from V_{DD} .

For a given range of analog inputs, the output digital code will be the same. This is due to the quantization of the analog input to a digital code. Quantization error is typically $\pm 1/2$ LSB and is inherent in the analog to digital conversion process. The only way to reduce quantization error is to increase the resolution of the A/D converter or oversample.

Offset error measures the first actual transition of a code versus the first ideal transition of a code. Offset error shifts the entire transfer function. Offset error can be calibrated out of a system or introduced into a system through the interaction of the total leakage current and source impedance at the analog input.

Gain error measures the maximum deviation of the last actual transition and the last ideal transition adjusted for offset error. This error appears as a change in slope of the transfer function. The difference in gain error to full scale error is that full scale does not take offset error into account. Gain error can be calibrated out in software.

Linearity error refers to the uniformity of the code changes. Linearity errors cannot be calibrated out of the system. Integral non-linearity error measures the actual code transition versus the ideal code transition, adjusted by the gain error for each code.

Differential non-linearity measures the maximum actual code width versus the ideal code width. This measure is unadjusted.

The maximum pin leakage current is specified in the Device Data Sheet electrical specification (Table 20-2, parameter #D060).

In systems where the device frequency is low, use of the A/D RC clock is preferred. At moderate to high frequencies, T_{AD} should be derived from the device oscillator. T_{AD} must not violate the minimum and should be minimized to reduce inaccuracies due to noise and sampling capacitor bleed off.

In systems where the device will enter SLEEP mode after the start of the A/D conversion, the RC clock source selection is required. In this mode, the digital noise from the modules in SLEEP are stopped. This method gives high accuracy.

16.8 Connection Considerations

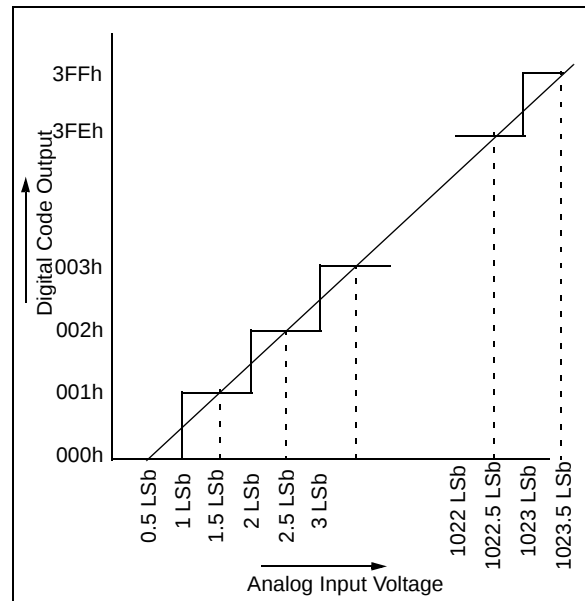
If the input voltage exceeds the rail values (V_{SS} or V_{DD}) by greater than 0.3V, then the accuracy of the conversion is out of specification.

An external RC filter is sometimes added for anti-aliasing of the input signal. The R component should be selected to ensure that the total source impedance is kept under the 10 k Ω recommended specification. Any external components connected (via hi-impedance) to an analog input pin (capacitor, zener diode, etc.) should have very little leakage current at the pin.

16.9 Transfer Function

The transfer function of the A/D converter is as follows: the first transition occurs when the analog input voltage (V_{AIN}) equals Analog $V_{REF} / 1024$ (Figure 16-7).

FIGURE 16-7: A/D TRANSFER FUNCTION



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16.10 References

A good reference for understanding A/D converter is the "Analog-Digital Conversion Handbook" third edition, published by Prentice Hall (ISBN 0-13-03-2848-0).

TABLE 16-3: REGISTERS/BITS ASSOCIATED WITH A/D

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR, BOR	MCLR, WDT
06h, unbanked	CPUSTA	—	—	STAKAV	GLINTD	TO	PD	POR	BOR	--11 1100	--11 qq11
07h, unbanked	INTSTA	PEIF	T0CKIF	T0IF	INTF	PEIE	T0CKIE	T0IE	INTE	0000 0000	0000 0000
10h, Bank 4	PIR2	SSPIF	BCLIF	ADIF	—	CA4IF	CA3IF	TX2IF	RC2IF	000- 0010	000- 0010
11h, Bank 4	PIE2	SSPIE	BCLIE	ADIE	—	CA4IE	CA3IE	TX2IE	RC2IE	000- 0000	000- 0000
10h, Bank 5	DDRF	Data Direction Register for PORTF								1111 1111	1111 1111
11h, Bank 5	PORTF	RF7/ AN11	RF6/ AN10	RF5/ AN9	RF4/ AN8	RF3/ AN7	RF2/ AN6	RF1/ AN5	RF0/ AN4	0000 0000	0000 0000
12h, Bank 5	DDRG	Data Direction register for PORTG								1111 1111	1111 1111
13h, Bank 5	PORTG	RG7/ TX2/CK2	RG6/ RX2/DT2	RG5/ PWM3	RG4/ CAP3	RG3/ AN0/VREF+	RG2/ AN1/VREF-	RG1/ AN2	RG0/ AN3	xxxx 0000	uuuu 0000
14h, Bank 5	ADCON0	CHS3	CHS2	CHS1	CHS0	—	GO/DONE	—	ADON	0000 -0-0	0000 -0-0
15h, Bank 5	ADCON1	ADCS1	ADCS0	ADFM	—	PCFG3	PCFG2	PCFG1	PCFG0	000- 0000	000- 0000
16h, Bank 5	ADRESL	A/D Result Low Register								xxxx xxxx	uuuu uuuu
17h, Bank 5	ADRESH	A/D Result High Register								xxxx xxxx	uuuu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used for A/D conversion.

Note: Other (non power-up) RESETS include: external RESET through MCLR and Watchdog Timer Reset.

PIC17C7XX

MOVFP Move f to p

Syntax: `[label] MOVFP f,p`

Operands: $0 \leq f \leq 255$
 $0 \leq p \leq 31$

Operation: $(f) \rightarrow (p)$

Status Affected: None

Encoding:

011p	pppp	ffff	ffff
------	------	------	------

Description: Move data from data memory location 'f' to data memory location 'p'. Location 'f' can be anywhere in the 256 byte data space (00h to FFh), while 'p' can be 00h to 1Fh.

Either 'p' or 'f' can be WREG (a useful, special situation).

MOVFP is particularly useful for transferring a data memory location to a peripheral register (such as the transmit buffer or an I/O port). Both 'f' and 'p' can be indirectly addressed.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write register 'p'

Example: `MOVFP REG1, REG2`

Before Instruction

REG1 = 0x33,
REG2 = 0x11

After Instruction

REG1 = 0x33,
REG2 = 0x33

MOVLB Move Literal to low nibble in BSR

Syntax: `[label] MOVLB k`

Operands: $0 \leq k \leq 15$

Operation: $k \rightarrow (\text{BSR}<3:0>)$

Status Affected: None

Encoding:

1011	1000	uuuu	kkkk
------	------	------	------

Description: The four-bit literal 'k' is loaded in the Bank Select Register (BSR). Only the low 4-bits of the Bank Select Register are affected. The upper half of the BSR is unchanged. The assembler will encode the "u" fields as '0'.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal 'k'	Process Data	Write literal 'k' to BSR<3:0>

Example: `MOVLB 5`

Before Instruction

BSR register = 0x22

After Instruction

BSR register = 0x25 (Bank 5)

PIC17C7XX

RRNCF Rotate Right f (no carry)

Syntax: `[label] RRNCF f,d`

Operands: $0 \leq f \leq 255$
 $d \in [0,1]$

Operation: $f < n \rightarrow d < n-1$;
 $f < 0 \rightarrow d < 7$

Status Affected: None

Encoding:

0010	000d	ffff	ffff
------	------	------	------

Description: The contents of register 'f' are rotated one bit to the right. If 'd' is 0, the result is placed in WREG. If 'd' is 1, the result is placed back in register 'f'.



Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

Example 1: `RRNCF REG, 1`

Before Instruction

WREG = ?
 REG = 1101 0111

After Instruction

WREG = 0
 REG = 1110 1011

Example 2: `RRNCF REG, 0`

Before Instruction

WREG = ?
 REG = 1101 0111

After Instruction

WREG = 1110 1011
 REG = 1101 0111

SETF Set f

Syntax: `[label] SETF f,s`

Operands: $0 \leq f \leq 255$
 $s \in [0,1]$

Operation: $FFh \rightarrow f$;
 $FFh \rightarrow d$

Status Affected: None

Encoding:

0010	101s	ffff	ffff
------	------	------	------

Description: If 's' is 0, both the data memory location 'f' and WREG are set to FFh. If 's' is 1, only the data memory location 'f' is set to FFh.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write register 'f' and other specified register

Example1: `SETF REG, 0`

Before Instruction

REG = 0xDA
 WREG = 0x05

After Instruction

REG = 0xFF
 WREG = 0xFF

Example2: `SETF REG, 1`

Before Instruction

REG = 0xDA
 WREG = 0x05

After Instruction

REG = 0xFF
 WREG = 0x05

PIC17C7XX

FIGURE 20-23: A/D CONVERSION TIMING

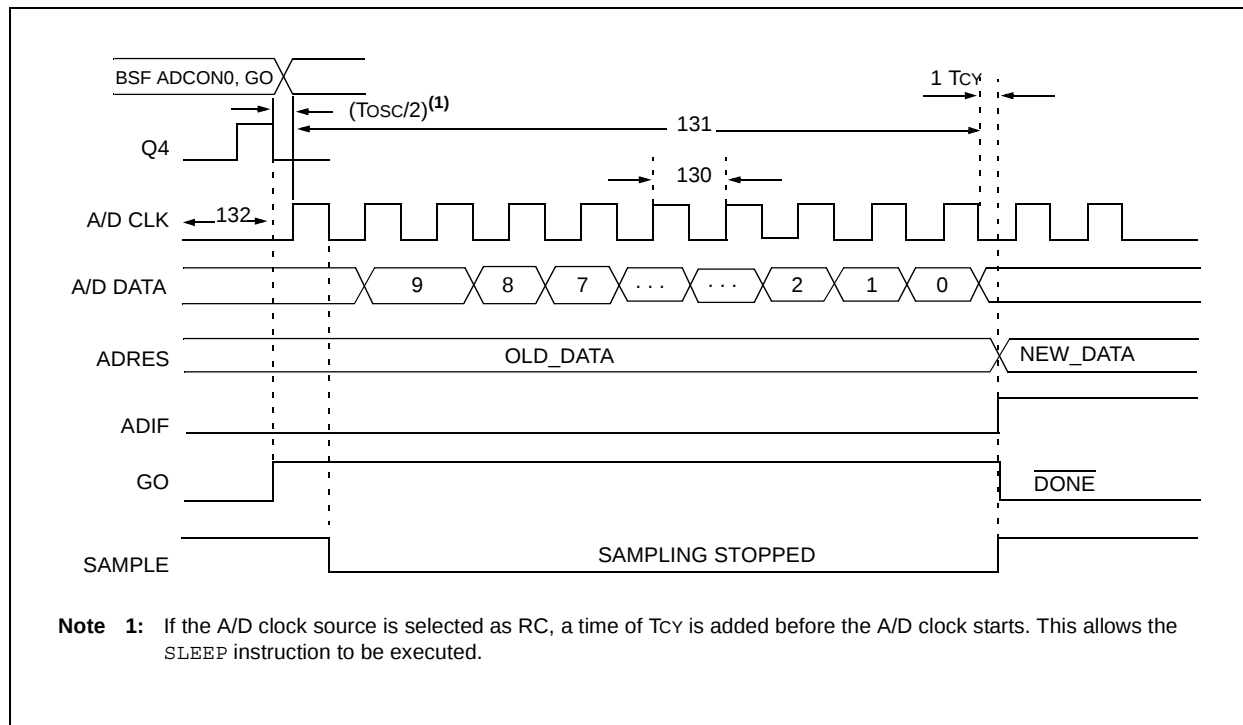


TABLE 20-19: A/D CONVERSION REQUIREMENTS

Param. No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
130	TAD	A/D clock period	PIC17CXXX	1.6	—	—	μs TOSC based, $V_{REF} \geq 3.0\text{V}$
			PIC17LCXXX	3.0	—	—	μs TOSC based, V_{REF} full range
			PIC17CXXX	2.0	4.0	6.0	μs A/D RC mode
			PIC17LCXXX	3.0	6.0	9.0	μs A/D RC mode
131	TCNV	Conversion time (not including acquisition time) (Note 1)	11	—	12	Tad	
132	TACQ	Acquisition time	(Note 2)	20	—	μs	The minimum time is the amplifier settling time. This may be used if the "new" input voltage has not changed by more than 1LSb (i.e., 5 mV @ 5.12V) from the last sampled voltage (as stated on CHOLD).
			10	—	—	μs	
134	TGO	Q4 to ADCLK start	—	Tosc/2	—	—	If the A/D clock source is selected as RC, a time of T_{cy} is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated.

Note 1: ADRES register may be read on the following T_{cy} cycle.

Note 2: See Section 16.1 for minimum conditions when input voltage has changed more than 1 LSb.

FIGURE 21-4: TYPICAL RC OSCILLATOR FREQUENCY vs. V_{DD}

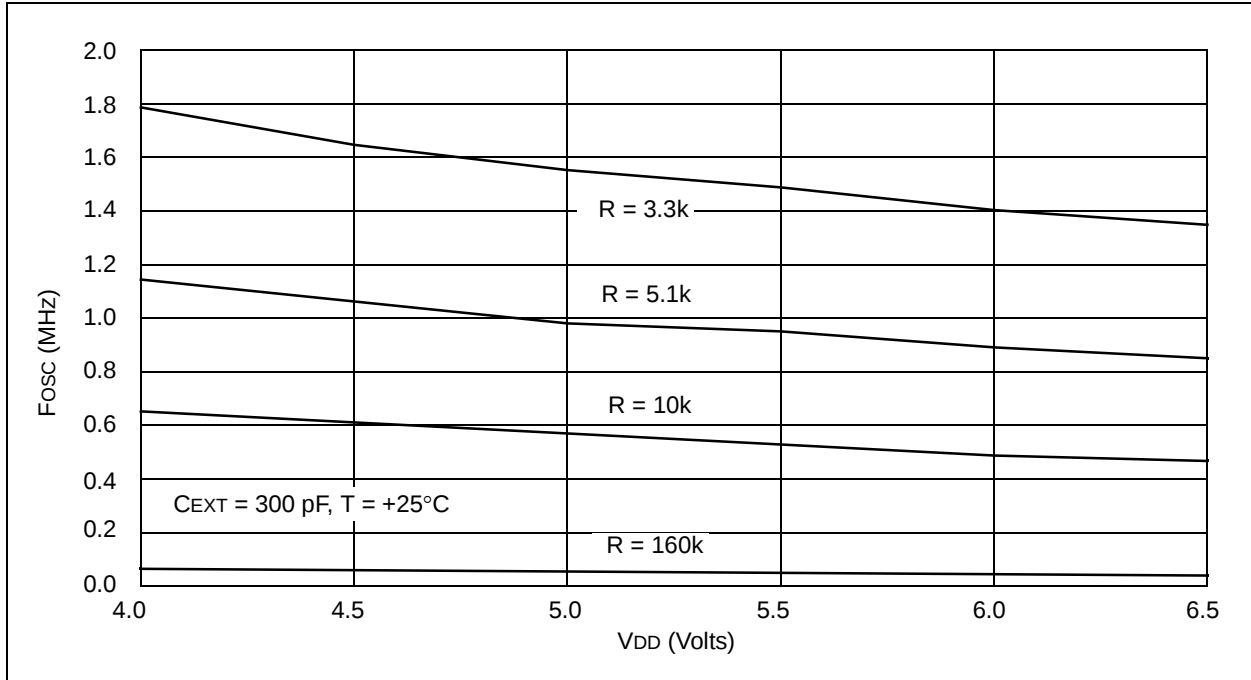


TABLE 21-2: RC OSCILLATOR FREQUENCIES

C _{EXT}	R _{EXT}	Average F _{osc} @ 5V, +25°C	
		F _{osc} (MHz)	Accuracy
22 pF	10k	3.33 MHz	± 12%
	100k	353 kHz	± 13%
100 pF	3.3k	3.54 MHz	± 10%
	5.1k	2.43 MHz	± 14%
	10k	1.30 MHz	± 17%
	100k	129 kHz	± 10%
300 pF	3.3k	1.54 MHz	± 14%
	5.1k	980 kHz	± 12%
	10k	564 kHz	± 16%
	160k	35 kHz	± 18%

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