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Details

Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	16MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	50
Program Memory Size	16KB (8K x 16)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	454 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	68-LCC (J-Lead)
Supplier Device Package	68-PLCC (24.23x24.23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic17c752t-16e-l

PIC17C7XX

NOTES:

3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC17CXXX can be attributed to a number of architectural features, commonly found in RISC microprocessors. To begin with, the PIC17CXXX uses a modified Harvard architecture. This architecture has the program and data accessed from separate memories. So, the device has a program memory bus and a data memory bus. This improves bandwidth over traditional von Neumann architecture, where program and data are fetched from the same memory (accesses over the same bus). Separating program and data memory further allows instructions to be sized differently than the 8-bit wide data word. PIC17CXXX opcodes are 16-bits wide, enabling single word instructions. The full 16-bit wide program memory bus fetches a 16-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions. Consequently, all instructions execute in a single cycle (121 ns @ 33 MHz), except for program branches and two special instructions that transfer data between program and data memory.

The PIC17CXXX can address up to 64K x 16 of program memory space.

The **PIC17C752** and **PIC17C762** integrate 8K x 16 of EPROM program memory on-chip.

The **PIC17C756A** and **PIC17C766** integrate 16K x 16 EPROM program memory on-chip.

A simplified block diagram is shown in Figure 3-1. The descriptions of the device pins are listed in Table 3-1.

Program execution can be internal only (Microcontroller or Protected Microcontroller mode), external only (Microprocessor mode), or both (Extended Microcontroller mode). Extended Microcontroller mode does not allow code protection.

The PIC17CXXX can directly or indirectly address its register files or data memory. All special function registers, including the Program Counter (PC) and Working Register (WREG), are mapped in data memory. The PIC17CXXX has an orthogonal (symmetrical) instruction set that makes it possible to carry out any operation on any register using any addressing mode. This symmetrical nature and lack of 'special optimal situations' make programming with the PIC17CXXX simple, yet efficient. In addition, the learning curve is reduced significantly.

One of the PIC17CXXX family architectural enhancements from the PIC16CXX family, allows two file registers to be used in some two operand instructions. This allows data to be moved directly between two registers without going through the WREG register, thus increasing performance and decreasing program memory usage.

The PIC17CXXX devices contain an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

The WREG register is an 8-bit working register used for ALU operations.

All PIC17CXXX devices have an 8 x 8 hardware multiplier. This multiplier generates a 16-bit result in a single cycle.

The ALU is 8-bits wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two's complement in nature.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC), Zero (Z) and Overflow (OV) bits in the ALUSTA register. The C and DC bits operate as a borrow and digit borrow out bit, respectively, in subtraction. See the SUBLW and SUBWF instructions for examples.

Signed arithmetic is comprised of a magnitude and a sign bit. The overflow bit indicates if the magnitude overflows and causes the sign bit to change state. That is, if the result of 8-bit signed operations is greater than 127 (7Fh), or less than -128 (80h).

Signed math can have greater than 7-bit values (magnitude), if more than one byte is used. The overflow bit only operates on bit6 (MSb of magnitude) and bit7 (sign bit) of each byte value in the ALU. That is, the overflow bit is not useful if trying to implement signed math where the magnitude, for example, is 11-bits.

If the signed math values are greater than 7-bits (such as 15-, 24-, or 31-bit), the algorithm must ensure that the low order bytes of the signed value ignore the overflow status bit.

Example 3-1 shows two cases of doing signed arithmetic. The Carry (C) bit and the Overflow (OV) bit are the most important status bits for signed math operations.

EXAMPLE 3-1: 8-BIT MATH ADDITION

Hex Value	Signed Values	Unsigned Values
FFh	-1	255
+ 01h	+ 1	+ 1
= 00h	= 0 (FEh)	= 256 → 00h
C bit = 1	C bit = 1	C bit = 1
OV bit = 0	OV bit = 0	OV bit = 0
DC bit = 1	DC bit = 1	DC bit = 1
Z bit = 1	Z bit = 1	Z bit = 1

Hex Value	Signed Values	Unsigned Values
7Fh	127	127
+ 01h	+ 1	+ 1
= 80h	= 128 → 00h	= 128
C bit = 0	C bit = 0	C bit = 0
OV bit = 1	OV bit = 1	OV bit = 1
DC bit = 1	DC bit = 1	DC bit = 1
Z bit = 0	Z bit = 0	Z bit = 0

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4.1.6 RC OSCILLATOR

For timing insensitive applications, the RC device option offers additional cost savings. RC oscillator frequency is a function of the supply voltage, the resistor (REXT) and capacitor (CEXT) values, and the operating temperature. In addition to this, oscillator frequency will vary from unit to unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect oscillation frequency, especially for low CEXT values. The user also needs to take into account variation due to tolerance of external R and C components used. Figure 4-7 shows how the R/C combination is connected to the PIC17CXXX. For REXT values below 2.2 k Ω , the oscillator operation may become unstable, or stop completely. For very high REXT values (e.g. 1 M Ω), the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend to keep REXT between 3 k Ω and 100 k Ω .

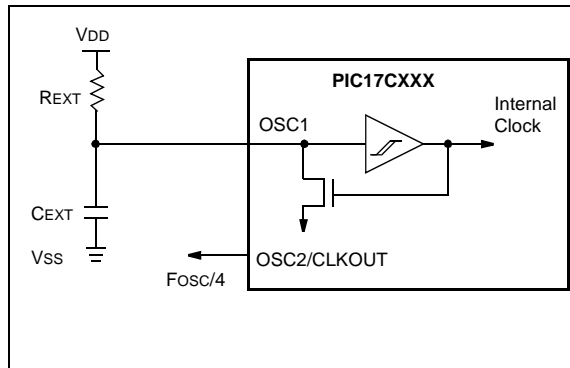
Although the oscillator will operate with no external capacitor (CEXT = 0 pF), we recommend using values above 20 pF for noise and stability reasons. With little or no external capacitance, oscillation frequency can vary dramatically due to changes in external capacitances, such as PCB trace capacitance or package lead frame capacitance.

See Section 21.0 for RC frequency variation from part to part due to normal process variation. The variation is larger for larger R (since leakage current variation will affect RC frequency more for large R) and for smaller C (since variation of input capacitance will affect RC frequency more).

See Section 21.0 for variation of oscillator frequency due to VDD for given REXT/CEXT values, as well as frequency variation due to operating temperature for given R, C, and VDD values.

The oscillator frequency, divided by 4, is available on the OSC2/CLKOUT pin and can be used for test purposes or to synchronize other logic (see Figure 4-8 for waveform).

FIGURE 4-7: RC OSCILLATOR MODE



4.1.6.1 RC Start-up

As the device voltage increases, the RC will immediately start its oscillations once the pin voltage levels meet the input threshold specifications (parameter #D032 and parameter #D042 in the electrical specification section). The time required for the RC to start oscillating depends on many factors. These include:

- Resistor value used
- Capacitor value used
- Device VDD rise time
- System temperature

TABLE 5-4: INITIALIZATION CONDITIONS FOR SPECIAL FUNCTION REGISTERS

Register	Address	Power-on Reset Brown-out Reset	MCLR Reset WDT Reset	Wake-up from SLEEP through Interrupt
Unbanked				
INDF0	00h	N/A	N/A	N/A
FSR0	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	02h	0000h	0000h	PC + 1 ⁽²⁾
PCLATH	03h	0000 0000	uuuu uuuu	uuuu uuuu
ALUSTA	04h	1111 xxxx	1111 uuuu	1111 uuuu
T0STA	05h	0000 000-	0000 000-	0000 000-
CPUSTA ⁽³⁾	06h	--11 11qq	--11 qquu	--uu qquu
INTSTA	07h	0000 0000	0000 0000	uuuu uuuu ⁽¹⁾
INDF1	08h	N/A	N/A	N/A
FSR1	09h	xxxx xxxx	uuuu uuuu	uuuu uuuu
WREG	0Ah	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR0L	0Bh	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR0H	0Ch	xxxx xxxx	uuuu uuuu	uuuu uuuu
TBLPTRL	0Dh	0000 0000	0000 0000	uuuu uuuu
TBLPTRH	0Eh	0000 0000	0000 0000	uuuu uuuu
BSR	0Fh	0000 0000	0000 0000	uuuu uuuu
Bank 0				
PORTA ^(4,6)	10h	0-xx 11xx	0-uu 11uu	u-uu uuuu
DDRB	11h	1111 1111	1111 1111	uuuu uuuu
PORTB ⁽⁴⁾	12h	xxxx xxxx	uuuu uuuu	uuuu uuuu
RCSTA1	13h	0000 -00x	0000 -00u	uuuu -uuu
RCREG1	14h	xxxx xxxx	uuuu uuuu	uuuu uuuu
TXSTA1	15h	0000 --1x	0000 --1u	uuuu --uu
TXREG1	16h	xxxx xxxx	uuuu uuuu	uuuu uuuu
SPBRG1	17h	0000 0000	0000 0000	uuuu uuuu

Legend: u = unchanged, x = unknown, - = unimplemented, read as '0', q = value depends on condition

Note 1: One or more bits in INTSTA, PIR1, PIR2 will be affected (to cause wake-up).

2: When the wake-up is due to an interrupt and the GLINTD bit is cleared, the PC is loaded with the interrupt vector.

3: See Table 5-3 for RESET value of specific condition.

4: This is the value that will be in the port output latch.

5: When the device is configured for Microprocessor or Extended Microcontroller mode, the operation of this port does not rely on these registers.

6: On any device RESET, these pins are configured as inputs.

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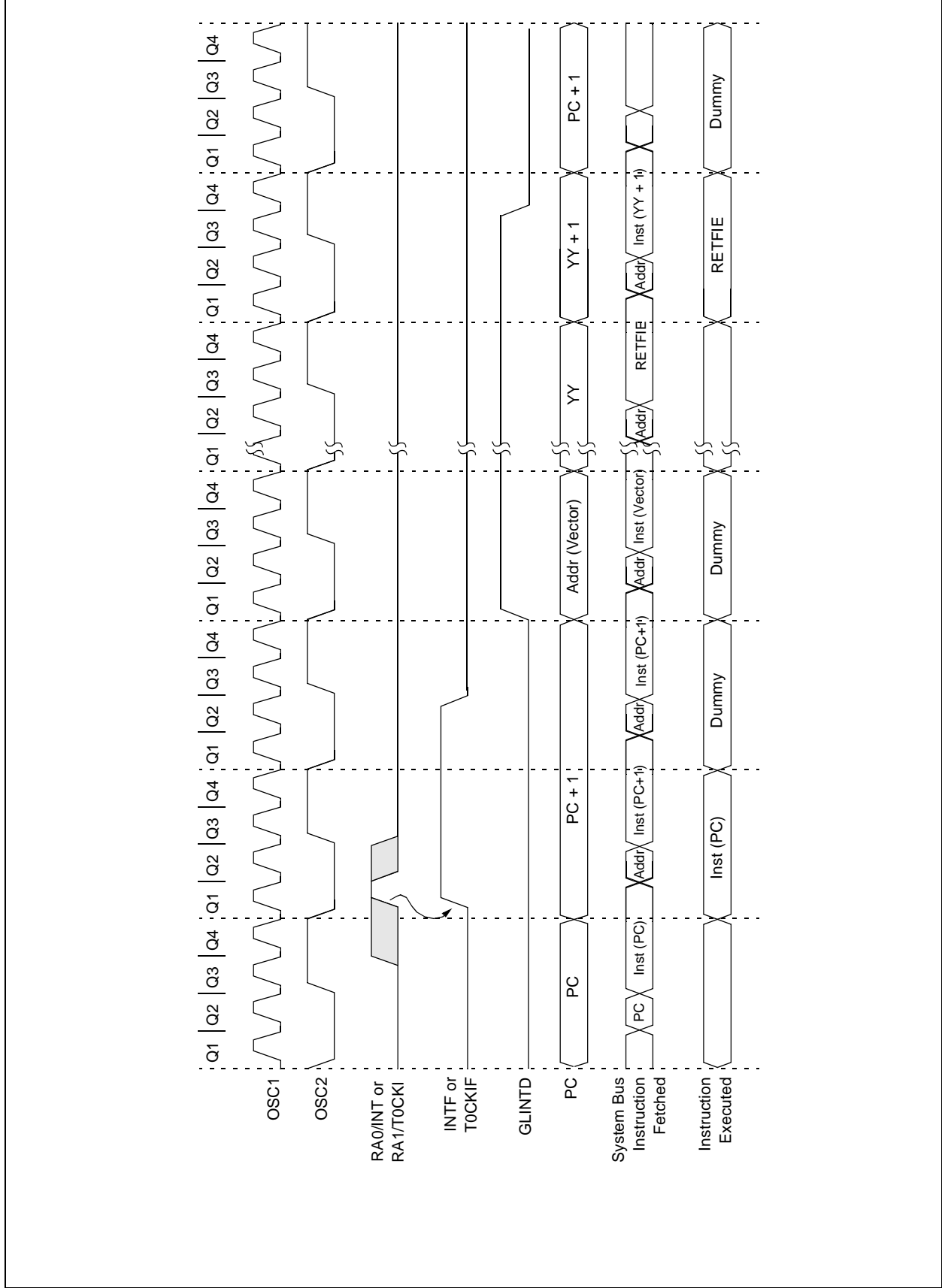


TABLE 7-3: SPECIAL FUNCTION REGISTERS (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	MCLR, WDT
Bank 2											
10h	TMR1	Timer1's Register								xxxx xxxx	uuuu uuuu
11h	TMR2	Timer2's Register								xxxx xxxx	uuuu uuuu
12h	TMR3L	Timer3's Register; Low Byte								xxxx xxxx	uuuu uuuu
13h	TMR3H	Timer3's Register; High Byte								xxxx xxxx	uuuu uuuu
14h	PR1	Timer1's Period Register								xxxx xxxx	uuuu uuuu
15h	PR2	Timer2's Period Register								xxxx xxxx	uuuu uuuu
16h	PR3L/CA1L	Timer3's Period Register - Low Byte/Capture1 Register; Low Byte								xxxx xxxx	uuuu uuuu
17h	PR3H/CA1H	Timer3's Period Register - High Byte/Capture1 Register; High Byte								xxxx xxxx	uuuu uuuu
Bank 3											
10h	PW1DCL	DC1	DC0	—	—	—	—	—	—	xx-- ----	uu-- ----
11h	PW2DCL	DC1	DC0	TM2PW2	—	—	—	—	—	xx0- ----	uu0- ----
12h	PW1DCH	DC9	DC8	DC7	DC6	DC5	DC4	DC3	DC2	xxxx xxxx	uuuu uuuu
13h	PW2DCH	DC9	DC8	DC7	DC6	DC5	DC4	DC3	DC2	xxxx xxxx	uuuu uuuu
14h	CA2L	Capture2 Low Byte								xxxx xxxx	uuuu uuuu
15h	CA2H	Capture2 High Byte								xxxx xxxx	uuuu uuuu
16h	TCON1	CA2ED1	CA2ED0	CA1ED1	CA1ED0	T16	TMR3CS	TMR2CS	TMR1CS	0000 0000	0000 0000
17h	TCON2	CA2OVF	CA1OVF	PWM2ON	PWM1ON	CA1/PR3	TMR3ON	TMR2ON	TMR1ON	0000 0000	0000 0000
Bank 4											
10h	PIR2	SSPIF	BCLIF	ADIF	—	CA4IF	CA3IF	TX2IF	RC2IF	000- 0010	000- 0010
11h	PIE2	SSPIE	BCLIE	ADIE	—	CA4IE	CA3IE	TX2IE	RC2IE	000- 0000	000- 0000
12h	Unimplemented	—	—	—	—	—	—	—	—	---- ----	---- ----
13h	RCSTA2	SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D	0000 -00x	0000 -00u
14h	RCREG2	Serial Port Receive Register for USART2								xxxx xxxx	uuuu uuuu
15h	TXSTA2	CSRC	TX9	TXEN	SYNC	—	—	TRMT	TX9D	0000 --1x	0000 --1u
16h	TXREG2	Serial Port Transmit Register for USART2								xxxx xxxx	uuuu uuuu
17h	SPBRG2	Baud Rate Generator for USART2								0000 0000	0000 0000
Bank 5:											
10h	DDRF	Data Direction Register for PORTF								1111 1111	1111 1111
11h	PORTF ⁽⁴⁾	RF7/ AN11	RF6/ AN10	RF5/ AN9	RF4/ AN8	RF3/ AN7	RF2/ AN6	RF1/ AN5	RF0/ AN4	0000 0000	0000 0000
12h	DDRG	Data Direction Register for PORTG								1111 1111	1111 1111
13h	PORTG ⁽⁴⁾	RG7/ TX2/CK2	RG6/ RX2/DT2	RG5/ PWM3	RG4/ CAP3	RG3/ AN0	RG2/ AN1	RG1/ AN2	RG0/ AN3	xxxx 0000	uuuu 0000
14h	ADCON0	CHS3	CHS2	CHS1	CHS0	—	GO/DONE	—	ADON	0000 -0-0	0000 -0-0
15h	ADCON1	ADCS1	ADCS0	ADFM	—	PCFG3	PCFG2	PCFG1	PCFG0	000- 0000	000- 0000
16h	ADRESL	A/D Result Register Low Byte								xxxx xxxx	uuuu uuuu
17h	ADRESH	A/D Result Register High Byte								xxxx xxxx	uuuu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0', q = value depends on condition.
Shaded cells are unimplemented, read as '0'.

- Note**
- 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for PC<15:8> whose contents are updated from, or transferred to, the upper byte of the program counter.
 - 2: The TO and PD status bits in CPUSTA are not affected by a MCLR Reset.
 - 3: Bank 8 and associated registers are only implemented on the PIC17C76X devices.
 - 4: This is the value that will be in the port output latch.
 - 5: When the device is configured for Microprocessor or Extended Microcontroller mode, the operation of this port does not rely on these registers.
 - 6: On any device RESET, these pins are configured as inputs.

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10.4 PORTD and DDRD Registers

PORTD is an 8-bit bi-directional port. The corresponding data direction register is DDRD. A '1' in DDRD configures the corresponding port pin as an input. A '0' in the DDRD register configures the corresponding port pin as an output. Reading PORTD reads the status of the pins, whereas writing to PORTD will write to the port latch. PORTD is multiplexed with the system bus. When operating as the system bus, PORTD is the high order byte of the address/data bus (AD15:AD8). The timing for the system bus is shown in the Electrical Specifications section.

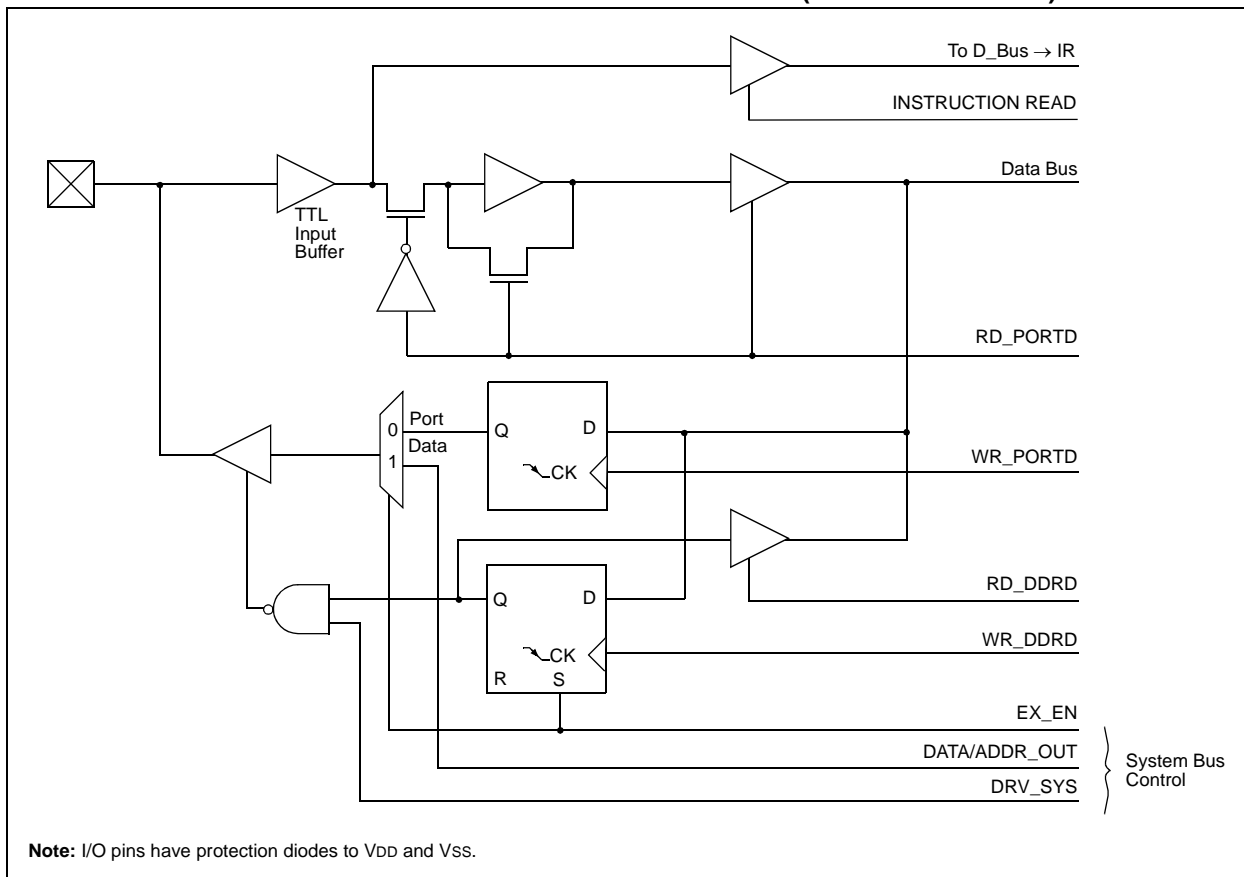
Note: This port is configured as the system bus when the device's configuration bits are selected to Microprocessor or Extended Microcontroller modes. In the two other microcontroller modes, this port is a general purpose I/O.

Example 10-4 shows an instruction sequence to initialize PORTD. The Bank Select Register (BSR) must be selected to Bank 1 for the port to be initialized. The following example uses the MOVLB instruction to load the BSR register for bank selection.

EXAMPLE 10-4: INITIALIZING PORTD

```
MOVLB 1      ; Select Bank 1
CLRF  PORTD, F ; Initialize PORTD data
               ; latches before setting
               ; the data direction reg
MOVLW 0xCF    ; Value used to initialize
               ; data direction
MOVWF  DDRD   ; Set RD<3:0> as inputs
               ; RD<5:4> as outputs
               ; RD<7:6> as inputs
```

FIGURE 10-10: BLOCK DIAGRAM OF RD7:RD0 PORT PINS (IN I/O PORT MODE)



12.1 Timer0 Operation

When the T0CS (T0STA<5>) bit is set, TMR0 increments on the internal clock. When T0CS is clear, TMR0 increments on the external clock (RA1/T0CKI pin). The external clock edge can be selected in software. When the T0SE (T0STA<6>) bit is set, the timer will increment on the rising edge of the RA1/T0CKI pin. When T0SE is clear, the timer will increment on the falling edge of the RA1/T0CKI pin. The prescaler can be programmed to introduce a prescale of 1:1 to 1:256. The timer increments from 0000h to FFFFh and rolls over to 0000h. On overflow, the TMR0 Interrupt Flag bit (T0IF) is set. The TMR0 interrupt can be masked by clearing the corresponding TMR0 Interrupt Enable bit (T0IE). The TMR0 Interrupt Flag bit (T0IF) is automatically cleared when vectoring to the TMR0 interrupt vector.

12.2 Using Timer0 with External Clock

When an external clock input is used for Timer0, it is synchronized with the internal phase clocks. Figure 12-2 shows the synchronization of the external clock. This synchronization is done after the prescaler. The output of the prescaler (PSOUT) is sampled twice in every instruction cycle to detect a rising or a falling edge. The timing requirements for the external clock are detailed in the electrical specification section.

12.2.1 DELAY FROM EXTERNAL CLOCK EDGE

Since the prescaler output is synchronized with the internal clocks, there is a small delay from the time the external clock edge occurs to the time TMR0 is actually incremented. Figure 12-2 shows that this delay is between $3T_{osc}$ and $7T_{osc}$. Thus, for example, measuring the interval between two edges (e.g. period) will be accurate within $\pm 4T_{osc}$ (± 121 ns @ 33 MHz).

FIGURE 12-1: TIMER0 MODULE BLOCK DIAGRAM

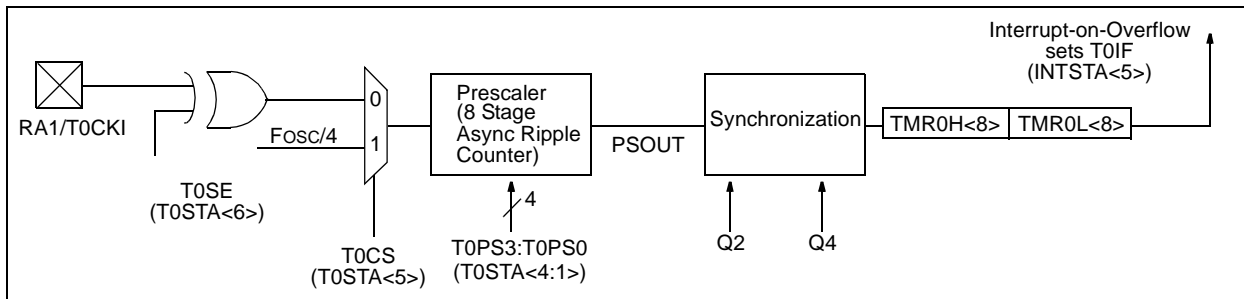
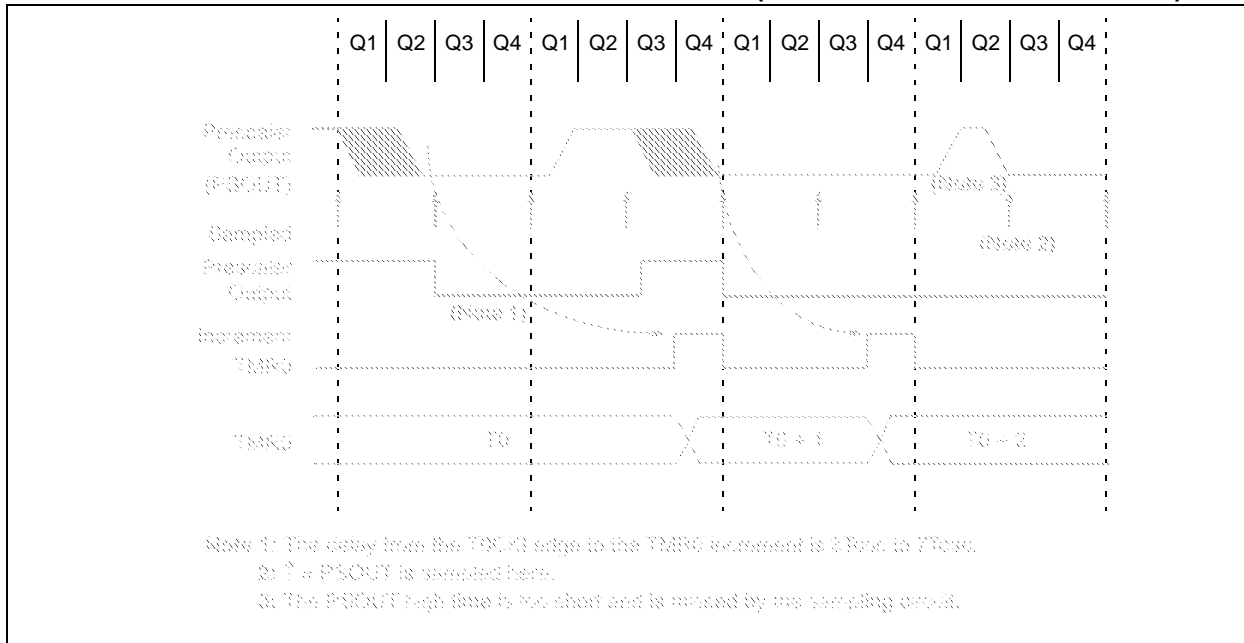


FIGURE 12-2: TMR0 TIMING WITH EXTERNAL CLOCK (INCREMENT ON FALLING EDGE)



13.1.3.3 External Clock Source

The PWMs will operate, regardless of the clock source of the timer. The use of an external clock has ramifications that must be understood. Because the external TCLK12 input is synchronized internally (sampled once per instruction cycle), the time TCLK12 changes to the time the timer increments, will vary by as much as 1Tcy (one instruction cycle). This will cause jitter in the duty cycle as well as the period of the PWM output.

This jitter will be $\pm 1Tcy$, unless the external clock is synchronized with the processor clock. Use of one of the PWM outputs as the clock source to the TCLK12 input, will supply a synchronized clock.

In general, when using an external clock source for PWM, its frequency should be much less than the device frequency (Fosc).

13.1.3.4 Maximum Resolution/Frequency for External Clock Input

The use of an external clock for the PWM time base (Timer1 or Timer2) limits the PWM output to a maximum resolution of 8-bits. The PWxDCL<7:6> bits must be kept cleared. Use of any other value will distort the PWM output. All resolutions are supported when internal clock mode is selected. The maximum attainable frequency is also lower. This is a result of the timing requirements of an external clock input for a timer (see the Electrical Specification section). The maximum PWM frequency, when the timers clock source is the RB4/TCLK12 pin, is shown in Table 13-4 (Standard Resolution mode).

TABLE 13-5: REGISTERS/BITS ASSOCIATED WITH PWM

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	MCLR, WDT
16h, Bank 3	TCON1	CA2ED1	CA2ED0	CA1ED1	CA1ED0	T16	TMR3CS	TMR2CS	TMR1CS	0000 0000	0000 0000
17h, Bank 3	TCON2	CA2OVF	CA1OVF	PWM2ON	PWM1ON	CA1/PR3	TMR3ON	TMR2ON	TMR1ON	0000 0000	0000 0000
16h, Bank 7	TCON3	—	CA4OVF	CA3OVF	CA4ED1	CA4ED0	CA3ED1	CA3ED0	PWM3ON	-000 0000	-000 0000
10h, Bank 2	TMR1	Timer1's Register								xxxx xxxx	uuuu uuuu
11h, Bank 2	TMR2	Timer2's Register								xxxx xxxx	uuuu uuuu
16h, Bank 1	PIR1	RBIF	TMR3IF	TMR2IF	TMR1IF	CA2IF	CA1IF	TX1IF	RC1IF	x000 0010	u000 0010
17h, Bank 1	PIE1	RBIE	TMR3IE	TMR2IE	TMR1IE	CA2IE	CA1IE	TX1IE	RC1IE	0000 0000	0000 0000
07h, Unbanked	INTSTA	PEIF	T0CKIF	T0IF	INTF	PEIE	T0CKIE	T0IE	INTE	0000 0000	0000 0000
06h, Unbanked	CPUSTA	—	—	STKAV	GLINTD	\overline{TO}	\overline{PD}	POR	BOR	--11 11qq	--11 qquu
14h, Bank 2	PR1	Timer1 Period Register								xxxx xxxx	uuuu uuuu
15h, Bank 2	PR2	Timer2 Period Register								xxxx xxxx	uuuu uuuu
10h, Bank 3	PW1DCL	DC1	DC0	—	—	—	—	—	—	xx-- ----	uu-- ----
11h, Bank 3	PW2DCL	DC1	DC0	TM2PW2	—	—	—	—	—	xx0- ----	uu0- ----
10h, Bank 7	PW3DCL	DC1	DC0	TM2PW3	—	—	—	—	—	xx0- ----	uu0- ----
12h, Bank 3	PW1DCH	DC9	DC8	DC7	DC6	DC5	DC4	DC3	DC2	xxxx xxxx	uuuu uuuu
13h, Bank 3	PW2DCH	DC9	DC8	DC7	DC6	DC5	DC4	DC3	DC2	xxxx xxxx	uuuu uuuu
11h, Bank 7	PW3DCH	DC9	DC8	DC7	DC6	DC5	DC4	DC3	DC2	xxxx xxxx	uuuu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0', q = value depends on conditions.
Shaded cells are not used by PWM Module.

14.0 UNIVERSAL SYNCHRONOUS ASYNCHRONOUS RECEIVER TRANSMITTER (USART) MODULES

Each USART module is a serial I/O module. There are two USART modules that are available on the PIC17C7XX. They are specified as USART1 and USART2. The description of the operation of these modules is generic in regard to the register names and pin names used. Table 14-1 shows the generic names that are used in the description of operation and the actual names for both USART1 and USART2. Since the control bits in each register have the same function, their names are the same (there is no need to differentiate).

The Transmit Status and Control Register (TXSTA) is shown in Figure 14-1, while the Receive Status and Control Register (RCSTA) is shown in Figure 14-2.

TABLE 14-1: USART MODULE GENERIC NAMES

Generic Name	USART1 Name	USART2 Name
<i>Registers</i>		
RCSTA	RCSTA1	RCSTA2
TXSTA	TXSTA1	TXSTA2
SPBRG	SPBRG1	SPBRG2
RCREG	RCREG1	RCREG2
TXREG	TXREG1	TXREG2
<i>Interrupt Control Bits</i>		
RCIE	RC1IE	RC2IE
RCIF	RC1IF	RC2IF
TXIE	TX1IE	TX2IE
TXIF	TX1IF	TX2IF
<i>Pins</i>		
RX/DT	RA4/RX1/DT1	RG6/RX2/DT2
TX/CK	RA5/TX1/CK1	RG7/TX2/CK2

**REGISTER 14-1: TXSTA1 REGISTER (ADDRESS: 15h, BANK 0)
TXSTA2 REGISTER (ADDRESS: 15h, BANK 4)**

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R-1	R/W-x
CSRC	TX9	TXEN	SYNC	—	—	TRMT	TX9D
bit 7							bit 0

bit 7 **CSRC:** Clock Source Select bit

Synchronous mode:

1 = Master mode (clock generated internally from BRG)

0 = Slave mode (clock from external source)

Asynchronous mode:

Don't care

bit 6 **TX9:** 9-bit Transmit Select bit

1 = Selects 9-bit transmission

0 = Selects 8-bit transmission

bit 5 **TXEN:** Transmit Enable bit

1 = Transmit enabled

0 = Transmit disabled

SREN/CREN overrides TXEN in SYNC mode

bit 4 **SYNC:** USART Mode Select bit

(Synchronous/Asynchronous)

1 = Synchronous mode

0 = Asynchronous mode

bit 3-2 **Unimplemented:** Read as '0'

bit 1 **TRMT:** Transmit Shift Register (TSR) Empty bit

1 = TSR empty

0 = TSR full

bit 0 **TX9D:** 9th bit of Transmit Data (can be used to calculate the parity in software)

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

- n = Value at POR Reset

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

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TABLE 14-8: REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER TRANSMISSION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	MCLR, WDT
16h, Bank 1	PIR1	RBIF	TMR3IF	TMR2IF	TMR1IF	CA2IF	CA1IF	TX1IF	RC1IF	x000 0010	u000 0010
17h, Bank 1	PIE1	RBIE	TMR3IE	TMR2IE	TMR1IE	CA2IE	CA1IE	TX1IE	RC1IE	0000 0000	0000 0000
13h, Bank 0	RCSTA1	SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D	0000 -00x	0000 -00u
16h, Bank 0	TXREG1	TX7	TX6	TX5	TX4	TX3	TX2	TX1	TX0	xxxx xxxx	uuuu uuuu
15h, Bank 0	TXSTA1	CSRC	TX9	TXEN	SYNC	—	—	TRMT	TX9D	0000 --1x	0000 --1u
17h, Bank 0	SPBRG1	Baud Rate Generator Register								0000 0000	0000 0000
10h, Bank 4	PIR2	SSPIF	BCLIF	ADIF	—	CA4IF	CA3IF	TX2IF	RC2IF	000- 0010	000- 0010
11h, Bank 4	PIE2	SSPIE	BCLIE	ADIE	—	CA4IE	CA3IE	TX2IE	RC2IE	000- 0000	000- 0000
13h, Bank 4	RCSTA2	SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D	0000 -00x	0000 -00u
16h, Bank 4	TXREG2	TX7	TX6	TX5	TX4	TX3	TX2	TX1	TX0	xxxx xxxx	uuuu uuuu
15h, Bank 4	TXSTA2	CSRC	TX9	TXEN	SYNC	—	—	TRMT	TX9D	0000 --1x	0000 --1u
17h, Bank 4	SPBRG2	Baud Rate Generator Register								0000 0000	0000 0000

Legend: x = unknown, u = unchanged, - = unimplemented, read as a '0'. Shaded cells are not used for synchronous master transmission.

FIGURE 14-8: SYNCHRONOUS TRANSMISSION

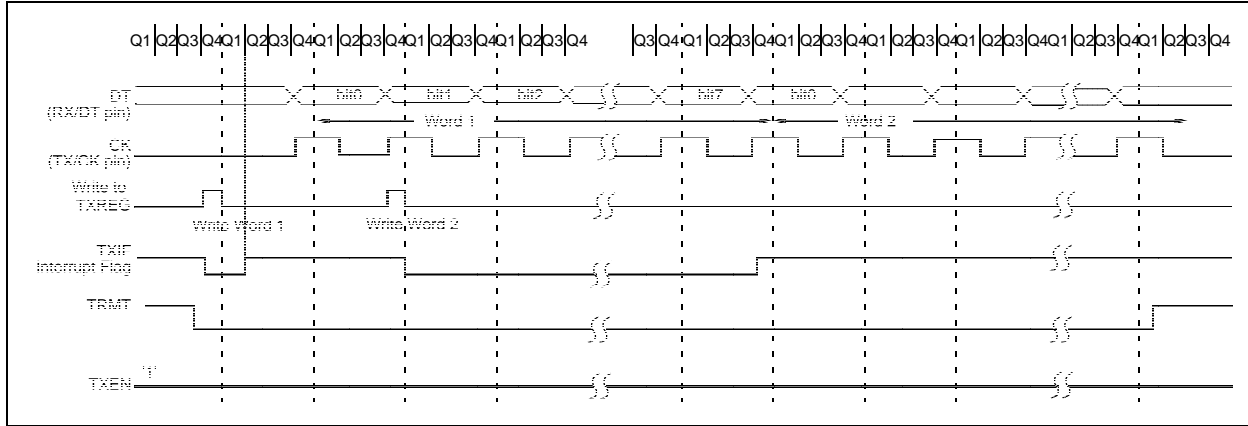
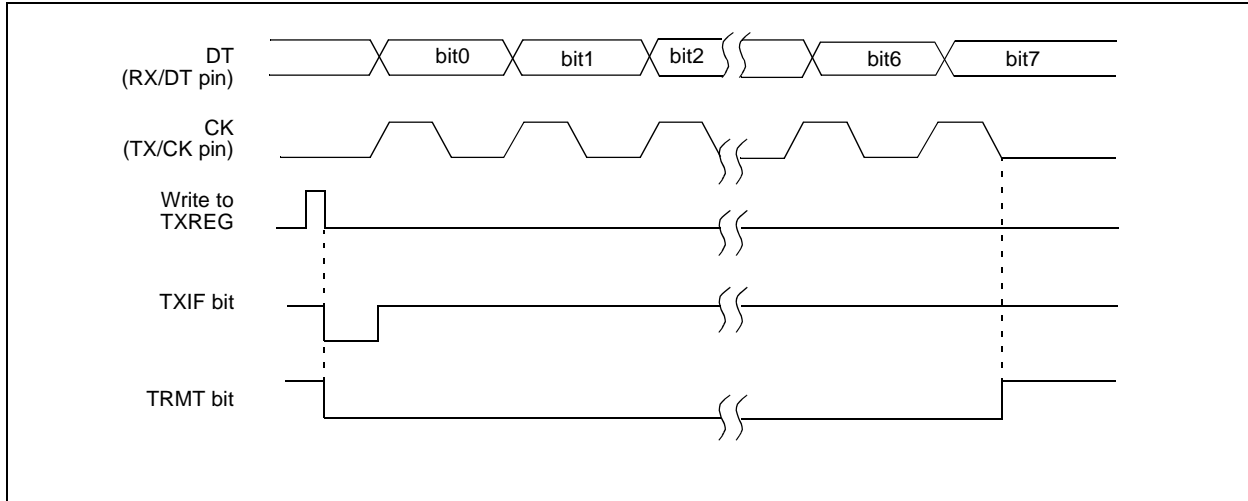


FIGURE 14-9: SYNCHRONOUS TRANSMISSION (THROUGH TXEN)



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15.1.5 SLAVE MODE

In Slave mode, the data is transmitted and received as the external clock pulses appear on SCK. When the last bit is latched, the interrupt flag bit SSPIF (PIR2<7>) is set.

While in Slave mode, the external clock is supplied by the external clock source on the SCK pin. This external clock must meet the minimum high and low times as specified in the electrical specifications.

While in SLEEP mode, the slave can transmit/receive data. When a byte is received, the device will wake-up from SLEEP.

15.1.6 SLAVE SELECT SYNCHRONIZATION

The \overline{SS} pin allows a Synchronous Slave mode. The SPI must be in Slave mode with \overline{SS} pin control enabled (SSPCON1<3:0> = 04h). The pin must not be driven low for the \overline{SS} pin to function as an input. The RA2 Data Latch must be high. When the \overline{SS} pin is low, transmission and reception are enabled and

the SDO pin is driven. When the \overline{SS} pin goes high, the SDO pin is no longer driven, even if in the middle of a transmitted byte and becomes a floating output. External pull-up/pull-down resistors may be desirable, depending on the application.

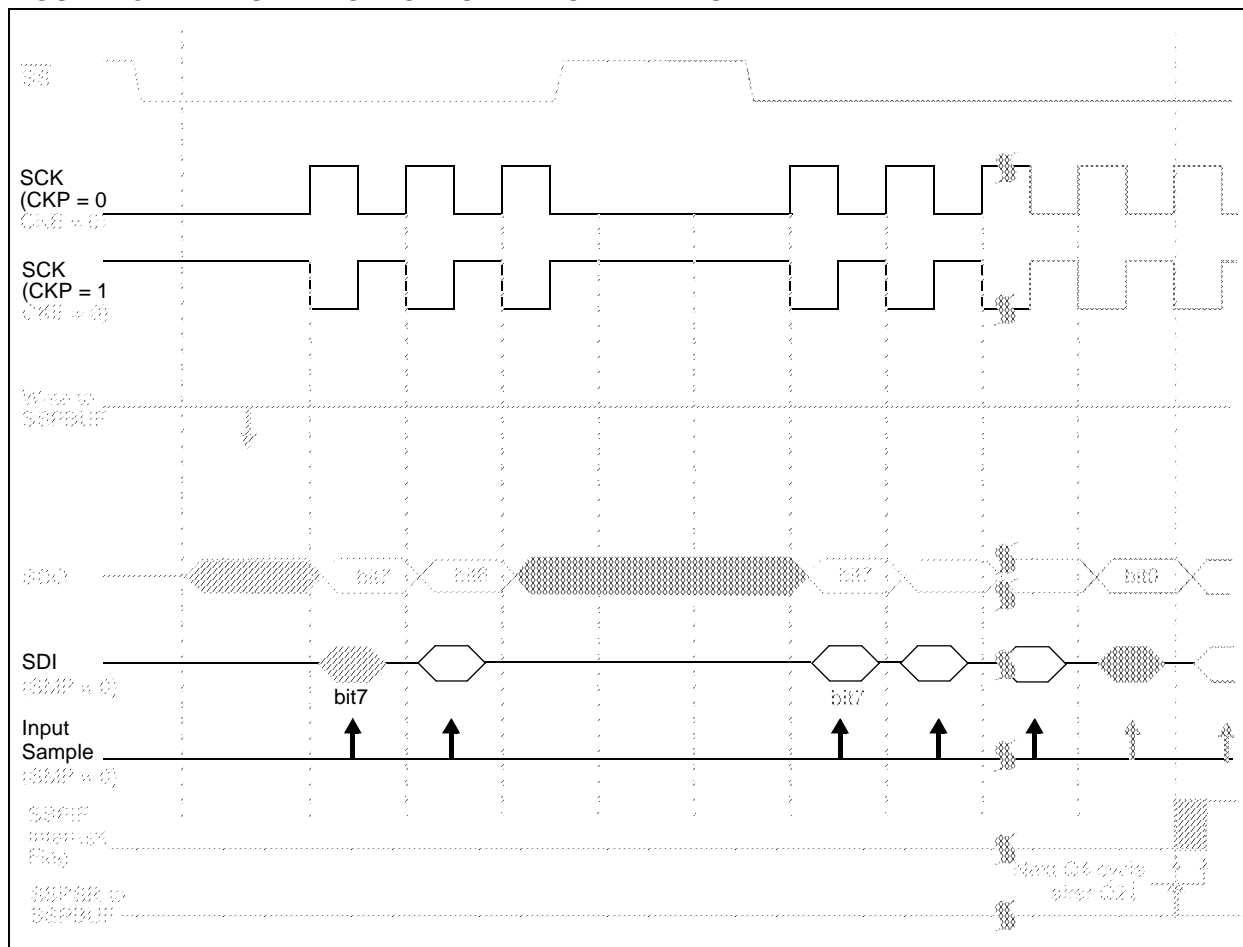
Note 1: When the SPI is in Slave mode with \overline{SS} pin control enabled (SSPCON<3:0> = 0100), the SPI module will reset if the \overline{SS} pin is set to VDD.

2: If the SPI is used in Slave mode with CKE = '1', then the \overline{SS} pin control must be enabled.

When the SPI module resets, the bit counter is forced to 0. This can be done by either forcing the \overline{SS} pin to a high level, or clearing the SSPEN bit.

To emulate two-wire communication, the SDO pin can be connected to the SDI pin. When the SPI needs to operate as a receiver, the SDO pin can be configured as an input. This disables transmissions from the SDO. The SDI can always be left as an input (SDI function), since it cannot create a bus conflict.

FIGURE 15-7: SLAVE SYNCHRONIZATION WAVEFORM



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15.2.3 SLEEP OPERATION

While in SLEEP mode, the I²C module can receive addresses or data and when an address match or complete byte transfer occurs, wake the processor from SLEEP (if the SSP interrupt is enabled).

15.2.4 EFFECTS OF A RESET

A RESET disables the SSP module and terminates the current transfer.

TABLE 15-3: REGISTERS ASSOCIATED WITH I²C OPERATION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR, BOR	MCLR, WDT
07h, Unbanked	INTSTA	PEIF	T0CKIF	T0IF	INTF	PEIE	T0CKIE	T0IE	INTE	0000 0000	0000 0000
10h, Bank 4	PIR2	SSPIF	BCLIF	ADIF	—	CA4IF	CA3IF	TX2IF	RC2IF	000- 0000	000- 0000
11h, Bank 4	PIE2	SSPIE	BCLIE	ADIE	—	CA4IE	CA3IE	TX2IE	RC2IE	000- 0000	000- 0000
10h, Bank 6	SSPADD	Synchronous Serial Port (I ² C mode) Address Register								0000 0000	0000 0000
14h, Bank 6	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register								xxxx xxxx	uuuu uuuu
11h, Bank 6	SSPCON1	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
12h, Bank 6	SSPCON2	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	0000 0000	0000 0000
13h, Bank 6	SSPSTAT	SMP	CKE	D/ \bar{A}	P	S	R/ \bar{W}	UA	BF	0000 0000	0000 0000

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by the SSP in I²C mode.

17.0 SPECIAL FEATURES OF THE CPU

What sets a microcontroller apart from other processors are special circuits to deal with the needs of real-time applications. The PIC17CXXX family has a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection. These are:

- Oscillator Selection (Section 4.0)
- RESET (Section 5.0)
 - Power-on Reset (POR)
 - Power-up Timer (PWRT)
 - Oscillator Start-up Timer (OST)
 - Brown-out Reset (BOR)
- Interrupts (Section 6.0)
- Watchdog Timer (WDT)
- SLEEP mode
- Code protection

The PIC17CXXX has a Watchdog Timer which can be shut-off only through EPROM bits. It runs off its own RC oscillator for added reliability. There are two timers that offer necessary delays on POR and BOR. One is the Oscillator Start-up Timer (OST), intended to keep the chip in RESET until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 96 ms (nominal) on power-up only, designed to keep the part in RESET while the power supply stabilizes. With these two timers on-chip, most applications need no external RESET circuitry.

The SLEEP mode is designed to offer a very low current power-down mode. The user can wake from SLEEP through external RESET, Watchdog Timer Reset, or through an interrupt. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost, while the LF crystal option saves power. Configuration bits are used to select various options. This configuration word has the format shown in Figure 17-1.

REGISTER 17-1: CONFIGURATION WORDS

High (H) Table Read Addr. FE0Fh - FE08h	U-x	R/P-1	R/P-1	U-x	U-x	U-x	U-x	U-x	U-x
	—	PM2	BODEN	—	—	—	—	—	—
	bit 15	bit 8	bit 7						bit 0
Low (L) Table Read Addr. FE07h - FE00h	U-x	U-x	R/P-1	U-x	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
	—	—	PM1	—	PM0	WDTPS1	WDTPS0	FOSC1	FOSC0
	bit 15	bit 8	bit 7						bit 0
bits 7H, 6L, 4L	PM2, PM1, PM0: Processor Mode Select bits 111 = Microprocessor mode 110 = Microcontroller mode 101 = Extended Microcontroller mode 000 = Code Protected Microcontroller mode								
bit 6H	BODEN: Brown-out Detect Enable 1 = Brown-out Detect circuitry is enabled 0 = Brown-out Detect circuitry is disabled								
bits 3L:2L	WDTPS1:WDTPS0: WDT Postscaler Select bits 11 = WDT enabled, postscaler = 1 10 = WDT enabled, postscaler = 256 01 = WDT enabled, postscaler = 64 00 = WDT disabled, 16-bit overflow timer								
bits 1L:0L	FOSC1:FOSC0: Oscillator Select bits 11 = EC oscillator 10 = XT oscillator 01 = RC oscillator 00 = LF oscillator								
Shaded bits (—)	Reserved								

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FIGURE 20-1: PIC17C7XX-33 VOLTAGE-FREQUENCY GRAPH

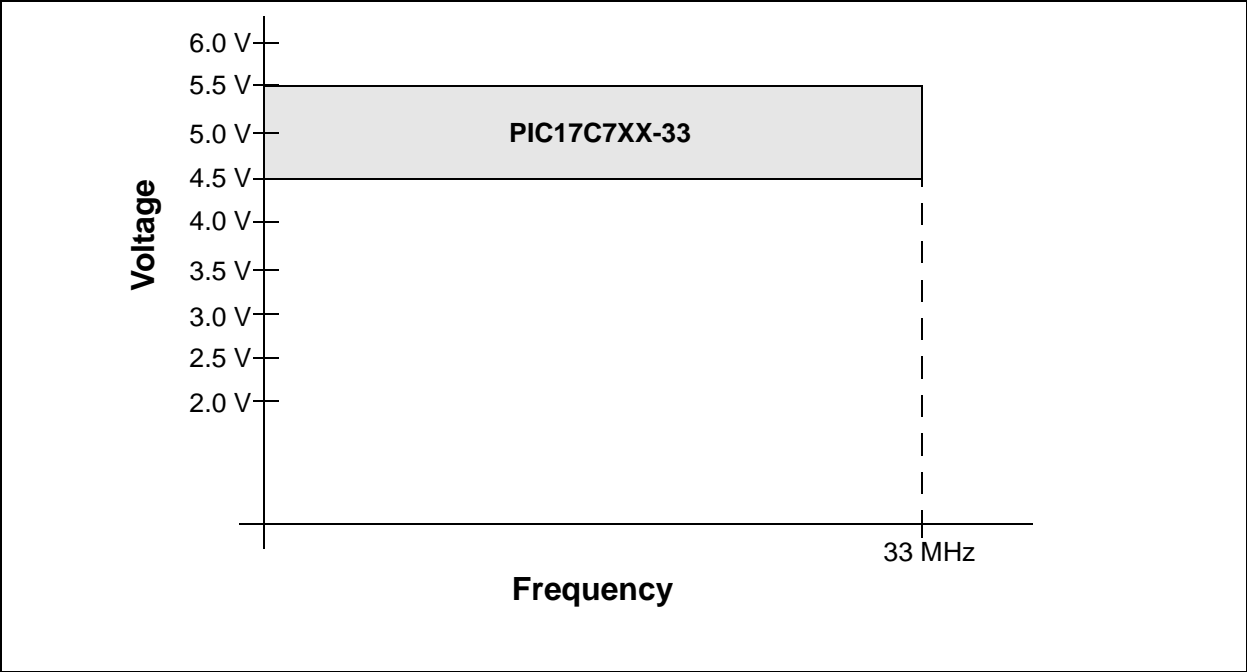
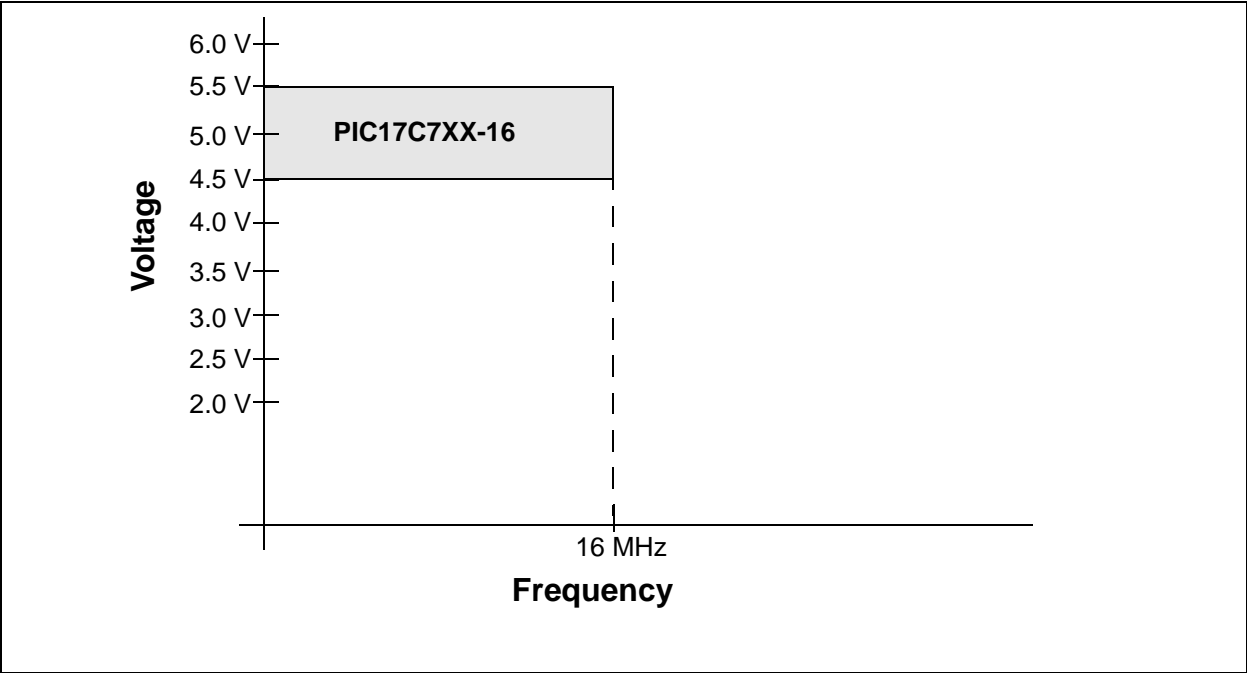


FIGURE 20-2: PIC17C7XX-16 VOLTAGE-FREQUENCY GRAPH



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20.2 DC Characteristics: PIC17C7XX-16 (Commercial, Industrial, Extended) PIC17C7XX-33 (Commercial, Industrial, Extended) PIC17LC7XX-08 (Commercial, Industrial)

Standard Operating Conditions (unless otherwise stated)							
Operating temperature							
DC CHARACTERISTICS							
Operating voltage VDD range as described in Section 20.1							
Param. No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D030	VIL	Input Low Voltage					
		I/O ports					
		with TTL buffer (Note 6)	Vss	—	0.8	V	4.5V ≤ VDD ≤ 5.5V
			Vss	—	0.2VDD	V	3.0V ≤ VDD ≤ 4.5V
D031		with Schmitt Trigger buffer					
		RA2, RA3	Vss	—	0.3VDD	V	I ² C compliant
		All others	Vss	—	0.2VDD	V	
D032		MCLR, OSC1 (in EC and RC mode)	Vss	—	0.2VDD	V	(Note 1)
D033		OSC1 (in XT, and LF mode)	—	0.5VDD	—	V	
D040	VIH	Input High Voltage					
		I/O ports					
		with TTL buffer (Note 6)	2.0	—	VDD	V	4.5V ≤ VDD ≤ 5.5V
			1 + 0.2VDD	—	VDD	V	3.0V ≤ VDD ≤ 4.5V
		with Schmitt Trigger buffer					
		RA2, RA3	0.7VDD	—	VDD	V	I ² C compliant
		All others	0.8VDD	—	VDD	V	
D042		MCLR	0.8VDD	—	VDD	V	(Note 1)
D043		OSC1 (XT, and LF mode)	—	0.5VDD	—	V	
D050	VHYS	Hysteresis of Schmitt Trigger Inputs	0.15VDD	—	—	V	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated.

- Note 1:** In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC17CXXX devices be driven with external clock in RC mode.
- 2:** The leakage current on the MCLR pin is strongly dependent on the applied voltage level. Higher leakage current may be measured at different input voltages.
- 3:** Negative current is defined as current sourced by the pin.
- 4:** These specifications are for the programming of the on-chip program memory EPROM through the use of the table write instructions. The complete programming specifications can be found in: PIC17C7XX Programming Specifications (Literature number DS TBD).
- 5:** The MCLR/VPP pin may be kept in this range at times other than programming, but is not recommended.
- 6:** For TTL buffers, the better of the two specifications may be used.

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FIGURE 20-9: TIMER0 EXTERNAL CLOCK TIMINGS

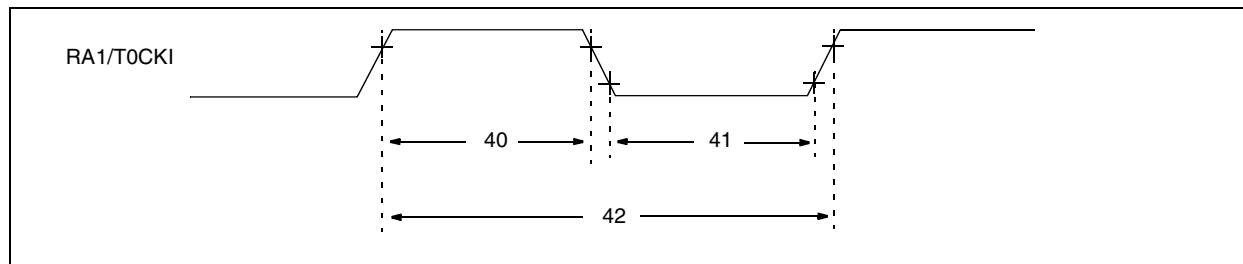


TABLE 20-4: TIMER0 EXTERNAL CLOCK REQUIREMENTS

Param No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width	No Prescaler	0.5Tcy + 20	—	—	ns	
			With Prescaler	10	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width	No Prescaler	0.5Tcy + 20	—	—	ns	
			With Prescaler	10	—	—	ns	
42	Tt0P	T0CKI Period		Greater of: 20 ns or $\frac{Tcy + 40}{N}$	—	—	ns	N = prescale value (1, 2, 4, ..., 256)

† Data in "Typ" column is at 5V, 25°C unless otherwise stated.

FIGURE 20-10: TIMER1, TIMER2 AND TIMER3 EXTERNAL CLOCK TIMINGS

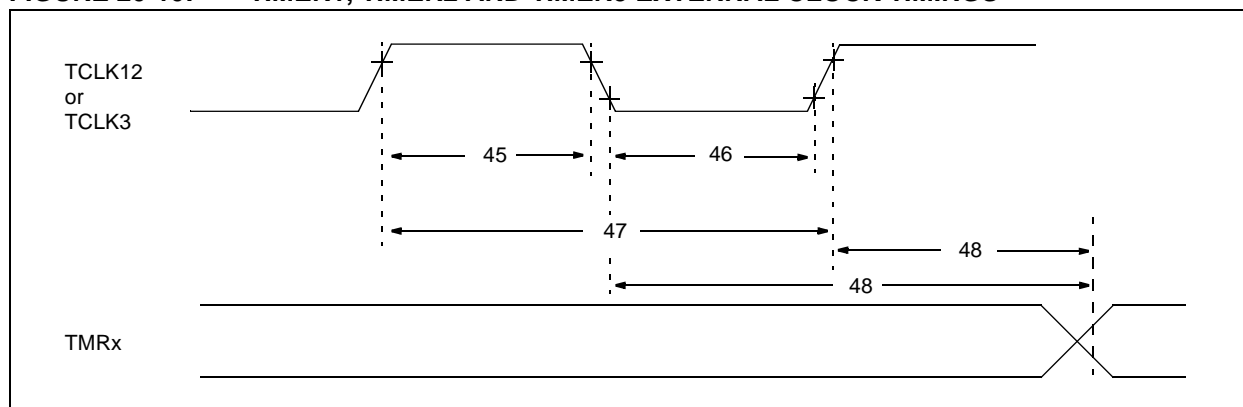


TABLE 20-5: TIMER1, TIMER2 AND TIMER3 EXTERNAL CLOCK REQUIREMENTS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
45	Tt123H	TCLK12 and TCLK3 high time	$0.5T_{CY} + 20$	—	—	ns	
46	Tt123L	TCLK12 and TCLK3 low time	$0.5T_{CY} + 20$	—	—	ns	
47	Tt123P	TCLK12 and TCLK3 input period	$\frac{T_{CY} + 40}{N}$	—	—	ns	N = prescale value (1, 2, 4, 8)
48	TckE2tmr1	Delay from selected External Clock Edge to Timer increment	$2T_{OSC}$	—	$6T_{OSC}$	—	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated.

APPENDIX A: MODIFICATIONS

The following is the list of modifications over the PIC16CXX microcontroller family:

1. Instruction word length is increased to 16-bit. This allows larger page sizes, both in program memory (8 Kwords versus 2 Kwords) and register file (256 bytes versus 128 bytes).
2. Four modes of operation: Microcontroller, Protected Microcontroller, Extended Microcontroller, and Microprocessor.
3. 22 new instructions. The `MOVF`, `TRIS` and `OPTION` instructions are no longer supported.
4. Four new instructions (`TLRD`, `TLWT`, `TABLRD`, `TABLWT`) for transferring data between data memory and program memory. They can be used to "self program" the EPROM program memory.
5. Single cycle data memory to data memory transfers possible (`MOVFP` and `MOVFP` instructions). These instructions do not affect the Working register (WREG).
6. W register (WREG) is now directly addressable.
7. A PC high latch register (PCLATH) is extended to 8-bits. The PCLATCH register is now both readable and writable.
8. Data memory paging is redefined slightly.
9. DDR registers replace function of TRIS registers.
10. Multiple Interrupt vectors added. This can decrease the latency for servicing interrupts.
11. Stack size is increased to 16 deep.
12. BSR register for data memory paging.
13. Wake-up from SLEEP operates slightly differently.
14. The Oscillator Start-Up Timer (OST) and Power-Up Timer (PWRT) operate in parallel and not in series.
15. PORTB interrupt-on-change feature works on all eight port pins.
16. TMR0 is 16-bit, plus 8-bit prescaler.
17. Second indirect addressing register added (FSR1 and FSR2). Control bits can select the FSR registers to auto-increment, auto-decrement, remain unchanged after an indirect address.
18. Hardware multiplier added (8 x 8 → 16-bit).
19. Peripheral modules operate slightly differently.
20. A/D has both VREF+ and VREF- inputs.
21. USARTs do not implement BRGH feature.
22. Oscillator modes slightly redefined.
23. Control/Status bits and registers have been placed in different registers and the control bit for globally enabling interrupts has inverse polarity.
24. In-circuit serial programming is implemented differently.

APPENDIX B: COMPATIBILITY

To convert code written for PIC16CXXX to PIC17CXXX, the user should take the following steps:

1. Remove any `TRIS` and `OPTION` instructions, and implement the equivalent code.
2. Separate the Interrupt Service Routine into its four vectors.
3. Replace:

```
MOVF    REG1, W
```

 with:

```
MOVFP   REG1, WREG
```
4. Replace:

```
MOVF    REG1, W
```

```
MOVWF   REG2
```

 with:

```
MOVFP   REG1, REG2 ; Addr(REG1) < 20h
```

 or

```
MOVFP   REG1, REG2 ; Addr(REG2) < 20h
```

Note: If REG1 and REG2 are both at addresses greater than 20h, two instructions are required.

```
MOVFP   REG1, WREG ;
MOVFP   WREG, REG2 ;
```

5. Ensure that all bit names and register names are updated to new data memory map locations.
6. Verify data memory banking.
7. Verify mode of operation for indirect addressing.
8. Verify peripheral routines for compatibility.
9. Weak pull-ups are enabled on RESET.
10. WDT time-outs always reset the device (in run or SLEEP mode).

B.1 Upgrading from PIC17C42 Devices

To convert code from the PIC17C42 to all the other PIC17CXXX devices, the user should take the following steps.

1. If the hardware multiply is to be used, ensure that any variables at address 18h and 19h are moved to another address.
2. Ensure that the upper nibble of the BSR was not written with a non-zero value. This may cause unexpected operation since the RAM bank is no longer 0.
3. The disabling of global interrupts has been enhanced, so there is no additional testing of the GLINTD bit after a `BSF CPUSTA, GLINTD` instruction.

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APPENDIX C: WHAT'S NEW

This is a new Data Sheet for the Following Devices:

- PIC17C752
- PIC17C756A
- PIC17C762
- PIC17C766

This Data Sheet is based on the PIC17C75X Data Sheet (DS30246A).

APPENDIX D: WHAT'S CHANGED

Clarified the TAD vs. device maximum operating frequency tables in Section 16.2.

Added device characteristic graphs and charts in Section 21.

Removed the "Preliminary" status from the entire document.

Revision C (January 2013)

Added a note to each package outline drawing.