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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	16MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	50
Program Memory Size	32KB (16K x 16)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	902 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic17c756a-16-pt

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PIC17C7XX

NOTES:

5.0 RESET

The PIC17CXXX differentiates between various kinds of RESET:

- Power-on Reset (POR)
- Brown-out Reset
- MCLR Reset
- WDT Reset

Some registers are not affected in any RESET condition, their status is unknown on POR and unchanged in any other RESET. Most other registers are forced to a "RESET state". The TO and PD bits are set or cleared differently in different RESET situations, as indicated in Table 5-3. These bits, in conjunction with the POR and BOR bits, are used in software to determine the nature of the RESET. See Table 5-4 for a full description of the RESET states of all registers.

When the device enters the "RESET state", the Data Direction registers (DDR) are forced set, which will make the I/O hi-impedance inputs. The RESET state of some peripheral modules may force the I/O to other operations, such as analog inputs or the system bus.

Note: While the device is in a RESET state, the internal phase clock is held in the Q1 state. Any processor mode that allows external execution will force the RE0/ALE pin as a low output and the RE1/OE and RE2/WR pins as high outputs.

A simplified block diagram of the On-Chip Reset Circuit is shown in Figure 5-1.



FIGURE 5-1: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT

PIC17C7XX

NOTES:

10.0 I/O PORTS

PIC17C75X devices have seven I/O ports, PORTA through PORTG. PIC17C76X devices have nine I/O ports, PORTA through PORTJ. PORTB through PORTJ have a corresponding Data Direction Register (DDR), which is used to configure the port pins as inputs or outputs. Some of these ports pins are multiplexed with alternate functions.

PORTC, PORTD, and PORTE are multiplexed with the system bus. These pins are configured as the system bus when the device's configuration bits are selected to Microprocessor or Extended Microcontroller modes. In the two other microcontroller modes, these pins are general purpose I/O.

PORTA, PORTB, PORTE<3>, PORTF, PORTG and the upper four bits of PORTH are multiplexed with the peripheral features of the device. These peripheral features are:

- Timer Modules
- Capture Modules
- PWM Modules
- USART/SCI Modules
- SSP Module
- A/D Module
- External Interrupt pin

When some of these peripheral modules are turned on, the port pin will automatically configure to the alternate function. The modules that do this are:

- PWM Module
- SSP Module
- USART/SCI Module

When a pin is automatically configured as an output by a peripheral module, the pins data direction (DDR) bit is unknown. After disabling the peripheral module, the user should re-initialize the DDR bit to the desired configuration.

The other peripheral modules (which require an input) must have their data direction bits configured appropriately.

Note:	A pin that is a peripheral input, can be con-
	figured as an output (DDRx <y> is cleared).</y>
	The peripheral events will be determined
	by the action output on the port pin.

When the device enters the "RESET state", the Data Direction registers (DDR) are forced set, which will make the I/O hi-impedance inputs. The RESET state of some peripheral modules may force the I/O to other operations, such as analog inputs or the system bus.



TABLE 10-1: **PORTA FUNCTIONS**

FIGURE 10-4: **RA4 AND RA5 BLOCK** DIAGRAM Serial Port Input Signal Data Bus RD PORTA (Q2) Serial Port Output Signals OE = SPEN, SYNC, TXEN, CREN, SREN for RA4 \overline{OE} = SPEN (\overline{SYNC} +SYNC, \overline{CSRC}) for RA5 Note: I/O pins have protection diodes to VDD and Vss.

Name	Bit0	Buffer Type	Function
RA0/INT	bit0	ST	Input or external interrupt input.
RA1/T0CKI	bit1	ST	Input or clock input to the TMR0 timer/counter and/or an external interrupt input.
RA2/SS/SCL	bit2	ST	Input/output or slave select input for the SPI, or clock input for the I ² C bus. Output is open drain type.
RA3/SDI/SDA	bit3	ST	Input/output or data input for the SPI, or data for the I ² C bus. Output is open drain type.
RA4/RX1/DT1	bit4	ST	Input or USART1 Asynchronous Receive input, or USART1 Synchronous Data input/output.
RA5/TX1/CK1	bit5	ST	Input or USART1 Asynchronous Transmit output, or USART1 Synchronous Clock input/output.
RBPU	bit7	—	Control bit for PORTB weak pull-ups.

Legend: ST = Schmitt Trigger input

TABLE 10-2: REGISTERS/BITS ASSOCIATED WITH PORTA

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	MCLR, WDT
10h, Bank 0	PORTA ⁽¹⁾	RBPU	—	RA5/ TX1/CK1	RA4/ RX1/DT1	RA3/ SDI/SDA	<u>R</u> A2/ SS/SCL	RA1/T0CKI	RA0/INT	0-xx 11xx	0-uu 11uu
05h, Unbanked	TOSTA	INTEDG	TOSE	TOCS	T0PS3	T0PS2	T0PS1	T0PS0	_	0000 000-	0000 000-
13h, Bank 0	RCSTA1	SPEN	RX9	SREN	CREN		FERR	OERR	RX9D	0000 -00x	0000 -00u
15h, Bank 0	TXSTA1	CSRC	TX9	TXEN	SYNC	_	_	TRMT	TX9D	00001x	00001u

Legend: x = unknown, u = unchanged, - = unimplemented, reads as '0'. Shaded cells are not used by PORTA. **Note 1:** On any device RESET, these pins are configured as inputs.

10.5 PORTE and DDRE Register

PORTE is a 4-bit bi-directional port. The corresponding data direction register is DDRE. A '1' in DDRE configures the corresponding port pin as an input. A '0' in the DDRE register configures the corresponding port pin as an output. Reading PORTE reads the status of the pins, whereas writing to PORTE will write to the port latch. PORTE is multiplexed with the system bus. When operating as the system bus, PORTE contains the control signals for the address/data bus (AD15:AD0). These control signals are Address Latch Enable (ALE), Output Enable (OE) and Write (WR). The control signals OE and WR are active low signals. The timing for the system bus is shown in the Electrical Specifications section.

Note: Three pins of this port are configured as the system bus when the device's configuration bits are selected to Microprocessor or Extended Microcontroller modes. The other pin is a general purpose I/O or Capture4 pin. In the two other microcontroller modes, RE2:RE0 are general purpose I/O pins. Example 10-5 shows an instruction sequence to initialize PORTE. The Bank Select Register (BSR) must be selected to Bank 1 for the port to be initialized. The following example uses the MOVLB instruction to load the BSR register for bank selection.

EXAMPLE 10-5: INITIALIZING PORTE

MOVLB	1		;	Select Bank 1
CLRF	PORTE,	F	;	Initialize PORTE data
			;	latches before setting
			;	the data direction
			;	register
MOVLW	0x03		;	Value used to initialize
			;	data direction
MOVWF	DDRE		;	Set RE<1:0> as inputs
			;	RE<3:2> as outputs
			;	RE<7:4> are always
			;	read as '0'

FIGURE 10-11: BLOCK DIAGRAM OF RE2:RE0 (IN I/O PORT MODE)



TABLE 10-11: PORTF FUNCTIONS

Name	Bit	Buffer Type	Function
RF0/AN4	bit0	ST	Input/output or analog input 4.
RF1/AN5	bit1	ST	Input/output or analog input 5.
RF2/AN6	bit2	ST	Input/output or analog input 6.
RF3/AN7	bit3	ST	Input/output or analog input 7.
RF4/AN8	bit4	ST	Input/output or analog input 8.
RF5/AN9	bit5	ST	Input/output or analog input 9.
RF6/AN10	bit6	ST	Input/output or analog input 10.
RF7/AN11	bit7	ST	Input/output or analog input 11.

Legend: ST = Schmitt Trigger input

TABLE 10-12: REGISTERS/BITS ASSOCIATED WITH PORTF

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	MCLR, WDT
10h, Bank 5	DDRF	Data Dir	ection Reg	gister for P	ORTF					1111 1111	1111 1111
11h, Bank 5	PORTF	RF7/ AN11	RF6/ AN10	RF5/ AN9	RF4/ AN8	RF3/ AN7	RF2/ AN6	RF1/ AN5	RF0/ AN4	0000 0000	0000 0000
15h, Bank 5	ADCON1	ADCS1	ADCS0	ADFM		PCFG3	PCFG2	PCFG1	PCFG0	000- 0000	000- 0000

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by PORTF.

13.0 TIMER1, TIMER2, TIMER3, PWMS AND CAPTURES

The PIC17C7XX has a wealth of timers and time based functions to ease the implementation of control applications. These time base functions include three PWM outputs and four Capture inputs.

Timer1 and Timer2 are two 8-bit incrementing timers, each with an 8-bit period register (PR1 and PR2, respectively) and separate overflow interrupt flags. Timer1 and Timer2 can operate either as timers (increment on internal FOSC/4 clock), or as counters (increment on falling edge of external clock on pin RB4/TCLK12). They are also software configurable to operate as a single 16-bit timer/counter. These timers are also used as the time base for the PWM (Pulse Width Modulation) modules.

Timer3 is a 16-bit timer/counter which uses the TMR3H and TMR3L registers. Timer3 also has two additional registers (PR3H/CA1H:PR3L/CA1L) that are configurable as a 16-bit period register or a 16-bit capture register. TMR3 can be software configured to increment from the internal system clock (FOSC/4), or from an external signal on the RB5/TCLK3 pin. Timer3 is the time base for all of the 16-bit captures.

Six other registers comprise the Capture2, Capture3, and Capture4 registers (CA2H:CA2L, CA3H:CA3L, and CA4H:CA4L).

Figure 13-1, Figure 13-2 and Figure 13-3 are the control registers for the operation of Timer1, Timer2 and Timer3, as well as PWM1, PWM2, PWM3, Capture1, Capture2, Capture3 and Capture4.

Table 13-1 shows the Timer resource requirements for these time base functions. Each timer is an open resource so that multiple functions may operate with it.

TABLE 13-1: TIME-BASE FUNCTION/ RESOURCE REQUIREMENTS

Time Base Function	Timer Resource
PWM1	Timer1
PWM2	Timer1 or Timer2
PWM3	Timer1 or Timer2
Capture1	Timer3
Capture2	Timer3
Capture3	Timer3
Capture4	Timer3

REGISTER 13-1: TCON1 REGISTER (ADDRESS: 16h, BANK 3)

	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0					
	CA2ED1	CA2ED0	CA1ED1	CA1ED0	T16	TMR3CS	TMR2CS	TMR1CS					
	bit 7							bit 0					
bit 7-6	CA2ED1:0	CA2ED0: Ca	pture2 Mode	e Select bits									
	00 = Capture on every falling edge												
	 01 = Capture on every rising edge 10 = Capture on every 4th rising edge 11 = Capture on every 16th rising edge 												
bit 5-4	CA1ED1:0	CA1ED0: Ca	pture1 Mode	e Select bits									
	00 = Capt	ure on every	falling edge										
	01 = Capte	ure on every	rising edge	lara									
	10 = Captill	ure on every	4th rising et	age									
bit 3	T16 . Time	r2·Timer1 M	nde Select h	it									
bito	1 = Timer2	2 and Timer1	form a 16-b	it timer									
	0 = Timer2	2 and Timer1	are two 8-b	it timers									
bit 2	TMR3CS:	Timer3 Cloc	k Source Se	lect bit									
	1 = TMR3	increments	off the falling	edge of the	RB5/TCLK3	3 pin							
1.11.4	0 = 1 MR3		off the intern										
bit 1	TMR2CS: Timer2 Clock Source Select bit												
	0 = TMR2	increments	off the intern	al clock		iz pin							
bit 0	TMR1CS:	Timer1 Cloc	k Source Se	lect bit									
	1 = TMR1	increments	off the falling	edge of the	RB4/TCLK1	l 2 pin							
	0 = TMR1	increments	off the intern	al clock									
								1					
	Legend:												
	R = Reada	ble bit	W = W	/ritable bit	U = Unin	nplemented b	oit, read as '()'					
	- n = Value	at POR Res	et '1' = B	it is set	'0' = Bit i	s cleared	x = Bit is u	nknown					

14.4 USART Synchronous Slave Mode

The Synchronous Slave mode differs from the Master mode, in the fact that the shift clock is supplied externally at the TX/CK pin (instead of being supplied internally in the Master mode). This allows the device to transfer or receive data in the SLEEP mode. The Slave mode is entered by clearing the CSRC (TXSTA<7>) bit.

14.4.1 USART SYNCHRONOUS SLAVE TRANSMIT

The operation of the SYNC Master and Slave modes are identical except in the case of the SLEEP mode.

If two words are written to TXREG and then the SLEEP instruction executes, the following will occur. The first word will immediately transfer to the TSR and will transmit as the shift clock is supplied. The second word will remain in TXREG. TXIF will not be set. When the first word has been shifted out of TSR, TXREG will transfer the second word to the TSR and the TXIF flag will now be set. If TXIE is enabled, the interrupt will wake the chip from SLEEP and if the global interrupt is enabled, then the program will branch to the interrupt vector (0020h).

Steps to follow when setting up a Synchronous Slave Transmission:

- 1. Enable the synchronous slave serial port by setting the SYNC and SPEN bits and clearing the CSRC bit.
- 2. Clear the CREN bit.
- 3. If interrupts are desired, then set the TXIE bit.
- 4. If 9-bit transmission is desired, then set the TX9 bit.
- 5. If 9-bit transmission is selected, the ninth bit should be loaded in TX9D.
- 6. Start transmission by loading data to TXREG.
- 7. Enable the transmission by setting TXEN.

Writing the transmit data to the TXREG, then enabling the transmit (setting TXEN), allows transmission to start sooner than doing these two events in the reverse order.



14.4.2 USART SYNCHRONOUS SLAVE RECEPTION

Operation of the Synchronous Master and Slave modes are identical except in the case of the SLEEP mode. Also, SREN is a "don't care" in Slave mode.

If receive is enabled (CREN) prior to the SLEEP instruction, then a word may be received during SLEEP. On completely receiving the word, the RSR will transfer the data to RCREG (setting RCIF) and if the RCIE bit is set, the interrupt generated will wake the chip from SLEEP. If the global interrupt is enabled, the program will branch to the interrupt vector (0020h).

Steps to follow when setting up a Synchronous Slave Reception:

- 1. Enable the synchronous master serial port by setting the SYNC and SPEN bits and clearing the CSRC bit.
- 2. If interrupts are desired, then set the RCIE bit.
- 3. If 9-bit reception is desired, then set the RX9 bit.
- 4. To enable reception, set the CREN bit.
- The RCIF bit will be set when reception is complete and an interrupt will be generated if the RCIE bit was set.
- 6. Read RCSTA to get the ninth bit (if enabled) and determine if any error occurred during reception.
- 7. Read the 8-bit received data by reading RCREG.
- 8. If any error occurred, clear the error by clearing the CREN bit.

Note: To abort reception, either clear the SPEN bit, or the CREN bit (when in Continuous Receive mode). This will reset the receive logic, so that it will be in the proper state when receive is re-enabled.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	MCLR, WDT
16h, Bank 1	PIR1	RBIF	TMR3IF	TMR2IF	TMR1IF	CA2IF	CA1IF	TX1IF	RC1IF	x000 0010	u000 0010
17h, Bank 1	PIE1	RBIE	TMR3IE	TMR2IE	TMR1IE	CA2IE	CA1IE	TX1IE	RC1IE	0000 0000	0000 0000
13h, Bank 0	RCSTA1	SPEN	RX9	SREN	CREN	_	FERR	OERR	RX9D	0000 -00x	0000 -00u
15h, Bank 0	TXSTA1	CSRC	TX9	TXEN	SYNC	—	_	TRMT	TX9D	00001x	00001u
16h, Bank 0	TXREG1	TX7	TX6	TX5	TX4	TX3	TX2	TX1	TX0	XXXX XXXX	uuuu uuuu
17h, Bank 0	SPBRG1	Baud Rate	Generato	r Register						0000 0000	0000 0000
10h, Bank 4	PIR2	SSPIF	BCLIF	ADIF	-	CA4IF	CA3IF	TX2IF	RC2IF	000- 0010	000- 0010
11h, Bank 4	PIE2	SSPIE	BCLIE	ADIE	-	CA4IE	CA3IE	TX2IE	RC2IE	000- 0000	000- 0000
13h, Bank 4	RCSTA2	SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D	0000 -00x	0000 -00u
16h, Bank 4	TXREG2	TX7	TX6	TX5	TX4	TX3	TX2	TX1	TX0	XXXX XXXX	uuuu uuuu
15h, Bank 4	TXSTA2	CSRC	TX9	TXEN	SYNC	—	—	TRMT	TX9D	00001x	00001u
17h, Bank 4	SPBRG2	Baud Rate	Generato	r Register						0000 0000	0000 0000

TABLE 14-10: REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE TRANSMISSION

Legend: x = unknown, u = unchanged, - = unimplemented, read as a '0'. Shaded cells are not used for synchronous slave transmission.

TABLE 14-11:	REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE RECEPTION
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Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	MCLR, WDT
16h, Bank1	PIR1	RBIF	TMR3IF	TMR2IF	TMR1IF	CA2IF	CA1IF	TX1IF	RC1IF	x000 0010	u000 0010
17h, Bank1	PIE1	RBIE	TMR3IE	TMR2IE	TMR1IE	CA2IE	CA1IE	TX1IE	RC1IE	0000 0000	0000 0000
13h, Bank0	RCSTA1	SPEN	RX9	SREN	CREN	_	FERR	OERR	RX9D	0000 - 00x	0000 -00u
14h, Bank0	RCREG1	RX7	RX6	RX5	RX4	RX3	RX2	RX1	RX0	xxxx xxxx	uuuu uuuu
15h, Bank 0	TXSTA1	CSRC	TX9	TXEN	SYNC	_	_	TRMT	TX9D	00001x	00001u
17h, Bank 0	SPBRG1	Baud Rate	Generato	r Register						0000 0000	0000 0000
10h, Bank 4	PIR2	SSPIF	BCLIF	ADIF	_	CA4IF	CA3IF	TX2IF	RC2IF	000- 0010	000- 0010
11h, Bank 4	PIE2	SSPIE	BCLIE	ADIE	_	CA4IE	CA3IE	TX2IE	RC2IE	000- 0000	000- 0000
13h, Bank 4	RCSTA2	SPEN	RX9	SREN	CREN	_	FERR	OERR	RX9D	0000 -00x	0000 -00u
14h, Bank 4	RCREG2	RX7	RX6	RX5	RX4	RX3	RX2	RX1	RX0	xxxx xxxx	uuuu uuuu
15h, Bank 4	TXSTA2	CSRC	TX9	TXEN	SYNC	_	—	TRMT	TX9D	00001x	00001u
17h, Bank 4	SPBRG2	Baud Rate	Generato	r Register						0000 0000	0000 0000

Legend: x = unknown, u = unchanged, - = unimplemented, read as a '0'. Shaded cells are not used for synchronous slave reception.

15.1.4 MASTER MODE

The master can initiate the data transfer at any time because it controls the SCK. The master determines when the slave (Processor 2, Figure 15-5) is to broadcast data by the software protocol.

In Master mode, the data is transmitted/received as soon as the SSPBUF register is written to. If the SPI is only going to receive, the SDO output could be disabled (programmed as an input). The SSPSR register will continue to shift in the signal present on the SDI pin at the programmed clock rate. As each byte is received, it will be loaded into the SSPBUF register as if a normal received byte (interrupts and status bits appropriately set). This could be useful in receiver applications as a "Line Activity Monitor" mode.

The clock polarity is selected by appropriately programming bit CKP (SSPCON1<4>). This then, would give waveforms for SPI communication as shown in

Figure 15-6, Figure 15-8 and Figure 15-9, where the MSb is transmitted first. In Master mode, the SPI clock rate (bit rate) is user programmable to be one of the following:

- Fosc/4 (or Tcy)
- Fosc/16 (or 4 Tcy)
- Fosc/64 (or 16 Tcy)
- Timer2 output/2

This allows a maximum bit clock frequency (at 33 MHz) of 8.25 MHz.

Figure 15-6 shows the waveforms for Master mode. When CKE = 1, the SDO data is valid before there is a clock edge on SCK. The change of the input sample is shown based on the state of the SMP bit. The time when the SSPBUF is loaded with the received data is shown.



FIGURE 15-6: SPI MODE WAVEFORM (MASTER MODE)





PIC17C7XX

FIGURE 15-30: ACKNOWLEDGE FLOW CHART



FIGURE 15-32: STOP CONDITION FLOW CHART



16.2 Selecting the A/D Conversion Clock

The A/D conversion time per bit is defined as TAD. The A/D conversion requires a minimum 12TAD per 10-bit conversion. The source of the A/D conversion clock is software selected. The four possible options for TAD are:

- 8Tosc
- 32Tosc
- 64Tosc
- Internal RC oscillator

For correct A/D conversions, the A/D conversion clock (TAD) must be selected to ensure a minimum TAD time of 1.6 $\mu s.$

Table 16-1 and Table 16-2 show the resultant TAD times derived from the device operating frequencies and the A/D clock source selected. These times are for standard voltage range devices.

TABLE 16-1: TAD VS. DEVICE OPERATING FREQUENCIES (STANDARD DEVICES (C))

AD Clock S	Max Fosc		
Operation	ADCS1:ADCS0	(MHz)	
8Tosc	00	5	
32Tosc	01	20	
64Tosc	10	33	
RC	11	_	

Note: When the device frequency is greater than 1 MHz, the RC A/D conversion clock source is only recommended for SLEEP operation.

TABLE 16-2: TAD VS. DEVICE OPERATING FREQUENCIES (EXTENDED VOLTAGE DEVICES (LC))

AD Clock S	Max Fosc		
Operation	ADCS1:ADCS0	(MHz)	
8Tosc	00	2.67	
32Tosc	01	10.67	
64Tosc	10	21.33	
RC	11	_	

Note: When the device frequency is greater than 1 MHz, the RC A/D conversion clock source is only recommended for SLEEP operation.

ADD	OWFC	ADD WREG and Carry bit to f					
Syntax: [label] ADDWFC f,d				f,d			
Ope	rands:	$0 \le f \le 255$ d $\in [0,1]$	$\begin{array}{l} 0 \leq f \leq 255 \\ d \in [0,1] \end{array}$				
Ope	ration:	(WREG) +	$(WREG) + (f) + C \rightarrow (dest)$				
State	us Affected:	OV, C, DC	OV, C, DC, Z				
Enco	oding:	0001	000d	ffff	ffff		
Description: Ac m pla pla pla		Add WREG memory loc placed in W placed in da	, the Carr ation 'f'. If /REG. If 'c ata memo	y Flag and 'd' is 0, th I' is 1, the ry location	l data e result is result is n 'f'.		
Wor	ds:	1					
Cycles:		1					
Q Cycle Activity:							
	Q1	Q2	Q3		Q4		
	Decode	Read register 'f'	Proces Data	ss W des	rite to tination		
<u>Exa</u>	<u>mple</u> :	ADDWFC	REG	0			
	Before Instru Carry bit REG WREG	iction = 1 = 0x02 = 0x4D					
	After Instruct	tion = 0					

AND	LW	And Liter	And Literal with WREG					
Synt	ax: [<i>label</i>] ANDLW k							
Ope	rands:	$0 \le k \le 25$	5					
Ope	ration:	(WREG) .AND. (k) \rightarrow (WREG)				EG)		
Statu	us Affected:	Z	Z					
Enco	oding:	1011	1011 0101 kkkk kkkk					
Description: The contents of WREG are AND'ed the 8-bit literal 'k'. The result is place WREG.			D'ed with placed in					
Words:		1	1					
Cycl	es:	1						
QC	cle Activity:							
	Q1	Q2	Q3	3		Q4		
	Decode	Read literal 'k'	Proce Dat	ess a	V V	Vrite to VREG		
Exar	<u>nple</u> :	ANDLW	0x5F					
	Before Instruction							

WREG = 0xA3 After Instruction WREG = 0x03

Carry bit	=	0
REG	=	0x02
WREG	=	0x50

			Standard Operating Conditions (unless otherwise state				Inless otherwise stated)	
PIC17LC7XX	-08		Operating temperature					
(Commercial, Industrial)		-40°C \leq TA \leq +85°C for industrial and						
			$0^{\circ}C \leq TA \leq +70^{\circ}C$ for commercial					
PIC17C7XX-16			Standard Operating Conditions (unless otherwise stated)					
(Commercial, Industrial, Extended)			Operating temperature					
PIC17C7XX-33		$-40^{\circ}C \le TA \le +125^{\circ}C$ for extended						
(Commerci	al, Industria	I, Extended)	$-40^{\circ}\text{C} \le \text{TA} \le +85^{\circ}\text{C}$ for industrial					
Derem	C	Characteristic	Mire	$0^{\circ}C \leq IA \leq +70^{\circ}C$ for commer				
Param.	Sym	Characteristic	IVIIN	турт	wax	Units	Conditions	
D010	חח	Supply Current (Note 2))					
DOTO			.) 	2	6	m۸	$E_{000} = 4 \text{ MHz} (\text{Note } 4)$	
D010				3	0	mA		
D010				3	6	mA		
D011		PIC1/LC/XX	_	5	10	mA	FOSC = 8 MHz	
D011		PIC17C7XX	-	5	10	mA	Fosc = 8 MHz	
D012			—	9	18	mA	FOSC = 16 MHz	
D014		PIC17LC7XX	—	85	150	μA	Fosc = 32 kHz,	
_							(EC osc configuration)	
D015		PIC17C7XX	—	15	30	mA	Fosc = 33 MHz	
D021	IPD	Power-down Current (N	Note 3)	-	-			
		PIC17LC7XX	—	<1	5	μA	VDD = 3.0V, WDT disabled	
D021		PIC17C7XX	—	<1	20	μΑ	VDD = 5.5V, WDT disabled	
(commercial,								
industrial)								
D021A			—	2	20	μA	VDD = 5.5V, WDT disabled	
(extended)								
		Module Differential Current						
D023	∆lbor	BOR circuitry	-	75	150	μA	VDD = 4.5V, BODEN	
							enabled	
D024	∆IWDT	Watchdog Timer	-	10	35	μA	VDD = 5.5V	
D026	∆IAD	A/D converter	-	1	-	μA	VDD = 5.5V, A/D not	
							converting	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

<u>OSC1</u> = external square wave, from rail to rail; all I/O pins tri-stated, pulled to VDD or VSS, T0CKI = VDD, MCLR = VDD; WDT disabled.

Current consumed from the oscillator and I/O's driving external capacitive or resistive loads needs to be considered.

For the RC oscillator, the current through the external pull-up resistor (R) can be estimated as: $VDD/(2 \bullet R)$.

For capacitive loads, the current can be estimated (for an individual I/O pin) as (CL \bullet VDD) \bullet f

CL = Total capacitive load on the I/O pin; f = average frequency the I/O pin switches.

The capacitive currents are most significant when the device is configured for external execution (includes Extended Microcontroller mode).

- **3:** The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or Vss.
- 4: For RC osc configuration, current through REXT is not included. The current through the resistor can be estimated by the formula IR = VDD/2REXT (mA) with REXT in kOhm.
- **5:** This is the voltage where the device enters the Brown-out Reset. When BOR is enabled, the device (-16) will operate correctly to this trip point.





TABLE 20-9: SPI MODE REQUIREMENTS (MASTER MODE, CKE = 1)

Param. No.	Symbol	Characteristic		Min	Тур†	Max	Units	Conditions
71	TscH	SCK input high time	Continuous	1.25Tcy + 30	—	-	ns	
71A		(Slave mode)	Single Byte	40	—	—	ns	(Note 1)
72	TscL	SCK input low time	Continuous	1.25 Tcy + 30	_	-	ns	
72A		(Slave mode)	Single Byte	40	—	—	ns	(Note 1)
73	TdiV2scH, TdiV2scL	Setup time of SDI data input to SCK edge		100	Ι	Ι	ns	
73A	Тв2в	Last clock edge of Byte1 to the 1st clock edge of Byte2		1.5Tcy + 40	—	_	ns	(Note 1)
74	TscH2diL, TscL2diL	Hold time of SDI data input to SCK edge		100	_	_	ns	
75	TdoR	SDO data output rise time		_	10	25	ns	
76	TdoF	SDO data output fall time		—	10	25	ns	
78	TscR	SCK output rise time (Master mode)		—	10	25	ns	
79	TscF	SCK output fall time (Master mode)		—	10	25	ns	
80	TscH2doV, TscL2doV	SDO data output valid after SCK edge		—		50	ns	
81	TdoV2scH, TdoV2scL	SDO data output setup to SCK	edge	Тсу	-	_	ns	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated.

Note 1: Specification 73A is only required if specifications 71A and 72A are used.





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