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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	50
Program Memory Size	32KB (16K x 16)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	902 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic17c756at-16-pt

TABLE 5-4: **INITIALIZATION CONDITIONS FOR SPECIAL FUNCTION REGISTERS**

Register	Address	Power-on Reset Brown-out Reset	MCLR Reset WDT Reset	Wake-up from SLEEP through Interrupt
Unbanked				
INDF0	00h	N/A	N/A	N/A
FSR0	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	02h	0000h	0000h	PC + 1[2]
PCLATH	03h	0000 0000	uuuu uuuu	uuuu uuuu
ALUSTA	04h	1111 xxxx	1111 uuuu	1111 uuuu
T0STA	05h	0000 000-	0000 000-	0000 000-
CPUSTA[3]	06h	--11 11qq	--11 qquu	--uu qquu
INTSTA	07h	0000 0000	0000 0000	uuuu uuuu[1]
INDF1	08h	N/A	N/A	N/A
FSR1	09h	xxxx xxxx	uuuu uuuu	uuuu uuuu
WREG	0Ah	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR0L	0Bh	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR0H	0Ch	xxxx xxxx	uuuu uuuu	uuuu uuuu
TBLPTRL	0Dh	0000 0000	0000 0000	uuuu uuuu
TBLPTRH	0Eh	0000 0000	0000 0000	uuuu uuuu
BSR	0Fh	0000 0000	0000 0000	uuuu uuuu
Bank 0				
PORTA[4,6]	10h	0-xx 11xx	0-uu 11uu	u-uu uuuu
DDRB	11h	1111 1111	1111 1111	uuuu uuuu
PORTB[4]	12h	xxxx xxxx	uuuu uuuu	uuuu uuuu
RCSTA1	13h	0000 -00x	0000 -00u	uuuu -uuu
RCREG1	14h	xxxx xxxx	uuuu uuuu	uuuu uuuu
TXSTA1	15h	0000 --1x	0000 --1u	uuuu --uu
TXREG1	16h	xxxx xxxx	uuuu uuuu	uuuu uuuu
SPBRG1	17h	0000 0000	0000 0000	uuuu uuuu

Legend: u = unchanged, x = unknown, - = unimplemented, read as '0', q = value depends on condition

Note 1: One or more bits in INTSTA, PIR1, PIR2 will be affected (to cause wake-up).

2: When the wake-up is due to an interrupt and the GLINTD bit is cleared, the PC is loaded with the interrupt vector.

3: See Table 5-3 for RESET value of specific condition.

4: This is the value that will be in the port output latch.

5: When the device is configured for Microprocessor or Extended Microcontroller mode, the operation of this port does not rely on these registers.

6: On any device RESET, these pins are configured as inputs.

REGISTER 6-3: PIE2 REGISTER (ADDRESS: 11h, BANK 4)

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
SSPIE	BCLIE	ADIE	—	CA4IE	CA3IE	TX2IE	RC2IE

bit 7   bit 0

bit 7   **SSPIE**: Synchronous Serial Port Interrupt Enable bit
1 = Enable SSP interrupt
0 = Disable SSP interrupt

bit 6   **BCLIE**: Bus Collision Interrupt Enable bit
1 = Enable bus collision interrupt
0 = Disable bus collision interrupt

bit 5   **ADIE**: A/D Module Interrupt Enable bit
1 = Enable A/D module interrupt
0 = Disable A/D module interrupt

bit 4   **Unimplemented:** Read as '0'

bit 3   **CA4IE**: Capture4 Interrupt Enable bit
1 = Enable Capture4 interrupt
0 = Disable Capture4 interrupt

bit 2   **CA3IE**: Capture3 Interrupt Enable bit
1 = Enable Capture3 interrupt
0 = Disable Capture3 interrupt

bit 1   **TX2IE**: USART2 Transmit Interrupt Enable bit
1 = Enable USART2 Transmit buffer empty interrupt
0 = Disable USART2 Transmit buffer empty interrupt

bit 0   **RC2IE**: USART2 Receive Interrupt Enable bit
1 = Enable USART2 Receive buffer full interrupt
0 = Disable USART2 Receive buffer full interrupt

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR Reset	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

EXAMPLE 6-2:   SAVING STATUS AND WREG IN RAM (NESTED)

```
; The addresses that are used to store the CPUSTA and WREG values must be in the data memory
; address range of 1Ah - 1Fh. Up to 6 locations can be saved and restored using the MOVFP
; instruction. This instruction neither affects the status bits, nor corrupts the WREG register.
; This routine uses the FRS0, so it controls the FS1 and FS0 bits in the ALUSTA register.
;
Nobank_FSR      EQU    0x40
Bank_FSR        EQU    0x41
ALU_Temp        EQU    0x42
WREG_TEMP       EQU    0x43
BSR_S1          EQU    0x01A       ; 1st location to save BSR
BSR_S2          EQU    0x01B       ; 2nd location to save BSR (Label Not used in program)
BSR_S3          EQU    0x01C       ; 3rd location to save BSR (Label Not used in program)
BSR_S4          EQU    0x01D       ; 4th location to save BSR (Label Not used in program)
BSR_S5          EQU    0x01E       ; 5th location to save BSR (Label Not used in program)
BSR_S6          EQU    0x01F       ; 6th location to save BSR (Label Not used in program)
;
INITIALIZATION                     ;
        CALL    CLEAR_RAM          ; Must Clear all Data RAM
;
INIT_POINTERS                      ; Must Initialize the pointers for POP and PUSH
        CLRF    BSR, F             ; Set All banks to 0
        CLRF    ALUSTA, F          ; FSR0 post increment
        BSF     ALUSTA, FS1
        CLRF    WREG, F            ; Clear WREG
        MOVLW   BSR_S1             ; Load FSR0 with 1st address to save BSR
        MOVWF   FSR0
        MOVWF   Nobank_FSR
        MOVLW   0x20
        MOVWF   Bank_FSR
        :
        :                          ; Your code
        :
        :                          ; At Interrupt Vector Address
PUSH    BSF     ALUSTA, FS0        ; FSR0 has auto-increment, does not affect status bits
        BCF     ALUSTA, FS1        ; does not affect status bits
        MOVFP   BSR, INDF0         ; No Status bits are affected
        CLRF    BSR, F             ; Peripheral and Data RAM Bank 0 No Status bits are affected
        MOVPF   ALUSTA, ALU_Temp   ;
        MOVPF   FSR0, Nobank_FSR   ; Save the FSR for BSR values
        MOVPF   WREG, WREG_TEMP    ;
        MOVFP   Bank_FSR, FSR0     ; Restore FSR value for other values
        MOVFP   ALU_Temp, INDF0    ; Push ALUSTA value
        MOVFP   WREG_TEMP, INDF0   ; Push WREG value
        MOVFP   PCLATH, INDF0      ; Push PCLATH value
        MOVPF   FSR0, Bank_FSR     ; Restore FSR value for other values
        MOVFP   Nobank_FSR, FSR0   ;
        ;
        :                          ; Interrupt Service Routine (ISR) code
        ;
POP     CLRF    ALUSTA, F          ; FSR0 has auto-decrement, does not affect status bits
        MOVFP   Bank_FSR, FSR0     ; Restore FSR value for other values
        DECF    FSR0, F            ;
        MOVFP   INDF0, PCLATH      ; Pop PCLATH value
        MOVFP   INDF0, WREG        ; Pop WREG value
        BSF     ALUSTA, FS1        ; FSR0 does not change
        MOVPF   INDF0, ALU_Temp    ; Pop ALUSTA value
        MOVPF   FSR0, Bank_FSR     ; Restore FSR value for other values
        DECF    Nobank_FSR, F      ;
        MOVFP   Nobank_FSR, FSR0   ; Save the FSR for BSR values
        MOVFP   ALU_Temp, ALUSTA   ;
        MOVFP   INDF0, BSR         ; No Status bits are affected
;
        RETFIE                     ; Return from interrupt (enable interrupts)
```

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TABLE 7-1: MODE MEMORY ACCESS

Operating Mode	Internal Program Memory	Configuration Bits, Test Memory, Boot ROM
Microprocessor	No Access	No Access
Microcontroller	Access	Access
Extended Microcontroller	Access	No Access
Protected Microcontroller	Access	Access

The PIC17C7XX can operate in modes where the program memory is off-chip. They are the Microprocessor and Extended Microcontroller modes. The Microprocessor mode is the default for an unprogrammed device.

Regardless of the processor mode, data memory is always on-chip.

## FIGURE 7-2: MEMORY MAP IN DIFFERENT MODES
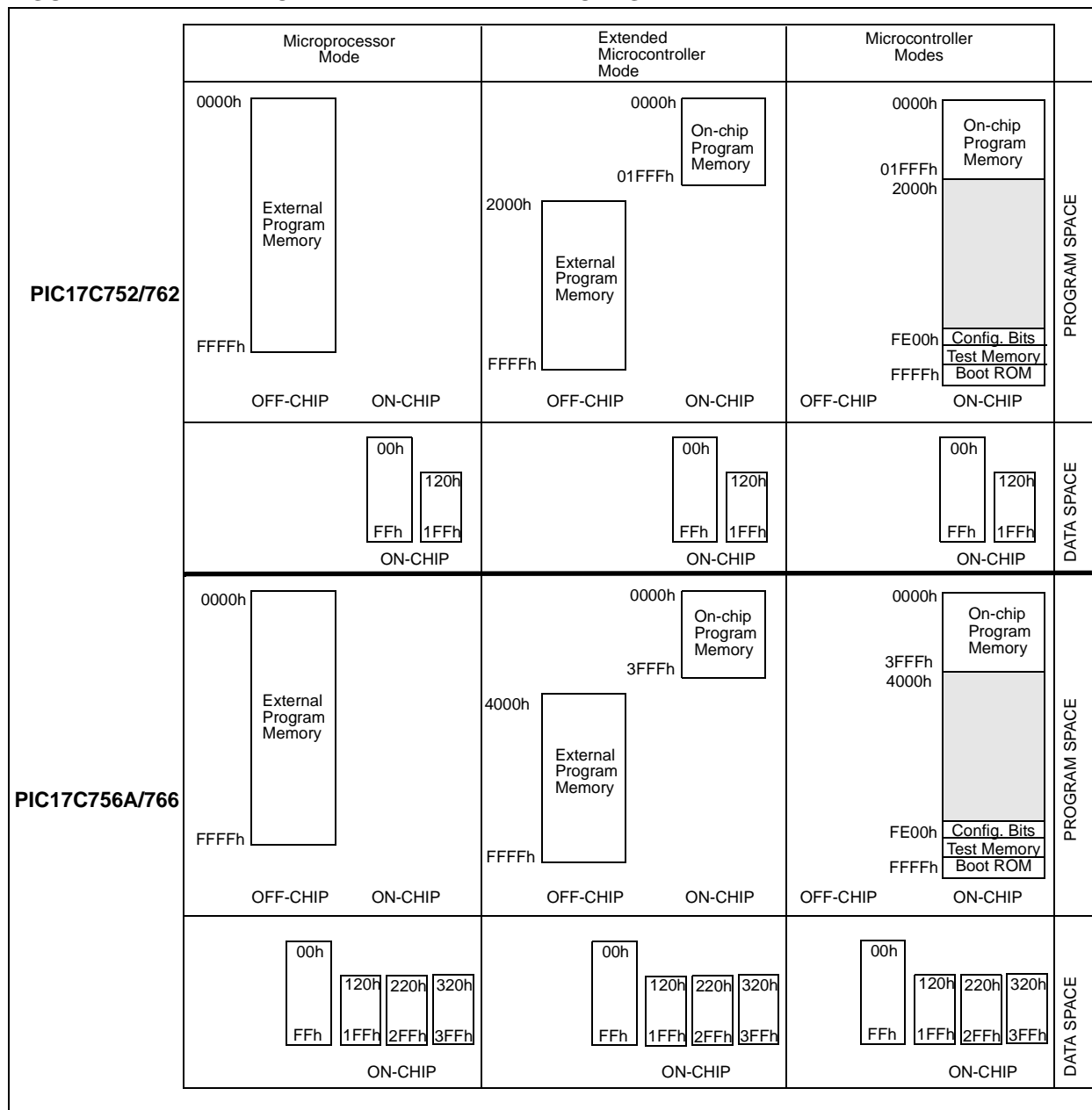
8.4 Operation with External Memory Interface

When the table reads/writes are accessing external memory (via the external system interface bus), the table latch for the table reads is different from the table latch for the table writes (see Figure 8-9).

This means that you cannot do a TABLRD instruction, and use the values that were loaded into the table latches for a TABLWT instruction. Any table write sequence should use both the TLWT and then the TABLWT instructions.

FIGURE 8-9: ACCESSING EXTERNAL MEMORY WITH TABLRD AND TABLWT INSTRUCTIONS
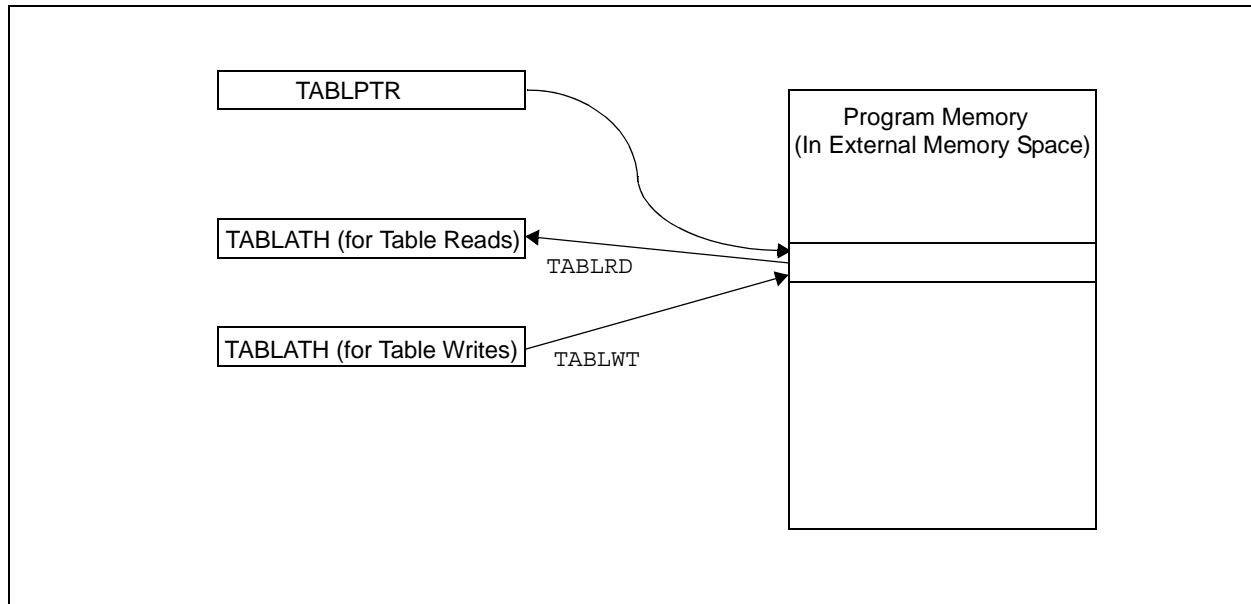
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Example 9-3 shows the sequence to do a 16 x 16 unsigned multiply. Equation 9-1 shows the algorithm that is used. The 32-bit result is stored in 4 registers, RES3:RES0.

EQUATION 9-1: 16 x 16 UNSIGNED MULTIPLICATION ALGORITHM

$$
\begin{aligned}
RES3:RES0 \quad = \quad & ARG1H:ARG1L \bullet ARG2H:ARG2L \\
= \quad & (ARG1H \bullet ARG2H \bullet 2^{16}) \quad + \\
& (ARG1H \bullet ARG2L \bullet 2^{8}) \quad + \\
& (ARG1L \bullet ARG2H \bullet 2^{8}) \quad + \\
& (ARG1L \bullet ARG2L)
\end{aligned}
$$

EXAMPLE 9-3: 16 x 16 UNSIGNED MULTIPLY ROUTINE

```
    MOVFP    ARG1L, WREG
    MULWF    ARG2L         ; ARG1L * ARG2L ->
                           ;    PRODH:PRODL
    MOVPF    PRODH, RES1 ;
    MOVPF    PRODL, RES0 ;
;
    MOVFP    ARG1H, WREG
    MULWF    ARG2H         ; ARG1H * ARG2H ->
                           ;    PRODH:PRODL
    MOVPF    PRODH, RES3 ;
    MOVPF    PRODL, RES2 ;
;
    MOVFP    ARG1L, WREG
    MULWF    ARG2H         ; ARG1L * ARG2H ->
                           ;    PRODH:PRODL
    MOVFP    PRODL, WREG ;
    ADDWF    RES1, F     ; Add cross
    MOVFP    PRODH, WREG ;    products
    ADDWFC   RES2, F     ;
    CLRF     WREG, F     ;
    ADDWFC   RES3, F     ;
;
    MOVFP    ARG1H, WREG ;
    MULWF    ARG2L         ; ARG1H * ARG2L ->
                           ;    PRODH:PRODL
    MOVFP    PRODL, WREG ;
    ADDWF    RES1, F     ; Add cross
    MOVFP    PRODH, WREG ;    products
    ADDWFC   RES2, F     ;
    CLRF     WREG, F     ;
    ADDWFC   RES3, F     ;
```

14.2   USART Asynchronous Mode

In this mode, the USART uses standard nonreturn-to-zero (NRZ) format (one START bit, eight or nine data bits, and one STOP bit). The most common data format is 8-bits. An on-chip dedicated 8-bit baud rate generator can be used to derive standard baud rate frequencies from the oscillator. The USART's transmitter and receiver are functionally independent but use the same data format and baud rate. The baud rate generator produces a clock x64 of the bit shift rate. Parity is not supported by the hardware, but can be implemented in software (and stored as the ninth data bit). Asynchronous mode is stopped during SLEEP.

The Asynchronous mode is selected by clearing the SYNC bit (TXSTA<4>).

The USART Asynchronous module consists of the following components:

- Baud Rate Generator
- Sampling Circuit
- Asynchronous Transmitter
- Asynchronous Receiver

14.2.1   USART ASYNCHRONOUS TRANSMITTER

The USART transmitter block diagram is shown in Figure 14-1. The heart of the transmitter is the transmit shift register (TSR). The shift register obtains its data from the read/write transmit buffer (TXREG). TXREG is loaded with data in software. The TSR is not loaded until the STOP bit has been transmitted from the previous load. As soon as the STOP bit is transmitted, the TSR is loaded with new data from the TXREG (if available). Once TXREG transfers the data to the TSR (occurs in one T_{CY} at the end of the current BRG cycle), the TXREG is empty and an interrupt bit, TXIF, is set. This interrupt can be enabled/disabled by setting/clearing the TXIE bit. TXIF will be set, regardless of TXIE and cannot be reset in software. It will reset only when new data is loaded into TXREG. While TXIF indicates the status of the TXREG, the TRMT (TXSTA<1>) bit shows the status of the TSR.

TRMT is a read only bit which is set when the TSR is empty. No interrupt logic is tied to this bit, so the user has to poll this bit in order to determine if the TSR is empty.

> **Note:** The TSR is not mapped in data memory, so it is not available to the user.

Transmission is enabled by setting the TXEN (TXSTA<5>) bit. The actual transmission will not occur until TXREG has been loaded with data and the baud rate generator (BRG) has produced a shift clock (Figure 14-3). The transmission can also be started by first loading TXREG and then setting TXEN. Normally, when transmission is first started, the TSR is empty, so a transfer to TXREG will result in an immediate transfer to TSR, resulting in an empty TXREG. A back-to-back transfer is thus possible (Figure 14-4). Clearing TXEN during a transmission will cause the transmission to be aborted. This will reset the transmitter and the TX/CK pin will revert to hi-impedance.

In order to select 9-bit transmission, the TX9 (TXSTA<6>) bit should be set and the ninth bit value should be written to TX9D (TXSTA<0>). The ninth bit value must be written before writing the 8-bit data to the TXREG. This is because a data write to TXREG can result in an immediate transfer of the data to the TSR (if the TSR is empty).

Steps to follow when setting up an Asynchronous Transmission:

1. Initialize the SPBRG register for the appropriate baud rate.
2. Enable the asynchronous serial port by clearing the SYNC bit and setting the SPEN bit.
3. If interrupts are desired, then set the TXIE bit.
4. If 9-bit transmission is desired, then set the TX9 bit.
5. If 9-bit transmission is selected, the ninth bit should be loaded in TX9D.
6. Load data to the TXREG register.
7. Enable the transmission by setting TXEN (starts transmission).

FIGURE 14-3:   ASYNCHRONOUS MASTER TRANSMISSION
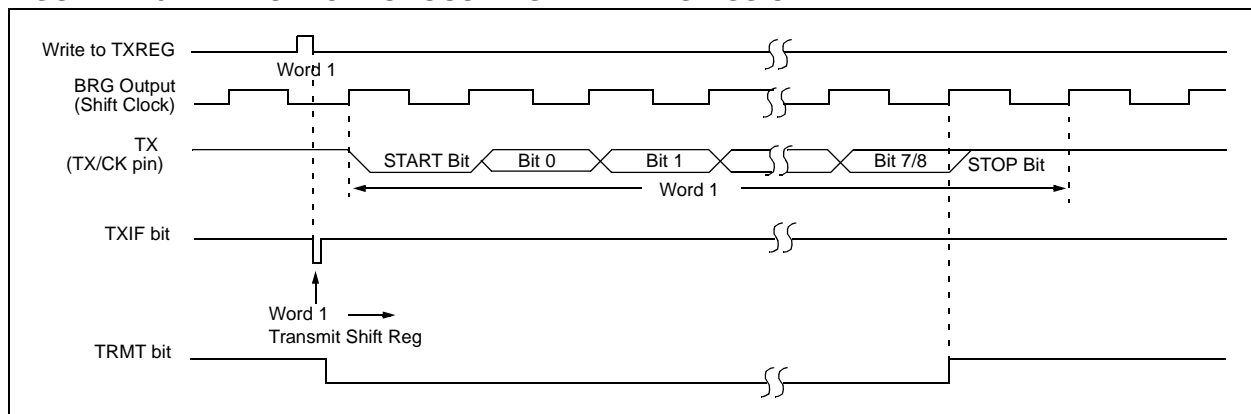
14.2.2 USART ASYNCHRONOUS RECEIVER

The receiver block diagram is shown in Figure 14-2. The data comes in the RX/DT pin and drives the data recovery block. The data recovery block is actually a high speed shifter operating at 16 times the baud rate, whereas the main receive serial shifter operates at the bit rate or at FOSC.

Once Asynchronous mode is selected, reception is enabled by setting bit CREN (RCSTA<4>).

The heart of the receiver is the receive (serial) shift register (RSR). After sampling the STOP bit, the received data in the RSR is transferred to the RCREG (if it is empty). If the transfer is complete, the interrupt bit, RCIF, is set. The actual interrupt can be enabled/disabled by setting/clearing the RCIE bit. RCIF is a read only bit which is cleared by the hardware. It is cleared when RCREG has been read and is empty. RCREG is a double buffered register (i.e., it is a two-deep FIFO). It is possible for two bytes of data to be received and transferred to the RCREG FIFO and a third byte begin shifting to the RSR. On detection of the STOP bit of the third byte, if the RCREG is still full, then the overrun error bit, OERR (RCSTA<1>) will be set. The word in the RSR will be lost. RCREG can be read twice to retrieve the two bytes in the FIFO. The OERR bit has to be cleared in software which is done by reset-ting the receive logic (CREN is set). If the OERR bit is set, transfers from the RSR to RCREG are inhibited, so it is essential to clear the OERR bit if it is set. The framing error bit FERR (RCSTA<2>) is set if a STOP bit is not detected.

> **Note:** The FERR and the 9th receive bit are buffered the same way as the receive data. Reading the RCREG register will allow the RX9D and FERR bits to be loaded with values for the next received data. Therefore, it is essential for the user to read the RCSTA register before reading RCREG, in order not to lose the old FERR and RX9D information.

14.2.3 SAMPLING

The data on the RX/DT pin is sampled three times by a majority detect circuit to determine if a high or a low level is present at the RX/DT pin. The sampling is done on the seventh, eighth and ninth falling edges of a x16 clock (Figure 14-5).

The x16 clock is a free running clock and the three sample points occur at a frequency of every 16 falling edges.

FIGURE 14-5: RX PIN SAMPLING SCHEME
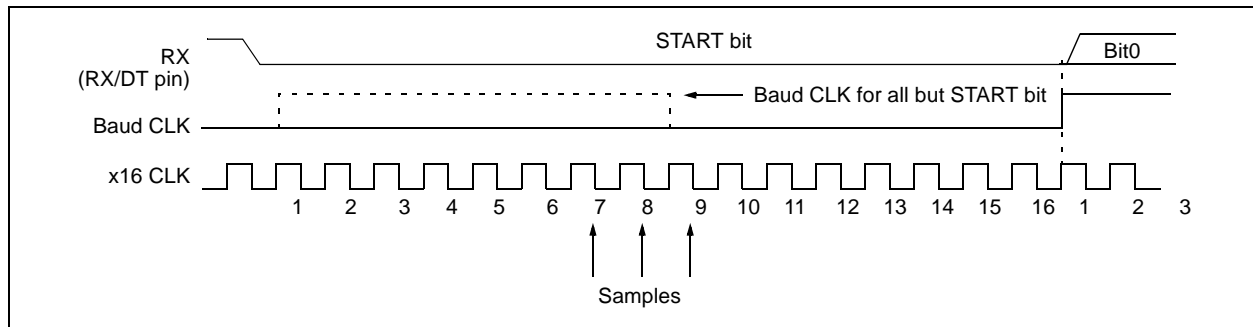
FIGURE 14-6: START BIT DETECT
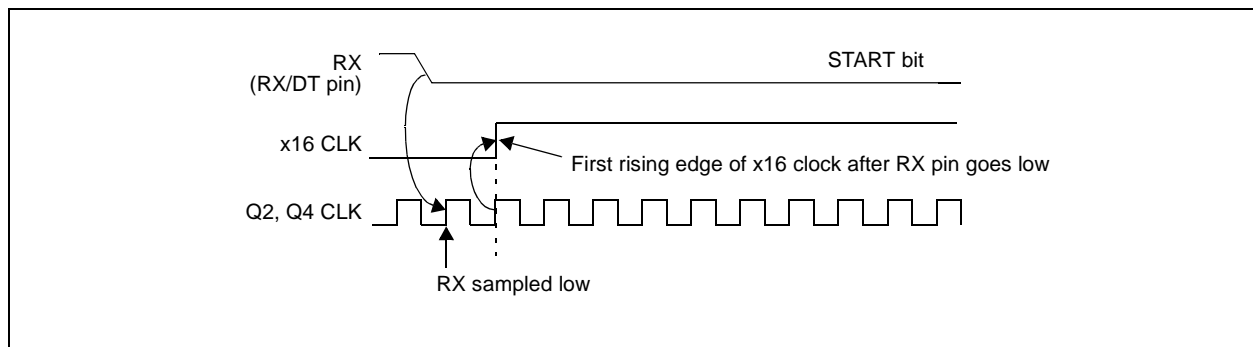
REGISTER 15-1: SSPSTAT: SYNC SERIAL PORT STATUS REGISTER (ADDRESS: 13h, BANK 6)

R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0	R-0
SMP	CKE	D/$\overline{\text{A}}$	P	S	R/$\overline{\text{W}}$	UA	BF
bit 7							bit 0

bit 7   **SMP:** Sample bit

SPI Master mode:
1 = Input data sampled at end of data output time
0 = Input data sampled at middle of data output time

SPI Slave mode:
SMP must be cleared when SPI is used in Slave mode

In I^{2}C Master or Slave mode:
1 = Slew rate control disabled for Standard Speed mode (100 kHz and 1 MHz)
0 = Slew rate control enabled for High Speed mode (400 kHz)

bit 6   **CKE**: SPI Clock Edge Select (Figure 15-6, Figure 15-8 and Figure 15-9)

CKP = 0:
1 = Data transmitted on rising edge of SCK
0 = Data transmitted on falling edge of SCK

CKP = 1:
1 = Data transmitted on falling edge of SCK
0 = Data transmitted on rising edge of SCK

bit 5   **D/$\overline{\text{A}}$**: Data/Address bit (I^{2}C mode only)
1 = Indicates that the last byte received or transmitted was data
0 = Indicates that the last byte received or transmitted was address

bit 4   **P**: STOP bit
(I^{2}C mode only. This bit is cleared when the MSSP module is disabled, SSPEN is cleared.)
1 = Indicates that a STOP bit has been detected last (this bit is '0' on RESET)
0 = STOP bit was not detected last

bit 3   **S**: START bit
(I^{2}C mode only. This bit is cleared when the MSSP module is disabled, SSPEN is cleared.)
1 = Indicates that a START bit has been detected last (this bit is '0' on RESET)
0 = START bit was not detected last

bit 2   **R/$\overline{\text{W}}$**: Read/Write bit Information (I^{2}C mode only)
This bit holds the R/W bit information following the last address match. This bit is only valid from
the address match to the next START bit, STOP bit, or not ACK bit.

In I^{2}C Slave mode:
1 = Read
0 = Write

In I^{2}C Master mode:
1 = Transmit is in progress
0 = Transmit is not in progress
Or'ing this bit with SEN, RSEN, PEN, RCEN, or ACKEN will indicate if the MSSP is in IDLE mode.

bit 1   **UA**: Update Address (10-bit I^{2}C mode only)
1 = Indicates that the user needs to update the address in the SSPADD register
0 = Address does not need to be updated

bit 0   **BF**: Buffer Full Status bit

Receive (SPI and I^{2}C modes)
1 = Receive complete, SSPBUF is full
0 = Receive not complete, SSPBUF is empty

Transmit (I^{2}C mode only)
1 = Data transmit in progress (does not include the $\overline{\text{ACK}}$ and STOP bits), SSPBUF is full
0 = Data transmit complete (does not include the $\overline{\text{ACK}}$ and STOP bits), SSPBUF is empty

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR Reset	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

REGISTER 15-2: SSPCON1: SYNC SERIAL PORT CONTROL REGISTER1 (ADDRESS 11h, BANK 6)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	$\overline{\text{SSPM1}}$	$\overline{\text{SSPM0}}$

bit 7   bit 0

bit 7   **WCOL**: Write Collision Detect bit

<u>Master mode:</u>
1 = A write to the SSPBUF register was attempted while the I^{2}C conditions were not valid for a transmission to be started
0 = No collision

<u>Slave mode:</u>
1 = The SSPBUF register is written while it is still transmitting the previous word (must be cleared in software)
0 = No collision

bit 6   **SSPOV**: Receive Overflow Indicator bit

<u>In SPI mode:</u>
1 = A new byte is received while the SSPBUF register is still holding the previous data. In case of overflow, the data in SSPSR is lost. Overflow can only occur in Slave mode. In Slave mode, the user must read the SSPBUF, even if only transmitting data, to avoid setting overflow. In Master mode, the overflow bit is not set, since each new reception (and transmission) is initiated by writing to the SSPBUF register. (Must be cleared in software.)
0 = No overflow

<u>In I^{2}C mode:</u>
1 = A byte is received while the SSPBUF register is still holding the previous byte. SSPOV is a "don't care" in Transmit mode. (Must be cleared in software.)
0 = No overflow

bit 5   **SSPEN**: Synchronous Serial Port Enable bit
In both modes, when enabled, these pins must be properly configured as input or output.

<u>In SPI mode:</u>
1 = Enables serial port and configures SCK, SDO, SDI and $\overline{\text{SS}}$ as the source of the serial port pins
0 = Disables serial port and configures these pins as I/O port pins

<u>In I^{2}C mode:</u>
1 = Enables the serial port and configures the SDA and SCL pins as the source of the serial port pins
0 = Disables serial port and configures these pins as I/O port pins

    Note: In SPI mode, these pins must be properly configured as input or output.

bit 4   **CKP**: Clock Polarity Select bit

<u>In SPI mode:</u>
1 = Idle state for clock is a high level
0 = Idle state for clock is a low level

<u>In I^{2}C Slave mode:</u>
SCK release control
1 = Enable clock
0 = Holds clock low (clock stretch). (Used to ensure data setup time.)

<u>In I^{2}C Master mode:</u>
Unused in this mode

bit 3-0   **SSPM3:SSPM0**: Synchronous Serial Port Mode Select bits
0000 = SPI Master mode, clock = F$_{OSC}$/4
0001 = SPI Master mode, clock = F$_{OSC}$/16
0010 = SPI Master mode, clock = F$_{OSC}$/64
0011 = SPI Master mode, clock = TMR2 output/2
0100 = SPI Slave mode, clock = SCK pin, $\overline{\text{SS}}$ pin control enabled
0101 = SPI Slave mode, clock = SCK pin, $\overline{\text{SS}}$ pin control disabled, $\overline{\text{SS}}$ can be used as I/O pin
0110 = I^{2}C Slave mode, 7-bit address
0111 = I^{2}C Slave mode, 10-bit address
1000 = I^{2}C Master mode, clock = F$_{OSC}$ / (4 * (SSPADD+1))
1xx1 = Reserved
1x1x = Reserved

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR Reset	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

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17.4   Power-down Mode (SLEEP)

The Power-down mode is entered by executing a SLEEP instruction. This clears the Watchdog Timer and postscaler (if enabled). The $\overline{PD}$ bit is cleared and the $\overline{TO}$ bit is set (in the CPUSTA register). In SLEEP mode, the oscillator driver is turned off. The I/O ports maintain their status (driving high,low, or hi-impedance input).

The $\overline{MCLR}$/VPP pin must be at a logic high level (VIHMC). A WDT time-out RESET does not drive the $\overline{MCLR}$/VPP pin low.

17.4.1   WAKE-UP FROM SLEEP

The device can wake-up from SLEEP through one of the following events:

- Power-on Reset
- Brown-out Reset
- External RESET input on $\overline{MCLR}$/VPP pin
- WDT Reset (if WDT was enabled)
- Interrupt from RA0/INT pin, RB port change, T0CKI interrupt, or some peripheral interrupts

The following peripheral interrupts can wake the device from SLEEP:

- Capture interrupts
- USART synchronous slave transmit interrupts
- USART synchronous slave receive interrupts
- A/D conversion complete
- SPI slave transmit/receive complete
- I^{2}C slave receive

Other peripherals cannot generate interrupts since during SLEEP, no on-chip Q clocks are present.

Any RESET event will cause a device RESET. Any interrupt event is considered a continuation of program execution. The $\overline{TO}$ and $\overline{PD}$ bits in the CPUSTA register can be used to determine the cause of a device RESET. The $\overline{PD}$ bit, which is set on power-up, is cleared when SLEEP is invoked. The $\overline{TO}$ bit is cleared if WDT time-out occurred (and caused a RESET).

When the SLEEP instruction is being executed, the next instruction (PC + 1) is pre-fetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up is regardless of the state of the GLINTD bit. If the GLINTD bit is set (disabled), the device continues execution at the instruction after the SLEEP instruction. If the GLINTD bit is clear (enabled), the device executes the instruction after the SLEEP instruction and then branches to the interrupt vector address. In cases where the execution of the instruction following SLEEP is not desirable, the user should have a NOP after the SLEEP instruction.
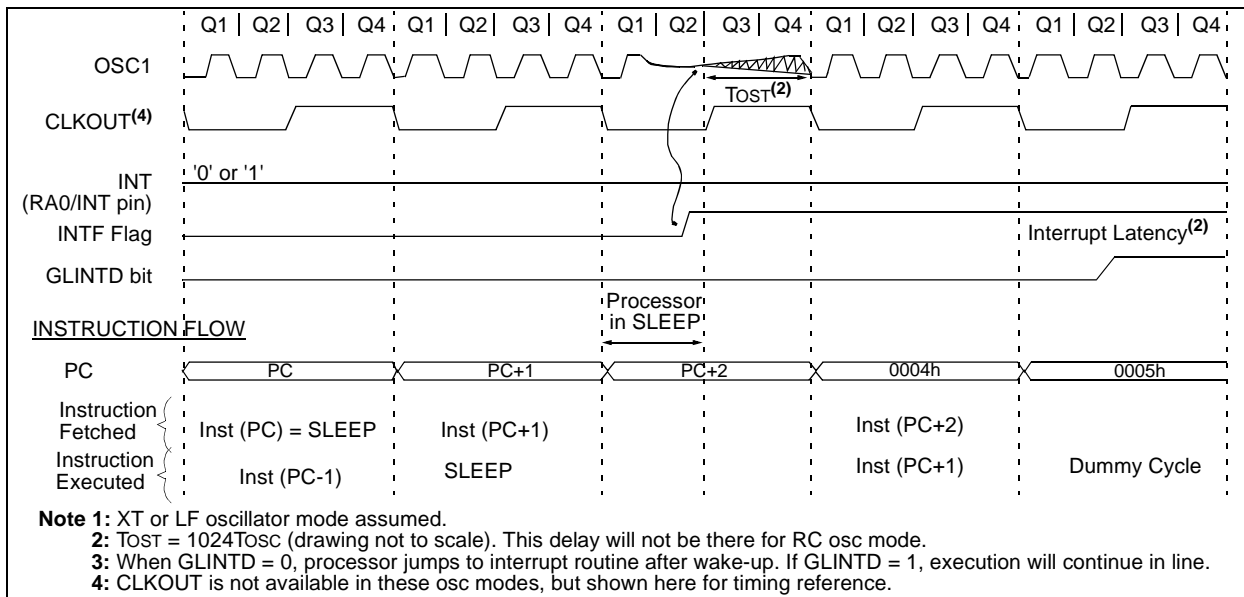
Note: If the global interrupt is disabled (GLINTD is set), but any interrupt source has both its interrupt enable bit and the corresponding interrupt flag bit set, the device will immediately wake-up from SLEEP. The $\overline{TO}$ bit is set and the $\overline{PD}$ bit is cleared.

The WDT is cleared when the device wakes from SLEEP, regardless of the source of wake-up.

17.4.1.1   Wake-up Delay

When the oscillator type is configured in XT or LF mode, the Oscillator Start-up Timer (OST) is activated on wake-up. The OST will keep the device in RESET for 1024TOSC. This needs to be taken into account when considering the interrupt response time when coming out of SLEEP.

FIGURE 17-2:   WAKE-UP FROM SLEEP THROUGH INTERRUPT

Note 1: XT or LF oscillator mode assumed.
2: TOST = 1024TOSC (drawing not to scale). This delay will not be there for RC osc mode.
3: When GLINTD = 0, processor jumps to interrupt routine after wake-up. If GLINTD = 1, execution will continue in line.
4: CLKOUT is not available in these osc modes, but shown here for timing reference.

PIC17C7XX

MOVPF	**Move p to f**
Syntax:	[*label*] MOVPF p,f
Operands:	0 ≤ f ≤ 255 0 ≤ p ≤ 31
Operation:	(p) → (f)
Status Affected:	Z

Encoding:

010p	pppp	ffff	ffff

Description: Move data from data memory location 'p' to data memory location 'f'. Location 'f' can be anywhere in the 256 byte data space (00h to FFh), while 'p' can be 00h to 1Fh.

Either 'p' or 'f' can be WREG (a useful, special situation).

MOVPF is particularly useful for transferring a peripheral register (e.g. the timer or an I/O port) to a data memory location. Both 'f' and 'p' can be indirectly addressed.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'p'	Process Data	Write register 'f'

Example: `MOVPF    REG1, REG2`

Before Instruction
- REG1 = 0x11
- REG2 = 0x33

After Instruction
- REG1 = 0x11
- REG2 = 0x11

MOVWF	**Move WREG to f**
Syntax:	[*label*] MOVWF f
Operands:	0 ≤ f ≤ 255
Operation:	(WREG) → (f)
Status Affected:	None

Encoding:

0000	0001	ffff	ffff

Description: Move data from WREG to register 'f'. Location 'f' can be anywhere in the 256 byte data space.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write register 'f'

Example: `MOVWF    REG`

Before Instruction
- WREG = 0x4F
- REG = 0xFF

After Instruction
- WREG = 0x4F
- REG = 0x4F

RLNCF	**Rotate Left f (no carry)**
Syntax:	[*label*] RLNCF f,d
Operands:	$0 \le f \le 255$ $d \in [0,1]$
Operation:	$f<n> \rightarrow d<n+1>$; $f<7> \rightarrow d<0>$
Status Affected:	None

Encoding:

0010	001d	ffff	ffff

Description: The contents of register 'f' are rotated one bit to the left. If 'd' is 0, the result is placed in WREG. If 'd' is 1, the result is stored back in register 'f'.
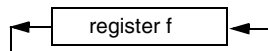
Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

Example: RLNCF   REG, 1

Before Instruction
        C   =   0
        REG   =   1110 1011

After Instruction
        C   =
        REG   =   1101 0111

RRCF	**Rotate Right f through Carry**
Syntax:	[*label*] RRCF f,d
Operands:	$0 \le f \le 255$ $d \in [0,1]$
Operation:	$f<n> \rightarrow d<n-1>$; $f<0> \rightarrow C$; $C \rightarrow d<7>$
Status Affected:	C

Encoding:

0001	100d	ffff	ffff

Description: The contents of register 'f' are rotated one bit to the right through the Carry Flag. If 'd' is 0, the result is placed in WREG. If 'd' is 1, the result is placed back in register 'f'.
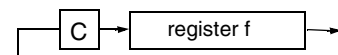
Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

Example: RRCF REG1,0

Before Instruction
        REG1   =   1110 0110
        C   =   0

After Instruction
        REG1   =   1110 0110
        WREG   =   0111 0011
        C   =   0

19.8   MPLAB ICD In-Circuit Debugger

Microchip's In-Circuit Debugger, MPLAB ICD, is a powerful, low cost, run-time development tool. This tool is based on the FLASH PIC16F87X and can be used to develop for this and other PIC microcontrollers from the PIC16CXXX family. The MPLAB ICD utilizes the in-circuit debugging capability built into the PIC16F87X. This feature, along with Microchip's In-Circuit Serial Programming™ protocol, offers cost-effective in-circuit FLASH debugging from the graphical user interface of the MPLAB Integrated Development Environment. This enables a designer to develop and debug source code by watching variables, single-stepping and setting break points. Running at full speed enables testing hardware in real-time.

19.9   PRO MATE II Universal Device Programmer

The PRO MATE II universal device programmer is a full-featured programmer, capable of operating in stand-alone mode, as well as PC-hosted mode. The PRO MATE II device programmer is CE compliant.

The PRO MATE II device programmer has programmable V_{DD} and V_{PP} supplies, which allow it to verify programmed memory at V_{DD} min and V_{DD} max for maximum reliability. It has an LCD display for instructions and error messages, keys to enter commands and a modular detachable socket assembly to support various package types. In stand-alone mode, the PRO MATE II device programmer can read, verify, or program PIC MCU devices. It can also set code protection in this mode.

19.10   PICSTART Plus Entry Level Development Programmer

The PICSTART Plus development programmer is an easy-to-use, low cost, prototype programmer. It connects to the PC via a COM (RS-232) port. MPLAB Integrated Development Environment software makes using the programmer simple and efficient.

The PICSTART Plus development programmer supports all PIC devices with up to 40 pins. Larger pin count devices, such as the PIC16C92X and PIC17C76X, may be supported with an adapter socket. The PICSTART Plus development programmer is CE compliant.

19.11   PICDEM 1 Low Cost PIC MCU Demonstration Board

The PICDEM 1 demonstration board is a simple board which demonstrates the capabilities of several of Microchip's microcontrollers. The microcontrollers supported are: PIC16C5X (PIC16C54 to PIC16C58A), PIC16C61, PIC16C62X, PIC16C71, PIC16C8X, PIC17C42, PIC17C43 and PIC17C44. All necessary hardware and software is included to run basic demo programs. The user can program the sample microcontrollers provided with the PICDEM 1 demonstration board on a PRO MATE II device programmer, or a PICSTART Plus development programmer, and easily test firmware. The user can also connect the PICDEM 1 demonstration board to the MPLAB ICE in-circuit emulator and download the firmware to the emulator for testing. A prototype area is available for the user to build some additional hardware and connect it to the microcontroller socket(s). Some of the features include an RS-232 interface, a potentiometer for simulated analog input, push button switches and eight LEDs connected to PORTB.

19.12   PICDEM 2 Low Cost PIC16CXX Demonstration Board

The PICDEM 2 demonstration board is a simple demonstration board that supports the PIC16C62, PIC16C64, PIC16C65, PIC16C73 and PIC16C74 microcontrollers. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM 2 demonstration board on a PRO MATE II device programmer, or a PICSTART Plus development programmer, and easily test firmware. The MPLAB ICE in-circuit emulator may also be used with the PICDEM 2 demonstration board to test firmware. A prototype area has been provided to the user for adding additional hardware and connecting it to the microcontroller socket(s). Some of the features include a RS-232 interface, push button switches, a potentiometer for simulated analog input, a serial EEPROM to demonstrate usage of the I²C™ bus and separate headers for connection to an LCD module and a keypad.

19.13   PICDEM 3 Low Cost PIC16CXXX Demonstration Board

The PICDEM 3 demonstration board is a simple demonstration board that supports the PIC16C923 and PIC16C924 in the PLCC package. It will also support future 44-pin PLCC microcontrollers with an LCD Module. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM 3 demonstration board on a PRO MATE II device programmer, or a PICSTART Plus development programmer with an adapter socket, and easily test firmware. The MPLAB ICE in-circuit emulator may also be used with the PICDEM 3 demonstration board to test firmware. A prototype area has been provided to the user for adding hardware and connecting it to the microcontroller socket(s). Some of the features include a RS-232 interface, push button switches, a potentiometer for simulated analog input, a thermistor and separate headers for connection to an external LCD module and a keypad. Also provided on the PICDEM 3 demonstration board is a LCD panel, with 4 commons and 12 segments, that is capable of displaying time, temperature and day of the week. The PICDEM 3 demonstration board provides an additional RS-232 interface and Windows software for showing the demultiplexed LCD signals on a PC. A simple serial interface allows the user to construct a hardware demultiplexer for the LCD signals.

## 19.14   PICDEM 17 Demonstration Board

The PICDEM 17 demonstration board is an evaluation board that demonstrates the capabilities of several Microchip microcontrollers, including PIC17C752, PIC17C756A, PIC17C762 and PIC17C766. All necessary hardware is included to run basic demo programs, which are supplied on a 3.5-inch disk. A programmed sample is included and the user may erase it and program it with the other sample programs using the PRO MATE II device programmer, or the PICSTART Plus development programmer, and easily debug and test the sample code. In addition, the PICDEM 17 demonstration board supports downloading of programs to and executing out of external FLASH memory on board. The PICDEM 17 demonstration board is also usable with the MPLAB ICE in-circuit emulator, or the PICMASTER emulator and all of the sample programs can be run and modified using either emulator. Additionally, a generous prototype area is available for user hardware.

19.15   KEELOQ Evaluation and Programming Tools

KEELOQ evaluation and programming tools support Microchip's HCS Secure Data Products. The HCS evaluation kit includes a LCD display to show changing codes, a decoder to decode transmissions and a programming interface to program test transmitters.
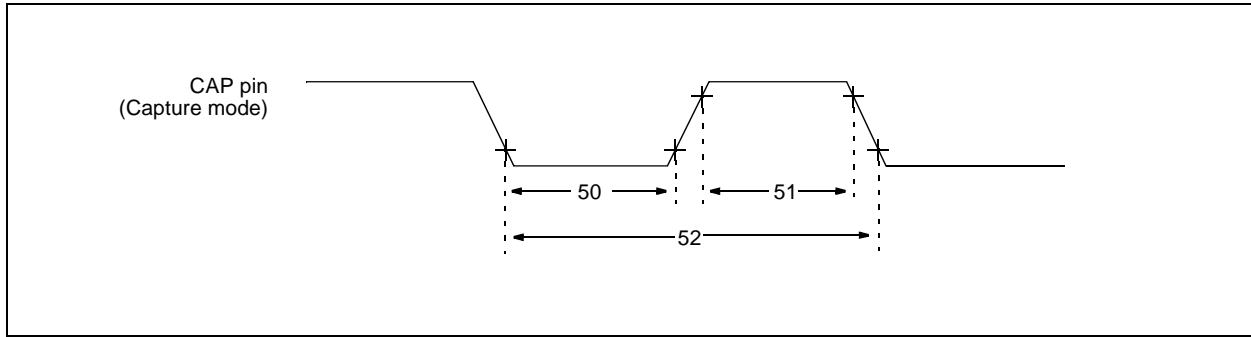
FIGURE 20-3: **PIC17LC7XX-08 VOLTAGE-FREQUENCY GRAPH**
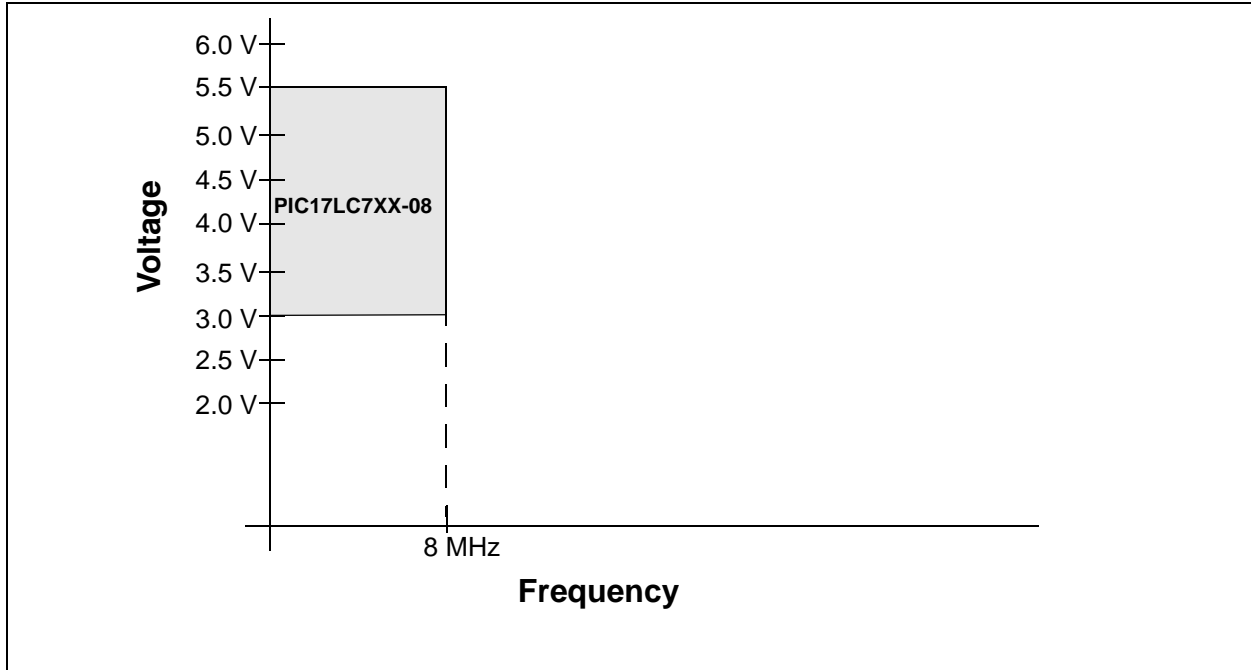
FIGURE 20-4: **PIC17C7XX/CL VOLTAGE-FREQUENCY GRAPH**
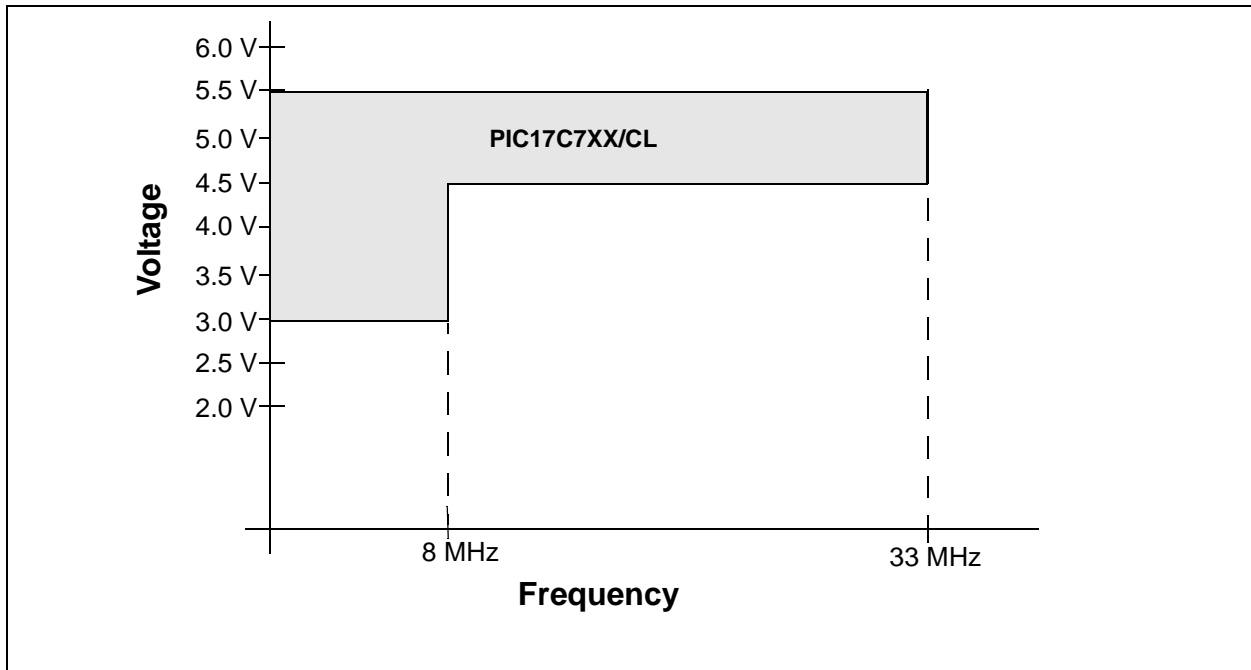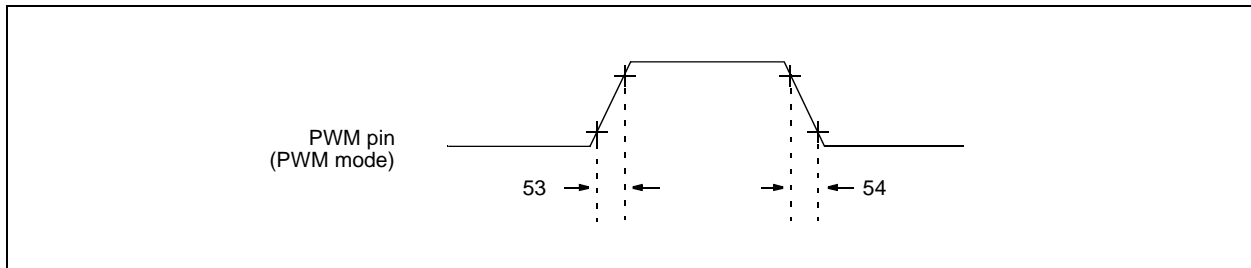
FIGURE 20-11: **CAPTURE TIMINGS**

TABLE 20-6: **CAPTURE REQUIREMENTS**

Param No.	Sym	Characteristic	Min	Typ †	Max	Units	Conditions
50	TccL	Capture pin input low time	10	—	—	ns	
51	TccH	Capture pin input high time	10	—	—	ns	
52	TccP	Capture pin input period	$\frac{2T_{CY}}{N}$	—	—	ns	N = prescale value (4 or 16)

† Data in "Typ" column is at 5V, 25°C unless otherwise stated.

FIGURE 20-12: **PWM TIMINGS**

TABLE 20-7: **PWM REQUIREMENTS**

Param No.	Sym	Characteristic	Min	Typ †	Max	Units	Conditions
53	TccR	PWM pin output rise time	—	10	35	ns	
54	TccF	PWM pin output fall time	—	10	35	ns	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated.

PIC17C7XX
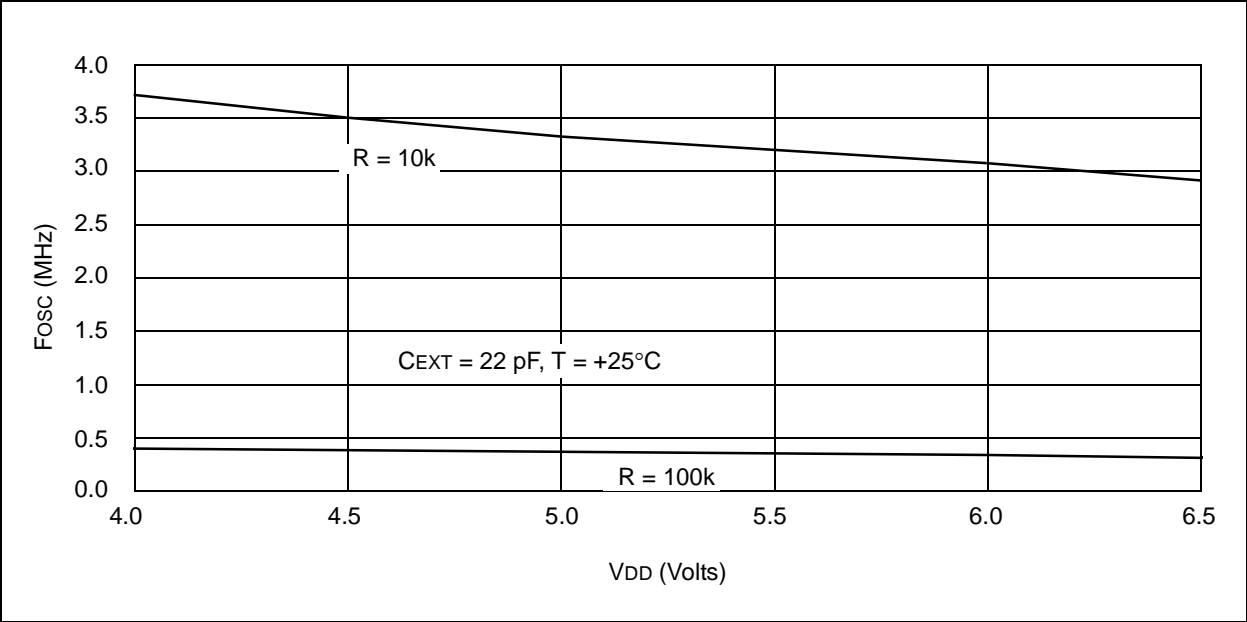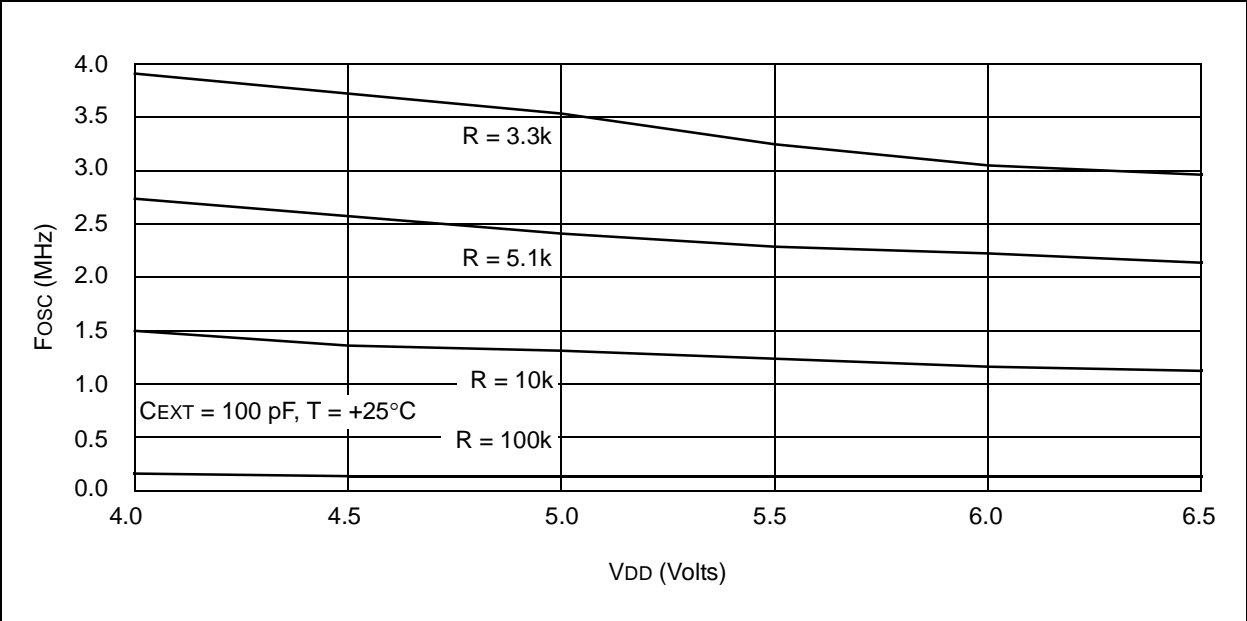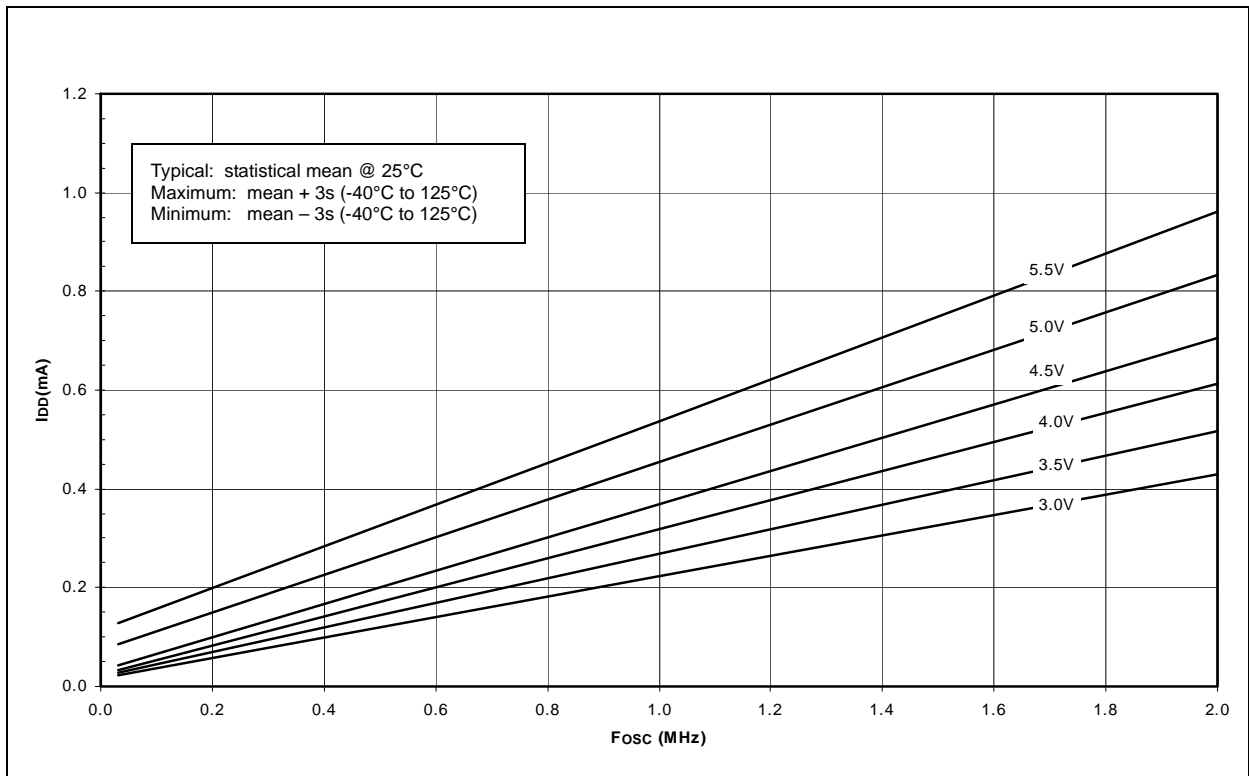
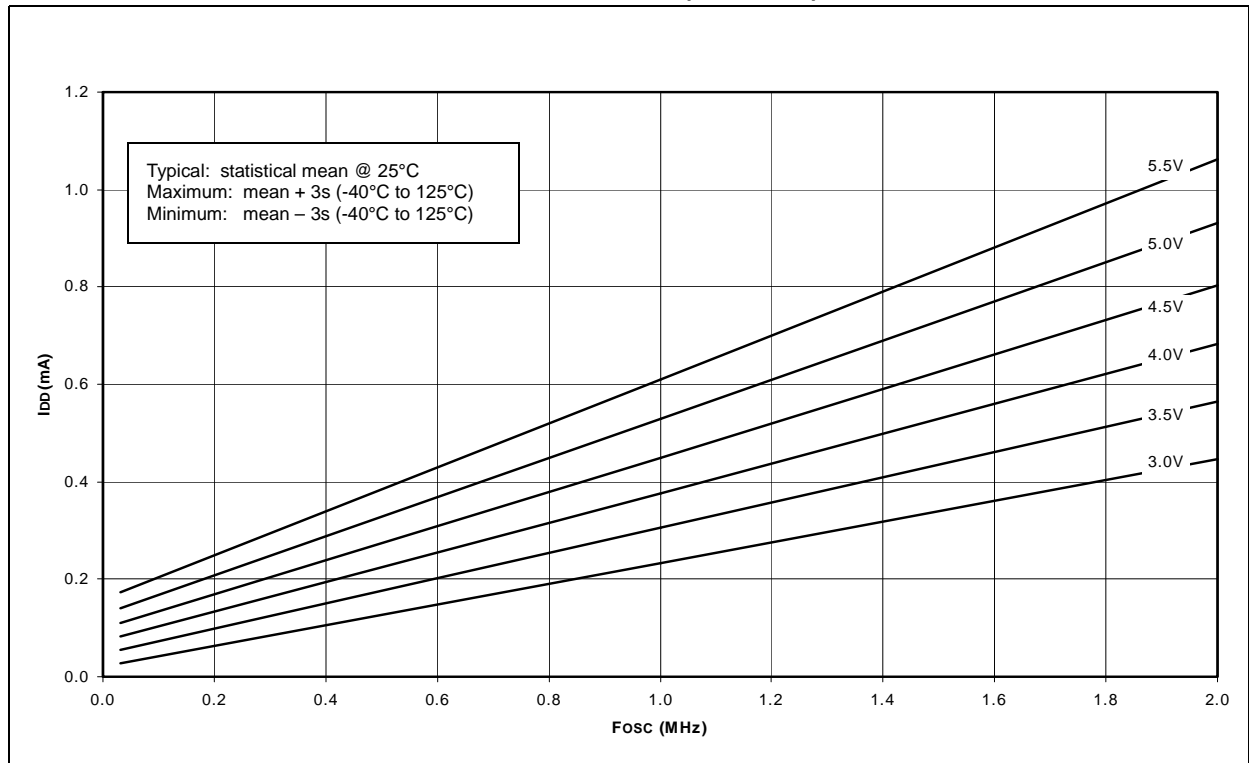**FIGURE 21-2:** **TYPICAL RC OSCILLATOR FREQUENCY vs. V**DD

FIGURE 21-3: **TYPICAL RC OSCILLATOR FREQUENCY vs. V**DD

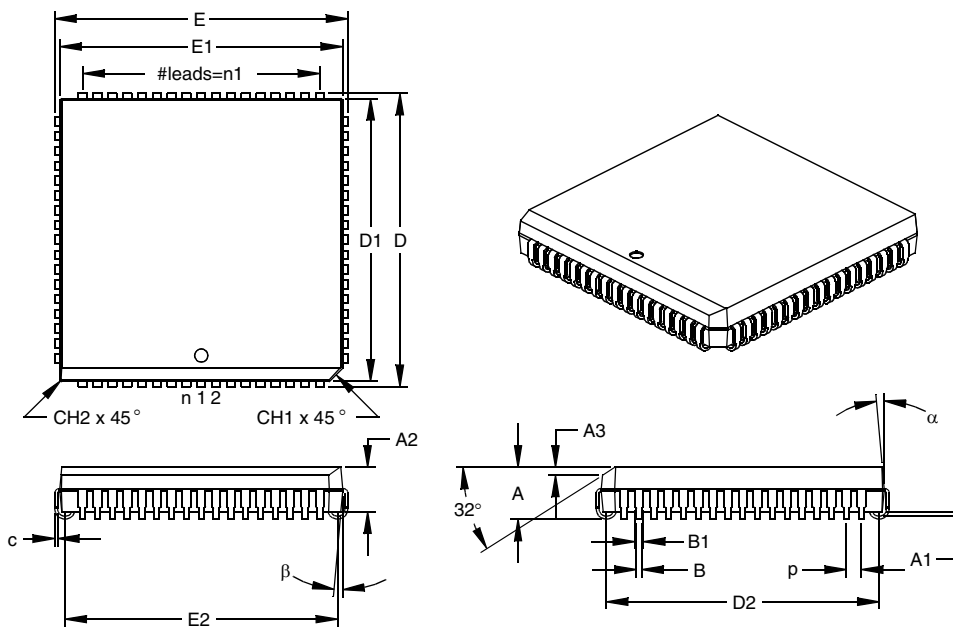**FIGURE 21-7:** **TYPICAL I**DD **vs. F**OSC **OVER V**DD **(LF MODE)**

FIGURE 21-8: **MAXIMUM I**DD **vs. F**OSC **OVER V**DD **(LF MODE)**

PIC17C7XX

68-Lead Plastic Leaded Chip Carrier (L) – Square (PLCC)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

	Units	INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		68			68	
Pitch	p		.050			1.27	
Pins per Side	n1		17			17	
Overall Height	A	.165	.173	.180	4.19	4.39	4.57
Molded Package Thickness	A2	.145	.153	.160	3.68	3.87	4.06
Standoff §	A1	.020	.028	.035	0.51	0.71	0.89
Side 1 Chamfer Height	A3	.024	.029	.034	0.61	0.74	0.86
Corner Chamfer 1	CH1	.040	.045	.050	1.02	1.14	1.27
Corner Chamfer (others)	CH2	.000	.005	.010	0.00	0.13	0.25
Overall Width	E	.985	.990	.995	25.02	25.15	25.27
Overall Length	D	.985	.990	.995	25.02	25.15	25.27
Molded Package Width	E1	.950	.954	.958	24.13	24.23	24.33
Molded Package Length	D1	.950	.954	.958	24.13	24.23	24.33
Footprint Width	E2	.890	.920	.930	22.61	23.37	23.62
Footprint Length	D2	.890	.920	.930	22.61	23.37	23.62
Lead Thickness	c	.008	.011	.013	0.20	0.27	0.33
Upper Lead Width	B1	.026	.029	.032	0.66	0.74	0.81
Lower Lead Width	B	.013	.020	.021	0.33	0.51	0.53
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

* Controlling Parameter
§ Significant Characteristic
Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.
JEDEC Equivalent: MO-047
Drawing No. C04-049

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