Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	66
Program Memory Size	16KB (8K x 16)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	678 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic17c762-16-l

FIGURE 3-1: PIC17C752/756A BLOCK DIAGRAM

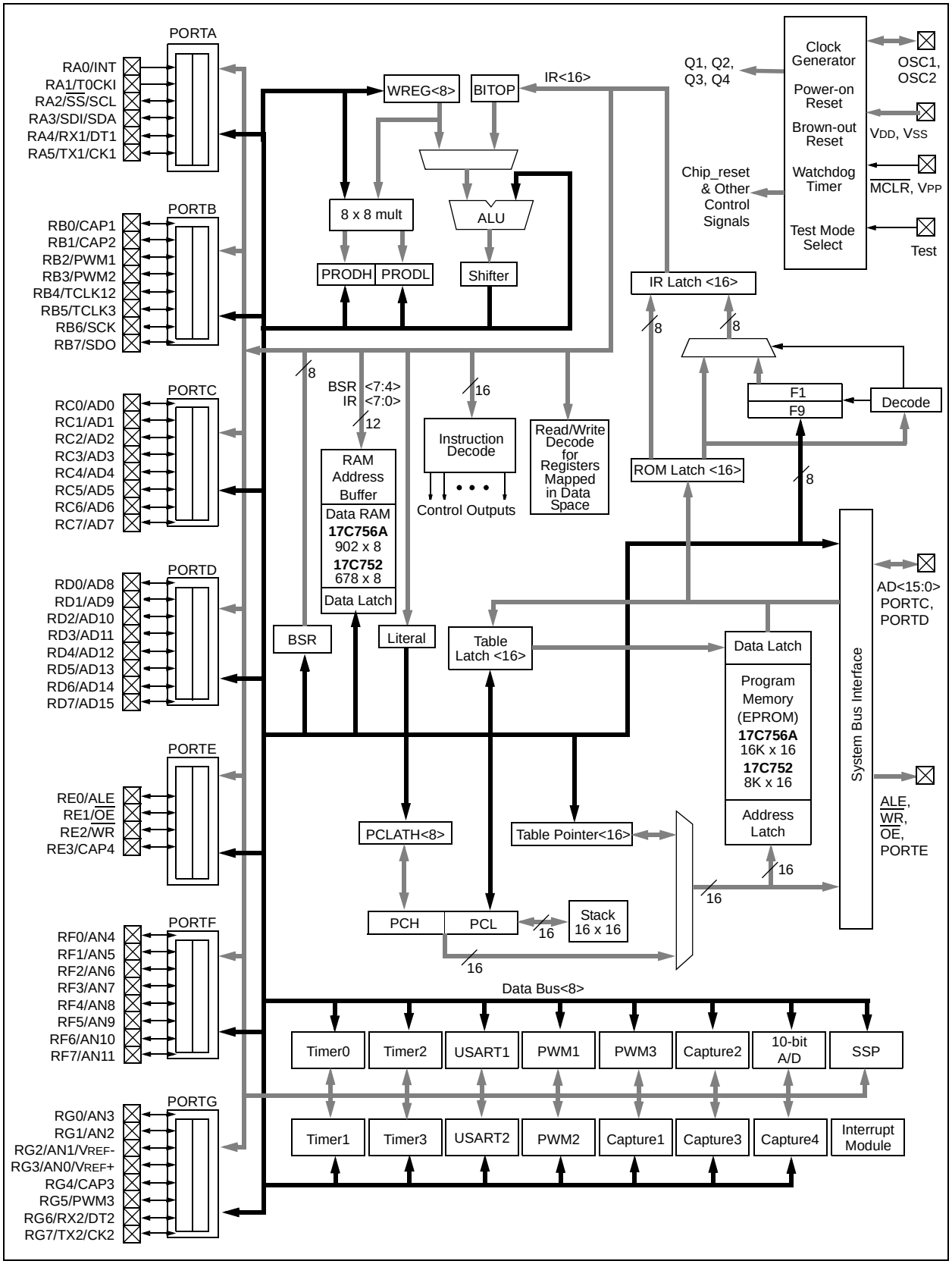


TABLE 3-1: PINOUT DESCRIPTIONS (CONTINUED)

Name	PIC17C75X			PIC17C76X		I/O/P Type	Buffer Type	Description
	DIP No.	PLCC No.	TQFP No.	PLCC No.	QFP No.			
								PORTG is a bi-directional I/O Port.
RG0/AN3	32	34	24	42	30	I/O	ST	RG0 can also be analog input 3.
RG1/AN2	31	33	23	41	29	I/O	ST	RG1 can also be analog input 2.
RG2/AN1/VREF-	30	32	22	40	28	I/O	ST	RG2 can also be analog input 1, or the ground reference voltage.
RG3/AN0/VREF+	29	31	21	39	27	I/O	ST	RG3 can also be analog input 0, or the positive reference voltage.
RG4/CAP3	35	38	27	46	33	I/O	ST	RG4 can also be the Capture3 input pin.
RG5/PWM3	36	39	28	47	34	I/O	ST	RG5 can also be the PWM3 output pin.
RG6/RX2/DT2	38	41	30	49	36	I/O	ST	RG6 can also be selected as the USART2 (SCI) Asynchronous Receive or USART2 (SCI) Synchronous Data.
RG7/TX2/CK2	37	40	29	48	35	I/O	ST	RG7 can also be selected as the USART2 (SCI) Asynchronous Transmit or USART2 (SCI) Synchronous Clock.
								PORTH is a bi-directional I/O Port. PORTH is only available on the PIC17C76X devices.
RH0	—	—	—	10	79	I/O	ST	
RH1	—	—	—	11	80	I/O	ST	
RH2	—	—	—	12	1	I/O	ST	
RH3	—	—	—	13	2	I/O	ST	
RH4/AN12	—	—	—	31	19	I/O	ST	RH4 can also be analog input 12.
RH5/AN13	—	—	—	32	20	I/O	ST	RH5 can also be analog input 13.
RH6/AN14	—	—	—	33	21	I/O	ST	RH6 can also be analog input 14.
RH7/AN15	—	—	—	34	22	I/O	ST	RH7 can also be analog input 15.
								PORTJ is a bi-directional I/O Port. PORTJ is only available on the PIC17C76X devices.
RJ0	—	—	—	52	39	I/O	ST	
RJ1	—	—	—	53	40	I/O	ST	
RJ2	—	—	—	54	41	I/O	ST	
RJ3	—	—	—	55	42	I/O	ST	
RJ4	—	—	—	73	59	I/O	ST	
RJ5	—	—	—	74	60	I/O	ST	
RJ6	—	—	—	75	61	I/O	ST	
RJ7	—	—	—	76	62	I/O	ST	
TEST	16	17	8	21	10	I	ST	Test mode selection control input. Always tie to VSS for normal operation.
VSS	17, 33, 49, 64	19, 36, 53, 68	9, 25, 41, 56	23, 44, 65, 84	11, 31, 51, 70	P		Ground reference for logic and I/O pins.
VDD	1, 18, 34, 46	2, 20, 37, 49,	10, 26, 38, 57	24, 45, 61, 2	12, 32, 48, 71	P		Positive supply for logic and I/O pins.
AVSS	28	30	20	38	26	P		Ground reference for A/D converter. This pin **MUST** be at the same potential as VSS.
AVDD	27	29	19	37	25	P		Positive supply for A/D converter. This pin **MUST** be at the same potential as VDD.
NC	—	1, 18, 35, 52	—	1, 22, 43, 64	—			No Connect. Leave these pins unconnected.

Legend: I = Input only; O = Output only; I/O = Input/Output;
P = Power; — = Not Used; TTL = TTL input; ST = Schmitt Trigger input

Note 1: The output is only available by the peripheral operation.

2: Open drain input/output pin. Pin forced to input upon any device RESET.

4.0 ON-CHIP OSCILLATOR CIRCUIT

The internal oscillator circuit is used to generate the device clock. Four device clock periods generate an internal instruction clock (T_{CY}).

There are four modes that the oscillator can operate in. They are selected by the device configuration bits during device programming. These modes are:

- LF Low Frequency ($F_{OSC} \leq 2$ MHz)
- XT Standard Crystal/Resonator Frequency (2 MHz $\leq F_{OSC} \leq$ 33 MHz)
- EC External Clock Input (Default oscillator configuration)
- RC External Resistor/Capacitor ($F_{OSC} \leq 4$ MHz)

There are two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in RESET until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 96 ms (nominal) on POR and BOR. The PWRT is designed to keep the part in RESET while the power supply stabilizes. With these two timers on-chip, most applications need no external RESET circuitry.

SLEEP mode is designed to offer a very low current power-down mode. The user can wake from SLEEP through external RESET, Watchdog Timer Reset, or through an interrupt.

Several oscillator options are made available to allow the part to better fit the application. The RC oscillator option saves system cost while the LF crystal option saves power. Configuration bits are used to select various options.

4.1 Oscillator Configurations

4.1.1 OSCILLATOR TYPES

The PIC17CXXX can be operated in four different oscillator modes. The user can program two configuration bits (FOSC1:FOSC0) to select one of these four modes:

- LF Low Power Crystal
- XT Crystal/Resonator
- EC External Clock Input
- RC Resistor/Capacitor

The main difference between the LF and XT modes is the gain of the internal inverter of the oscillator circuit, which allows the different frequency ranges.

For more details on the device configuration bits, see Section 17.0.

4.1.2 CRYSTAL OSCILLATOR/CERAMIC RESONATORS

In XT or LF modes, a crystal or ceramic resonator is connected to the OSC1/CLKIN and OSC2/CLKOUT pins to establish oscillation (Figure 4-2). The PIC17CXXX oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications.

For frequencies above 24 MHz, it is common for the crystal to be an overtone mode crystal. Use of overtone mode crystals require a tank circuit to attenuate the gain at the fundamental frequency. Figure 4-3 shows an example circuit.

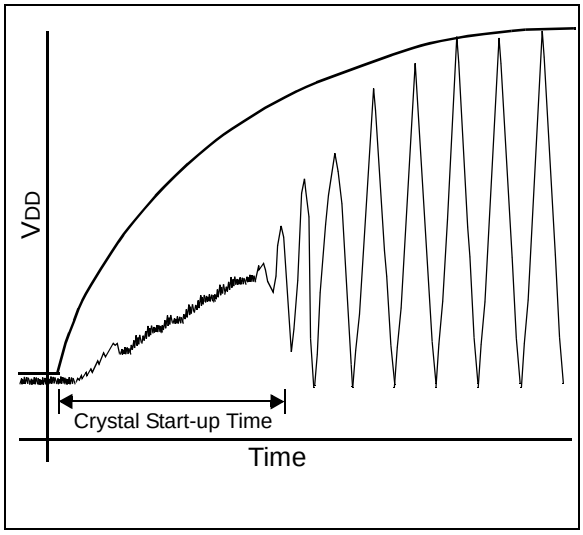
4.1.3 OSCILLATOR/RESONATOR START-UP

As the device voltage increases from Vss, the oscillator will start its oscillations. The time required for the oscillator to start oscillating depends on many factors. These include:

- Crystal/resonator frequency
- Capacitor values used (C1 and C2)
- Device V_{DD} rise time
- System temperature
- Series resistor value (and type) if used
- Oscillator mode selection of device (which selects the gain of the internal oscillator inverter)

Figure 4-1 shows an example of a typical oscillator/resonator start-up. The peak-to-peak voltage of the oscillator waveform can be quite low (less than 50% of device V_{DD}) when the waveform is centered at $V_{DD}/2$ (refer to parameter #D033 and parameter #D043 in the electrical specification section).

FIGURE 4-1: OSCILLATOR/ RESONATOR START-UP CHARACTERISTICS



5.1.5 BROWN-OUT RESET (BOR)

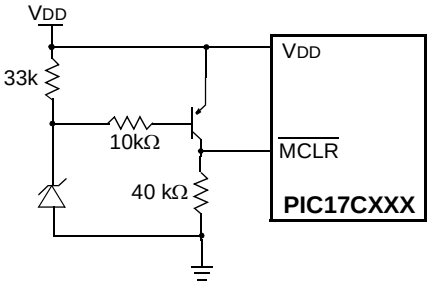
PIC17C7XX devices have on-chip Brown-out Reset circuitry. This circuitry places the device into a RESET when the device voltage falls below a trip point (BVDD). This ensures that the device does not continue program execution outside the valid operation range of the device. Brown-out Resets are typically used in AC line applications, or large battery applications, where large loads may be switched in (such as automotive).

Note:	Before using the on-chip Brown-out for a voltage supervisory function, please review the electrical specifications to ensure that they meet your requirements.

The BODEN configuration bit can disable (if clear/ programmed), or enable (if set) the Brown-out Reset circuitry. If VDD falls below BVDD (typically 4.0 V, paramter #D005 in electrical specification section), for greater than parameter #35, the Brown-out situation will reset the chip. A RESET is not guaranteed to occur if VDD falls below BVDD for less than paramter #35. The chip will remain in Brown-out Reset until VDD rises above BVDD. The Power-up Timer and Oscillator Start-up Timer will then be invoked. This will keep the chip in RESET the greater of 96 ms and 1024 TOSC. If VDD drops below BVDD while the Power-up Timer/Oscillator Start-up Timer is running, the chip will go back into a Brown-out Reset. The Power-up Timer/Oscillator Start-up Timer will be initialized. Once VDD rises above BVDD, the Power-up Timer/Oscillator Start-up Timer will start their time delays. Figure 5-10 shows typical Brown-out situations.

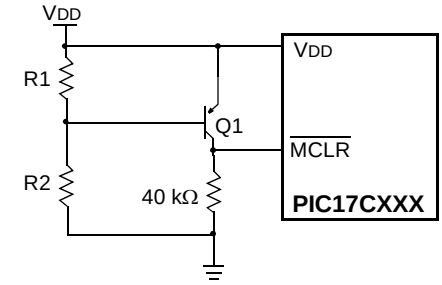
In some applications, the Brown-out Reset trip point of the device may not be at the desired level. Figure 5-8 and Figure 5-9 are two examples of external circuitry that may be implemented. Each needs to be evaluated to determine if they match the requirements of the application.

FIGURE 5-8: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 1



This circuit will activate RESET when VDD goes below (Vz + 0.7V) where Vz = Zener voltage.

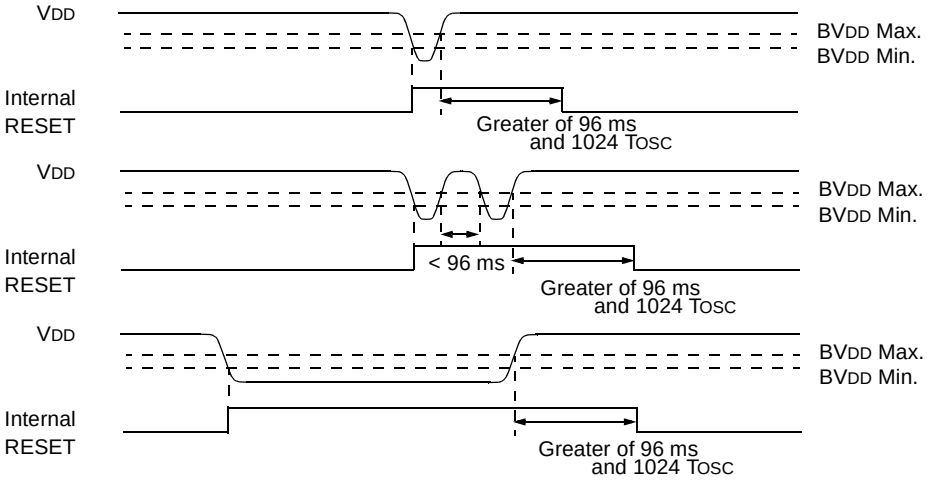
FIGURE 5-9: EXTERNAL BROWN-OUT PROTECTION CIRCUIT 2



This brown-out circuit is less expensive, albeit less accurate. Transistor Q1 turns off when VDD is below a certain level such that:

$$V_{DD} \bullet \frac{R1}{R1 + R2} = 0.7V$$

FIGURE 5-10: BROWN-OUT SITUATIONS



6.2 Peripheral Interrupt Enable Register1 (PIE1) and Register2 (PIE2)

These registers contains the individual enable bits for the peripheral interrupts.

REGISTER 6-2: PIE1 REGISTER (ADDRESS: 17h, BANK 1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RBIE	TMR3IE	TMR2IE	TMR1IE	CA2IE	CA1IE	TX1IE	RC1IE
bit 7							bit 0

bit 7 **RBIE**: PORTB Interrupt-on-Change Enable bit
1 = Enable PORTB interrupt-on-change
0 = Disable PORTB interrupt-on-change

bit 6 **TMR3IE**: TMR3 Interrupt Enable bit
1 = Enable TMR3 interrupt
0 = Disable TMR3 interrupt

bit 5 **TMR2IE**: TMR2 Interrupt Enable bit
1 = Enable TMR2 interrupt
0 = Disable TMR2 interrupt

bit 4 **TMR1IE**: TMR1 Interrupt Enable bit
1 = Enable TMR1 interrupt
0 = Disable TMR1 interrupt

bit 3 **CA2IE**: Capture2 Interrupt Enable bit
1 = Enable Capture2 interrupt
0 = Disable Capture2 interrupt

bit 2 **CA1IE**: Capture1 Interrupt Enable bit
1 = Enable Capture1 interrupt
0 = Disable Capture1 interrupt

bit 1 **TX1IE**: USART1 Transmit Interrupt Enable bit
1 = Enable USART1 Transmit buffer empty interrupt
0 = Disable USART1 Transmit buffer empty interrupt

bit 0 **RC1IE**: USART1 Receive Interrupt Enable bit
1 = Enable USART1 Receive buffer full interrupt
0 = Disable USART1 Receive buffer full interrupt

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
- n = Value at POR Reset	’1’ = Bit is set	’0’ = Bit is cleared	x = Bit is unknown

9.0 HARDWARE MULTIPLIER

All PIC17C7XX devices have an 8 x 8 hardware multiplier included in the ALU of the device. By making the multiply a hardware operation, it completes in a single instruction cycle. This is an unsigned multiply that gives a 16-bit result. The result is stored into the 16-bit Product register (PRODH:PRODL). The multiplier does not affect any flags in the ALUSTA register.

Making the 8 x 8 multiplier execute in a single cycle gives the following advantages:

- Higher computational throughput
- Reduces code size requirements for multiply algorithms

The performance increase allows the device to be used in applications previously reserved for Digital Signal Processors.

Table 9-1 shows a performance comparison between PIC17CXXX devices using the single cycle hardware multiply and performing the same function without the hardware multiply.

Example 9-1 shows the sequence to do an 8 x 8 unsigned multiply. Only one instruction is required when one argument of the multiply is already loaded in the WREG register.

Example 9-2 shows the sequence to do an 8 x 8 signed multiply. To account for the sign bits of the arguments, each argument's most significant bit (MSb) is tested and the appropriate subtractions are done.

EXAMPLE 9-1: 8 x 8 UNSIGNED MULTIPLY ROUTINE

```
MOVFP    ARG1, WREG  ;
MULWF    ARG2        ; ARG1 * ARG2 ->
                     ;   PRODH:PRODL
```

EXAMPLE 9-2: 8 x 8 SIGNED MULTIPLY ROUTINE

```
MOVFP    ARG1, WREG
MULWF    ARG2        ; ARG1 * ARG2 ->
                     ;   PRODH:PRODL
BTFSC    ARG2, SB    ; Test Sign Bit
SUBWF    PRODH, F    ; PRODH = PRODH
                     ;         - ARG1
MOVFP    ARG2, WREG
BTFSC    ARG1, SB    ; Test Sign Bit
SUBWF    PRODH, F    ; PRODH = PRODH
                     ;         - ARG2
```

TABLE 9-1: PERFORMANCE COMPARISON

Routine	Multiply Method	Program Memory (Words)	Cycles (Max)	Time		
				@ 33 MHz	@ 16 MHz	@ 8 MHz
8 x 8 unsigned	Without hardware multiply	13	69	8.364 μs	17.25 μs	34.50 μs
	Hardware multiply	1	1	0.121 μs	0.25 μs	0.50 μs
8 x 8 signed	Without hardware multiply	—	—	—	—	—
	Hardware multiply	6	6	0.727 μs	1.50 μs	3.0 μs
16 x 16 unsigned	Without hardware multiply	21	242	29.333 μs	60.50 μs	121.0 μs
	Hardware multiply	24	24	2.91 μs	6.0 μs	12.0 μs
16 x 16 signed	Without hardware multiply	52	254	30.788 μs	63.50 μs	127.0 μs
	Hardware multiply	36	36	4.36 μs	9.0 μs	18.0 μs

REGISTER 13-2: TCON2 REGISTER (ADDRESS: 17h, BANK 3)

R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CA2OVF	CA1OVF	PWM2ON	PWM1ON	CA1/$\overline{PR3}$	TMR3ON	TMR2ON	TMR1ON
bit 7							bit 0

bit 7 **CA2OVF**: Capture2 Overflow Status bit
This bit indicates that the capture value had not been read from the capture register pair (CA2H:CA2L) before the next capture event occurred. The capture register retains the oldest unread capture value (last capture before overflow). Subsequent capture events will not update the capture register with the TMR3 value until the capture register has been read (both bytes).
1 = Overflow occurred on Capture2 register
0 = No overflow occurred on Capture2 register

bit 6 **CA1OVF**: Capture1 Overflow Status bit
This bit indicates that the capture value had not been read from the capture register pair (PR3H/CA1H:PR3L/CA1L), before the next capture event occurred. The capture register retains the oldest unread capture value (last capture before overflow). Subsequent capture events will not update the capture register with the TMR3 value until the capture register has been read (both bytes).
1 = Overflow occurred on Capture1 register
0 = No overflow occurred on Capture1 register

bit 5 **PWM2ON**: PWM2 On bit
1 = PWM2 is enabled
(The RB3/PWM2 pin ignores the state of the DDRB<3> bit.)
0 = PWM2 is disabled
(The RB3/PWM2 pin uses the state of the DDRB<3> bit for data direction.)

bit 4 **PWM1ON**: PWM1 On bit
1 = PWM1 is enabled
(The RB2/PWM1 pin ignores the state of the DDRB<2> bit.)
0 = PWM1 is disabled
(The RB2/PWM1 pin uses the state of the DDRB<2> bit for data direction.)

bit 3 **CA1/$\overline{PR3}$**: CA1/$\overline{PR3}$ Register Mode Select bit
1 = Enables Capture1
(PR3H/CA1H:PR3L/CA1L is the Capture1 register. Timer3 runs without a period register.)
0 = Enables the Period register
(PR3H/CA1H:PR3L/CA1L is the Period register for Timer3.)

bit 2 **TMR3ON**: Timer3 On bit
1 = Starts Timer3
0 = Stops Timer3

bit 1 **TMR2ON**: Timer2 On bit
This bit controls the incrementing of the TMR2 register. When TMR2:TMR1 form the 16-bit timer (T16 is set), TMR2ON must be set. This allows the MSB of the timer to increment.
1 = Starts Timer2 (must be enabled if the T16 bit (TCON1<3>) is set)
0 = Stops Timer2

bit 0 **TMR1ON**: Timer1 On bit

When T16 is set (in 16-bit Timer mode):
1 = Starts 16-bit TMR2:TMR1
0 = Stops 16-bit TMR2:TMR1

When T16 is clear (in 8-bit Timer mode:
1 = Starts 8-bit Timer1
0 = Stops 8-bit Timer1

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR Reset	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

15.1.4 MASTER MODE

The master can initiate the data transfer at any time because it controls the SCK. The master determines when the slave (Processor 2, Figure 15-5) is to broadcast data by the software protocol.

In Master mode, the data is transmitted/received as soon as the SSPBUF register is written to. If the SPI is only going to receive, the SDO output could be disabled (programmed as an input). The SSPSR register will continue to shift in the signal present on the SDI pin at the programmed clock rate. As each byte is received, it will be loaded into the SSPBUF register as if a normal received byte (interrupts and status bits appropriately set). This could be useful in receiver applications as a “Line Activity Monitor” mode.

The clock polarity is selected by appropriately programming bit CKP (SSPCON1<4>). This then, would give waveforms for SPI communication as shown in Figure 15-6, Figure 15-8 and Figure 15-9, where the MSb is transmitted first. In Master mode, the SPI clock rate (bit rate) is user programmable to be one of the following:

- FOSC/4 (or TCY)
- FOSC/16 (or 4 • TCY)
- FOSC/64 (or 16 • TCY)
- Timer2 output/2

This allows a maximum bit clock frequency (at 33 MHz) of 8.25 MHz.

Figure 15-6 shows the waveforms for Master mode. When CKE = 1, the SDO data is valid before there is a clock edge on SCK. The change of the input sample is shown based on the state of the SMP bit. The time when the SSPBUF is loaded with the received data is shown.

FIGURE 15-6: SPI MODE WAVEFORM (MASTER MODE)

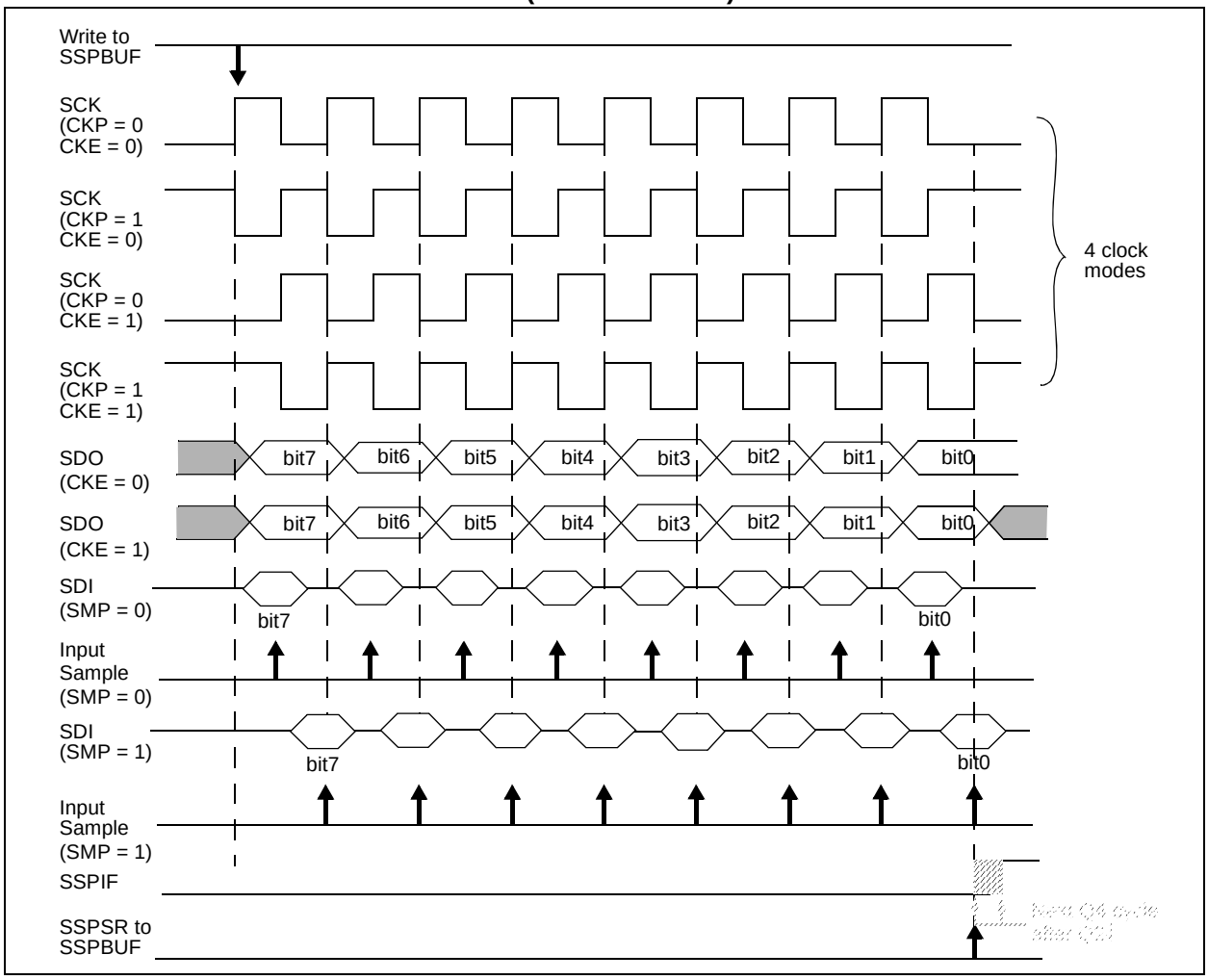


FIGURE 15-8: SPI MODE WAVEFORM (SLAVE MODE WITH CKE = 0)

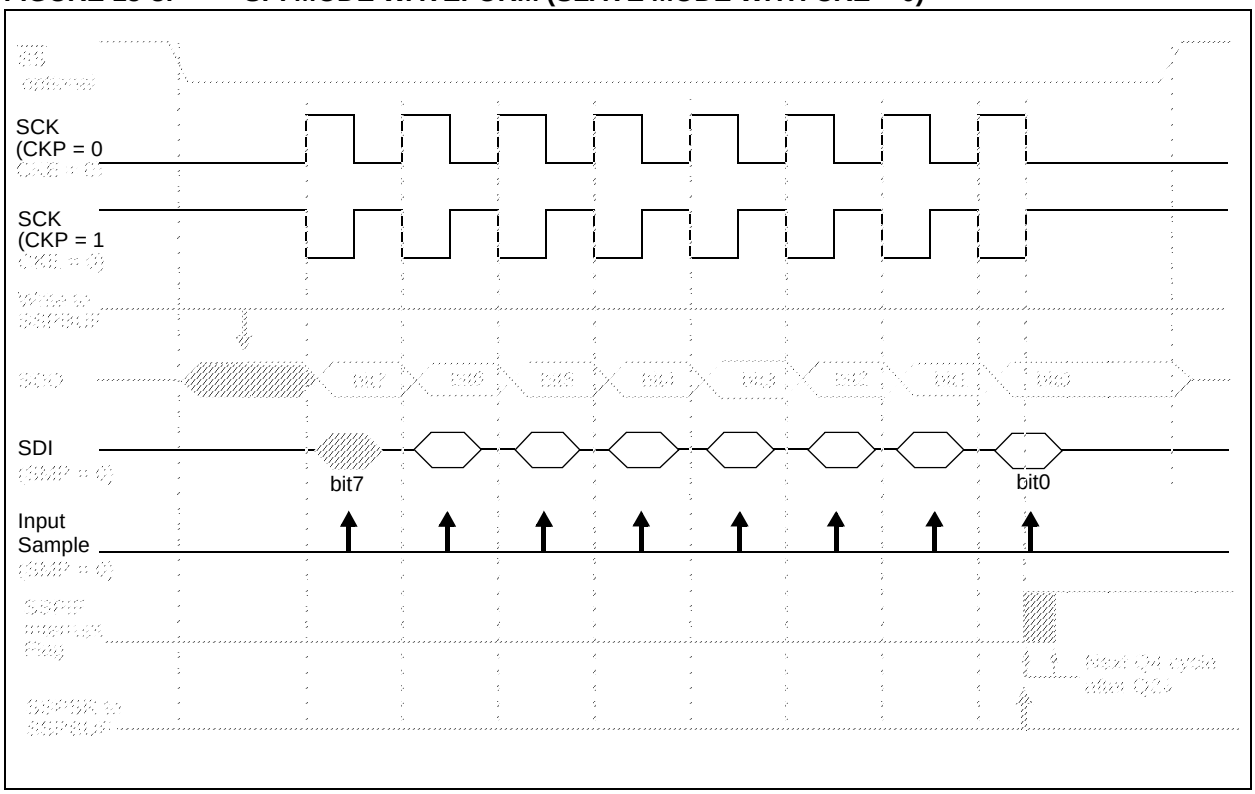


FIGURE 15-9: SPI MODE WAVEFORM (SLAVE MODE WITH CKE = 1)

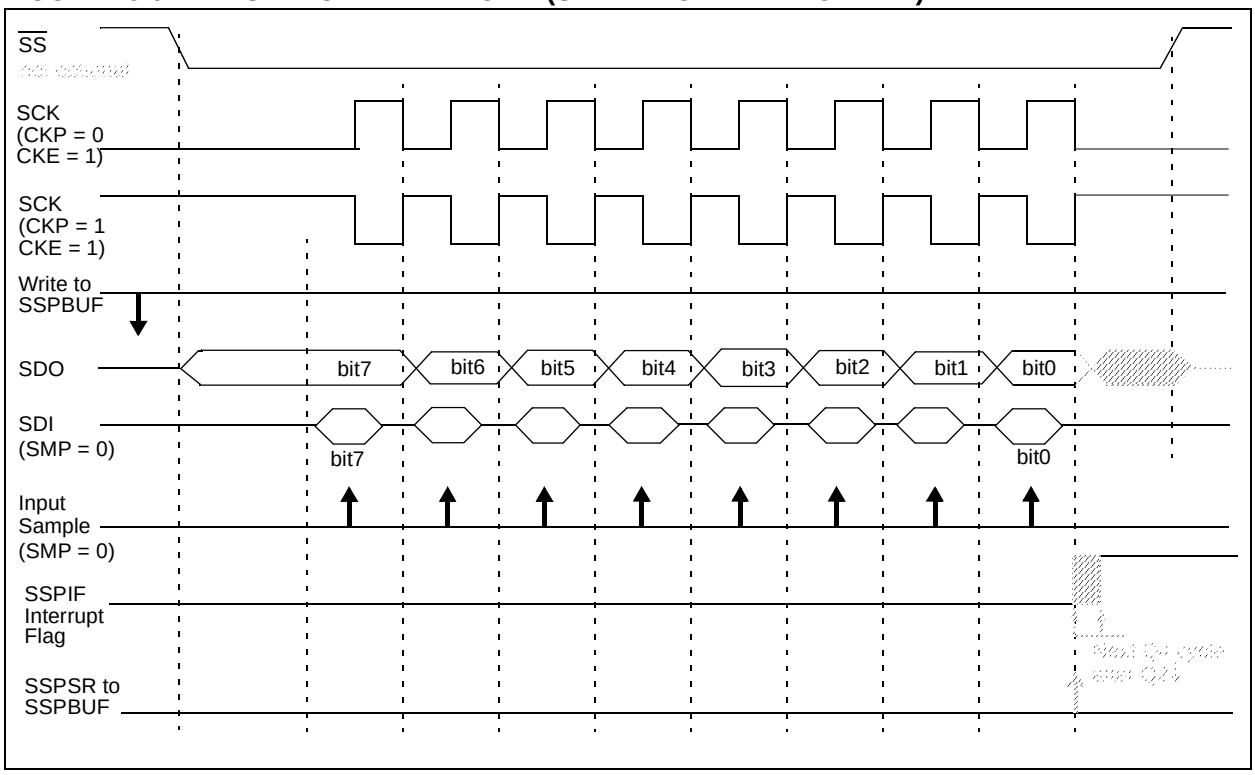
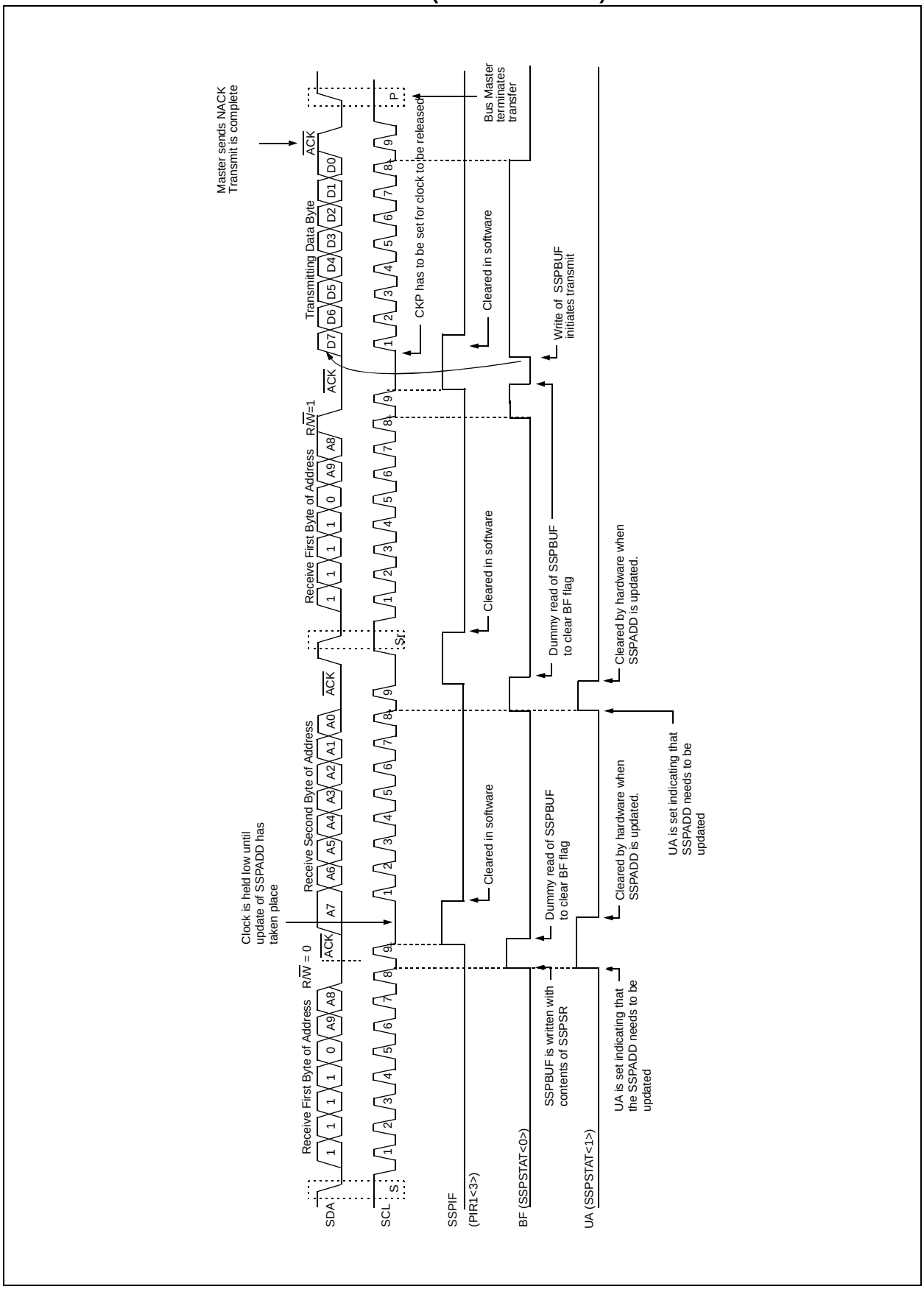


FIGURE 15-14: I²C SLAVE-TRANSMITTER (10-BIT ADDRESS)



15.2.3 SLEEP OPERATION

While in SLEEP mode, the I^2C module can receive addresses or data and when an address match or complete byte transfer occurs, wake the processor from SLEEP (if the SSP interrupt is enabled).

15.2.4 EFFECTS OF A RESET

A RESET disables the SSP module and terminates the current transfer.

TABLE 15-3: REGISTERS ASSOCIATED WITH I^2C OPERATION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR, BOR	$\overline{MCLR}$, WDT
07h, Unbanked	INTSTA	PEIF	T0CKIF	T0IF	INTF	PEIE	T0CKIE	T0IE	INTE	0000 0000	0000 0000
10h, Bank 4	PIR2	SSPIF	BCLIF	ADIF	—	CA4IF	CA3IF	TX2IF	RC2IF	000- 0000	000- 0000
11h, Bank 4	PIE2	SSPIE	BCLIE	ADIE	—	CA4IE	CA3IE	TX2IE	RC2IE	000- 0000	000- 0000
10h. Bank 6	SSPADD	Synchronous Serial Port (I^2C mode) Address Register								0000 0000	0000 0000
14h, Bank 6	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register								xxxx xxxx	uuuu uuuu
11h, Bank 6	SSPCON1	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
12h, Bank 6	SSPCON2	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	0000 0000	0000 0000
13h, Bank 6	SSPSTAT	SMP	CKE	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF	0000 0000	0000 0000

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by the SSP in I^2C mode.

15.4 Example Program

Example 15-2 shows MPLAB® C17 'C' code for using the I^2C module in Master mode to communicate with a 24LC01B serial EEPROM. This example uses the PIC® MCU 'C' libraries included with MPLAB C17.

EXAMPLE 15-2: INTERFACING TO A 24LC01B SERIAL EEPROM (USING MPLAB C17)

```
// Include necessary header files
#include <p17c756.h>     // Processor header file
#include <delays.h>      // Delay routines header file
#include <stdlib.h>      // Standard Library header file
#include <i2c16.h>       // I2C routines header file

#define CONTROL 0xa0     // Control byte definition for 24LC01B

// Function declarations
void main(void);
void WritePORTD(static unsigned char data);
void ByteWrite(static unsigned char address,static unsigned char data);
unsigned char ByteRead(static unsigned char address);
void ACKPoll(void);

// Main program
void main(void)
{
static unsigned char address;    // I2C address of 24LC01B
static unsigned char datao;      // Data written to 24LC01B
static unsigned char datai;      // Data read from 24LC01B

    address = 0;                 // Preset address to 0
    OpenI2C(MASTER,SLEW_ON);     // Configure I2C Module Master mode, Slew rate control on
    SSPADD = 39;                 // Configure clock for 100KHz

    while(address<128)           // Loop 128 times, 24LC01B is 128x8
    {
        datao = PORTB;
        do
        {
            ByteWrite(address,datao);   // Write data to EEPROM
            ACKPoll();                  // Poll the 24LC01B for state
            datai = ByteRead(address);  // Read data from EEPROM into SSPBUF
        } while(datai != datao);        // Loop as long as data not correctly
                                        //    written to 24LC01B

        address++;                      // Increment address
    }
    while(1)                            // Done writing 128 bytes to 24LC01B, Loop forever
    {
        Nop();
    }
}
```

RRNCF **Rotate Right f (no carry)**

Syntax: [*label*] RRNCF f,d

Operands: $0 \le f \le 255$
$d \in [0,1]$

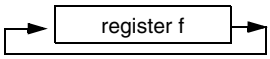
Operation: f<n> → d<n-1>;
f<0> → d<7>

Status Affected: None

Encoding:

0010	000d	ffff	ffff

Description: The contents of register 'f' are rotated one bit to the right. If 'd' is 0, the result is placed in WREG. If 'd' is 1, the result is placed back in register 'f'.



Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

Example 1: `RRNCF REG, 1`

Before Instruction
WREG = ?
REG = 1101 0111

After Instruction
WREG = 0
REG = 1110 1011

Example 2: `RRNCF REG, 0`

Before Instruction
WREG = ?
REG = 1101 0111

After Instruction
WREG = 1110 1011
REG = 1101 0111

SETF **Set f**

Syntax: [*label*] SETF f,s

Operands: $0 \le f \le 255$
$s \in [0,1]$

Operation: FFh → f;
FFh → d

Status Affected: None

Encoding:

0010	101s	ffff	ffff

Description: If 's' is 0, both the data memory location 'f' and WREG are set to FFh. If 's' is 1, only the data memory location 'f' is set to FFh.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write register 'f' and other specified register

Example1: `SETF REG, 0`

Before Instruction
REG = 0xDA
WREG = 0x05

After Instruction
REG = 0xFF
WREG = 0xFF

Example2: `SETF REG, 1`

Before Instruction
REG = 0xDA
WREG = 0x05

After Instruction
REG = 0xFF
WREG = 0x05

FIGURE 20-13: SPI MASTER MODE TIMING (CKE = 0)

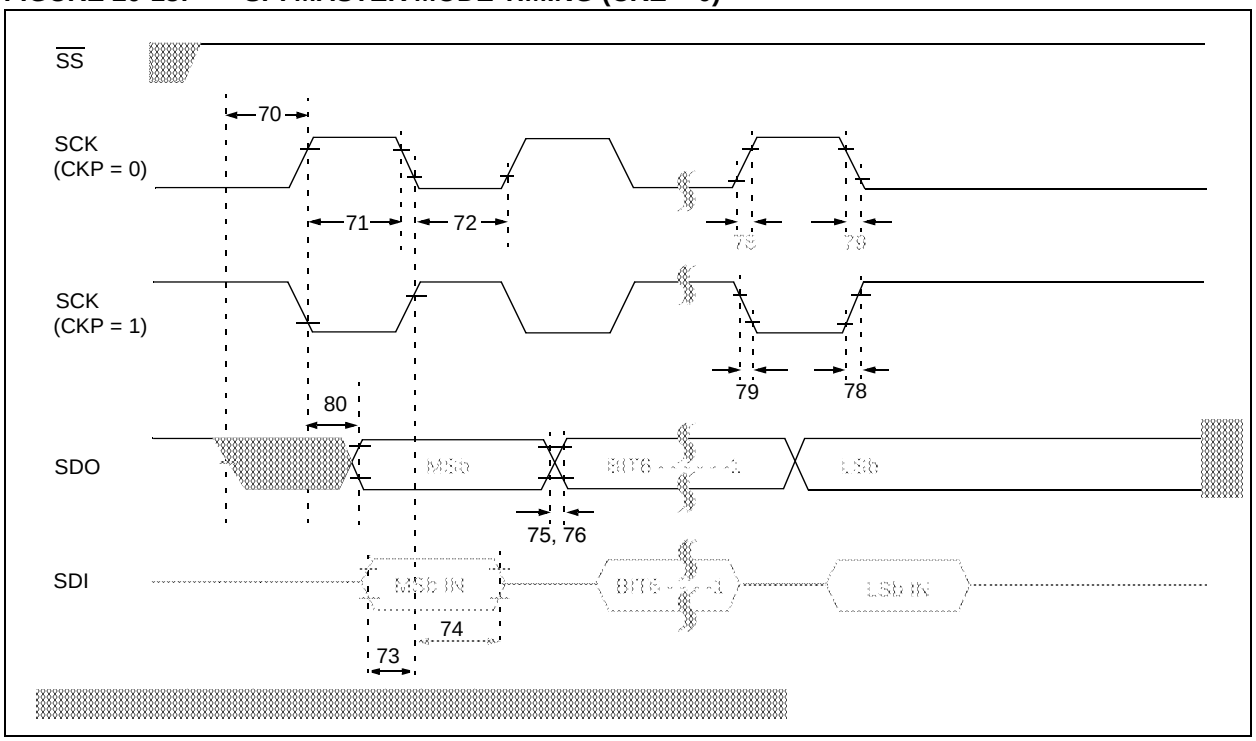


TABLE 20-8: SPI MODE REQUIREMENTS (MASTER MODE, CKE = 0)

Param. No.	Symbol	Characteristic		Min	Typ†	Max	Units	Conditions
70	TssL2scH, TssL2scL	$\overline{SS}\downarrow$ to SCK$\downarrow$ or SCK$\uparrow$ input		Tcy	—	—	ns	
71	TscH	SCK input high time (Slave mode)	Continuous	1.25TCY + 30	—	—	ns	
71A			Single Byte	40	—	—	ns	**(Note 1)**
72	TscL	SCK input low time (Slave mode)	Continuous	1.25TCY + 30	—	—	ns	
72A			Single Byte	40	—	—	ns	**(Note 1)**
73	TdiV2scH, TdiV2scL	Setup time of SDI data input to SCK edge		100	—	—	ns	
73A	TB2B	Last clock edge of Byte1 to the 1st clock edge of Byte2		1.5TCY + 40	—	—	ns	**(Note 1)**
74	TscH2diL, TscL2diL	Hold time of SDI data input to SCK edge		100	—	—	ns	
75	TdoR	SDO data output rise time		—	10	25	ns	
76	TdoF	SDO data output fall time		—	10	25	ns	
78	TscR	SCK output rise time (Master mode)		—	10	25	ns	
79	TscF	SCK output fall time (Master mode)		—	10	25	ns	
80	TscH2doV, TscL2doV	SDO data output valid after SCK edge		—	—	50	ns	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated.

Note 1: Specification 73A is only required if specifications 71A and 72A are used.

FIGURE 20-15: SPI SLAVE MODE TIMING (CKE = 0)

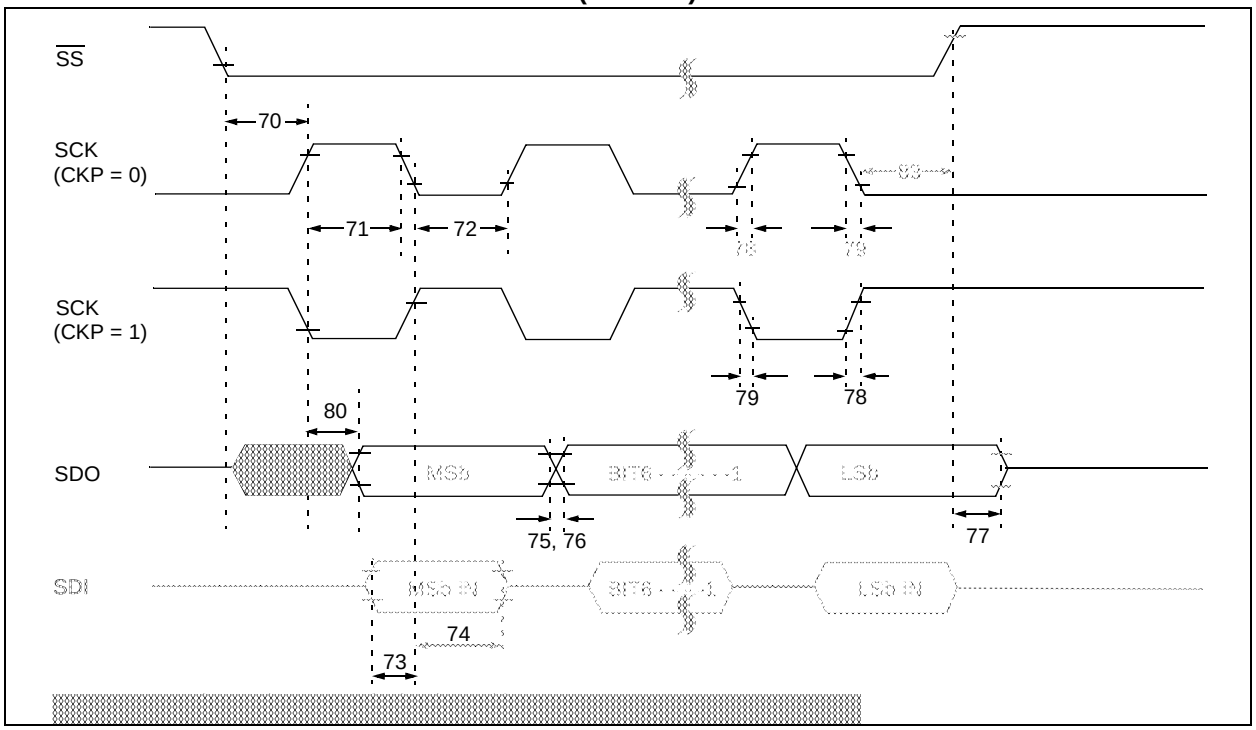


TABLE 20-10: SPI MODE REQUIREMENTS (SLAVE MODE TIMING, CKE = 0)

Param. No.	Symbol	Characteristic		Min	Typ†	Max	Units	Conditions
70	TssL2scH, TssL2scL	$\overline{SS}$↓ to SCK↓ or SCK↑ input		Tcy	—	—	ns	
71	TscH	SCK input high time (Slave mode)	Continuous	1.25TCY + 30	—	—	ns	
71A			Single Byte	40	—	—	ns	**(Note 1)**
72	TscL	SCK input low time (Slave mode)	Continuous	1.25TCY + 30	—	—	ns	
72A			Single Byte	40	—	—	ns	**(Note 1)**
73	TdiV2scH, TdiV2scL	Setup time of SDI data input to SCK edge		100	—	—	ns	
73A	TB2B	Last clock edge of Byte1 to the 1st clock edge of Byte2		1.5TCY + 40	—	—	ns	**(Note 1)**
74	TscH2diL, TscL2diL	Hold time of SDI data input to SCK edge		100	—	—	ns	
75	TdoR	SDO data output rise time		—	10	25	ns	
76	TdoF	SDO data output fall time		—	10	25	ns	
77	TssH2doZ	$\overline{SS}$↑ to SDO output hi-impedance		10	—	50	ns	
78	TscR	SCK output rise time (Master mode)		—	10	25	ns	
79	TscF	SCK output fall time (Master mode)		—	10	25	ns	
80	TscH2doV, TscL2doV	SDO data output valid after SCK edge		—	—	50	ns	
83	TscH2ssH, TscL2ssH	$\overline{SS}$ ↑ after SCK edge		1.5TCY + 40	—	—	ns	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated.

Note 1: Specification 73A is only required if specifications 71A and 72A are used.

Param No.	Sym	Characteristic		Min	Max	Units	Conditions
110	Tbuf	Bus free time	100 kHz mode	4.7	—	ms	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	ms	
			1 MHz mode(1)	0.5	—	ms	
D102	Cb	Bus capacitive loading		—	400	pF	

Note 1: Maximum pin capacitance = 10 pF for all I^2C pins.

2: A fast mode (400 KHz) I^2C bus device can be used in a standard mode I^2C bus system, but the parameter # 107 ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line. Parameter #102 + #107 = 1000 + 250 = 1250 ns (for 100 kHz mode) before the SCL line is released.

3: C_b is specified to be from 10-400pF. The minimum specifications are characterized with C_b=10pF. The rise time spec (t_r) is characterized with R_p=R_p min. The minimum fall time specification (t_f) is characterized with C_b=10pF,and R_p=R_p max. These are only valid for fast mode operation (V_{DD}=4.5-5.5V) and where the SPM bit (SSPSTAT<7>) =1.)

4: Max specifications for these parameters are valid for falling edge only. Specs are characterized with R_p=R_p min and C_b=400pF for standard mode, 200pF for fast mode, and 10pF for 1MHz mode.

FIGURE 20-19: USART SYNCHRONOUS TRANSMISSION (MASTER/SLAVE) TIMING

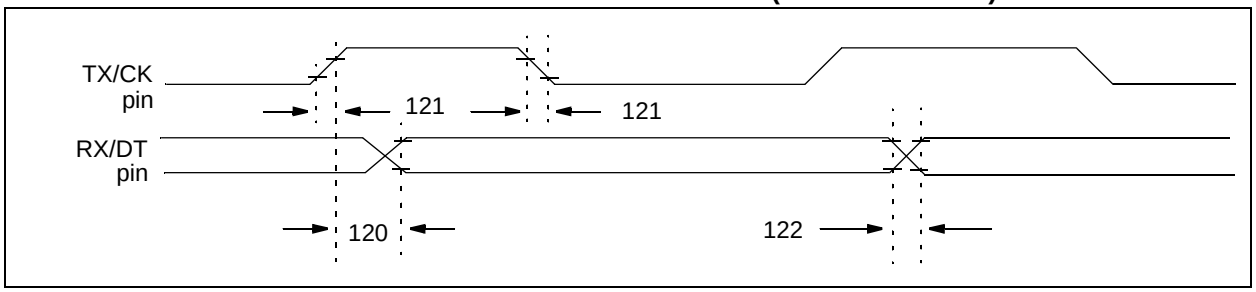


TABLE 20-14: USART SYNCHRONOUS TRANSMISSION REQUIREMENTS

Param No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
120	TckH2dtV	SYNC XMIT (MASTER & SLAVE) Clock high to data out valid	PIC17**C**XXX	—	—	50	ns	
			PIC17**LC**XXX	—	—	75	ns	
121	TckRF	Clock out rise time and fall time (Master mode)	PIC17**C**XXX	—	—	25	ns	
			PIC17**LC**XXX	—	—	40	ns	
122	TdtRF	Data out rise time and fall time	PIC17**C**XXX	—	—	25	ns	
			PIC17**LC**XXX	—	—	40	ns	

† Data in “Typ” column is at 5V, 25°C unless otherwise stated.

TABLE 20-18: A/D CONVERTER CHARACTERISTICS

Param. No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
A01	NR	Resolution		—	—	10	bit	VREF+ = VDD = 5.12V, VSS ≤ VAIN ≤ VREF+
				—	—	10	bit	(VREF+ — VREF-) ≥ 3.0V, VREF- ≤ VAIN ≤ VREF+
A02	EABS	Absolute error		—	—	< ±1	LSb	VREF+ = VDD = 5.12V, VSS ≤ VAIN ≤ VREF+
				—	—	< ±1	LSb	(VREF+ — VREF-) ≥ 3.0V, VREF- ≤ VAIN ≤ VREF+
A03	EIL	Integral linearity error		—	—	< ±1	LSb	VREF+ = VDD = 5.12V, VSS ≤ VAIN ≤ VREF+
				—	—	< ±1	LSb	(VREF+ — VREF-) ≥ 3.0V, VREF- ≤ VAIN ≤ VREF+
A04	EDL	Differential linearity error		—	—	< ±1	LSb	VREF+ = VDD = 5.12V, VSS ≤ VAIN ≤ VREF+
				—	—	< ±1	LSb	(VREF+ — VREF-) ≥ 3.0V, VREF- ≤ VAIN ≤ VREF+
A05	EFS	Full scale error		—	—	< ±1	LSb	VREF+ = VDD = 5.12V, VSS ≤ VAIN ≤ VREF+
				—	—	< ±1	LSb	(VREF+ — VREF-) ≥ 3.0V, VREF- ≤ VAIN ≤ VREF+
A06	EOFF	Offset error		—	—	< ±1	LSb	VREF+ = VDD = 5.12V, VSS ≤ VAIN ≤ VREF+
				—	—	< ±1	LSb	(VREF+ — VREF-) ≥ 3.0V, VREF- ≤ VAIN ≤ VREF+
A10	—	Monotonicity		—	guaranteed(3)	—	—	VSS ≤ VAIN ≤ VREF
A20	VREF	Reference voltage (VREF+ — VREF-)		0V	—	—	V	VREF delta when changing voltage levels on VREF inputs
A20A				3V	—	—	V	Absolute minimum electrical spec. to ensure 10-bit accuracy
A21	VREF+	Reference voltage high		AVSS + 3.0V	—	AVDD + 0.3V	V	
A22	VREF-	Reference voltage low		Avss - 0.3V	—	AVDD - 3.0V	V	
A25	VAIN	Analog input voltage		AVSS - 0.3V	—	Vref + 0.3V	V	
A30	ZAIN	Recommended impedance of analog voltage source		—	—	10.0	kΩ	
A40	IAD	A/D conversion current (VDD)	PIC17**C**XXX	—	180	—	μA	Average current consumption when A/D is on **(Note 1)**
			PIC17**LC**XXX	—	90	—	μA	
A50	IREF	VREF input current **(Note 2)**		10	—	1000	μA	During VAIN acquisition. Based on differential of VHOLD to VAIN
				—	—	10	μA	During A/D conversion cycle

† Data in "Typ" column is at 5V, 25°C unless otherwise stated.

Note 1: When A/D is off, it will not consume any current other than minor leakage current. The power-down current spec includes any such leakage from the A/D module.

2: VREF current is from RG0 and RG1 pins or AVDD and AVSS pins, whichever is selected as reference input.

3: The A/D conversion result never decreases with an increase in the Input Voltage and has no missing codes.

FIGURE 21-15: TYPICAL, MINIMUM AND MAXIMUM WDT PERIOD vs. VDD (-40°C TO +125°C)

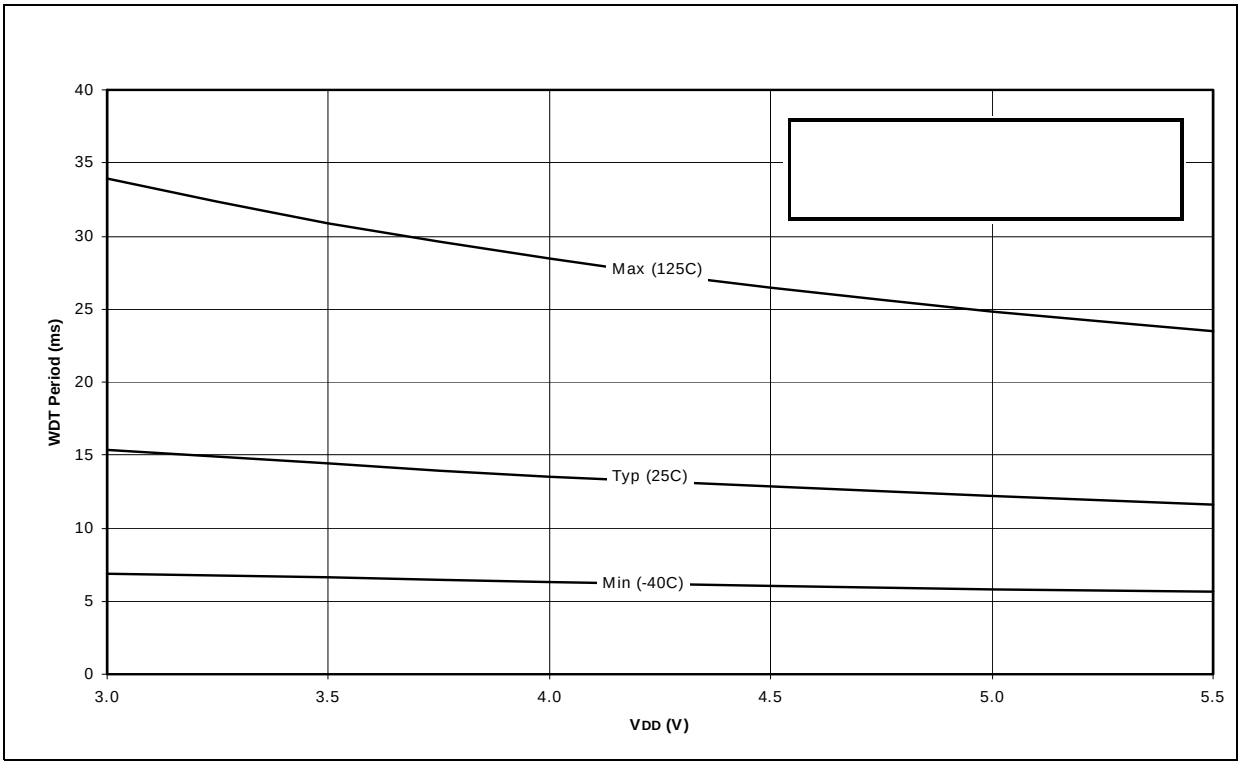


FIGURE 21-16: TYPICAL WDT PERIOD vs. VDD OVER TEMPERATURE (-40°C TO +125°C)

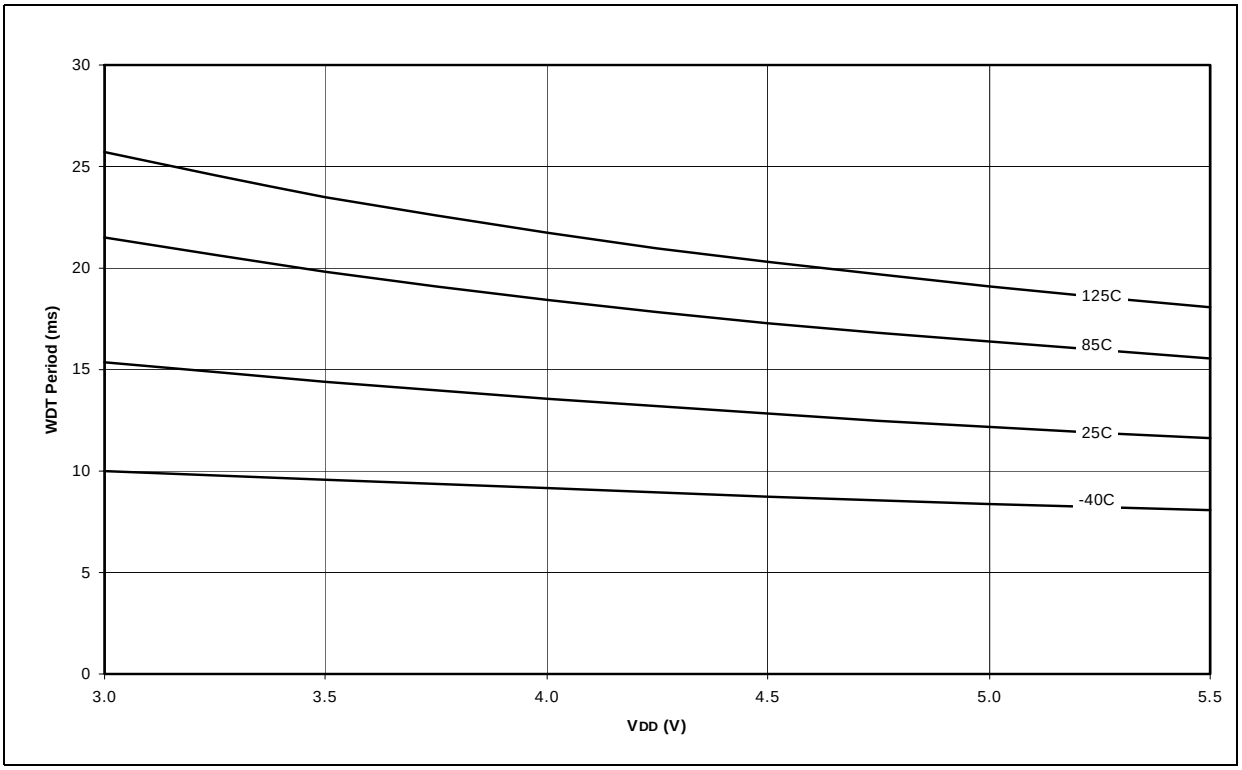


FIGURE 21-21: TYPICAL, MAXIMUM AND MINIMUM VIN vs. VDD (TTL INPUT, -40°C to 125°C)

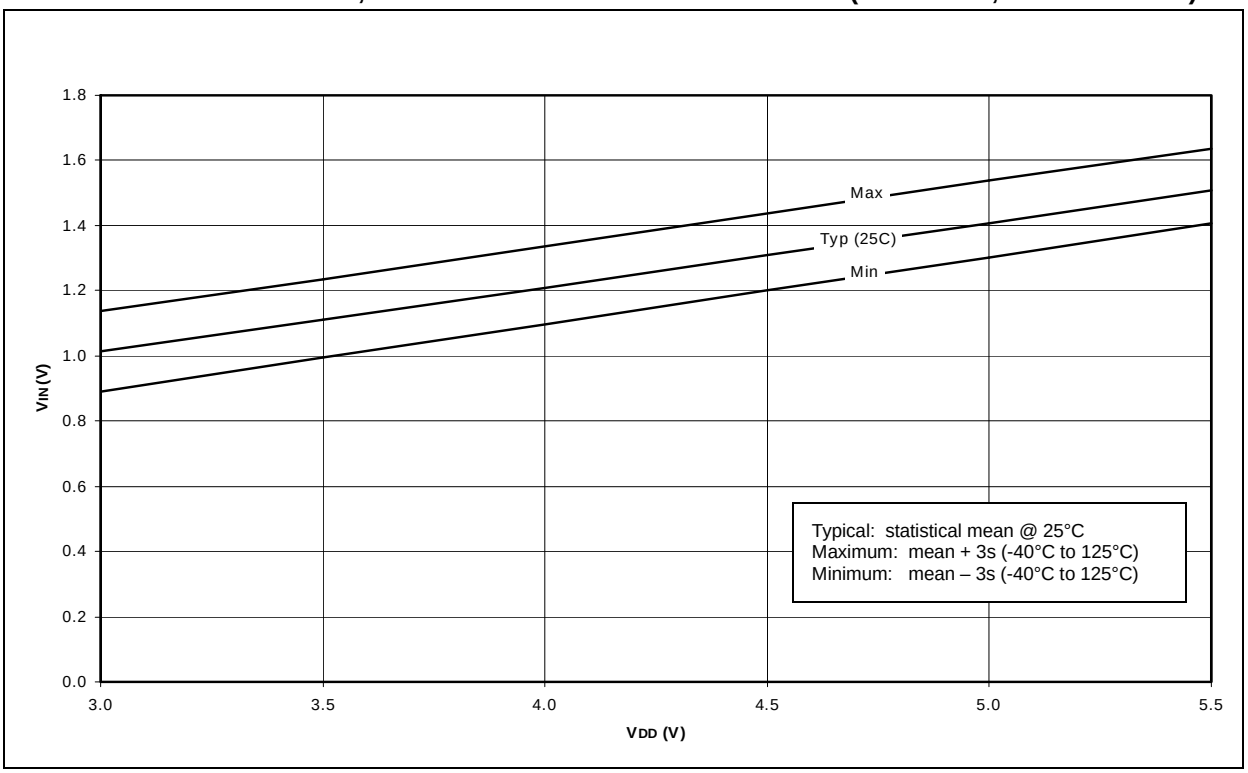


FIGURE 21-22: MAXIMUM AND MINIMUM VIN vs. VDD (ST Input, -40° C to +125°C)

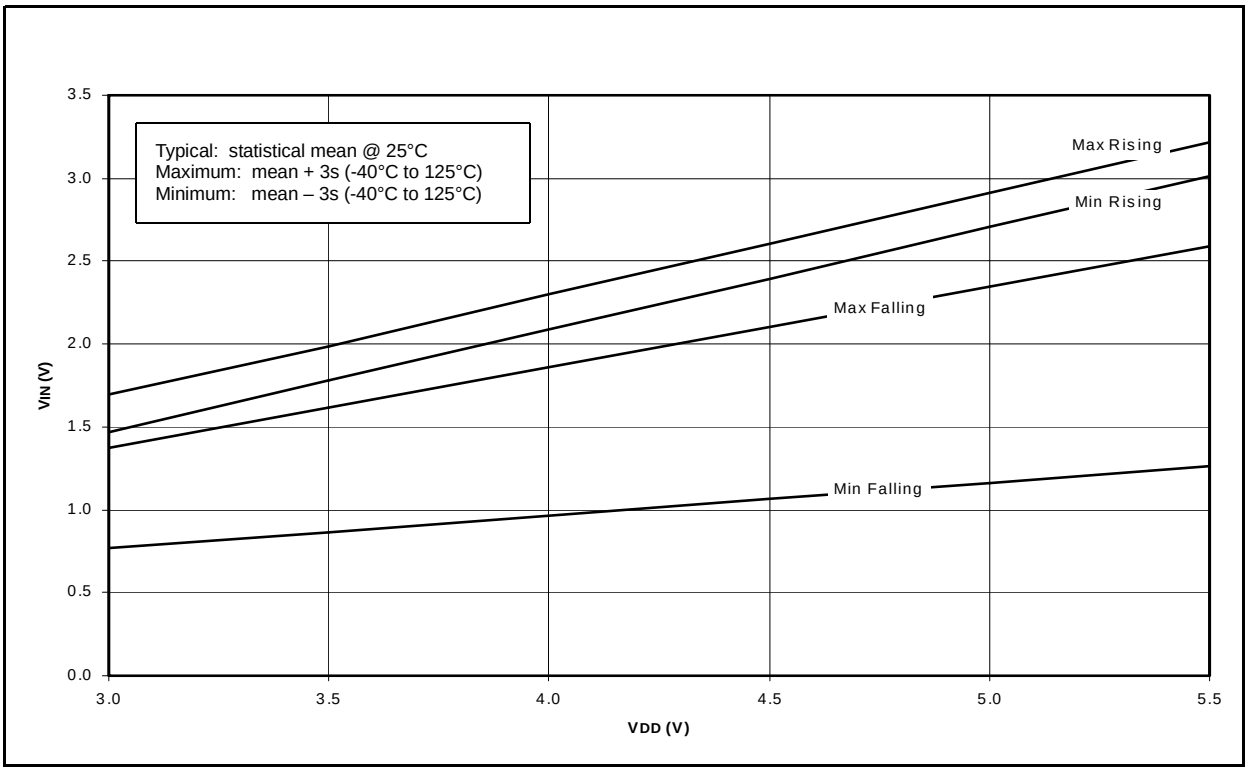


FIGURE 21-23: MAXIMUM AND MINIMUM VIN vs. VDD (I^2C Input, -40°C to +125°C)