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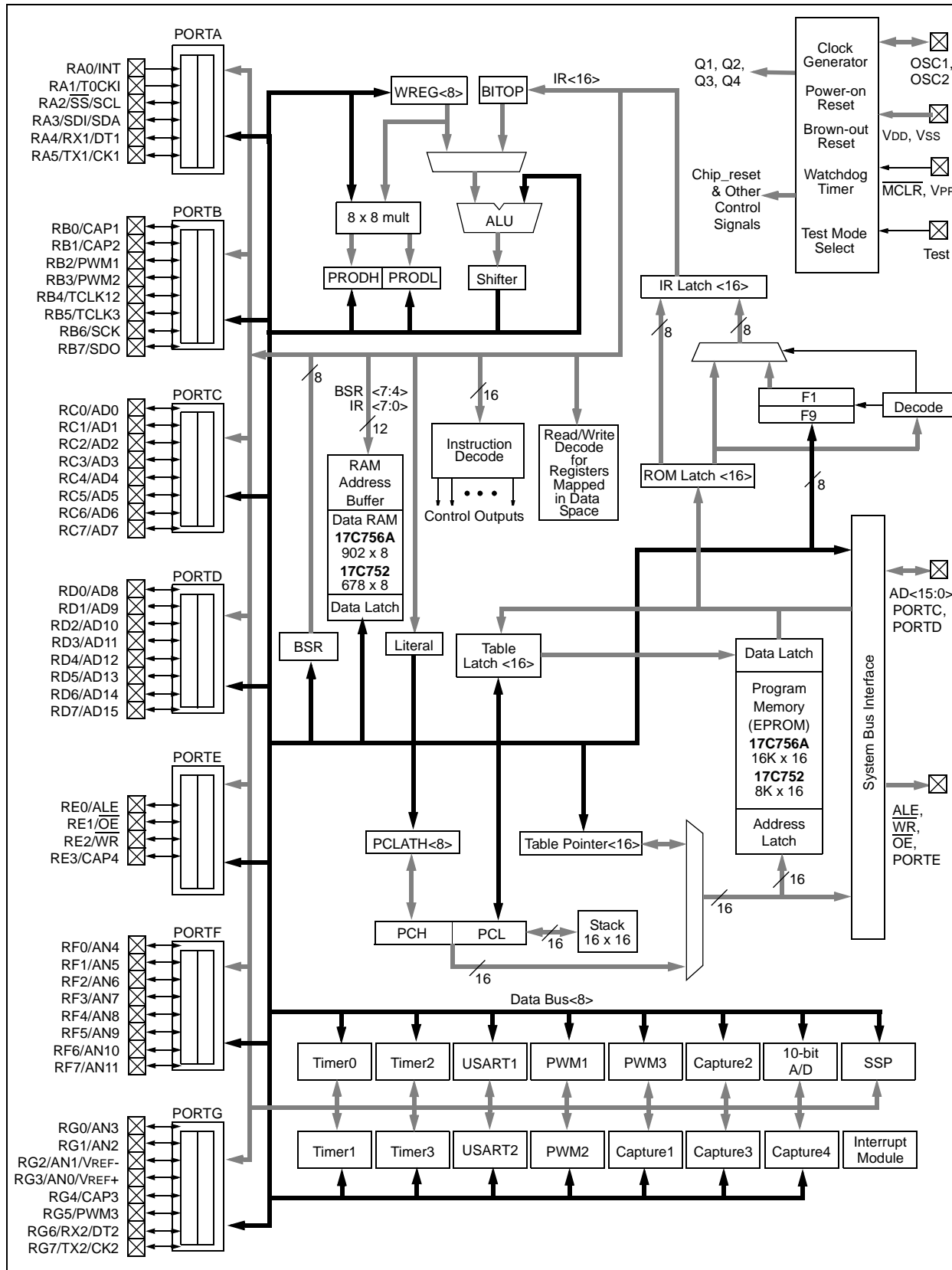
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Details

Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	33MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	66
Program Memory Size	16KB (8K x 16)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	678 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic17c762-33-l

PIC17C7XX

FIGURE 3-1: PIC17C752/756A BLOCK DIAGRAM



7.2 Data Memory Organization

Data memory is partitioned into two areas. The first is the General Purpose Registers (GPR) area, and the second is the Special Function Registers (SFR) area. The SFRs control and provide status of device operation.

Portions of data memory are banked, this occurs in both areas. The GPR area is banked to allow greater than 232 bytes of general purpose RAM.

Banking requires the use of control bits for bank selection. These control bits are located in the Bank Select Register (BSR). If an access is made to the unbanked region, the BSR bits are ignored. Figure 7-5 shows the data memory map organization.

Instructions `MOVWF` and `MOVF` provide the means to move values from the peripheral area ("P") to any location in the register file ("F"), and vice-versa. The definition of the "P" range is from 0h to 1Fh, while the "F" range is 0h to FFh. The "P" range has six more locations than peripheral registers, which can be used as General Purpose Registers. This can be useful in some applications where variables need to be copied to other locations in the general purpose RAM (such as saving status information during an interrupt).

The entire data memory can be accessed either directly, or indirectly (through file select registers FSR0 and FSR1) (see Section 7.4). Indirect addressing uses the appropriate control bits of the BSR for access into the banked areas of data memory. The BSR is explained in greater detail in Section 7.8.

7.2.1 GENERAL PURPOSE REGISTER (GPR)

All devices have some amount of GPR area. The GPRs are 8-bits wide. When the GPR area is greater than 232, it must be banked to allow access to the additional memory space.

All the PIC17C7XX devices have banked memory in the GPR area. To facilitate switching between these banks, the `MOVLB` bank instruction has been added to the instruction set. GPRs are not initialized by a Power-on Reset and are unchanged on all other RESETS.

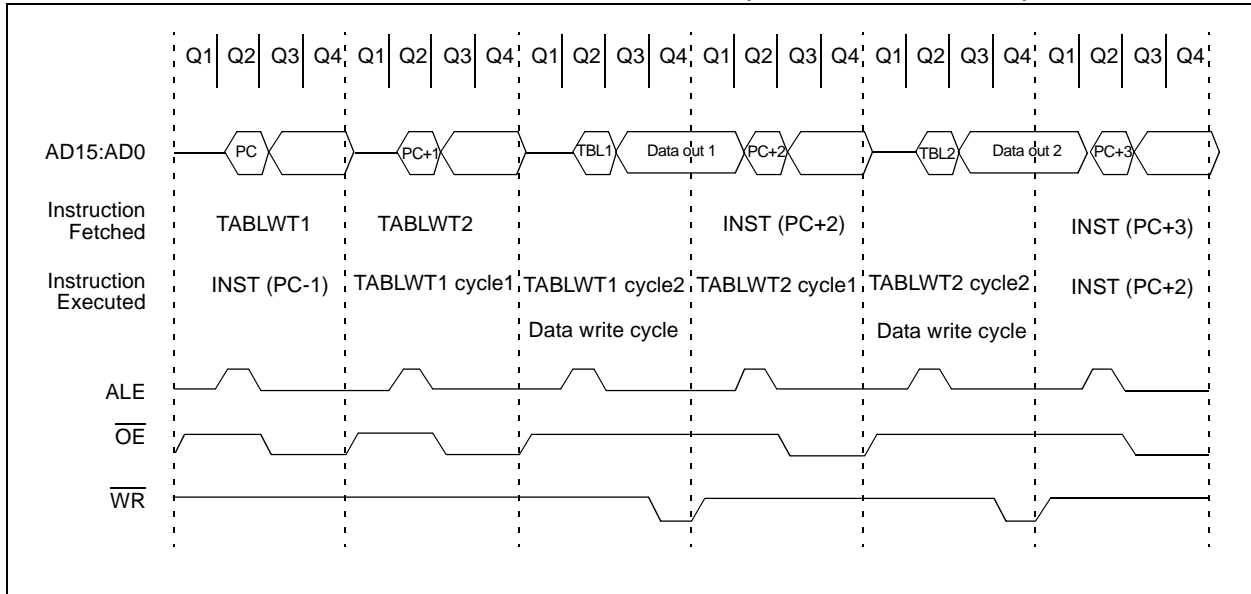
7.2.2 SPECIAL FUNCTION REGISTERS (SFR)

The SFRs are used by the CPU and peripheral functions to control the operation of the device (Figure 7-5). These registers are static RAM.

The SFRs can be classified into two sets, those associated with the "core" function and those related to the peripheral functions. Those registers related to the "core" are described here, while those related to a peripheral feature are described in the section for each peripheral feature.

The peripheral registers are in the banked portion of memory, while the core registers are in the unbanked region. To facilitate switching between the peripheral banks, the `MOVLB` bank instruction has been provided.

FIGURE 8-6: CONSECUTIVE TABLWT WRITE TIMING (EXTERNAL MEMORY)



10.9 PORTJ and DDRJ Registers (PIC17C76X only)

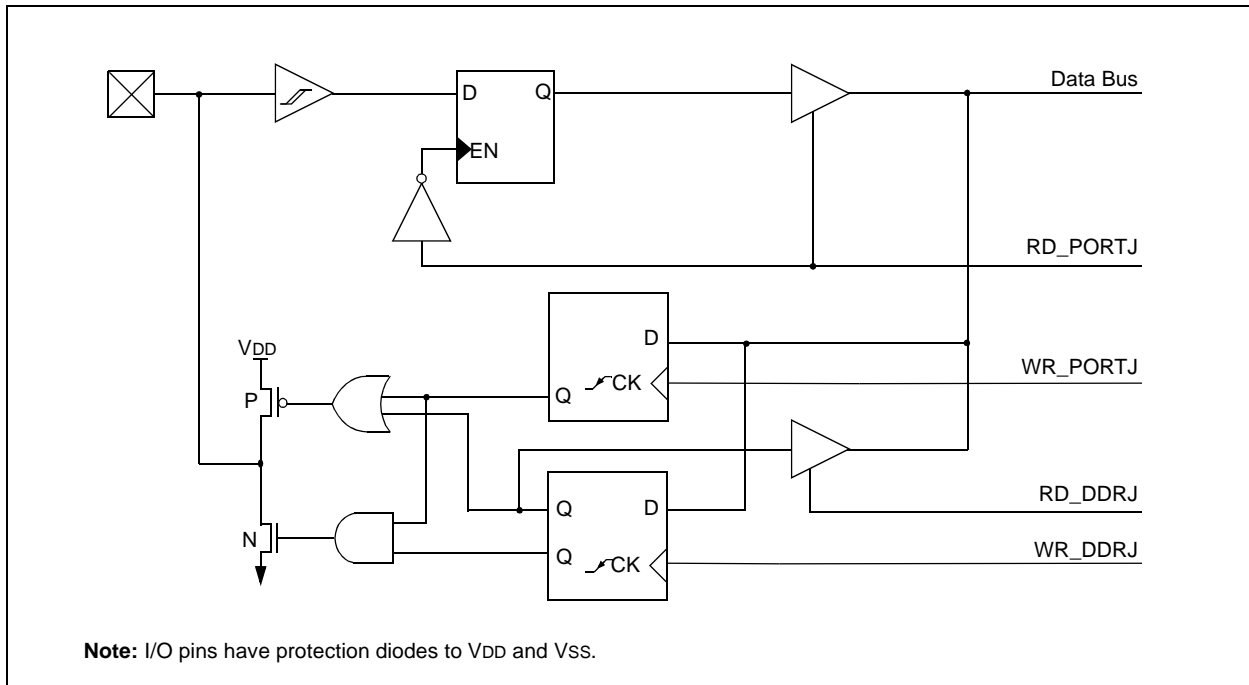
PORTJ is an 8-bit wide, bi-directional port. The corresponding data direction register is DDRJ. A '1' in DDRJ configures the corresponding port pin as an input. A '0' in the DDRJ register configures the corresponding port pin as an output. Reading PORTJ reads the status of the pins, whereas writing to PORTJ will write to the respective port latch.

PORTJ is a general purpose I/O port.

EXAMPLE 10-9: INITIALIZING PORTJ

```
MOVLB 8      ; Select Bank 8
CLRF  PORTJ, F ; Initialize PORTJ data
               ; latches before setting
               ; the data direction
               ; register
MOVLW  0xCF   ; Value used to initialize
               ; data direction
MOVWF  DDRJ   ; Set RJ<3:0> as inputs
               ; RJ<5:4> as outputs
               ; RJ<7:6> as inputs
```

FIGURE 10-19: PORTJ BLOCK DIAGRAM



12.0 TIMER0

The Timer0 module consists of a 16-bit timer/counter, TMR0. The high byte is register TMR0H and the low byte is register TMR0L. A software programmable 8-bit prescaler makes Timer0 an effective 24-bit overflow timer. The clock source is software programmable as either the internal instruction clock, or an external clock on the RA1/T0CKI pin. The control bits for this module are in register T0STA (Figure 12-1).

REGISTER 12-1: T0STA REGISTER (ADDRESS: 05h, UNBANKED)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
INTEDG	T0SE	T0CS	T0PS3	T0PS2	T0PS1	T0PS0	—
bit 7							bit 0

- bit 7 **INTEDG:** RA0/INT Pin Interrupt Edge Select bit
This bit selects the edge upon which the interrupt is detected.
1 = Rising edge of RA0/INT pin generates interrupt
0 = Falling edge of RA0/INT pin generates interrupt
- bit 6 **T0SE:** Timer0 Clock Input Edge Select bit
This bit selects the edge upon which TMR0 will increment.
When T0CS = 0 (External Clock):
1 = Rising edge of RA1/T0CKI pin increments TMR0 and/or sets the T0CKIF bit
0 = Falling edge of RA1/T0CKI pin increments TMR0 and/or sets the T0CKIF bit
When T0CS = 1 (Internal Clock):
Don't care
- bit 5 **T0CS:** Timer0 Clock Source Select bit
This bit selects the clock source for TMR0.
1 = Internal instruction clock cycle (Tcy)
0 = External clock input on the T0CKI pin
- bit 4-1 **T0PS3:T0PS0:** Timer0 Prescale Selection bits
These bits select the prescale value for TMR0.
- | T0PS3:T0PS0 | Prescale Value |
|-------------|----------------|
| 0000 | 1:1 |
| 0001 | 1:2 |
| 0010 | 1:4 |
| 0011 | 1:8 |
| 0100 | 1:16 |
| 0101 | 1:32 |
| 0110 | 1:64 |
| 0111 | 1:128 |
| 1xxx | 1:256 |
- bit 0 **Unimplemented:** Read as '0'

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR Reset	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

13.2.3 READING THE CAPTURE REGISTERS

The Capture overflow status flag bits are double buffered. The master bit is set if one captured word is already residing in the Capture register and another “event” has occurred on the CAPx pin. The new event will not transfer the TMR3 value to the capture register, protecting the previous unread capture value. When the user reads both the high and the low bytes (in any

order) of the Capture register, the master overflow bit is transferred to the slave overflow bit (CAxOVF) and then the master bit is reset. The user can then read TCONx to determine the value of CAxOVF.

An example of an instruction sequence to read capture registers and capture overflow flag bits is shown in Example 13-1. Depending on the capture source, different registers will need to be read.

EXAMPLE 13-1: SEQUENCE TO READ CAPTURE REGISTERS

```
MOVLB 3           ; Select Bank 3
MOVFPF CA2L, LO_BYTE ; Read Capture2 low byte, store in LO_BYTE
MOVFPF CA2H, HI_BYTE ; Read Capture2 high byte, store in HI_BYTE
MOVFPF TCON2, STAT_VAL ; Read TCON2 into file STAT_VAL
```

TABLE 13-6: REGISTERS ASSOCIATED WITH CAPTURE

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	MCLR, WDT
16h, Bank 3	TCON1	CA2ED1	CA2ED0	CA1ED1	CA1ED0	T16	TMR3CS	TMR2CS	TMR1CS	0000 0000	0000 0000
17h, Bank 3	TCON2	CA2OVF	CA1OVF	PWM2ON	PWM1ON	CA1/PR3	TMR3ON	TMR2ON	TMR1ON	0000 0000	0000 0000
16h, Bank 7	TCON3	—	CA4OVF	CA3OVF	CA4ED1	CA4ED0	CA3ED1	CA3ED0	PWM3ON	-000 0000	-000 0000
12h, Bank 2	TMR3L	Holding Register for the Low Byte of the 16-bit TMR3 Register								xxxx xxxx	uuuu uuuu
13h, Bank 2	TMR3H	Holding Register for the High Byte of the 16-bit TMR3 Register								xxxx xxxx	uuuu uuuu
16h, Bank 1	PIR1	RBIF	TMR3IF	TMR2IF	TMR1IF	CA2IF	CA1IF	TX1IF	RC1IF	x000 0010	u000 0010
17h, Bank 1	PIE1	RBIE	TMR3IE	TMR2IE	TMR1IE	CA2IE	CA1IE	TX1IE	RC1IE	0000 0000	0000 0000
10h, Bank 4	PIR2	SSPIF	BCLIF	ADIF	—	CA4IF	CA3IF	TX2IF	RC2IF	000- 0010	000- 0010
11h, Bank 4	PIE2	SSPIE	BCLIE	ADIE	—	CA4IE	CA3IE	TX2IE	RC2IE	000- 0000	000- 0000
07h, Unbanked	INTSTA	PEIF	T0CKIF	T0IF	INTF	PEIE	T0CKIE	T0IE	INTE	0000 0000	0000 0000
06h, Unbanked	CPUSTA	—	—	STKAV	GLINTD	T0	PD	POR	BOR	--11 11qq	--11 qquu
16h, Bank 2	PR3L/CA1L	Timer3 Period Register, Low Byte/Capture1 Register, Low Byte								xxxx xxxx	uuuu uuuu
17h, Bank 2	PR3H/CA1H	Timer3 Period Register, High Byte/Capture1 Register, High Byte								xxxx xxxx	uuuu uuuu
14h, Bank 3	CA2L	Capture2 Low Byte								xxxx xxxx	uuuu uuuu
15h, Bank 3	CA2H	Capture2 High Byte								xxxx xxxx	uuuu uuuu
12h, Bank 7	CA3L	Capture3 Low Byte								xxxx xxxx	uuuu uuuu
13h, Bank 7	CA3H	Capture3 High Byte								xxxx xxxx	uuuu uuuu
14h, Bank 7	CA4L	Capture4 Low Byte								xxxx xxxx	uuuu uuuu
15h, Bank 7	CA4H	Capture4 High Byte								xxxx xxxx	uuuu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0', q = value depends on condition.
Shaded cells are not used by Capture.

PIC17C7XX

13.2.4 EXTERNAL CLOCK INPUT FOR TIMER3

When TMR3CS is set, the 16-bit TMR3 increments on the falling edge of clock input TCLK3. The input on the RB5/TCLK3 pin is sampled and synchronized by the internal phase clocks, twice every instruction cycle. This causes a delay from the time a falling edge appears on TCLK3 to the time TMR3 is actually incremented. For the external clock input timing requirements, see the Electrical Specification section. Figure 13-7 shows the timing diagram when operating from an external clock.

13.2.5 READING/WRITING TIMER3

Since Timer3 is a 16-bit timer and only 8-bits at a time can be read or written, care should be taken when reading or writing while the timer is running. The best method is to stop the timer, perform any read or write operation and then restart Timer3 (using the TMR3ON bit). However, if it is necessary to keep Timer3 free-running, care must be taken. For writing to the 16-bit TMR3, Example 13-2 may be used. For reading the 16-bit TMR3, Example 13-3 may be used. Interrupts must be disabled during this routine.

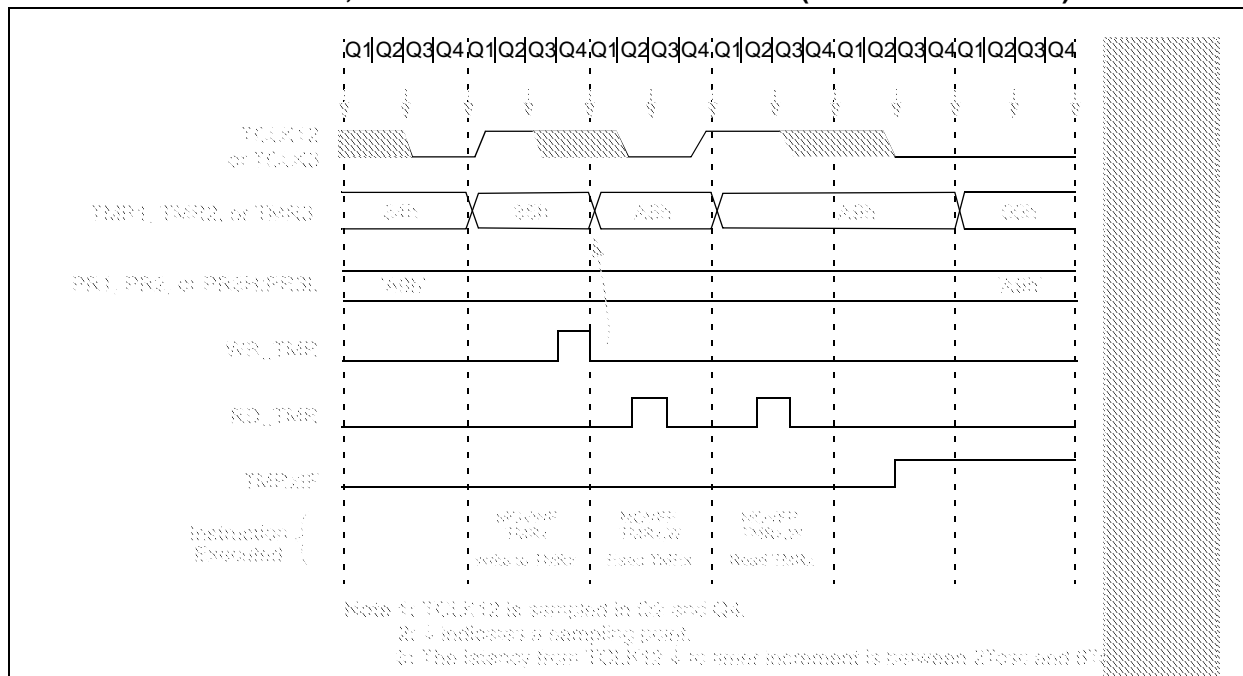
EXAMPLE 13-2: WRITING TO TMR3

```
BSF    CPUSTA, GLINTD    ; Disable interrupts
MOVFP  RAM_L,  TMR3L     ;
MOVFP  RAM_H,  TMR3H     ;
BCF    CPUSTA, GLINTD    ; Done, enable interrupts
```

EXAMPLE 13-3: READING FROM TMR3

```
MOVFP  TMR3L, TMPLO      ; read low TMR3
MOVFP  TMR3H, TMPHI      ; read high TMR3
MOVFP  TMPLO, WREG        ; tmplo -> wreg
CPFSLT TMR3L              ; TMR3L < wreg?
RETURN                                ; no then return
MOVFP  TMR3L, TMPLO      ; read low TMR3
MOVFP  TMR3H, TMPHI      ; read high TMR3
RETURN                                ; return
```

FIGURE 13-7: TIMER1, TIMER2 AND TIMER3 OPERATION (IN COUNTER MODE)



14.3.2 USART SYNCHRONOUS MASTER RECEPTION

Once Synchronous mode is selected, reception is enabled by setting either the SREN (RCSTA<5>) bit or the CREN (RCSTA<4>) bit. Data is sampled on the RX/DT pin on the falling edge of the clock. If SREN is set, then only a single word is received. If CREN is set, the reception is continuous until CREN is reset. If both bits are set, then CREN takes precedence. After clocking the last bit, the received data in the Receive Shift Register (RSR) is transferred to RCREG (if it is empty). If the transfer is complete, the interrupt bit RCIF is set. The actual interrupt can be enabled/disabled by setting/clearing the RCIE bit. RCIF is a read only bit which is reset by the hardware. In this case, it is reset when RCREG has been read and is empty. RCREG is a double buffered register; i.e., it is a two deep FIFO. It is possible for two bytes of data to be received and transferred to the RCREG FIFO and a third byte to begin shifting into the RSR. On the clocking of the last bit of the third byte, if RCREG is still full, then the overrun error bit OERR (RCSTA<1>) is set. The word in the RSR will be lost. RCREG can be read twice to retrieve the two bytes in the FIFO. The OERR bit has to be cleared in software. This is done by clearing the CREN bit. If OERR is set, transfers from RSR to RCREG are inhibited, so it is essential to clear the OERR bit if it is set. The 9th receive bit is buffered the same way as the receive data. Reading the RCREG register will allow the RX9D and FERR bits to be loaded with values for the next received data; therefore, it is essential for the user to read the RCSTA register before reading RCREG in order not to lose the old FERR and RX9D information.

Steps to follow when setting up a Synchronous Master Reception:

1. Initialize the SPBRG register for the appropriate baud rate. See Section 14.1 for details.
2. Enable the synchronous master serial port by setting bits SYNC, SPEN, and CSRC.
3. If interrupts are desired, then set the RCIE bit.
4. If 9-bit reception is desired, then set the RX9 bit.
5. If a single reception is required, set bit SREN. For continuous reception set bit CREN.
6. The RCIF bit will be set when reception is complete and an interrupt will be generated if the RCIE bit was set.
7. Read RCSTA to get the ninth bit (if enabled) and determine if any error occurred during reception.
8. Read the 8-bit received data by reading RCREG.
9. If any error occurred, clear the error by clearing CREN.

Note: To terminate a reception, either clear the SREN and CREN bits, or the SPEN bit. This will reset the receive logic so that it will be in the proper state when receive is re-enabled.

FIGURE 14-10: SYNCHRONOUS RECEPTION (MASTER MODE, SREN)

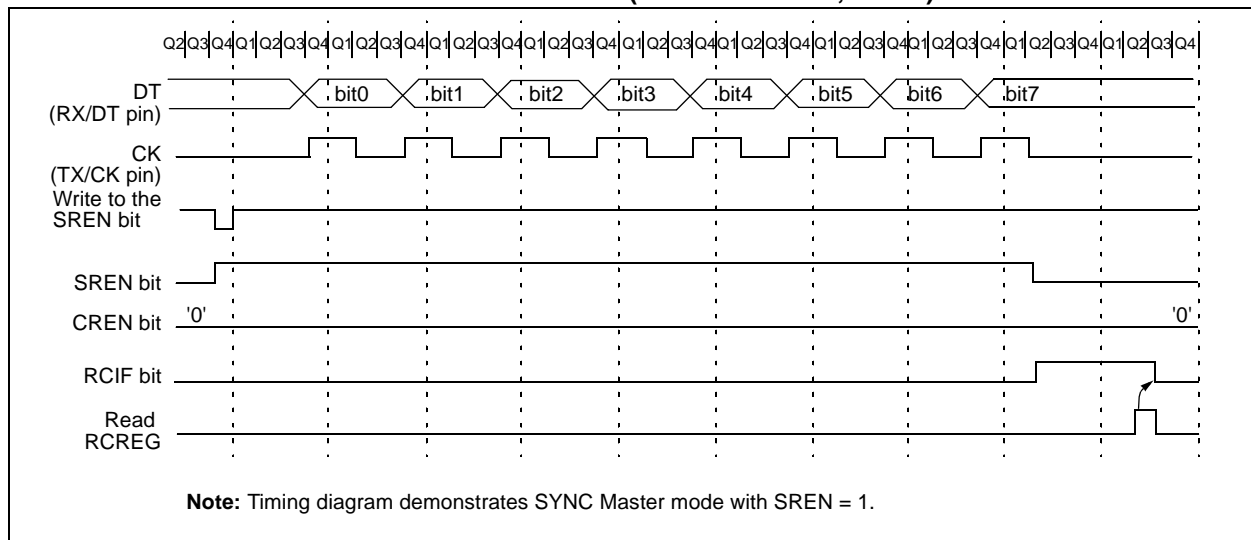
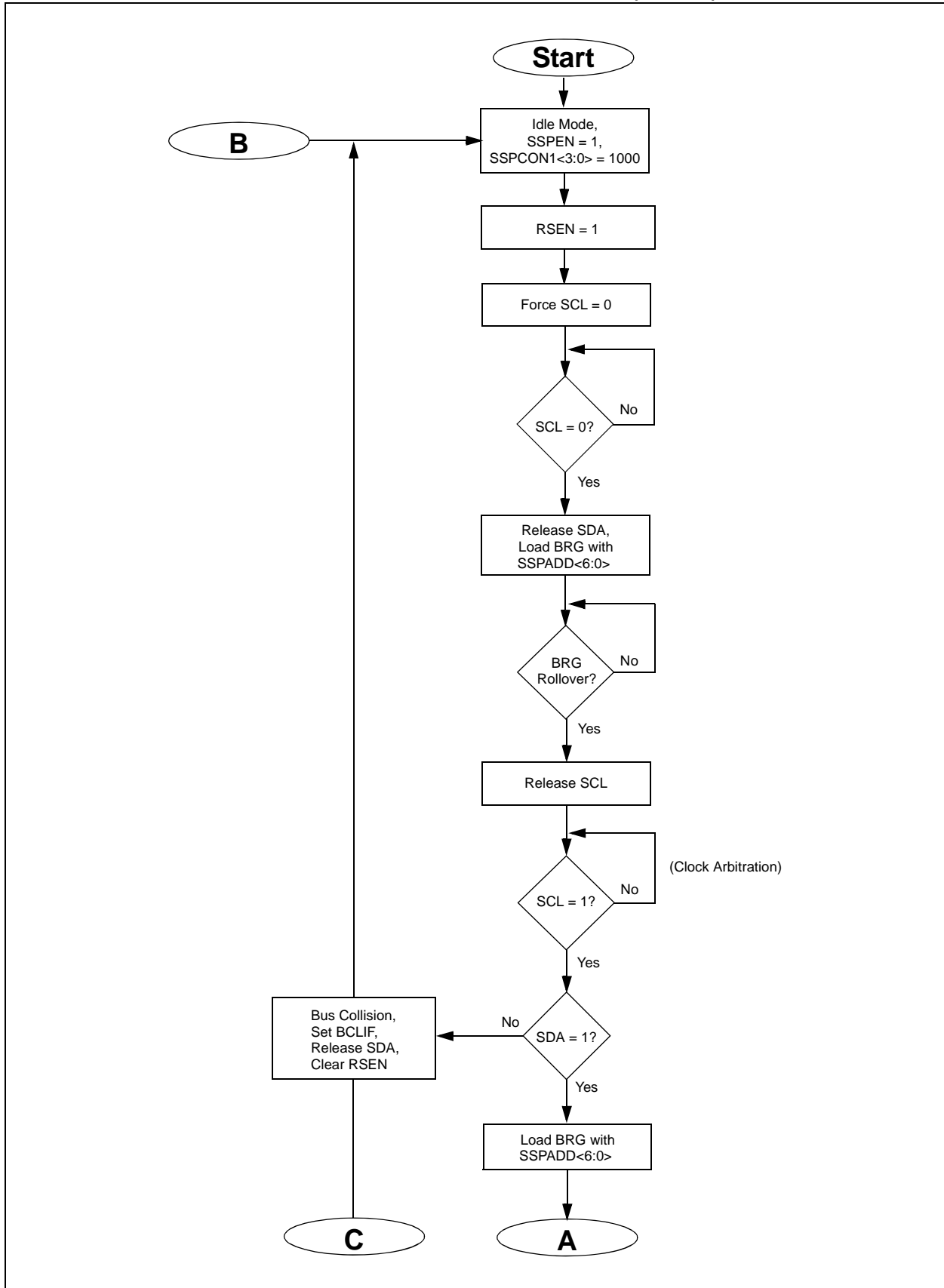


FIGURE 15-23: REPEATED START CONDITION FLOW CHART (PAGE 1)



15.2.11 I²C MASTER MODE TRANSMISSION

Transmission of a data byte, a 7-bit address, or either half of a 10-bit address, is accomplished by simply writing a value to SSPBUF register. This action will set the buffer full flag (BF) and allow the baud rate generator to begin counting and start the next transmission. Each bit of address/data will be shifted out onto the SDA pin after the falling edge of SCL is asserted (see data hold time spec). SCL is held low for one baud rate generator roll over count (TBRG). Data should be valid before SCL is released high (see Data setup time spec). When the SCL pin is released high, it is held that way for TBRG, the data on the SDA pin must remain stable for that duration and some hold time after the next falling edge of SCL. After the eighth bit is shifted out (the falling edge of the eighth clock), the BF flag is cleared and the master releases SDA, allowing the slave device being addressed to respond with an ACK bit during the ninth bit time, if an address match occurs or if data was received properly. The status of ACK is read into the ACKDT on the falling edge of the ninth clock. If the master receives an acknowledge, the acknowledge status bit (AKSTAT) is cleared. If not, the bit is set. After the ninth clock, the SSPIF is set and the master clock (baud rate generator) is suspended until the next data byte is loaded into the SSPBUF, leaving SCL low and SDA unchanged (Figure 15-26).

After the write to the SSPBUF, each bit of address will be shifted out on the falling edge of SCL until all seven address bits and the R/W bit are completed. On the falling edge of the eighth clock, the master will de-assert the SDA pin, allowing the slave to respond with an acknowledge. On the falling edge of the ninth clock, the master will sample the SDA pin to see if the address was recognized by a slave. The status of the ACK bit is loaded into the ACKSTAT status bit (SSPCON2<6>). Following the falling edge of the ninth clock transmission of the address, the SSPIF is set, the BF flag is cleared and the baud rate generator is turned off until another write to the SSPBUF takes place, holding SCL low and allowing SDA to float.

15.2.11.1 BF Status Flag

In Transmit mode, the BF bit (SSPSTAT<0>) is set when the CPU writes to SSPBUF and is cleared when all 8 bits are shifted out.

15.2.11.2 WCOL Status Flag

If the user writes the SSPBUF when a transmit is already in progress (i.e., SSPSR is still shifting out a data byte), then WCOL is set and the contents of the buffer are unchanged (the write doesn't occur).

WCOL must be cleared in software.

15.2.11.3 AKSTAT Status Flag

In Transmit mode, the AKSTAT bit (SSPCON2<6>) is cleared when the slave has sent an acknowledge (ACK = 0) and is set when the slave does not acknowledge (ACK = 1). A slave sends an acknowledge when it has recognized its address (including a general call), or when the slave has properly received its data.

18.2 Q Cycle Activity

Each instruction cycle (Tcy) is comprised of four Q cycles (Q1-Q4). The Q cycle is the same as the device oscillator cycle (Tosc). The Q cycles provide the timing/designation for the Decode, Read, Process Data, Write, etc., of each instruction cycle. The following diagram shows the relationship of the Q cycles to the instruction cycle.

The four Q cycles that make up an instruction cycle (Tcy) can be generalized as:

Q1: Instruction Decode Cycle or forced No operation

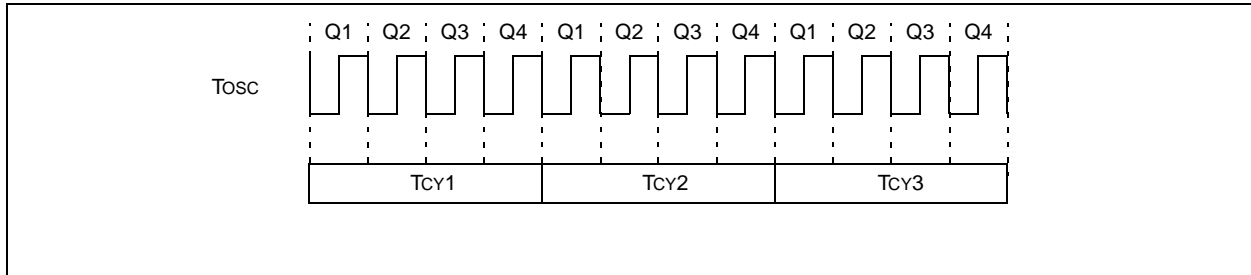
Q2: Instruction Read Cycle or No operation

Q3: Process the Data

Q4: Instruction Write Cycle or No operation

Each instruction will show the detailed Q cycle operation for the instruction.

FIGURE 18-2: Q CYCLE ACTIVITY



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MOVPF Move p to f

Syntax:	[label] MOVPF p,f			
Operands:	$0 \leq f \leq 255$ $0 \leq p \leq 31$			
Operation:	(p) → (f)			
Status Affected:	Z			
Encoding:	010p	pppp	ffff	ffff
Description:	<p>Move data from data memory location 'p' to data memory location 'f'. Location 'f' can be anywhere in the 256 byte data space (00h to FFh), while 'p' can be 00h to 1Fh.</p> <p>Either 'p' or 'f' can be WREG (a useful, special situation).</p> <p>MOVPF is particularly useful for transferring a peripheral register (e.g. the timer or an I/O port) to a data memory location. Both 'f' and 'p' can be indirectly addressed.</p>			
Words:	1			
Cycles:	1			
Q Cycle Activity:				
	Q1	Q2	Q3	Q4
	Decode	Read register 'p'	Process Data	Write register 'f'

Example: MOVPF REG1, REG2

Before Instruction

REG1 = 0x11
REG2 = 0x33

After Instruction

REG1 = 0x11
REG2 = 0x11

MOVWF Move WREG to f

Syntax:	[<i>label</i>] MOVWF <i>f</i>			
Operands:	$0 \leq f \leq 255$			
Operation:	(WREG) \rightarrow (<i>f</i>)			
Status Affected:	None			
Encoding:	0000	0001	ffff	ffff
Description:	Move data from WREG to register ' <i>f</i> '. Location ' <i>f</i> ' can be anywhere in the 256 byte data space.			
Words:	1			
Cycles:	1			
Q Cycle Activity:				
	Q1	Q2	Q3	Q4
	Decode	Read register ' <i>f</i> '	Process Data	Write register ' <i>f</i> '

Example: MOVWF REG

Before Instruction

WREG = 0x4F
REG = 0xFF

After Instruction

WREG = 0x4F
REG = 0x4F

PIC17C7XX

NOTES:

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Standard Operating Conditions (unless otherwise stated)							
Operating temperature							
-40°C ≤ TA ≤ +125°C for extended							
-40°C ≤ TA ≤ +85°C for industrial							
0°C ≤ TA ≤ +70°C for commercial							
Operating voltage VDD range as described in Section 20.1							
Param. No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D150	VOD	Open Drain High Voltage	–	–	8.5	V	RA2 and RA3 pins only pulled up to externally applied voltage
D100	Cosc2	Capacitive Loading Specs on Output Pins OSC2/CLKOUT pin	–	–	25	pF	In EC or RC osc modes, when OSC2 pin is outputting CLKOUT. External clock is used to drive OSC1.
D101	CIO	All I/O pins and OSC2 (in RC mode)	–	–	50	pF	
D102	CAD	System Interface Bus (PORTC, PORTD and PORTE)	–	–	50	pF	In Microprocessor or Extended Microcontroller mode
Internal Program Memory Programming Specs (Note 4)							
D110	VPP	Voltage on MCLR/VPP pin	12.75	–	13.25	V	(Note 5)
D111	VDDP	Supply voltage during programming	4.75	5.0	5.25	V	
D112	IPP	Current into MCLR/VPP pin	–	25	50	mA	
D113	IDDP	Supply current during programming	–	–	30	mA	
D114	TPROG	Programming pulse width	100	–	1000	ms	
							Terminated via internal/external interrupt or a RESET

† Data in “Typ” column is at 5V, 25°C unless otherwise stated.

- Note 1:** In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC17CXXX devices be driven with external clock in RC mode.
- 2:** The leakage current on the MCLR pin is strongly dependent on the applied voltage level. Higher leakage current may be measured at different input voltages.
- 3:** Negative current is defined as current sourced by the pin.
- 4:** These specifications are for the programming of the on-chip program memory EPROM through the use of the table write instructions. The complete programming specifications can be found in: PIC17C7XX Programming Specifications (Literature number DS TBD).
- 5:** The MCLR/VPP pin may be kept in this range at times other than programming, but is not recommended.
- 6:** For TTL buffers, the better of the two specifications may be used.

- Note 1:** When using the Table Write for internal programming, the device temperature must be less than 40°C.
- 2:** For In-Circuit Serial Programming (ICSP™), refer to the device programming specification.

20.4 Timing Diagrams and Specifications

FIGURE 20-6: EXTERNAL CLOCK TIMING

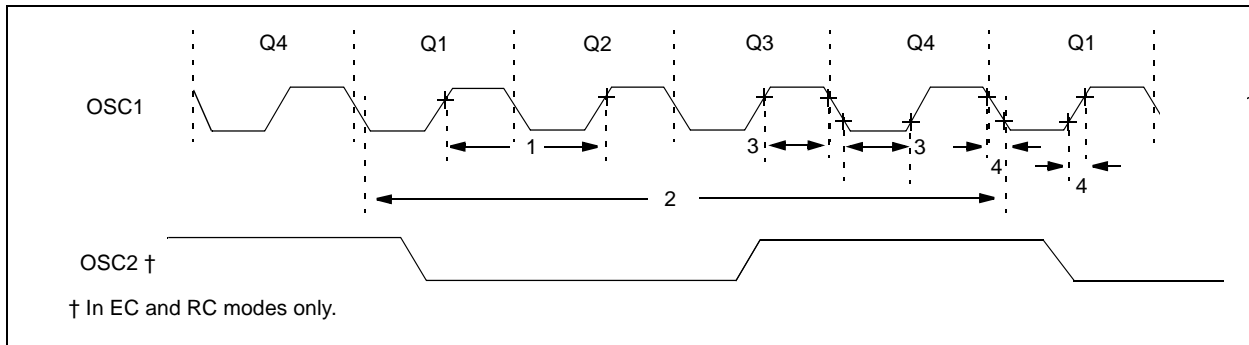


TABLE 20-1: EXTERNAL CLOCK TIMING REQUIREMENTS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	FOSC	External CLKIN Frequency (Note 1)	DC	—	8	MHz	EC osc mode - 08 devices (8 MHz devices)
			DC	—	16	MHz	- 16 devices (16 MHz devices)
			DC	—	33	MHz	- 33 devices (33 MHz devices)
		Oscillator Frequency (Note 1)	DC	—	4	MHz	RC osc mode
			2	—	8	MHz	XT osc mode - 08 devices (8 MHz devices)
			2	—	16	MHz	- 16 devices (16 MHz devices)
			2	—	33	MHz	- 33 devices (33 MHz devices)
			DC	—	2	MHz	LF osc mode
1	TOSC	External CLKIN Period (Note 1)	125	—	—	ns	EC osc mode - 08 devices (8 MHz devices)
			62.5	—	—	ns	- 16 devices (16 MHz devices)
			30.3	—	—	ns	- 33 devices (33 MHz devices)
		Oscillator Period (Note 1)	250	—	—	ns	RC osc mode
			125	—	1,000	ns	XT osc mode - 08 devices (8 MHz devices)
			62.5	—	1,000	ns	- 16 devices (16 MHz devices)
			30.3	—	1,000	ns	- 33 devices (33 MHz devices)
			500	—	—	ns	LF osc mode
2	Tcy	Instruction Cycle Time (Note 1)	121.2	4/FOSC	DC	ns	
3	TosL, TosH	Clock in (OSC1) High or Low Time	10	—	—	ns	EC oscillator
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	—	—	5	ns	EC oscillator

† Data in "Typ" column is at 5V, 25°C unless otherwise stated.

Note 1: Instruction cycle period (Tcy) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKIN pin. When an external clock input is used, the "max." cycle time limit is "DC" (no clock) for all devices.

FIGURE 20-20: USART SYNCHRONOUS RECEIVE (MASTER/SLAVE) TIMING

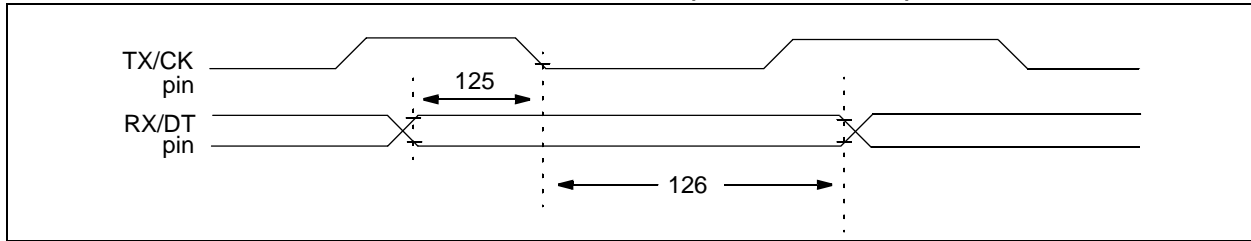


TABLE 20-15: USART SYNCHRONOUS RECEIVE REQUIREMENTS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
125	TdtV2ckL	<u>SYNC RCV (MASTER & SLAVE)</u> Data setup before CK↓ (DT setup time)	15	—	—	ns	
126	TckL2dtl	Data hold after CK↓ (DT hold time)	15	—	—	ns	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated.

TABLE 20-18: A/D CONVERTER CHARACTERISTICS

Param. No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
A01	NR	Resolution	—	—	10	bit	VREF+ = VDD = 5.12V, VSS ≤ VAIN ≤ VREF+
			—	—	10	bit	(VREF+ — VREF-) ≥ 3.0V, VREF- ≤ VAIN ≤ VREF+
A02	EABS	Absolute error	—	—	< ±1	LSb	VREF+ = VDD = 5.12V, VSS ≤ VAIN ≤ VREF+
			—	—	< ±1	LSb	(VREF+ — VREF-) ≥ 3.0V, VREF- ≤ VAIN ≤ VREF+
A03	EIL	Integral linearity error	—	—	< ±1	LSb	VREF+ = VDD = 5.12V, VSS ≤ VAIN ≤ VREF+
			—	—	< ±1	LSb	(VREF+ — VREF-) ≥ 3.0V, VREF- ≤ VAIN ≤ VREF+
A04	EDL	Differential linearity error	—	—	< ±1	LSb	VREF+ = VDD = 5.12V, VSS ≤ VAIN ≤ VREF+
			—	—	< ±1	LSb	(VREF+ — VREF-) ≥ 3.0V, VREF- ≤ VAIN ≤ VREF+
A05	EFS	Full scale error	—	—	< ±1	LSb	VREF+ = VDD = 5.12V, VSS ≤ VAIN ≤ VREF+
			—	—	< ±1	LSb	(VREF+ — VREF-) ≥ 3.0V, VREF- ≤ VAIN ≤ VREF+
A06	EOFF	Offset error	—	—	< ±1	LSb	VREF+ = VDD = 5.12V, VSS ≤ VAIN ≤ VREF+
			—	—	< ±1	LSb	(VREF+ — VREF-) ≥ 3.0V, VREF- ≤ VAIN ≤ VREF+
A10	—	Monotonicity	—	guaranteed ⁽³⁾	—	—	VSS ≤ VAIN ≤ VREF
A20	VREF	Reference voltage (VREF+ — VREF-)	0V	—	—	V	VREF delta when changing voltage levels on VREF inputs
A20A			3V	—	—	V	Absolute minimum electrical spec. to ensure 10-bit accuracy
A21	VREF+	Reference voltage high	AVSS + 3.0V	—	AVDD + 0.3V	V	
A22	VREF-	Reference voltage low	AVSS - 0.3V	—	AVDD - 3.0V	V	
A25	VAIN	Analog input voltage	AVSS - 0.3V	—	Vref + 0.3V	V	
A30	ZAIN	Recommended impedance of analog voltage source	—	—	10.0	kΩ	
A40	IAD	A/D conversion current (VDD)	—	180	—	μA	Average current consumption when A/D is on (Note 1)
			—	90	—	μA	
A50	IREF	VREF input current (Note 2)	10	—	1000	μA	During VAIN acquisition. Based on differential of VHOLD to VAIN
			—	—	10	μA	During A/D conversion cycle

† Data in "Typ" column is at 5V, 25°C unless otherwise stated.

Note 1: When A/D is off, it will not consume any current other than minor leakage current. The power-down current spec includes any such leakage from the A/D module.

2: VREF current is from RG0 and RG1 pins or AVDD and AVSS pins, whichever is selected as reference input.

3: The A/D conversion result never decreases with an increase in the Input Voltage and has no missing codes.

FIGURE 21-15: TYPICAL, MINIMUM AND MAXIMUM WDT PERIOD vs. V_{DD} (-40°C TO +125°C)

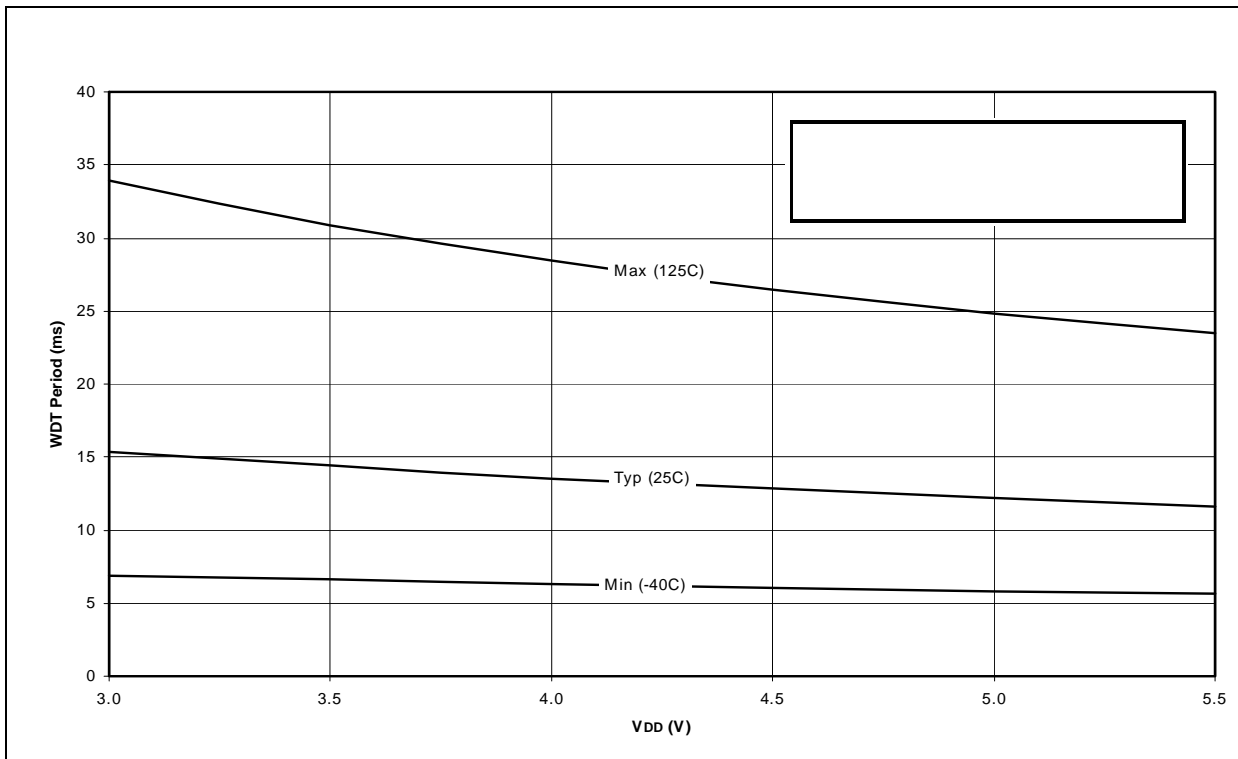
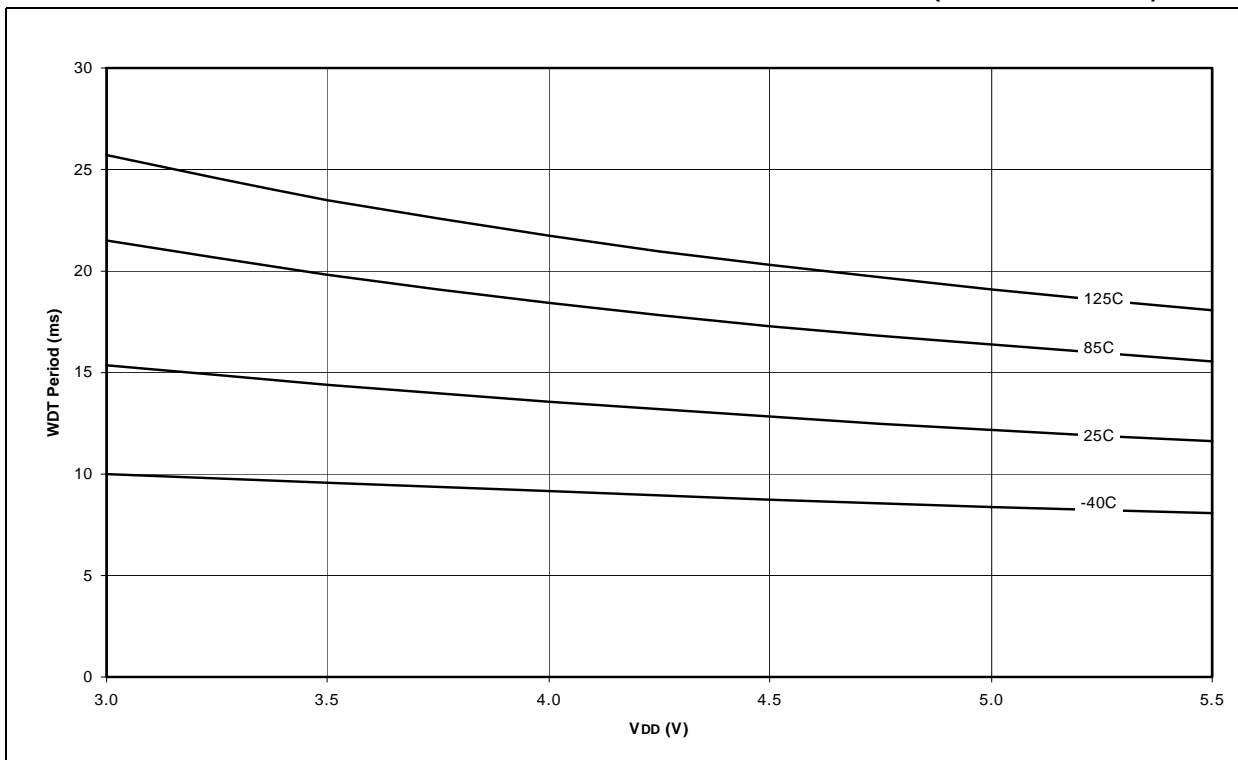


FIGURE 21-16: TYPICAL WDT PERIOD vs. V_{DD} OVER TEMPERATURE (-40°C TO +125°C)



PIC17C7XX

BTG.....	206	Capture4 Interrupt	38
CALL.....	207	Context Saving	39
CLRF.....	207	Flag bits	
CLRWDT.....	208	TMR1IE	33
COMF.....	208	TMR1IF.....	33
CPFSEQ.....	209	TMR2IE	33
CPFSGT.....	209	TMR2IF.....	33
CPFSLT.....	210	TMR3IE	33
DAW.....	210	TMR3IF.....	33
DECF.....	211	Global Interrupt Disable.....	39
DECFSNZ.....	212	Interrupts	33
DECFSZ.....	211	Logic	33
GOTO.....	212	Operation	39
INCF.....	213	Peripheral Interrupt Enable.....	35
INCFSNZ.....	214	Peripheral Interrupt Request.....	37
INCFSZ.....	213	PIE2 Register	36
IORLW.....	214	PIR1 Register	37
IORWF.....	215	PIR2 Register	38
LCALL.....	215	PORTB Interrupt on Change	37
MOVFP.....	216	PWM.....	108
MOVLB.....	216	RA0/INT	39
MOVLR.....	217	Status Register	34
MOVLW.....	217	Synchronous Serial Port Interrupt.....	38
MOVFP.....	218	T0CKI Interrupt	39
MOVWF.....	218	Timing.....	40
MULLW.....	219	TMR1 Overflow Interrupt	37
MULWF.....	219	TMR2 Overflow Interrupt	37
NEGW.....	220	TMR3 Overflow Interrupt	37
NOP.....	220	USART1 Receive Interrupt	37
RETFIE.....	221	USART1 Transmit Interrupt	37
RETLW.....	221	USART2 Receive Interrupt	38
RETURN.....	222	Vectors	
RLCF.....	222	Peripheral Interrupt.....	39
RLNCF.....	223	Program Memory Locations	43
RRCF.....	223	RA0/INT Interrupt	39
RRNCF.....	224	T0CKI Interrupt.....	39
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Capture1 Interrupt.....	37	MOVLB.....	46, 216
Capture2 Interrupt.....	37	MOVLR.....	217
Capture3 Interrupt.....	38	MOVLW.....	217