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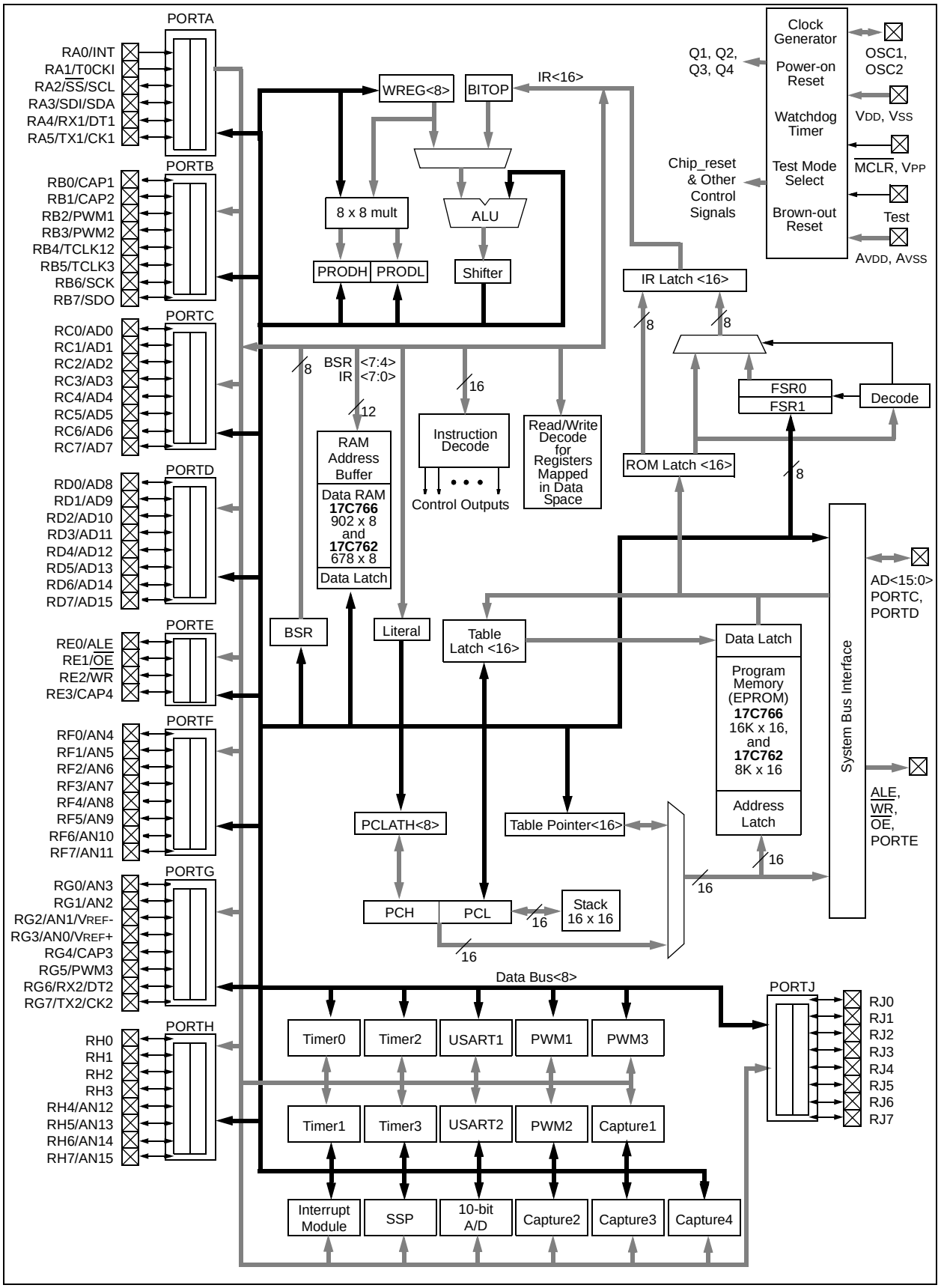
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	66
Program Memory Size	16KB (8K x 16)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	678 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic17c762t-16e-l

FIGURE 3-2: PIC17C762/766 BLOCK DIAGRAM



6.3 Peripheral Interrupt Request Register1 (PIR1) and Register2 (PIR2)

These registers contains the individual flag bits for the peripheral interrupts.

Note: These bits will be set by the specified condition, even if the corresponding interrupt enable bit is cleared (interrupt disabled), or the GLINTD bit is set (all interrupts disabled). Before enabling an interrupt, the user may wish to clear the interrupt flag to ensure that the program does not immediately branch to the peripheral Interrupt Service Routine.

REGISTER 6-4: PIR1 REGISTER (ADDRESS: 16h, BANK 1)

R/W-x	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-1	R-0
RBIF	TMR3IF	TMR2IF	TMR1IF	CA2IF	CA1IF	TX1IF	RC1IF
bit 7							bit 0

bit 7 **RBIF**: PORTB Interrupt-on-Change Flag bit
1 = One of the PORTB inputs changed (software must end the mismatch condition)
0 = None of the PORTB inputs have changed

bit 6 **TMR3IF**: TMR3 Interrupt Flag bit

If Capture1 is enabled (CA1/$\overline{PR3}$ = 1):
1 = TMR3 overflowed
0 = TMR3 did not overflow

If Capture1 is disabled (CA1/$\overline{PR3}$ = 0):
1 = TMR3 value has rolled over to 0000h from equalling the period register (PR3H:PR3L) value
0 = TMR3 value has not rolled over to 0000h from equalling the period register (PR3H:PR3L) value

bit 5 **TMR2IF**: TMR2 Interrupt Flag bit
1 = TMR2 value has rolled over to 0000h from equalling the period register (PR2) value
0 = TMR2 value has not rolled over to 0000h from equalling the period register (PR2) value

bit 4 **TMR1IF**: TMR1 Interrupt Flag bit

If TMR1 is in 8-bit mode (T16 = 0):
1 = TMR1 value has rolled over to 0000h from equalling the period register (PR1) value
0 = TMR1 value has not rolled over to 0000h from equalling the period register (PR1) value

If Timer1 is in 16-bit mode (T16 = 1):
1 = TMR2:TMR1 value has rolled over to 0000h from equalling the period register (PR2:PR1) value
0 = TMR2:TMR1 value has not rolled over to 0000h from equalling the period register (PR2:PR1) value

bit 3 **CA2IF**: Capture2 Interrupt Flag bit
1 = Capture event occurred on RB1/CAP2 pin
0 = Capture event did not occur on RB1/CAP2 pin

bit 2 **CA1IF**: Capture1 Interrupt Flag bit
1 = Capture event occurred on RB0/CAP1 pin
0 = Capture event did not occur on RB0/CAP1 pin

bit 1 **TX1IF**: USART1 Transmit Interrupt Flag bit (state controlled by hardware)
1 = USART1 Transmit buffer is empty
0 = USART1 Transmit buffer is full

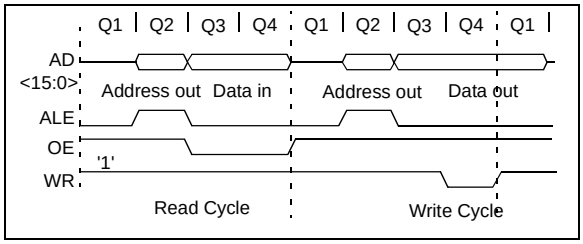
bit 0 **RC1IF**: USART1 Receive Interrupt Flag bit (state controlled by hardware)
1 = USART1 Receive buffer is full
0 = USART1 Receive buffer is empty

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR Reset	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

7.1.2 EXTERNAL MEMORY INTERFACE

When either Microprocessor or Extended Microcontroller mode is selected, PORTC, PORTD and PORTE are configured as the system bus. PORTC and PORTD are the multiplexed address/data bus and PORTE<2:0> is for the control signals. External components are needed to demultiplex the address and data. This can be done as shown in Figure 7-4. The waveforms of address and data are shown in Figure 7-3. For complete timings, please refer to the electrical specification section.

FIGURE 7-3: EXTERNAL PROGRAM MEMORY ACCESS WAVEFORMS



The system bus requires that there is no bus conflict (minimal leakage), so the output value (address) will be capacitively held at the desired value.

As the speed of the processor increases, external EPROM memory with faster access time must be used. Table 7-2 lists external memory speed requirements for a given PIC17C7XX device frequency.

In Extended Microcontroller mode, when the device is executing out of internal memory, the control signals will continue to be active. That is, they indicate the action that is occurring in the internal memory. The external memory access is ignored.

The following selection is for use with Microchip EPROMs. For interfacing to other manufacturers memory, please refer to the electrical specifications of the desired PIC17C7XX device, as well as the desired memory device to ensure compatibility.

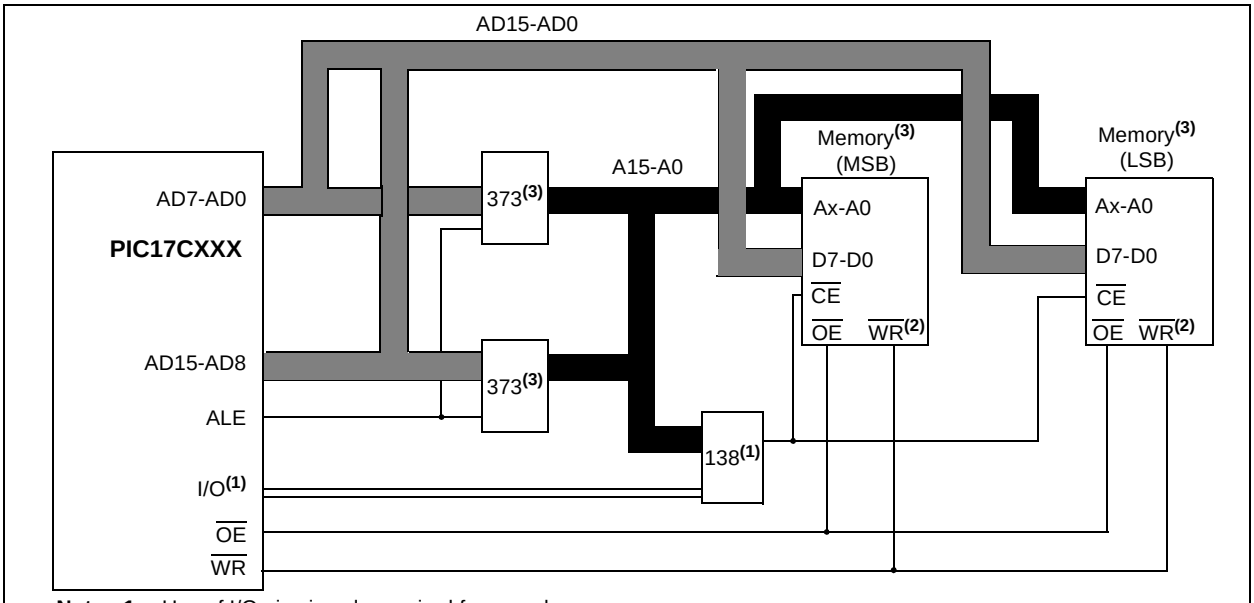
TABLE 7-2: EPROM MEMORY ACCESS TIME ORDERING SUFFIX

PIC17C7XX Oscillator Frequency	Instruction Cycle Time (TCY)	EPROM Suffix
8 MHz	500 ns	-25
16 MHz	250 ns	-15
20 MHz	200 ns	-10
25 MHz	160 ns	-70

Note: The access times for this requires the use of fast SRAMs.

The electrical specifications now include timing specifications for the memory interface with PIC17**LC**XXX devices. These specifications reflect the capability of the device by characterization. Please validate your design with these timings.

FIGURE 7-4: TYPICAL EXTERNAL PROGRAM MEMORY CONNECTION DIAGRAM



Note 1: Use of I/O pins is only required for paged memory.
2: This signal is unused for ROM and EPROM devices.
3: 16-bit wide devices are now common and could be used instead of 8-bit wide devices.

TABLE 7-3: SPECIAL FUNCTION REGISTERS (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	$\overline{\text{MCLR}}$, WDT
Bank 2											
10h	TMR1	Timer1's Register								xxxx xxxx	uuuu uuuu
11h	TMR2	Timer2's Register								xxxx xxxx	uuuu uuuu
12h	TMR3L	Timer3's Register; Low Byte								xxxx xxxx	uuuu uuuu
13h	TMR3H	Timer3's Register; High Byte								xxxx xxxx	uuuu uuuu
14h	PR1	Timer1's Period Register								xxxx xxxx	uuuu uuuu
15h	PR2	Timer2's Period Register								xxxx xxxx	uuuu uuuu
16h	PR3L/CA1L	Timer3's Period Register - Low Byte/Capture1 Register; Low Byte								xxxx xxxx	uuuu uuuu
17h	PR3H/CA1H	Timer3's Period Register - High Byte/Capture1 Register; High Byte								xxxx xxxx	uuuu uuuu
Bank 3											
10h	PW1DCL	DC1	DC0	—	—	—	—	—	—	xx-- ----	uu-- ----
11h	PW2DCL	DC1	DC0	TM2PW2	—	—	—	—	—	xx0- ----	uu0- ----
12h	PW1DCH	DC9	DC8	DC7	DC6	DC5	DC4	DC3	DC2	xxxx xxxx	uuuu uuuu
13h	PW2DCH	DC9	DC8	DC7	DC6	DC5	DC4	DC3	DC2	xxxx xxxx	uuuu uuuu
14h	CA2L	Capture2 Low Byte								xxxx xxxx	uuuu uuuu
15h	CA2H	Capture2 High Byte								xxxx xxxx	uuuu uuuu
16h	TCON1	CA2ED1	CA2ED0	CA1ED1	CA1ED0	T16	TMR3CS	TMR2CS	TMR1CS	0000 0000	0000 0000
17h	TCON2	CA2OVF	CA1OVF	PWM2ON	PWM1ON	CA1/$\overline{\text{PR3}}$	TMR3ON	TMR2ON	TMR1ON	0000 0000	0000 0000
Bank 4											
10h	PIR2	SSPIF	BCLIF	ADIF	—	CA4IF	CA3IF	TX2IF	RC2IF	000- 0010	000- 0010
11h	PIE2	SSPIE	BCLIE	ADIE	—	CA4IE	CA3IE	TX2IE	RC2IE	000- 0000	000- 0000
12h	Unimplemented	—	—	—	—	—	—	—	—	---- ----	---- ----
13h	RCSTA2	SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D	0000 -00x	0000 -00u
14h	RCREG2	Serial Port Receive Register for USART2								xxxx xxxx	uuuu uuuu
15h	TXSTA2	CSRC	TX9	TXEN	SYNC	—	—	TRMT	TX9D	0000 --1x	0000 --1u
16h	TXREG2	Serial Port Transmit Register for USART2								xxxx xxxx	uuuu uuuu
17h	SPBRG2	Baud Rate Generator for USART2								0000 0000	0000 0000
Bank 5:											
10h	DDRF	Data Direction Register for PORTF								1111 1111	1111 1111
11h	PORTF(4)	RF7/ AN11	RF6/ AN10	RF5/ AN9	RF4/ AN8	RF3/ AN7	RF2/ AN6	RF1/ AN5	RF0/ AN4	0000 0000	0000 0000
12h	DDRG	Data Direction Register for PORTG								1111 1111	1111 1111
13h	PORTG(4)	RG7/ TX2/CK2	RG6/ RX2/DT2	RG5/ PWM3	RG4/ CAP3	RG3/ AN0	RG2/ AN1	RG1/ AN2	RG0/ AN3	xxxx 0000	uuuu 0000
14h	ADCON0	CHS3	CHS2	CHS1	CHS0	—	GO/$\overline{\text{DONE}}$	—	ADON	0000 -0-0	0000 -0-0
15h	ADCON1	ADCS1	ADCS0	ADFM	—	PCFG3	PCFG2	PCFG1	PCFG0	000- 0000	000- 0000
16h	ADRESL	A/D Result Register Low Byte								xxxx xxxx	uuuu uuuu
17h	ADRESH	A/D Result Register High Byte								xxxx xxxx	uuuu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0', q = value depends on condition.
Shaded cells are unimplemented, read as '0'.

Note 1: The upper byte of the program counter is not directly accessible. PCLATH is a holding register for PC<15:8> whose contents are updated from, or transferred to, the upper byte of the program counter.

2: The $\overline{\text{TO}}$ and $\overline{\text{PD}}$ status bits in CPUSTA are not affected by a $\overline{\text{MCLR}}$ Reset.

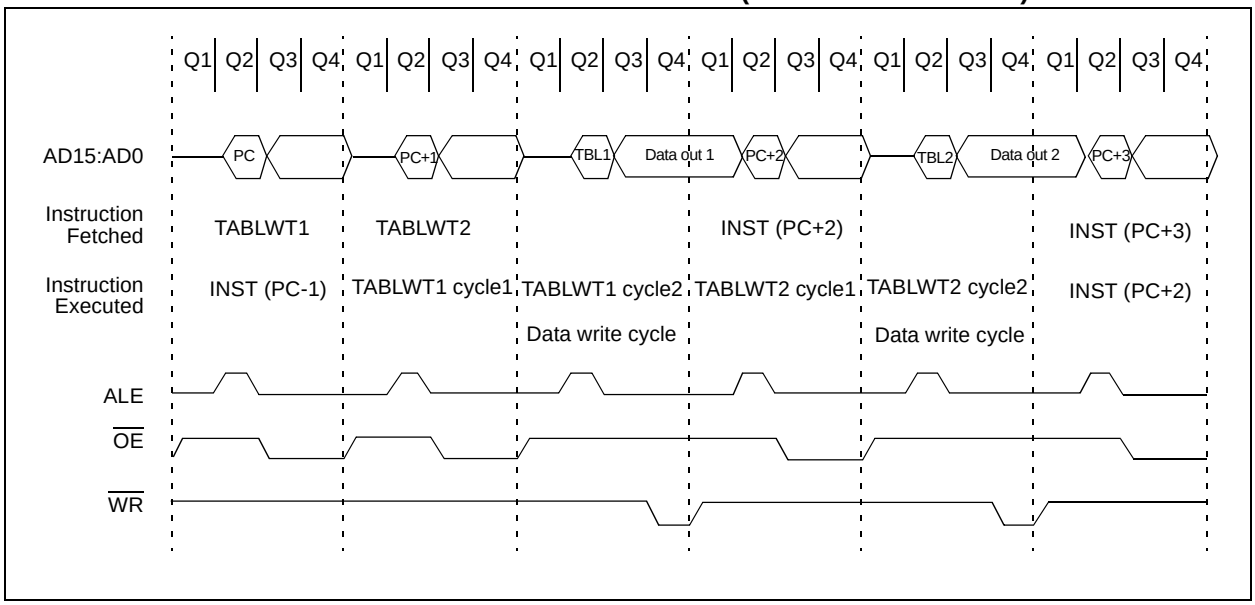
3: Bank 8 and associated registers are only implemented on the PIC17C76X devices.

4: This is the value that will be in the port output latch.

5: When the device is configured for Microprocessor or Extended Microcontroller mode, the operation of this port does not rely on these registers.

6: On any device RESET, these pins are configured as inputs.

FIGURE 8-6: CONSECUTIVE `TABLWT` WRITE TIMING (EXTERNAL MEMORY)



8.3 Table Reads

The table read allows the program memory to be read. This allows constants to be stored in the program memory space and retrieved into data memory when needed. Example 8-2 reads the 16-bit value at program memory address TBLPTR. After the dummy byte has been read from the TABLATH, the TABLATH is loaded with the 16-bit data from program memory address TBLPTR and then increments the TBLPTR value. The first read loads the data into the latch and can be considered a dummy read (unknown data loaded into 'f'). INDF0 should be configured for either auto-increment or auto-decrement.

EXAMPLE 8-2: TABLE READ

```
MOVLW   HIGH (TBL_ADDR) ; Load the Table
MOVWF   TBLPTRH         ;   address
MOVLW   LOW (TBL_ADDR)  ;
MOVWF   TBLPTRL         ;
TABLRD  0, 1, DUMMY   ; Dummy read,
                      ;  Updates TABLATH
                      ;  Increments TBLPTR
TLRD    1, INDF0      ; Read HI byte
                      ;   of TABLATH
TABLRD  0, 1, INDF0   ; Read LO byte
                      ;   of TABLATL and
                      ;   Update TABLATH
                      ;   Increment TBLPTR
```

FIGURE 8-7: `TABLRD` TIMING

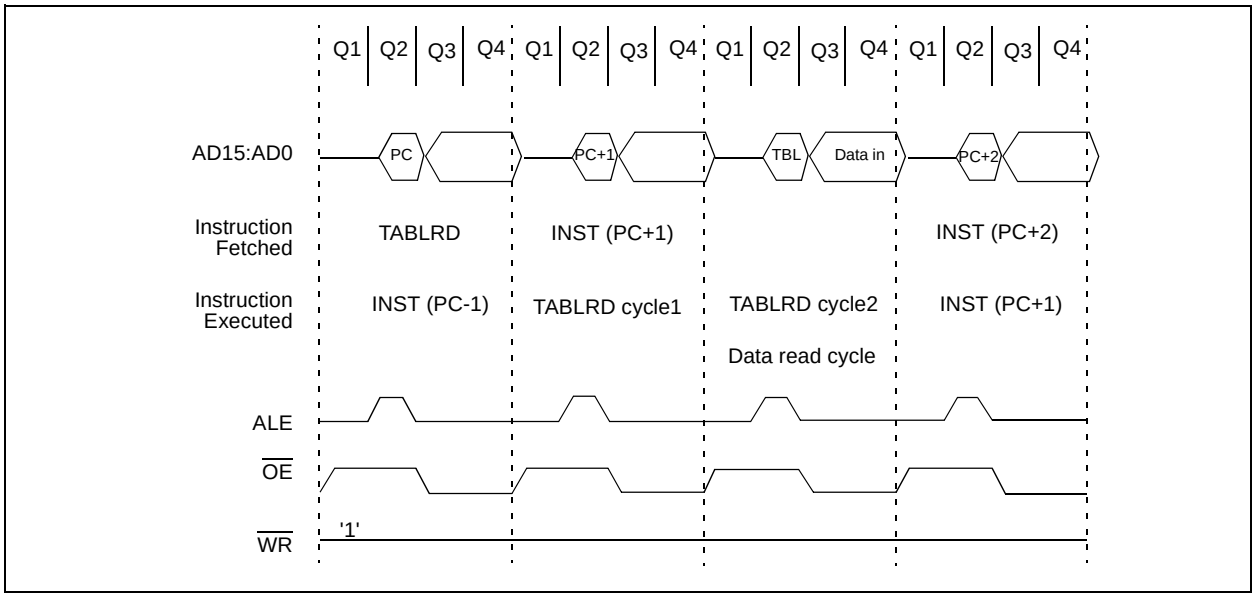
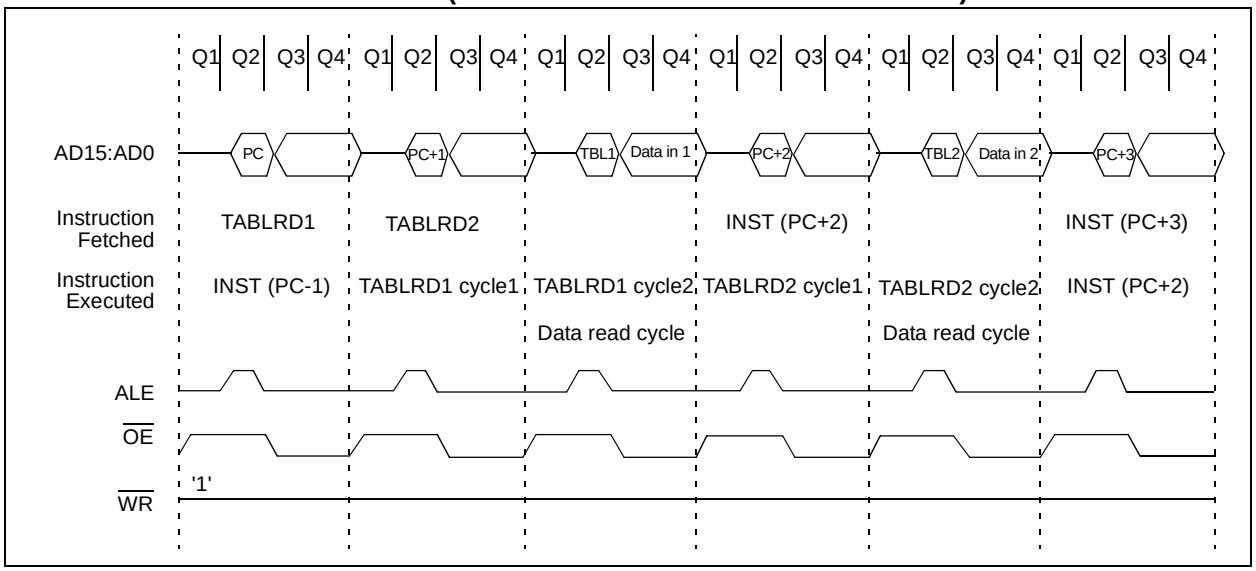
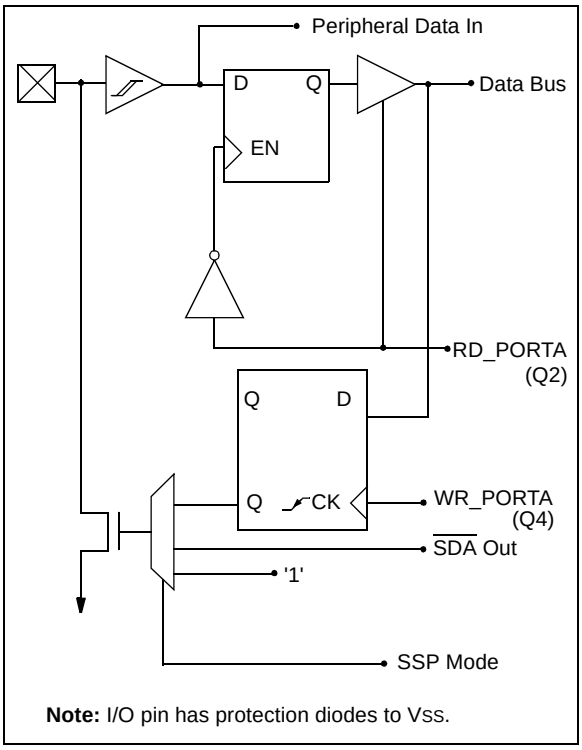


FIGURE 8-8: `TABLRD` TIMING (CONSECUTIVE `TABLRD` INSTRUCTIONS)



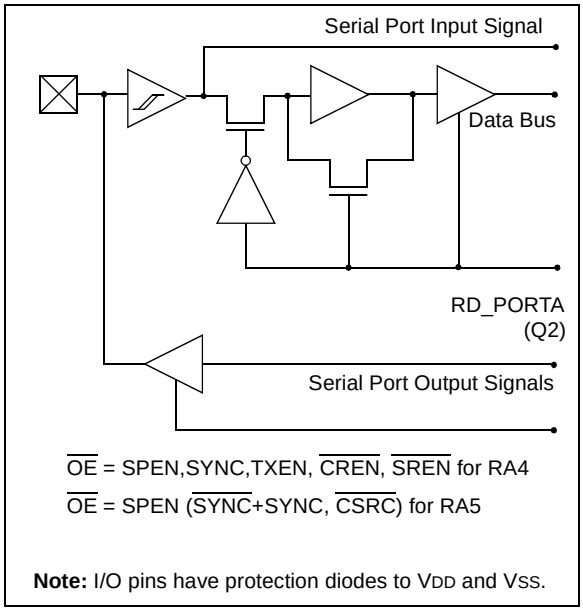
NOTES:

FIGURE 10-3: RA3 BLOCK DIAGRAM



Note: I/O pin has protection diodes to VSS.

FIGURE 10-4: RA4 AND RA5 BLOCK DIAGRAM



Note: I/O pins have protection diodes to VDD and VSS.

TABLE 10-1: PORTA FUNCTIONS

Name	Bit0	Buffer Type	Function
RA0/INT	bit0	ST	Input or external interrupt input.
RA1/T0CKI	bit1	ST	Input or clock input to the TMR0 timer/counter and/or an external interrupt input.
RA2/SS/SCL	bit2	ST	Input/output or slave select input for the SPI, or clock input for the I^2C bus. Output is open drain type.
RA3/SDI/SDA	bit3	ST	Input/output or data input for the SPI, or data for the I^2C bus. Output is open drain type.
RA4/RX1/DT1	bit4	ST	Input or USART1 Asynchronous Receive input, or USART1 Synchronous Data input/output.
RA5/TX1/CK1	bit5	ST	Input or USART1 Asynchronous Transmit output, or USART1 Synchronous Clock input/output.
RBPU	bit7	—	Control bit for PORTB weak pull-ups.

Legend: ST = Schmitt Trigger input

TABLE 10-2: REGISTERS/BITS ASSOCIATED WITH PORTA

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	MCLR, WDT
10h, Bank 0	PORTA(1)	RBPU	—	RA5/ TX1/CK1	RA4/ RX1/DT1	RA3/ SDI/SDA	RA2/ SS/SCL	RA1/T0CKI	RA0/INT	0-xx 11xx	0-uu 11uu
05h, Unbanked	T0STA	INTEDG	T0SE	T0CS	T0PS3	T0PS2	T0PS1	T0PS0	—	0000 000-	0000 000-
13h, Bank 0	RCSTA1	SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D	0000 -00x	0000 -00u
15h, Bank 0	TXSTA1	CSRC	TX9	TXEN	SYNC	—	—	TRMT	TX9D	0000 --1x	0000 --1u

Legend: x = unknown, u = unchanged, - = unimplemented, reads as '0'. Shaded cells are not used by PORTA.
Note 1: On any device RESET, these pins are configured as inputs.

10.7 PORTG and DDRG Registers

PORTG is an 8-bit wide, bi-directional port. The corresponding data direction register is DDRG. A '1' in DDRG configures the corresponding port pin as an input. A '0' in the DDRG register configures the corresponding port pin as an output. Reading PORTG reads the status of the pins, whereas writing to PORTG will write to the port latch.

The lower four bits of PORTG are multiplexed with four channels of the 10-bit A/D converter.

The remaining bits of PORTG are multiplexed with peripheral output and inputs. RG4 is multiplexed with the CAP3 input, RG5 is multiplexed with the PWM3 output, RG6 and RG7 are multiplexed with the USART2 functions.

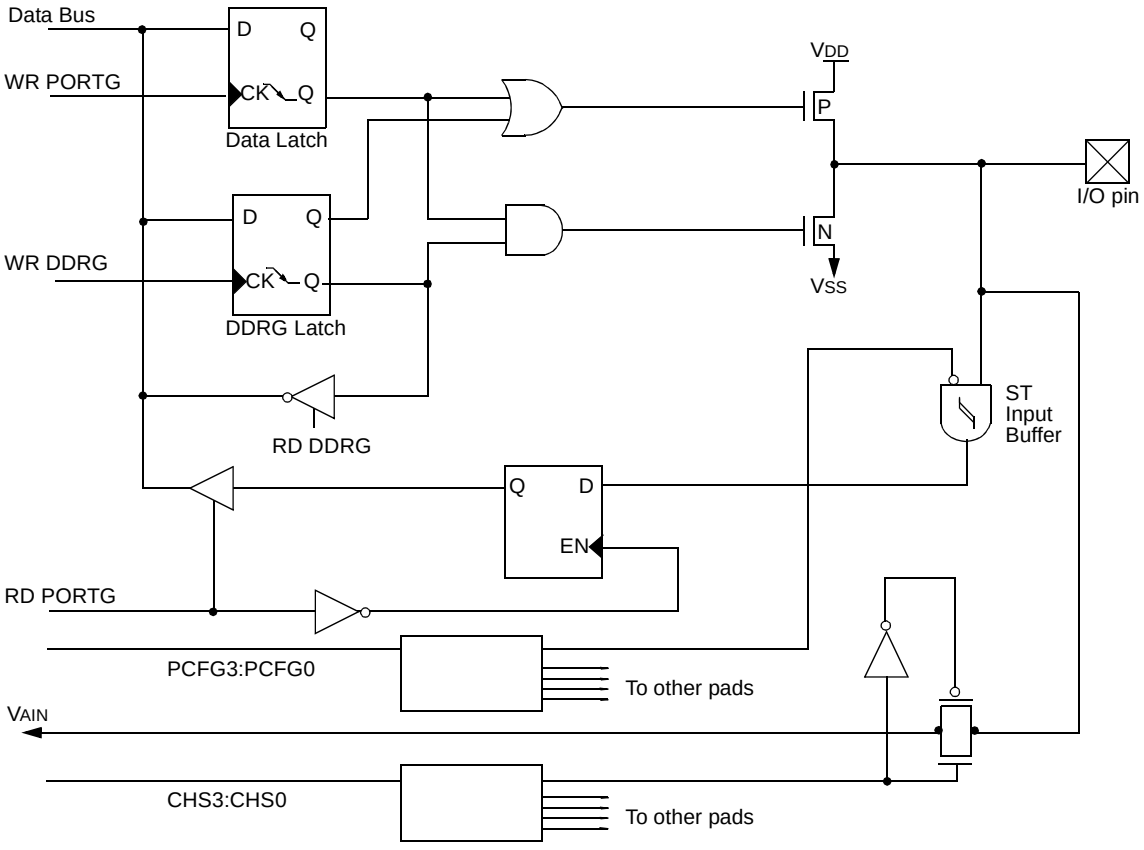
Upon RESET, RG3:RG0 is automatically configured as analog inputs and must be configured in software to be a digital I/O.

Example 10-7 shows the instruction sequence to initialize PORTG. The Bank Select Register (BSR) must be selected to Bank 5 for the port to be initialized. The following example uses the `MOVLB` instruction to load the BSR register for bank selection.

EXAMPLE 10-7: INITIALIZING PORTG

```
MOVLB  5              ; Select Bank 5
MOVLW  0x0E           ; Configure PORTG as
MOVPF  WREG, ADCON1   ; digital
CLRF   PORTG, F      ; Initialize PORTG data
                      ;   latches before
                      ;   the data direction
                      ;   register
MOVLW   0x03          ; Value used to init
                      ;   data direction
MOVWF   DDRG         ; Set RG<1:0> as inputs
                      ;   RG<7:2> as outputs
```

FIGURE 10-14: BLOCK DIAGRAM OF RG3:RG0



Note: I/O pins have protection diodes to V_{DD} and V_{SS}.

10.8 PORTH and DDRH Registers (PIC17C76X only)

PORTH is an 8-bit wide, bi-directional port. The corresponding data direction register is DDRH. A '1' in DDRH configures the corresponding port pin as an input. A '0' in the DDRH register configures the corresponding port pin as an output. Reading PORTH reads the status of the pins, whereas writing to PORTH will write to the respective port latch.

The upper four bits of PORTH are multiplexed with 4 channels of the 10-bit A/D converter.

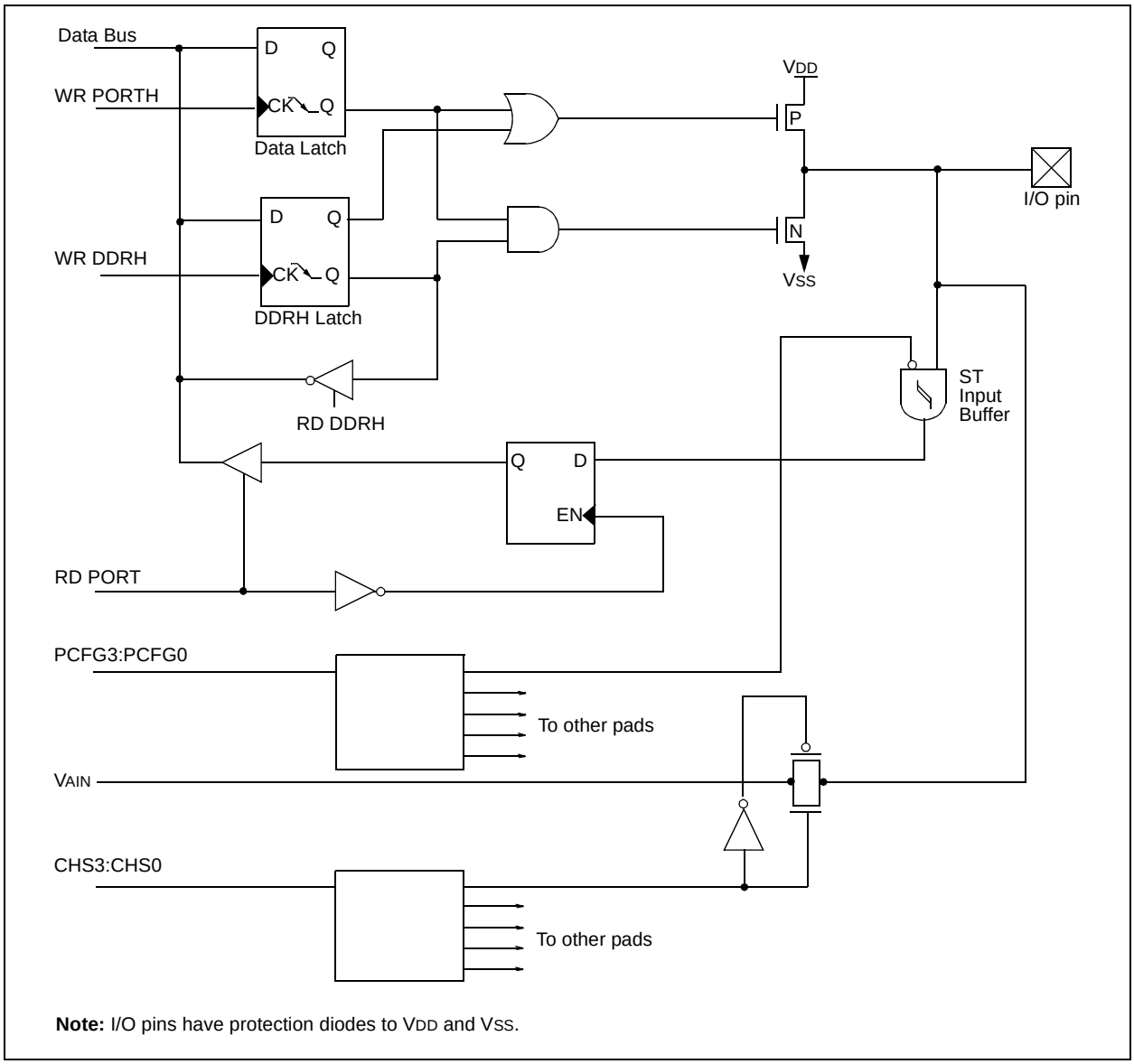
The remaining bits of PORTH are general purpose I/O.

Upon RESET, RH7:RH4 are automatically configured as analog inputs and must be configured in software to be a digital I/O.

EXAMPLE 10-8: INITIALIZING PORTH

```
MOVLB   8           ; Select Bank 8
MOVLW   0x0E        ; Configure PORTH as
MOVPF   ADCON1      ; digital
CLRF    PORTH, F    ; Initialize PORTH data
                    ;   latches before
                    ;   the data direction
                    ;   register
MOVLW    0x03       ; Value used to init
                    ;   data direction
MOVWF    DDRH       ; Set RH<1:0> as inputs
                    ;   RH<7:2> as outputs
```

FIGURE 10-17: BLOCK DIAGRAM OF RH7:RH4



Note: I/O pins have protection diodes to VDD and VSS.

15.1.5 SLAVE MODE

In Slave mode, the data is transmitted and received as the external clock pulses appear on SCK. When the last bit is latched, the interrupt flag bit SSPIF (PIR2<7>) is set.

While in Slave mode, the external clock is supplied by the external clock source on the SCK pin. This external clock must meet the minimum high and low times as specified in the electrical specifications.

While in SLEEP mode, the slave can transmit/receive data. When a byte is received, the device will wake-up from SLEEP.

15.1.6 SLAVE SELECT SYNCHRONIZATION

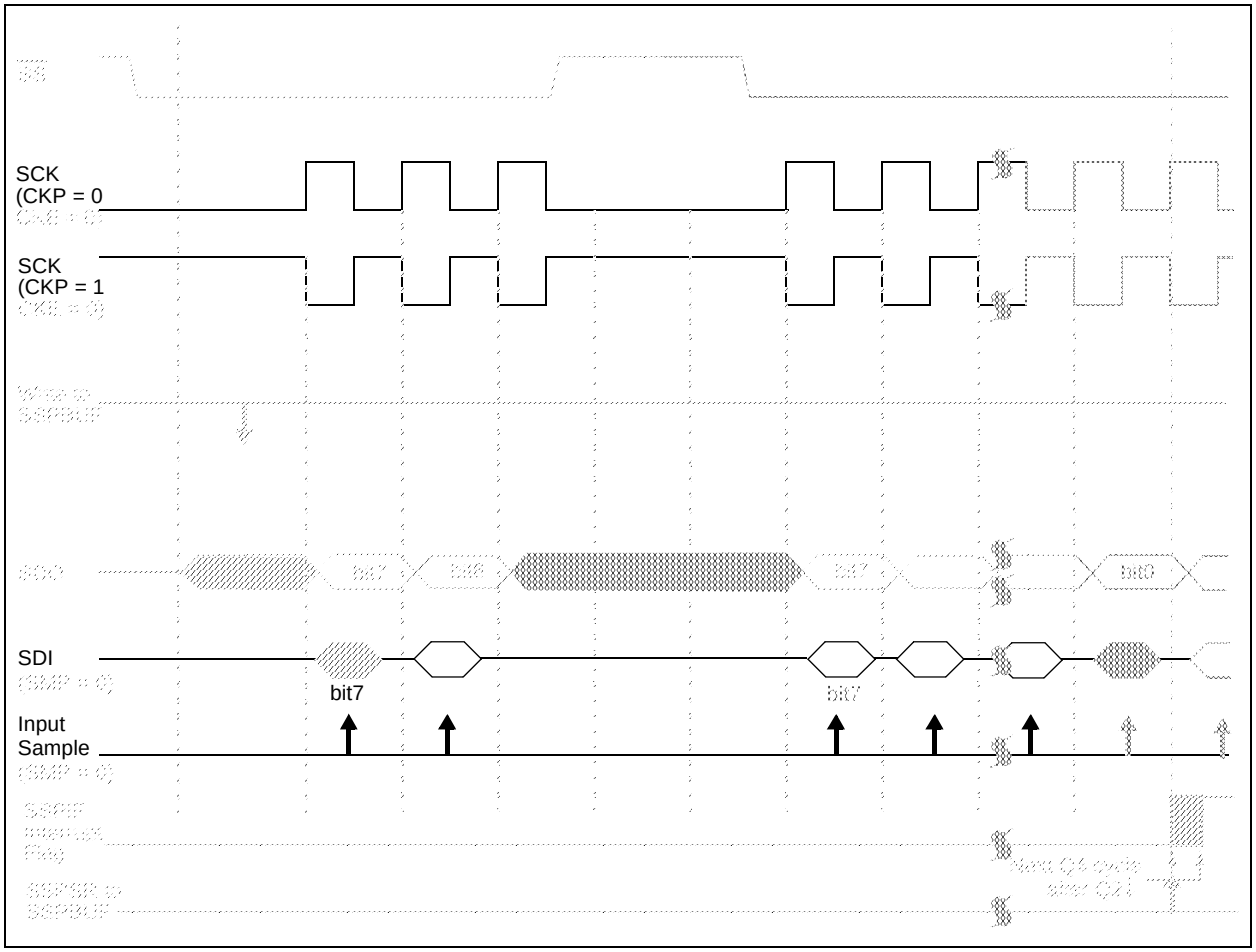
The $\overline{SS}$ pin allows a Synchronous Slave mode. The SPI must be in Slave mode with $\overline{SS}$ pin control enabled (SSPCON1<3:0> = 04h). The pin must not be driven low for the $\overline{SS}$ pin to function as an input. The RA2 Data Latch must be high. When the $\overline{SS}$ pin is low, transmission and reception are enabled and the SDO pin is driven. When the $\overline{SS}$ pin goes high, the SDO pin is no longer driven, even if in the middle of a transmitted byte and becomes a floating output. External pull-up/pull-down resistors may be desirable, depending on the application.

Note 1:	When the SPI is in Slave mode with $\overline{SS}$ pin control enabled (SSPCON<3:0> = 0100), the SPI module will reset if the $\overline{SS}$ pin is set to V_{DD}.
2:	If the SPI is used in Slave mode with CKE = '1', then the $\overline{SS}$ pin control must be enabled.

When the SPI module resets, the bit counter is forced to 0. This can be done by either forcing the $\overline{SS}$ pin to a high level, or clearing the SSPEN bit.

To emulate two-wire communication, the SDO pin can be connected to the SDI pin. When the SPI needs to operate as a receiver, the SDO pin can be configured as an input. This disables transmissions from the SDO. The SDI can always be left as an input (SDI function), since it cannot create a bus conflict.

FIGURE 15-7: SLAVE SYNCHRONIZATION WAVEFORM



15.2.9 I²C MASTER MODE START CONDITION TIMING

To initiate a START condition, the user sets the START condition enable bit, SEN (SSPCON2<0>). If the SDA and SCL pins are sampled high, the baud rate generator is reloaded with the contents of SSPADD<6:0> and starts its count. If SCL and SDA are both sampled high when the baud rate generator times out (TBRG), the SDA pin is driven low. The action of the SDA being driven low while SCL is high is the START condition and causes the S bit (SSPSTAT<3>) to be set. Following this, the baud rate generator is reloaded with the contents of SSPADD<6:0> and resumes its count. When the baud rate generator times out (TBRG), the SEN bit (SSPCON2<0>) will be automatically cleared by hardware, the baud rate generator is suspended, leaving the SDA line held low and the START condition is complete.

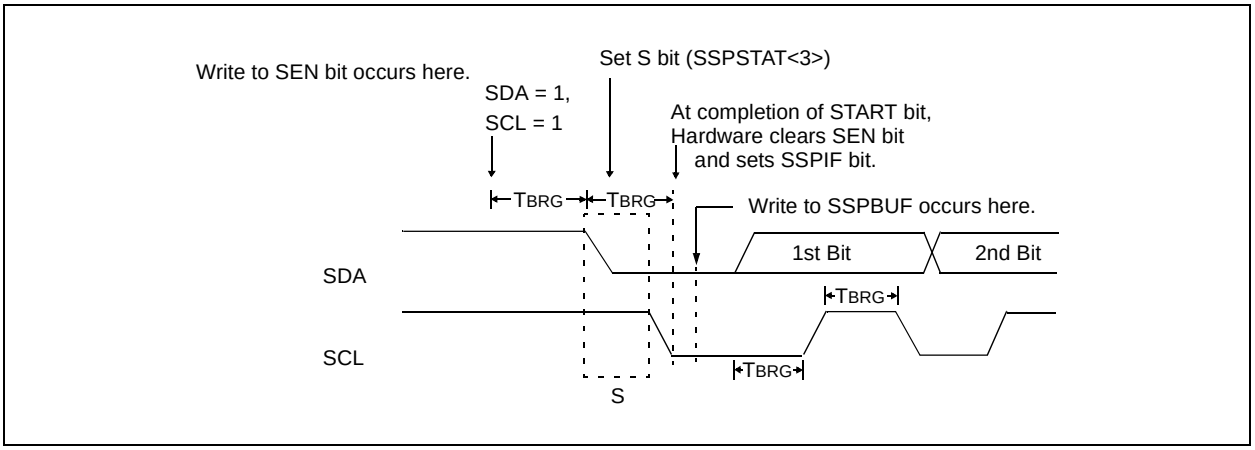
Note:	If at the beginning of START condition, the SDA and SCL pins are already sampled low, or if during the START condition, the SCL line is sampled low before the SDA line is driven low, a bus collision occurs. The Bus Collision Interrupt Flag (BCLIF) is set, the START condition is aborted and the I²C module is reset into its IDLE state.

15.2.9.1 WCOL Status Flag

If the user writes the SSPBUF when a START sequence is in progress, then WCOL is set and the contents of the buffer are unchanged (the write doesn't occur).

Note:	Because queueing of events is not allowed, writing to the lower 5 bits of SSPCON2 is disabled until the START condition is complete.

FIGURE 15-20: FIRST START BIT TIMING



EXAMPLE 15-2: INTERFACING TO A 24LC01B SERIAL EEPROM (USING MPLAB C17)

```
void ACKPoll(void)
{
        StartI2C();                     // Send start bit
        IdleI2C();                      // Wait for idle condition
        WriteI2C(CONTROL);              // Send control byte
        IdleI2C();                      // Wait for idle condition
        // Poll the ACK bit coming from the 24LC01B
        // Loop as long as the 24LC01B NACKs
        while (SSPCON2bits.ACKSTAT)
        {
                RestartI2C();           // Send a restart bit
                IdleI2C();              // Wait for idle condition
                WriteI2C(CONTROL);      // Send control byte
                IdleI2C();              // Wait for idle condition
        }
        IdleI2C();                      // Wait for idle condition
        StopI2C();                      // Send stop bit
        IdleI2C();                      // Wait for idle condition
        return;
}
```

16.7 A/D Accuracy/Error

In systems where the device frequency is low, use of the A/D RC clock is preferred. At moderate to high frequencies, TAD should be derived from the device oscillator.

The absolute accuracy specified for the A/D converter includes the sum of all contributions for quantization error, integral error, differential error, full scale error, offset error, and monotonicity. It is defined as the maximum deviation from an actual transition versus an ideal transition for any code. The absolute error of the A/D converter is specified at < ±1 LSb for VDD = VREF (over the device's specified operating range). However, the accuracy of the A/D converter will degrade as VREF diverges from VDD.

For a given range of analog inputs, the output digital code will be the same. This is due to the quantization of the analog input to a digital code. Quantization error is typically ± 1/2 LSb and is inherent in the analog to digital conversion process. The only way to reduce quantization error is to increase the resolution of the A/D converter or oversample.

Offset error measures the first actual transition of a code versus the first ideal transition of a code. Offset error shifts the entire transfer function. Offset error can be calibrated out of a system or introduced into a system through the interaction of the total leakage current and source impedance at the analog input.

Gain error measures the maximum deviation of the last actual transition and the last ideal transition adjusted for offset error. This error appears as a change in slope of the transfer function. The difference in gain error to full scale error is that full scale does not take offset error into account. Gain error can be calibrated out in software.

Linearity error refers to the uniformity of the code changes. Linearity errors cannot be calibrated out of the system. Integral non-linearity error measures the actual code transition versus the ideal code transition, adjusted by the gain error for each code.

Differential non-linearity measures the maximum actual code width versus the ideal code width. This measure is unadjusted.

The maximum pin leakage current is specified in the Device Data Sheet electrical specification (Table 20-2, parameter #D060).

In systems where the device frequency is low, use of the A/D RC clock is preferred. At moderate to high frequencies, TAD should be derived from the device oscillator. TAD must not violate the minimum and should be minimized to reduce inaccuracies due to noise and sampling capacitor bleed off.

In systems where the device will enter SLEEP mode after the start of the A/D conversion, the RC clock source selection is required. In this mode, the digital noise from the modules in SLEEP are stopped. This method gives high accuracy.

16.8 Connection Considerations

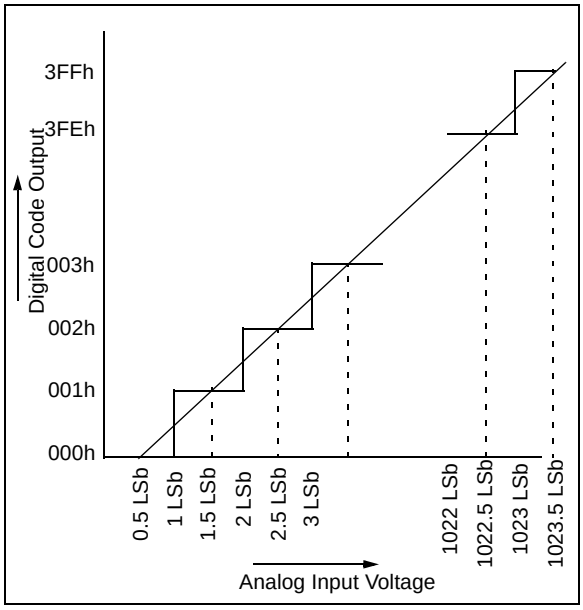
If the input voltage exceeds the rail values (VSS or VDD) by greater than 0.3V, then the accuracy of the conversion is out of specification.

An external RC filter is sometimes added for anti-aliasing of the input signal. The R component should be selected to ensure that the total source impedance is kept under the 10 kΩ recommended specification. Any external components connected (via hi-impedance) to an analog input pin (capacitor, zener diode, etc.) should have very little leakage current at the pin.

16.9 Transfer Function

The transfer function of the A/D converter is as follows: the first transition occurs when the analog input voltage (VAIN) equals Analog VREF / 1024 (Figure 16-7).

FIGURE 16-7: A/D TRANSFER FUNCTION



18.2 Q Cycle Activity

Each instruction cycle (TCY) is comprised of four Q cycles (Q1-Q4). The Q cycle is the same as the device oscillator cycle (TOSC). The Q cycles provide the timing/ designation for the Decode, Read, Process Data, Write, etc., of each instruction cycle. The following diagram shows the relationship of the Q cycles to the instruction cycle.

The four Q cycles that make up an instruction cycle (TCY) can be generalized as:

Q1: Instruction Decode Cycle or forced No operation

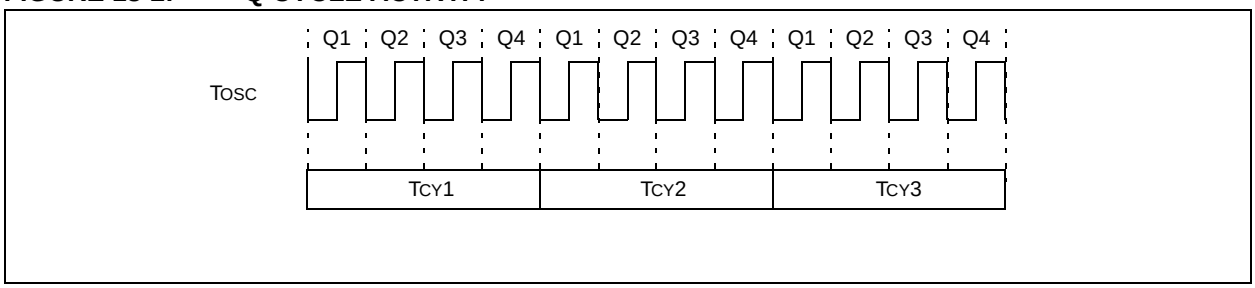
Q2: Instruction Read Cycle or No operation

Q3: Process the Data

Q4: Instruction Write Cycle or No operation

Each instruction will show the detailed Q cycle operation for the instruction.

FIGURE 18-2: Q CYCLE ACTIVITY



DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +125°C for extended -40°C ≤ TA ≤ +85°C for industrial 0°C ≤ TA ≤ +70°C for commercial Operating voltage VDD range as described in Section 20.1				
Param. No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
D150	VOD	**Open Drain High Voltage**	–	–	8.5	V	RA2 and RA3 pins only pulled up to externally applied voltage
		Capacitive Loading Specs on Output Pins					
D100	COSC2	OSC2/CLKOUT pin	–	–	25	pF	In EC or RC osc modes, when OSC2 pin is outputting CLKOUT. External clock is used to drive OSC1.
D101	CIO	All I/O pins and OSC2 (in RC mode)	–	–	50	pF	
D102	CAD	System Interface Bus (PORTC, PORTD and PORTE)	–	–	50	pF	In Microprocessor or Extended Microcontroller mode
		Internal Program Memory Programming Specs (Note 4)					
D110	VPP	Voltage on MCLR/VPP pin	12.75	–	13.25	V	**(Note 5)**
D111	VDDP	Supply voltage during programming	4.75	5.0	5.25	V	
D112	IPP	Current into MCLR/VPP pin	–	25	50	mA	
D113	IDDP	Supply current during programming	–	–	30	mA	
D114	TPROG	Programming pulse width	100	–	1000	ms	Terminated via internal/ external interrupt or a RESET

† Data in "Typ" column is at 5V, 25°C unless otherwise stated.

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC17CXXX devices be driven with external clock in RC mode.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

4: These specifications are for the programming of the on-chip program memory EPROM through the use of the table write instructions. The complete programming specifications can be found in: PIC17C7XX Programming Specifications (Literature number DS TBD).

5: The MCLR/VPP pin may be kept in this range at times other than programming, but is not recommended.

6: For TTL buffers, the better of the two specifications may be used.

Note 1: When using the Table Write for internal programming, the device temperature must be less than 40°C.

2: For In-Circuit Serial Programming (ICSP™), refer to the device programming specification.

FIGURE 21-7: TYPICAL IDD vs. FOSC OVER VDD (LF MODE)

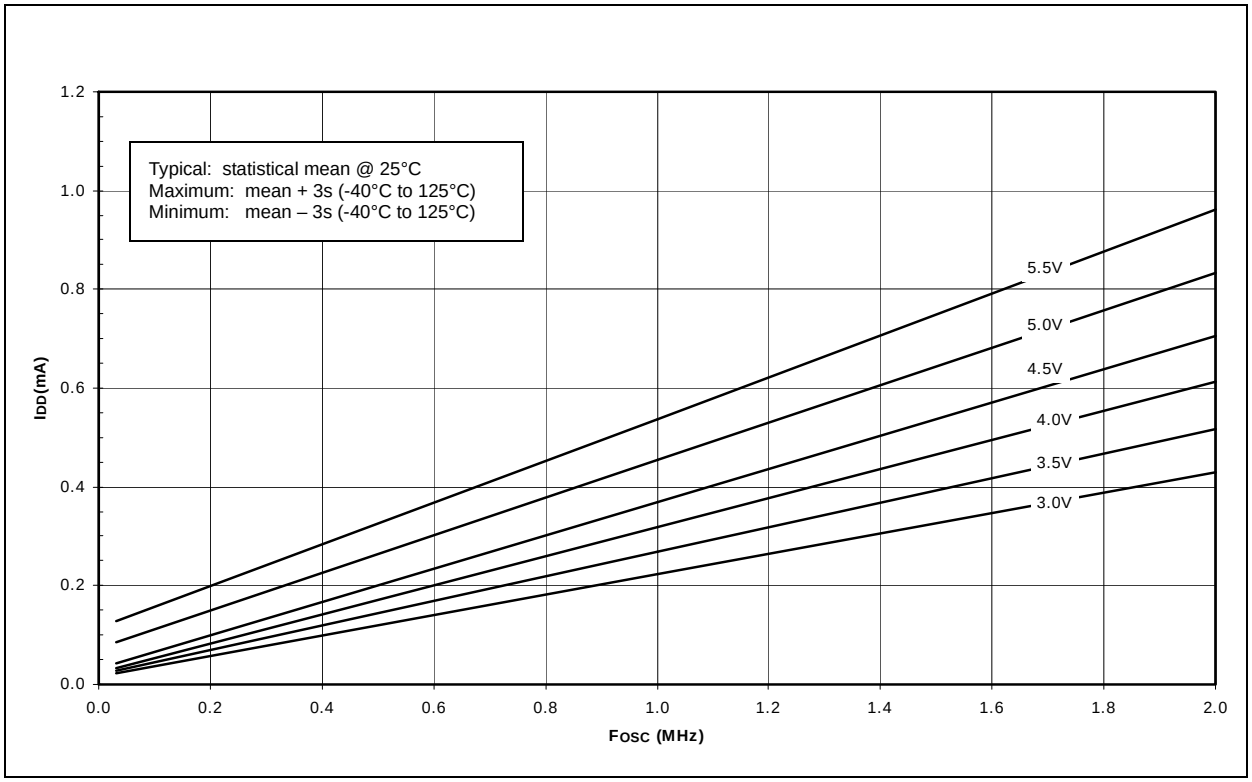
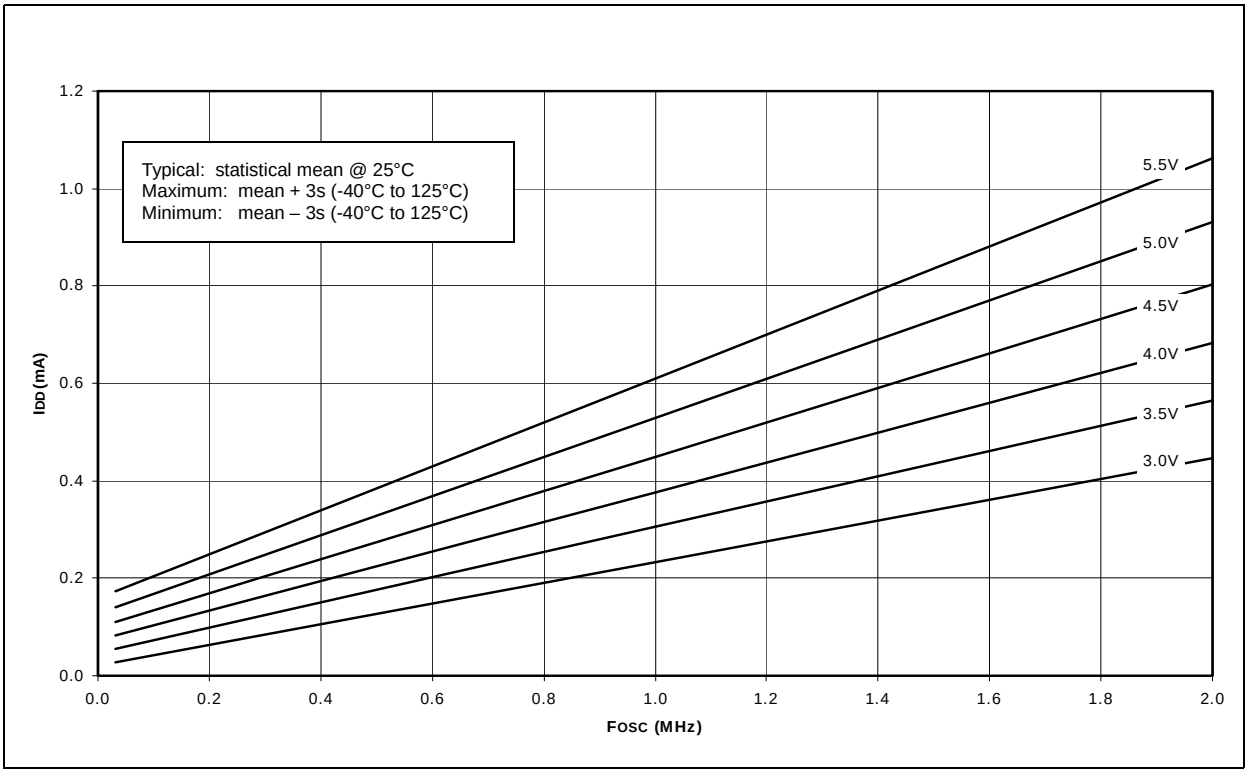


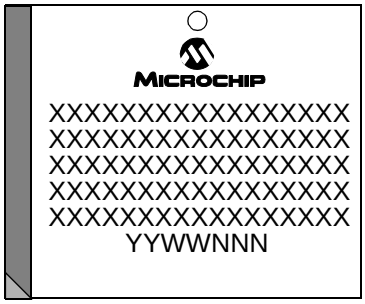
FIGURE 21-8: MAXIMUM IDD vs. FOSC OVER VDD (LF MODE)



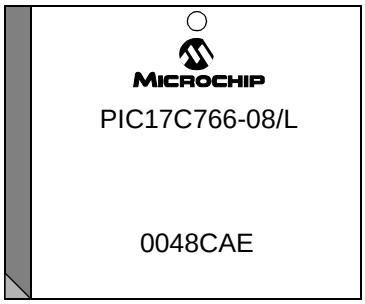
NOTES:

Package Marking Information (Cont.)

84-Lead PLCC



Example



INDEX

A

A/D
- Accuracy/Error ... 189
- ADCON0 Register ... 179
- ADCON1 Register ... 180
- ADIF bit ... 181
- Analog Input Model Block Diagram ... 184
- Analog-to-Digital Converter ... 179
- Block Diagram ... 181
- Configuring Analog Port Pins ... 186
- Configuring the Interrupt ... 181
- Configuring the Module ... 181
- Connection Considerations ... 189
- Conversion Clock ... 185
- Conversions ... 186
- Converter Characteristics ... 263
- Delays ... 183
- Effects of a RESET ... 188
- Equations ... 183
- Flow Chart of A/D Operation ... 187
- GO/$\overline{\text{DONE}}$ bit ... 181
- Internal Sampling Switch (Rss) Impedence ... 183
- Operation During SLEEP ... 188
- Sampling Requirements ... 183
- Sampling Time ... 183
- Source Impedence ... 183
- Time Delays ... 183
- Transfer Function ... 189

A/D Interrupt ... 38
A/D Interrupt Flag bit, ADIF ... 38
A/D Module Interrupt Enable, ADIE ... 36
$\overline{\text{ACK}}$ ... 144
Acknowledge Data bit, AKD ... 136
Acknowledge Pulse ... 144
Acknowledge Sequence Enable bit, AKE ... 136
Acknowledge Status bit, AKS ... 136
ADCON0 ... 49
ADCON1 ... 49
ADDLW ... 202
ADDWF ... 202
ADDWFC ... 203
ADIE ... 36
ADIF ... 38
ADRES Register ... 179
ADRESH ... 49
ADRESL ... 49
AKD ... 136
AKE ... 136
AKS ... 136, 159
ALU ... 11
ALUSTA ... 198
ALUSTA Register ... 51
ANDLW ... 203
ANDWF ... 204
Application Note AN552, 'Implementing Wake-up on Keystroke.' ... 74
Application Note AN578, "Use of the SSP Module in the I^2C Multi-Master Environment." ... 143
Assembler
- MPASM Assembler ... 233

Asynchronous Master Transmission ... 123
Asynchronous Transmitter ... 123

B

Bank Select Register (BSR) ... 57
Banking ... 46, 57
Baud Rate Formula ... 120
Baud Rate Generator ... 153
Baud Rate Generator (BRG) ... 120
Baud Rates
- Asynchronous Mode ... 122
- Synchronous Mode ... 121

BCF ... 204
BCLIE ... 36
BCLIF ... 38
BF ... 134, 144, 159, 162
Bit Manipulation ... 198
Block Diagrams
- A/D ... 181
- Analog Input Model ... 184
- Baud Rate Generator ... 153
- BSR Operation ... 57
- External Brown-out Protection Circuit (Case1) ... 31
- External Power-on Reset Circuit ... 24
- External Program Memory Connection ... 45
- I^2C Master Mode ... 151
- I^2C Module ... 143
- Indirect Addressing ... 54
- On-chip Reset Circuit ... 23
- PORTD ... 80
- PORTE ... 82, 90, 91
- Program Counter Operation ... 56
- PWM ... 107
- RA0 and RA1 ... 72
- RA2 ... 72
- RA3 ... 73
- RA4 and RA5 ... 73
- RB3:RB2 Port Pins ... 75
- RB7:RB4 and RB1:RB0 Port Pins ... 74
- RC7:RC0 Port Pins ... 78
- SSP (I^2C Mode) ... 143
- SSP (SPI Mode) ... 137
- SSP Module (I^2C Master Mode) ... 133
- SSP Module (I^2C Slave Mode) ... 133
- SSP Module (SPI Mode) ... 133
- Timer3 with One Capture and One Period Register ... 110
- TMR1 and TMR2 in 16-bit Timer/Counter Mode ... 105
- TMR1 and TMR2 in Two 8-bit Timer/Counter Mode ... 104
- TMR3 with Two Capture Registers ... 112
- Using CALL, GOTO ... 56
- WDT ... 193

BODEN ... 31
$\overline{\text{Borrow}}$ ... 11
BRG ... 120, 153
Brown-out Protection ... 31
Brown-out Reset (BOR) ... 31
BSF ... 205
BSR ... 57
BSR Operation ... 57
BTFSC ... 205
BTFSS ... 206
BTG ... 206
Buffer Full bit, BF ... 144
Buffer Full Status bit, BF ... 134
Bus Arbitration ... 170
Bus Collision
- Section ... 170