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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	16MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	66
Program Memory Size	32KB (16K x 16)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	902 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic17c766-16-pt

PIC17C7XX

TABLE 3-1: PINOUT DESCRIPTIONS (CONTINUED)

Name	PIC17C75X			PIC17C76X		I/O/P Type	Buffer Type	Description
	DIP No.	PLCC No.	TQFP No.	PLCC No.	QFP No.			
RG0/AN3	32	34	24	42	30	I/O	ST	PORTG is a bi-directional I/O Port. RG0 can also be analog input 3. RG1 can also be analog input 2. RG2 can also be analog input 1, or the ground reference voltage. RG3 can also be analog input 0, or the positive reference voltage. RG4 can also be the Capture3 input pin. RG5 can also be the PWM3 output pin. RG6 can also be selected as the USART2 (SCI) Asynchronous Receive or USART2 (SCI) Synchronous Data. RG7 can also be selected as the USART2 (SCI) Asynchronous Transmit or USART2 (SCI) Synchronous Clock.
RG1/AN2	31	33	23	41	29	I/O	ST	
RG2/AN1/VREF-	30	32	22	40	28	I/O	ST	
RG3/AN0/VREF+	29	31	21	39	27	I/O	ST	
RG4/CAP3	35	38	27	46	33	I/O	ST	
RG5/PWM3	36	39	28	47	34	I/O	ST	
RG6/RX2/DT2	38	41	30	49	36	I/O	ST	
RG7/TX2/CK2	37	40	29	48	35	I/O	ST	
RH0	—	—	—	10	79	I/O	ST	PORTH is a bi-directional I/O Port. PORTH is only available on the PIC17C76X devices. RH4 can also be analog input 12. RH5 can also be analog input 13. RH6 can also be analog input 14. RH7 can also be analog input 15.
RH1	—	—	—	11	80	I/O	ST	
RH2	—	—	—	12	1	I/O	ST	
RH3	—	—	—	13	2	I/O	ST	
RH4/AN12	—	—	—	31	19	I/O	ST	
RH5/AN13	—	—	—	32	20	I/O	ST	
RH6/AN14	—	—	—	33	21	I/O	ST	
RH7/AN15	—	—	—	34	22	I/O	ST	
RJ0	—	—	—	52	39	I/O	ST	PORTJ is a bi-directional I/O Port. PORTJ is only available on the PIC17C76X devices.
RJ1	—	—	—	53	40	I/O	ST	
RJ2	—	—	—	54	41	I/O	ST	
RJ3	—	—	—	55	42	I/O	ST	
RJ4	—	—	—	73	59	I/O	ST	
RJ5	—	—	—	74	60	I/O	ST	
RJ6	—	—	—	75	61	I/O	ST	
RJ7	—	—	—	76	62	I/O	ST	
TEST	16	17	8	21	10	I	ST	Test mode selection control input. Always tie to Vss for normal operation.
Vss	17, 33, 49, 64	19, 36, 53, 68	9, 25, 41, 56	23, 44, 65, 84	11, 31, 51, 70	P		Ground reference for logic and I/O pins.
VDD	1, 18, 34, 46	2, 20, 37, 49	10, 26, 38, 57	24, 45, 61, 2	12, 32, 48, 71	P		Positive supply for logic and I/O pins.
AVss	28	30	20	38	26	P		Ground reference for A/D converter. This pin MUST be at the same potential as Vss.
AVDD	27	29	19	37	25	P		Positive supply for A/D converter. This pin MUST be at the same potential as VDD.
NC	—	1, 18, 35, 52	—	1, 22, 43, 64	—			No Connect. Leave these pins unconnected.

Legend: I = Input only; O = Output only; I/O = Input/Output;
 P = Power; — = Not Used; TTL = TTL input; ST = Schmitt Trigger input

Note 1: The output is only available by the peripheral operation.
Note 2: Open drain input/output pin. Pin forced to input upon any device RESET.

TABLE 5-4: INITIALIZATION CONDITIONS FOR SPECIAL FUNCTION REGISTERS

Register	Address	Power-on Reset Brown-out Reset	MCLR Reset WDT Reset	Wake-up from SLEEP through Interrupt
Unbanked				
INDF0	00h	N/A	N/A	N/A
FSR0	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	02h	0000h	0000h	PC + 1 ⁽²⁾
PCLATH	03h	0000 0000	uuuu uuuu	uuuu uuuu
ALUSTA	04h	1111 xxxx	1111 uuuu	1111 uuuu
T0STA	05h	0000 000-	0000 000-	0000 000-
CPUSTA ⁽³⁾	06h	--11 11qq	--11 qquu	--uu qquu
INTSTA	07h	0000 0000	0000 0000	uuuu uuuu ⁽¹⁾
INDF1	08h	N/A	N/A	N/A
FSR1	09h	xxxx xxxx	uuuu uuuu	uuuu uuuu
WREG	0Ah	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR0L	0Bh	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR0H	0Ch	xxxx xxxx	uuuu uuuu	uuuu uuuu
TBLPTRL	0Dh	0000 0000	0000 0000	uuuu uuuu
TBLPTRH	0Eh	0000 0000	0000 0000	uuuu uuuu
BSR	0Fh	0000 0000	0000 0000	uuuu uuuu
Bank 0				
PORTA ^(4,6)	10h	0-xx 11xx	0-uu 11uu	u-uu uuuu
DDRB	11h	1111 1111	1111 1111	uuuu uuuu
PORTB ⁽⁴⁾	12h	xxxx xxxx	uuuu uuuu	uuuu uuuu
RCSTA1	13h	0000 -00x	0000 -00u	uuuu -uuu
RCREG1	14h	xxxx xxxx	uuuu uuuu	uuuu uuuu
TXSTA1	15h	0000 --1x	0000 --1u	uuuu --uu
TXREG1	16h	xxxx xxxx	uuuu uuuu	uuuu uuuu
SPBRG1	17h	0000 0000	0000 0000	uuuu uuuu

Legend: u = unchanged, x = unknown, - = unimplemented, read as '0', q = value depends on condition

Note 1: One or more bits in INTSTA, PIR1, PIR2 will be affected (to cause wake-up).

2: When the wake-up is due to an interrupt and the GLINTD bit is cleared, the PC is loaded with the interrupt vector.

3: See Table 5-3 for RESET value of specific condition.

4: This is the value that will be in the port output latch.

5: When the device is configured for Microprocessor or Extended Microcontroller mode, the operation of this port does not rely on these registers.

6: On any device RESET, these pins are configured as inputs.

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10.2 PORTB and DDRB Registers

PORTB is an 8-bit wide, bi-directional port. The corresponding data direction register is DDRB. A '1' in DDRB configures the corresponding port pin as an input. A '0' in the DDRB register configures the corresponding port pin as an output. Reading PORTB reads the status of the pins, whereas writing to PORTB will write to the port latch.

Each of the PORTB pins has a weak internal pull-up. A single control bit can turn on all the pull-ups. This is done by clearing the RBPU (PORTA<7>) bit. The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are enabled on any RESET.

PORTB also has an interrupt-on-change feature. Only pins configured as inputs can cause this interrupt to occur (i.e., any RB7:RB0 pin configured as an output is excluded from the interrupt-on-change comparison). The input pins (of RB7:RB0) are compared with the value in the PORTB data latch. The "mismatch" outputs of RB7:RB0 are OR'd together to set the PORTB Interrupt Flag bit, RBIF (PIR1<7>).

This interrupt can wake the device from SLEEP. The user, in the Interrupt Service Routine, can clear the interrupt by:

- Read-Write PORTB (such as: `MOVWF PORTB, PORTB`). This will end the mismatch condition.
- Then, clear the RBIF bit.

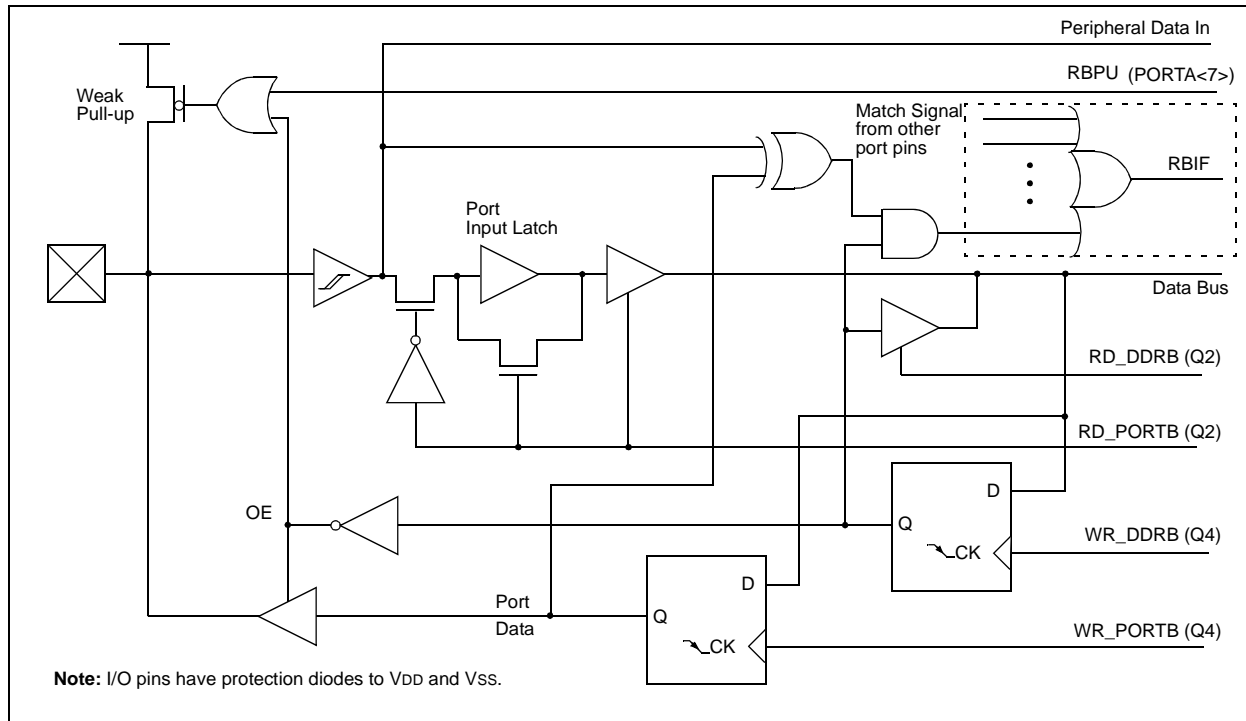
A mismatch condition will continue to set the RBIF bit. Reading, then writing PORTB, will end the mismatch condition and allow the RBIF bit to be cleared.

This interrupt-on-mismatch feature, together with software configurable pull-ups on this port, allows easy interface to a keypad and makes it possible for wake-up on key depression. For an example, refer to Application Note AN552, "Implementing Wake-up on Keystroke."

The interrupt-on-change feature is recommended for wake-up on operations, where PORTB is only used for the interrupt-on-change feature and key depression operations.

Note: On a device RESET, the RBIF bit is indeterminate, since the value in the latch may be different than the pin.

FIGURE 10-5: BLOCK DIAGRAM OF RB5:RB4 AND RB1:RB0 PORT PINS

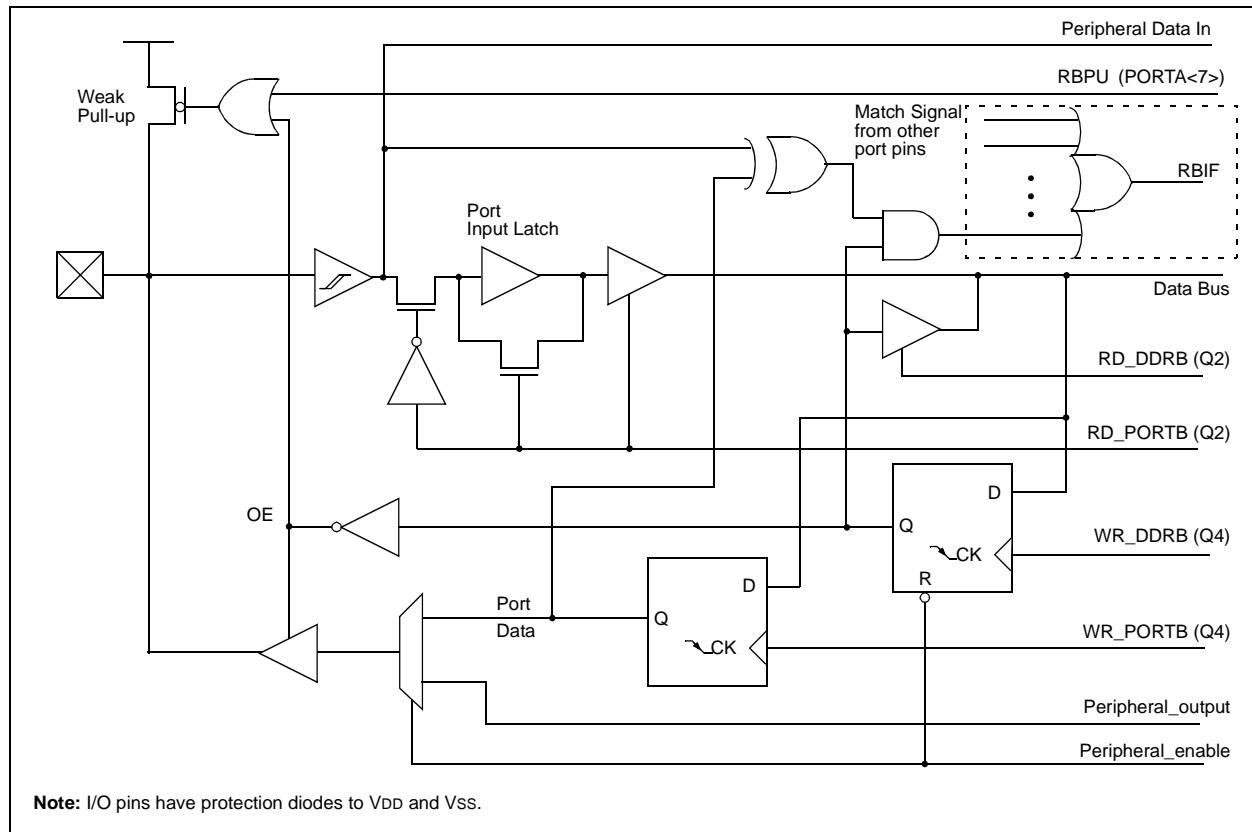


Example 10-2 shows an instruction sequence to initialize PORTB. The Bank Select Register (BSR) must be selected to Bank 0 for the port to be initialized. The following example uses the MOVLB instruction to load the BSR register for bank selection.

EXAMPLE 10-2: INITIALIZING PORTB

```
MOVLB  0      ; Select Bank 0
CLRF   PORTB, F ; Init PORTB by clearing
                ; output data latches
MOVLW  0xCF    ; Value used to initialize
                ; data direction
MOVWF  DDRB    ; Set RB<3:0> as inputs
                ; RB<5:4> as outputs
                ; RB<7:6> as inputs
```

FIGURE 10-6: BLOCK DIAGRAM OF RB3:RB2 PORT PINS



REGISTER 13-3: TCON3 REGISTER (ADDRESS: 16h, BANK 7)

U-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	CA4OVF	CA3OVF	CA4ED1	CA4ED0	CA3ED1	CA3ED0	PWM3ON

bit 7

bit 0

bit 7 **Unimplemented:** Read as '0'

bit 6 **CA4OVF:** Capture4 Overflow Status bit

This bit indicates that the capture value had not been read from the capture register pair (CA4H:CA4L) before the next capture event occurred. The capture register retains the oldest unread capture value (last capture before overflow). Subsequent capture events will not update the capture register with the TMR3 value until the capture register has been read (both bytes).

1 = Overflow occurred on Capture4 registers

0 = No overflow occurred on Capture4 registers

bit 5 **CA3OVF:** Capture3 Overflow Status bit

This bit indicates that the capture value had not been read from the capture register pair (CA3H:CA3L) before the next capture event occurred. The capture register retains the oldest unread capture value (last capture before overflow). Subsequent capture events will not update the capture register with the TMR3 value until the capture register has been read (both bytes).

1 = Overflow occurred on Capture3 registers

0 = No overflow occurred on Capture3 registers

bit 4-3 **CA4ED1:CA4ED0:** Capture4 Mode Select bits

00 = Capture on every falling edge

01 = Capture on every rising edge

10 = Capture on every 4th rising edge

11 = Capture on every 16th rising edge

bit 2-1 **CA3ED1:CA3ED0:** Capture3 Mode Select bits

00 = Capture on every falling edge

01 = Capture on every rising edge

10 = Capture on every 4th rising edge

11 = Capture on every 16th rising edge

bit 0 **PWM3ON:** PWM3 On bit

1 = PWM3 is enabled (the RG5/PWM3 pin ignores the state of the DDRG<5> bit)

0 = PWM3 is disabled (the RG5/PWM3 pin uses the state of the DDRG<5> bit for data direction)

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

- n = Value at POR Reset

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

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13.1 Timer1 and Timer2

13.1.1 TIMER1, TIMER2 IN 8-BIT MODE

Both Timer1 and Timer2 will operate in 8-bit mode when the T16 bit is clear. These two timers can be independently configured to increment from the internal instruction cycle clock (Tcy), or from an external clock source on the RB4/TCLK12 pin. The timer clock source is configured by the TMRxCS bit (x = 1 for Timer1, or = 2 for Timer2). When TMRxCS is clear, the clock source is internal and increments once every instruction cycle (Fosc/4). When TMRxCS is set, the clock source is the RB4/TCLK12 pin and the counters will increment on every falling edge of the RB4/TCLK12 pin.

The timer increments from 00h until it equals the Period register (PRx). It then resets to 00h at the next increment cycle. The timer interrupt flag is set when the timer is reset. TMR1 and TMR2 have individual interrupt flag bits. The TMR1 interrupt flag bit is latched into TMR1IF and the TMR2 interrupt flag bit is latched into TMR2IF.

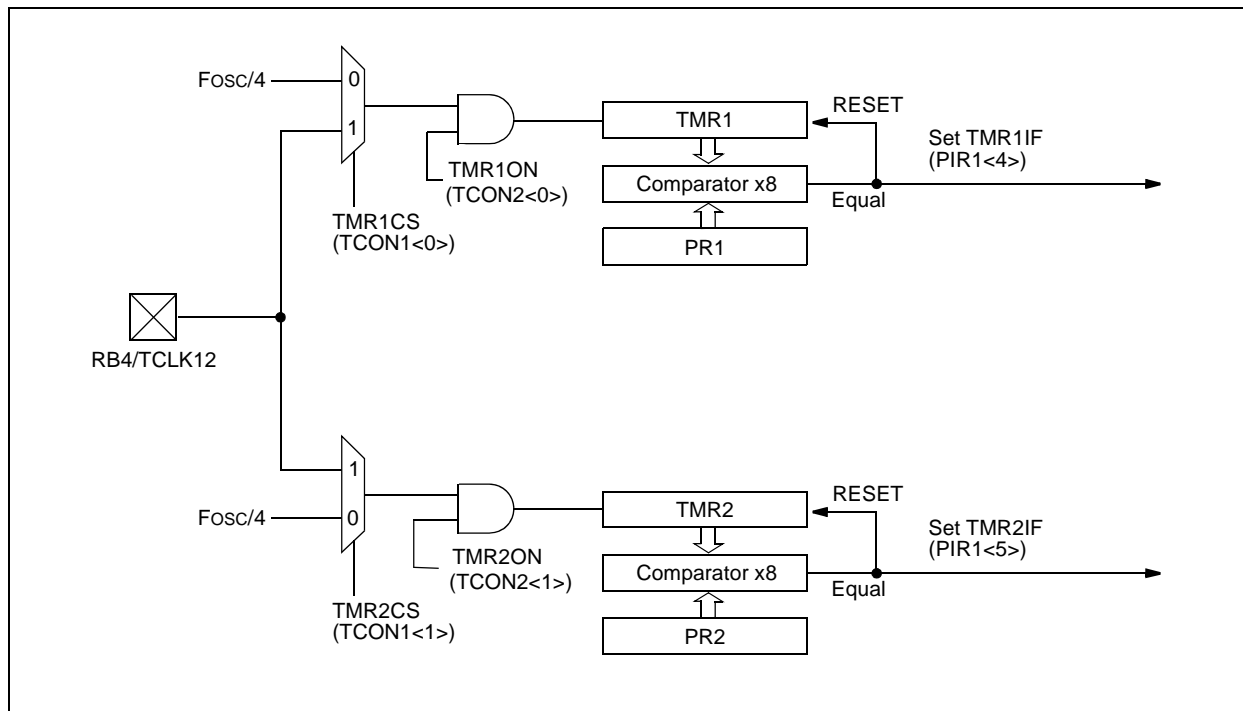
Each timer also has a corresponding interrupt enable bit (TMRxIE). The timer interrupt can be enabled/disabled by setting/clearing this bit. For peripheral interrupts to be enabled, the Peripheral Interrupt Enable bit must be set (PEIE = '1') and global interrupt must be enabled (GLINTD = '0').

The timers can be turned on and off under software control. When the timer on control bit (TMRxON) is set, the timer increments from the clock source. When TMRxON is cleared, the timer is turned off and cannot cause the timer interrupt flag to be set.

13.1.1.1 External Clock Input for Timer1 and Timer2

When TMRxCS is set, the clock source is the RB4/TCLK12 pin, and the counter will increment on every falling edge on the RB4/TCLK12 pin. The TCLK12 input is synchronized with internal phase clocks. This causes a delay from the time a falling edge appears on TCLK12 to the time TMR1 or TMR2 is actually incremented. For the external clock input timing requirements, see the Electrical Specification section.

FIGURE 13-1: TIMER1 AND TIMER2 IN TWO 8-BIT TIMER/COUNTER MODE



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15.1.5 SLAVE MODE

In Slave mode, the data is transmitted and received as the external clock pulses appear on SCK. When the last bit is latched, the interrupt flag bit SSPIF (PIR2<7>) is set.

While in Slave mode, the external clock is supplied by the external clock source on the SCK pin. This external clock must meet the minimum high and low times as specified in the electrical specifications.

While in SLEEP mode, the slave can transmit/receive data. When a byte is received, the device will wake-up from SLEEP.

15.1.6 SLAVE SELECT SYNCHRONIZATION

The \overline{SS} pin allows a Synchronous Slave mode. The SPI must be in Slave mode with \overline{SS} pin control enabled (SSPCON1<3:0> = 04h). The pin must not be driven low for the \overline{SS} pin to function as an input. The RA2 Data Latch must be high. When the \overline{SS} pin is low, transmission and reception are enabled and

the SDO pin is driven. When the \overline{SS} pin goes high, the SDO pin is no longer driven, even if in the middle of a transmitted byte and becomes a floating output. External pull-up/pull-down resistors may be desirable, depending on the application.

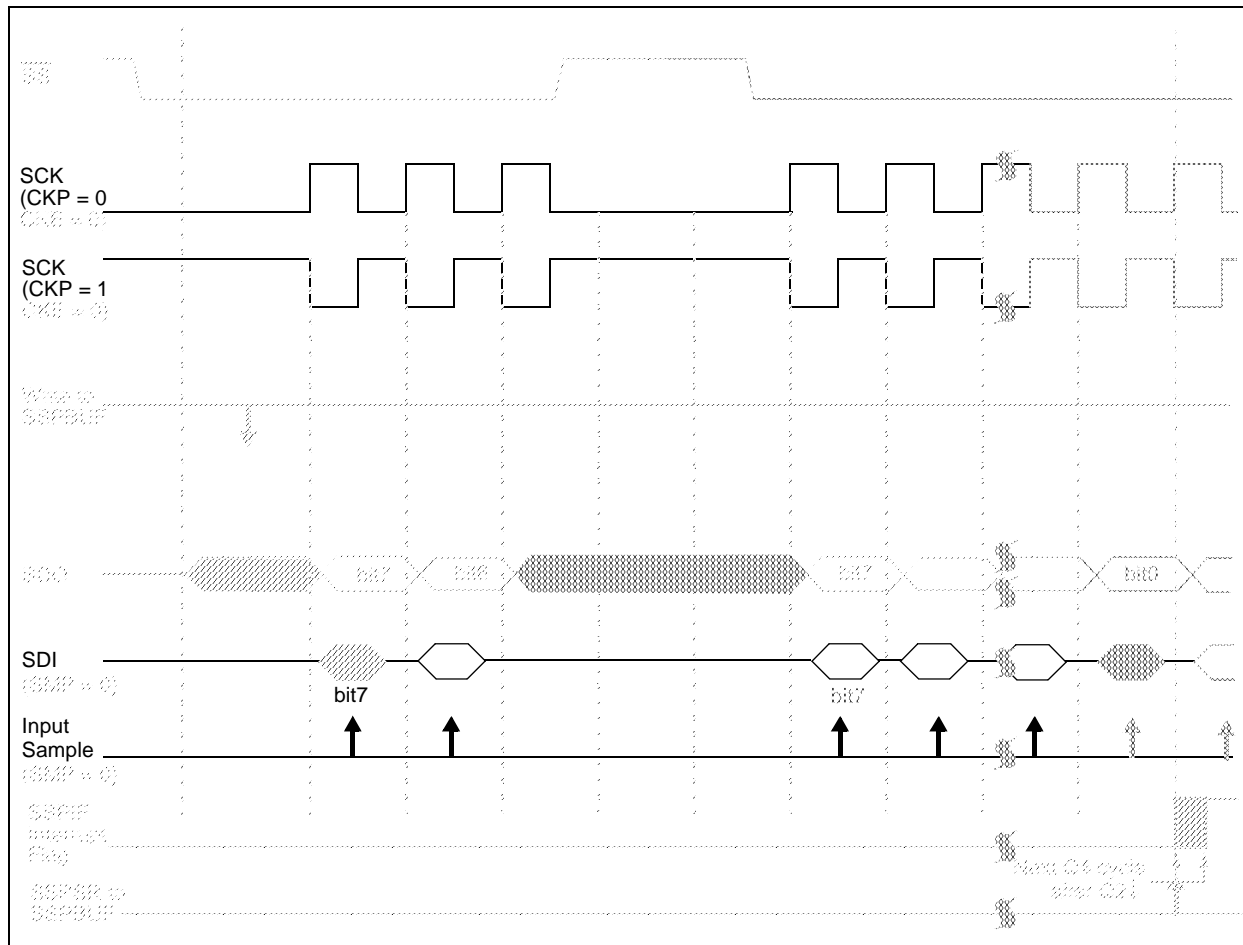
Note 1: When the SPI is in Slave mode with \overline{SS} pin control enabled (SSPCON<3:0> = 0100), the SPI module will reset if the \overline{SS} pin is set to VDD.

2: If the SPI is used in Slave mode with CKE = '1', then the \overline{SS} pin control must be enabled.

When the SPI module resets, the bit counter is forced to 0. This can be done by either forcing the \overline{SS} pin to a high level, or clearing the SSPEN bit.

To emulate two-wire communication, the SDO pin can be connected to the SDI pin. When the SPI needs to operate as a receiver, the SDO pin can be configured as an input. This disables transmissions from the SDO. The SDI can always be left as an input (SDI function), since it cannot create a bus conflict.

FIGURE 15-7: SLAVE SYNCHRONIZATION WAVEFORM



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15.1.7 SLEEP OPERATION

In Master mode, all module clocks are halted, and the transmission/reception will remain in that state until the device wakes from SLEEP. After the device returns to normal mode, the module will continue to transmit/receive data.

In Slave mode, the SPI transmit/receive shift register operates asynchronously to the device. This allows the device to be placed in SLEEP mode and data to be

shifted into the SPI transmit/receive shift register. When all 8-bits have been received, the MSSP interrupt flag bit will be set and if enabled, will wake the device from SLEEP.

15.1.8 EFFECTS OF A RESET

A RESET disables the MSSP module and terminates the current transfer.

TABLE 15-1: REGISTERS ASSOCIATED WITH SPI OPERATION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	POR, BOR	MCLR, WDT
07h, Unbanked	INTSTA	PEIF	T0CKIF	T0IF	INTF	PEIE	T0CKIE	T0IE	INTE	0000 0000	0000 0000
10h, Bank 4	PIR2	SSPIF	BCLIF	ADIF	—	CA4IF	CA3IF	TX2IF	RC2IF	000- 0010	000- 0010
11h, Bank 4	PIE2	SSPIE	BCLIE	ADIE	—	CA4IE	CA3IE	TX2IE	RC2IE	000- 0000	000- 0000
14h, Bank 6	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register								xxxx xxxx	uuuu uuuu
11h, Bank 6	SSPCON1	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
13h, Bank 6	SSPSTAT	SMP	CKE	D/ \bar{A}	P	S	R/ \bar{W}	UA	BF	0000 0000	0000 0000

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by the SSP in SPI mode.

15.2.12 I²C MASTER MODE RECEPTION

Master mode reception is enabled by programming the receive enable bit, RCEN (SSPCON2<3>).

Note: The SSP Module must be in an IDLE STATE before the RCEN bit is set, or the RCEN bit will be disregarded.

The baud rate generator begins counting and on each rollover, the state of the SCL pin changes (high to low/low to high) and data is shifted into the SSPSR. After the falling edge of the eighth clock, the receive enable flag is automatically cleared, the contents of the SSPSR are loaded into the SSPBUF, the BF flag is set, the SSPIF is set and the baud rate generator is suspended from counting, holding SCL low. The SSP is now in IDLE state, awaiting the next command. When the buffer is read by the CPU, the BF flag is automatically cleared. The user can then send an acknowledge bit at the end of reception, by setting the acknowledge sequence enable bit, ACKEN (SSPCON2<4>).

15.2.12.1 BF Status Flag

In receive operation, BF is set when an address or data byte is loaded into SSPBUF from SSPSR. It is cleared when SSPBUF is read.

15.2.12.2 SSPOV Status Flag

In receive operation, SSPOV is set when 8 bits are received into the SSPSR, and the BF flag is already set from a previous reception.

15.2.12.3 WCOL Status Flag

If the user writes the SSPBUF when a receive is already in progress (i.e., SSPSR is still shifting in a data byte), then WCOL is set and the contents of the buffer are unchanged (the write doesn't occur).

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EXAMPLE 15-2: INTERFACING TO A 24LC01B SERIAL EEPROM (USING MPLAB C17)

```
void ACKPoll(void)
{
    StartI2C();           // Send start bit
    IdleI2C();            // Wait for idle condition
    WriteI2C(CONTROL);    // Send control byte
    IdleI2C();            // Wait for idle condition
    // Poll the ACK bit coming from the 24LC01B
    // Loop as long as the 24LC01B NACKs
    while (SSPCON2bits.ACKSTAT)
    {
        RestartI2C();     // Send a restart bit
        IdleI2C();        // Wait for idle condition
        WriteI2C(CONTROL); // Send control byte
        IdleI2C();        // Wait for idle condition
    }
    IdleI2C();            // Wait for idle condition
    StopI2C();            // Send stop bit
    IdleI2C();            // Wait for idle condition
    return;
}
```

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REGISTER 16-2: ADCON1 REGISTER (ADDRESS 15h, BANK 5)

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
ADCS1	ADCS0	ADFM	—	PCFG3	PCFG2	PCFG1	PCFG0
bit 7				bit 0			

- bit 7-6 **ADCS1:ADCS0:** A/D Conversion Clock Select bits
 00 = FOSC/8
 01 = FOSC/32
 10 = FOSC/64
 11 = FRC (clock derived from an internal RC oscillator)
- bit 5 **ADFM:** A/D Result Format Select
 1 = Right justified. 6 Most Significant bits of ADRESH are read as '0'.
 0 = Left justified. 6 Least Significant bits of ADRESL are read as '0'.
- bit 4 **Unimplemented:** Read as '0'
- bit 3-1 **PCFG3:PCFG1:** A/D Port Configuration Control bits
- bit 0 **PCFG0:** A/D Voltage Reference Select bit
 1 = A/D reference is the VREF+ and VREF- pins
 0 = A/D reference is AVDD and AVSS
- Note:** When this bit is set, ensure that the A/D voltage reference specifications are met.

PCFG3:PCFG0	AN15	AN14	AN13	AN12	AN11	AN10	AN9	AN8	AN7	AN6	AN5	AN4	AN3	AN2	AN1	AN0
000x	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
001x	D	A	A	A	A	A	A	A	D	A	A	A	A	A	A	A
010x	D	D	A	A	A	A	A	A	D	D	A	A	A	A	A	A
011x	D	D	D	A	A	A	A	A	D	D	D	A	A	A	A	A
100x	D	D	D	D	A	A	A	A	D	D	D	D	A	A	A	A
101x	D	D	D	D	D	A	A	A	D	D	D	D	D	A	A	A
110x	D	D	D	D	D	D	A	A	D	D	D	D	D	D	A	A
111x	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

A = Analog input D = Digital I/O

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 - n = Value at POR Reset '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

16.1 A/D Acquisition Requirements

For the A/D converter to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 16-3. The source impedance (Rs) and the internal sampling switch (Rss) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (Rss) impedance varies over the device voltage (VDD), Figure 16-3. **The maximum recommended impedance for analog sources is 10 kΩ.** As the impedance is decreased, the acquisition time may be decreased. After the analog input channel is selected (changed) this acquisition must be done before the conversion can be started.

To calculate the minimum acquisition time, Equation 16-1 may be used. This equation assumes that 1/2 LSB error is used (1024 steps for the A/D). The 1/2 LSB error is the maximum error allowed for the A/D to meet its specified resolution.

Example 16-1 shows the calculation of the minimum required acquisition time (TACQ). This is based on the following application system assumptions.

CHOLD	=	120 pF
Rs	=	10 kΩ
Conversion Error	≤	1/2 LSB
VDD	=	5V → Rss = 7 kΩ (see graph in Figure 16-3)
Temperature	=	50°C (system max.)
VHOLD	=	0V @ time = 0

EQUATION 16-1: ACQUISITION TIME

$$\begin{aligned} T_{ACQ} &= \text{Amplifier Settling Time} + \\ &\quad \text{Holding Capacitor Charging Time} + \\ &\quad \text{Temperature Coefficient} \\ &= T_{AMP} + T_C + T_{COFF} \end{aligned}$$

EQUATION 16-2: A/D MINIMUM CHARGING TIME

$$\begin{aligned} V_{HOLD} &= (V_{REF} - (V_{REF}/2048)) \cdot (1 - e^{-(T_C/CHOLD)(R_{IC} + R_{SS} + R_S)}) \\ \text{or} \\ T_C &= -(120 \text{ pF})(1 \text{ k}\Omega + R_{SS} + R_S) \ln(1/2047) \end{aligned}$$

EXAMPLE 16-1: CALCULATING THE MINIMUM REQUIRED ACQUISITION TIME

$$\begin{aligned} T_{ACQ} &= T_{AMP} + T_C + T_{COFF} \\ \text{Temperature coefficient is only required for temperatures} &> 25^\circ\text{C}. \\ T_{ACQ} &= 2 \mu\text{s} + T_C + [(Temp - 25^\circ\text{C})(0.05 \mu\text{s}/^\circ\text{C})] \\ T_C &= -CHOLD (R_{IC} + R_{SS} + R_S) \ln(1/2047) \\ &= -120 \text{ pF} (1 \text{ k}\Omega + 7 \text{ k}\Omega + 10 \text{ k}\Omega) \ln(0.0004885) \\ &= -120 \text{ pF} (18 \text{ k}\Omega) \ln(0.0004885) \\ &= -2.16 \mu\text{s} (-7.6241) \\ &= 16.47 \mu\text{s} \\ T_{ACQ} &= 2 \mu\text{s} + 16.47 \mu\text{s} + [(50^\circ\text{C} - 25^\circ\text{C})(0.05 \mu\text{s}/^\circ\text{C})] \\ &= 18.447 \mu\text{s} + 1.25 \mu\text{s} \\ &= 19.72 \mu\text{s} \end{aligned}$$

- Note 1:** The reference voltage (VREF) has no effect on the equation since it cancels itself out.
- 2:** The charge holding capacitor (CHOLD) is not discharged after each conversion.
- 3:** The maximum recommended impedance for analog sources is 10 kΩ. This is required to meet the pin leakage specification.
- 4:** After a conversion has completed, a 2.0 TAD delay must complete before acquisition can begin again. During this time, the holding capacitor is not connected to the selected A/D input channel.

PIC17C7XX

BTFSS Bit Test, skip if Set

Syntax: [*label*] BTFSS *f*,*b*

Operands: $0 \leq f \leq 127$
 $0 \leq b < 7$

Operation: skip if (*f*<*b*>) = 1

Status Affected: None

Encoding:

1001	0bbb	ffff	ffff
------	------	------	------

Description: If bit 'b' in register 'f' is 1, then the next instruction is skipped.
If bit 'b' is 1, then the next instruction fetched during the current instruction execution is discarded and a NOP is executed instead, making this a two-cycle instruction.

Words: 1

Cycles: 1(2)

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	No operation

If skip:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation

Example:

```
HERE    BTFSS    FLAG,1
FALSE   :
TRUE    :
```

Before Instruction

PC = address (HERE)

After Instruction

```
If FLAG<1> = 0;
    PC = address (FALSE)
If FLAG<1> = 1;
    PC = address (TRUE)
```

BTG Bit Toggle f

Syntax: [*label*] BTG *f*,*b*

Operands: $0 \leq f \leq 255$
 $0 \leq b < 7$

Operation: ($\overline{f\langle b \rangle}$) \rightarrow (*f*<*b*>)

Status Affected: None

Encoding:

0011	1bbb	ffff	ffff
------	------	------	------

Description: Bit 'b' in data memory location 'f' is inverted.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write register 'f'

Example: BTG PORTC, 4

Before Instruction:

PORTC = 0111 0101 [0x75]

After Instruction:

PORTC = 0110 0101 [0x65]

RLNCF Rotate Left f (no carry)

Syntax: [label] RLNCF f,d

Operands: $0 \leq f \leq 255$
 $d \in [0,1]$

Operation: $f\langle n \rangle \rightarrow d\langle n+1 \rangle$;
 $f\langle 7 \rangle \rightarrow d\langle 0 \rangle$

Status Affected: None

Encoding:

0010	001d	ffff	ffff
------	------	------	------

Description: The contents of register 'f' are rotated one bit to the left. If 'd' is 0, the result is placed in WREG. If 'd' is 1, the result is stored back in register 'f'.



Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

Example: RLNCF REG, 1

Before Instruction

C = 0
 REG = 1110 1011

After Instruction

C =
 REG = 1101 0111

RRCF Rotate Right f through Carry

Syntax: [label] RRCF f,d

Operands: $0 \leq f \leq 255$
 $d \in [0,1]$

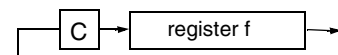
Operation: $f\langle n \rangle \rightarrow d\langle n-1 \rangle$;
 $f\langle 0 \rangle \rightarrow C$;
 $C \rightarrow d\langle 7 \rangle$

Status Affected: C

Encoding:

0001	100d	ffff	ffff
------	------	------	------

Description: The contents of register 'f' are rotated one bit to the right through the Carry Flag. If 'd' is 0, the result is placed in WREG. If 'd' is 1, the result is placed back in register 'f'.



Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

Example: RRCF REG1, 0

Before Instruction

REG1 = 1110 0110
 C = 0

After Instruction

REG1 = 1110 0110
 WREG = 0111 0011
 C = 0

PIC17C7XX

Param No.	Sym	Characteristic		Min	Max	Units	Conditions
110	Tbuf	Bus free time	100 kHz mode	4.7	—	ms	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	ms	
			1 MHz mode ⁽¹⁾	0.5	—	ms	
D102	Cb	Bus capacitive loading		—	400	pF	

Note 1: Maximum pin capacitance = 10 pF for all I²C pins.

2: A fast mode (400 KHz) I²C bus device can be used in a standard mode I²C bus system, but the parameter # 107 \geq 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line.

Parameter #102 + #107 = 1000 + 250 = 1250 ns (for 100 kHz mode) before the SCL line is released.
3: C_b is specified to be from 10-400pF. The minimum specifications are characterized with C_b=10pF. The rise time spec (t_r) is characterized with R_p=R_p min. The minimum fall time specification (t_f) is characterized with C_b=10pF, and R_p=R_p max. These are only valid for fast mode operation (V_{DD}=4.5-5.5V) and where the SPM bit (SSPSTAT<7>) =1.)

4: Max specifications for these parameters are valid for falling edge only. Specs are characterized with R_p=R_p min and C_b=400pF for standard mode, 200pF for fast mode, and 10pF for 1MHz mode.

FIGURE 20-19: USART SYNCHRONOUS TRANSMISSION (MASTER/SLAVE) TIMING

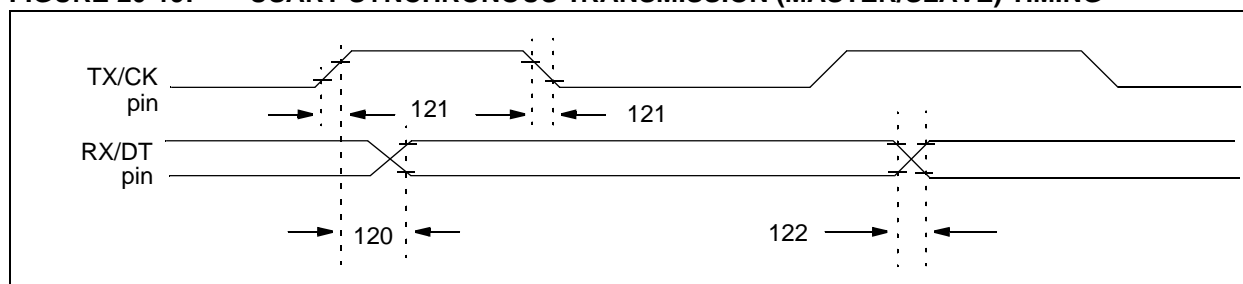


TABLE 20-14: USART SYNCHRONOUS TRANSMISSION REQUIREMENTS

Param No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
120	TckH2dtV	<u>SYNC XMIT (MASTER & SLAVE)</u>						
		Clock high to data out valid						
121	TckRF	Clock out rise time and fall time (Master mode)	PIC17CXXX	—	—	50	ns	
			PIC17LCXXX	—	—	75	ns	
			PIC17CXXX	—	—	25	ns	
122	TdtRF	Data out rise time and fall time	PIC17CXXX	—	—	40	ns	
			PIC17LCXXX	—	—	40	ns	
			PIC17CXXX	—	—	25	ns	

† Data in "Typ" column is at 5V, 25°C unless otherwise stated.

PIC17C7XX

FIGURE 20-25: MEMORY INTERFACE READ TIMING

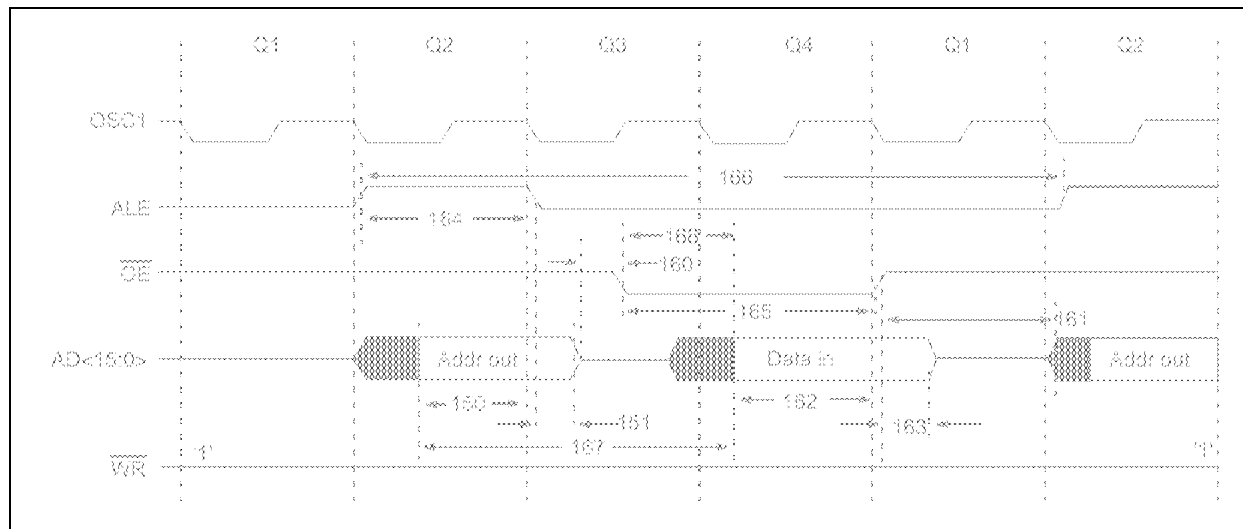
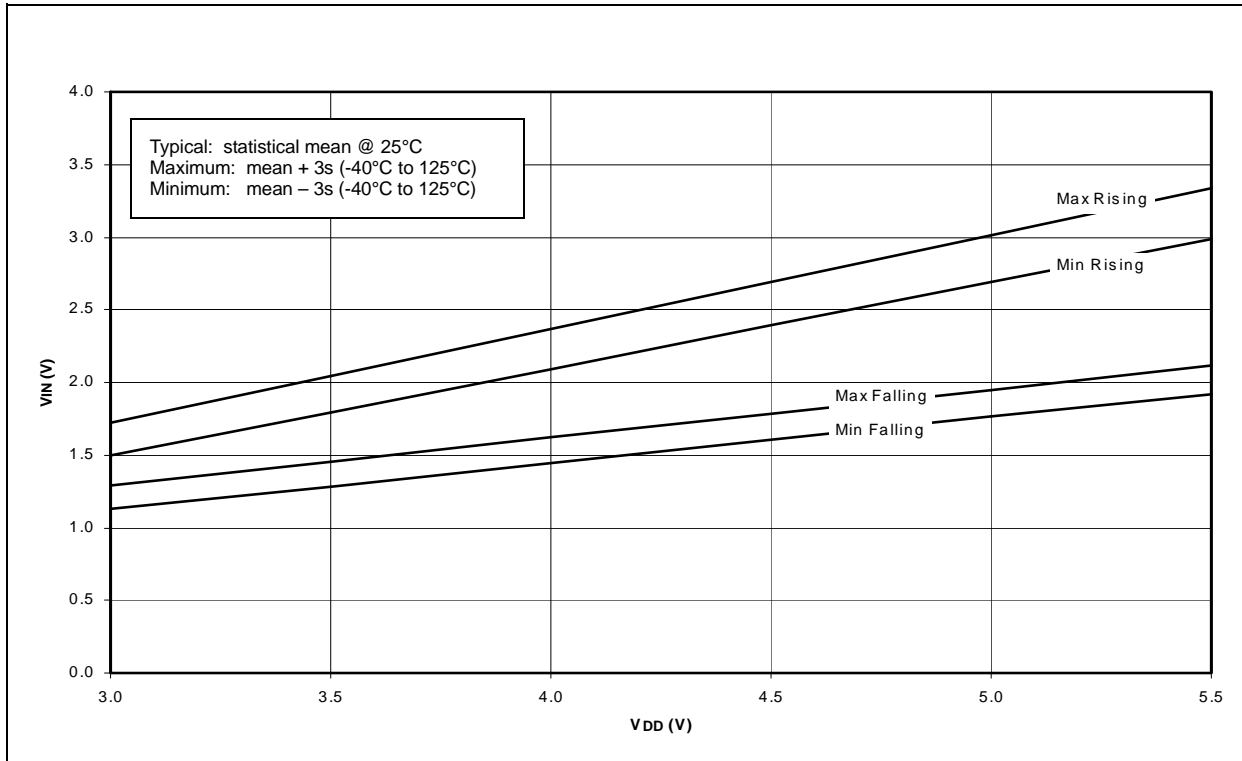


TABLE 20-21: MEMORY INTERFACE READ REQUIREMENTS

Param. No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
150	TadV2alL	AD15:AD0 (address) valid to ALE↓ (address setup time)	PIC17CXXX 0.25Tcy - 10	—	—	ns	
151	TalL2adl	ALE↓ to address out invalid (address hold time)	PIC17CXXX 5	—	—	ns	
160	TadZ2oeL	AD15:AD0 hi-impedance to OE↓	PIC17CXXX 0	—	—	ns	
161	ToeH2adD	OE↑ to AD15:AD0 driven	PIC17CXXX 0.25Tcy - 15	—	—	ns	
162	TadV2oeH	Data in valid before OE↑ (data setup time)	PIC17CXXX 35	—	—	ns	
163	ToeH2adl	OE↑ to data in invalid (data hold time)	PIC17CXXX 0	—	—	ns	
164	TalH	ALE pulse width	PIC17CXXX —	0.25Tcy	—	ns	
165	ToeL	OE pulse width	PIC17CXXX 0.5Tcy - 35	—	—	ns	
166	TalH2alH	ALE↑ to ALE↑(cycle time)	PIC17CXXX —	Tcy	—	ns	
167	Tacc	Address access time	PIC17CXXX —	—	0.75Tcy - 30	ns	
168	Toe	Output enable access time (OE low to data valid)	PIC17CXXX —	—	0.5Tcy - 45	ns	

† Data in "Typ" column is at 5V, 25 °C unless otherwise stated.

FIGURE 21-23: MAXIMUM AND MINIMUM V_{IN} vs. V_{DD} (I^2C Input, -40°C to $+125^{\circ}\text{C}$)



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