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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	33MHz
Connectivity	I <sup>2</sup> C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	66
Program Memory Size	32KB (16K x 16)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	902 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	External
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic17c766t-33-pt">https://www.e-xfl.com/product-detail/microchip-technology/pic17c766t-33-pt</a>



## 1.0 OVERVIEW

This data sheet covers the PIC17C7XX group of the PIC17CXXX family of microcontrollers. The following devices are discussed in this data sheet:

- PIC17C752
- PIC17C756A
- PIC17C762
- PIC17C766

The PIC17C7XX devices are 68/84-pin, EPROM based members of the versatile PIC17CXXX family of low cost, high performance, CMOS, fully static, 8-bit microcontrollers.

All PIC® microcontrollers employ an advanced RISC architecture. The PIC17CXXX has enhanced core features, 16-level deep stack, and multiple internal and external interrupt sources. The separate instruction and data buses of the Harvard architecture allow a 16-bit wide instruction word with a separate 8-bit wide data path. The two stage instruction pipeline allows all instructions to execute in a single cycle, except for program branches (which require two cycles). A total of 58 instructions (reduced instruction set) are available. Additionally, a large register set gives some of the architectural innovations used to achieve a very high performance. For mathematical intensive applications, all devices have a single cycle 8 x 8 Hardware Multiplier.

PIC17CXXX microcontrollers typically achieve a 2:1 code compression and a 4:1 speed improvement over other 8-bit microcontrollers in their class.

PIC17C7XX devices have up to 902 bytes of RAM and 66 I/O pins. In addition, the PIC17C7XX adds several peripheral features, useful in many high performance applications, including:

- Four timer/counters
- Four capture inputs
- Three PWM outputs
- Two independent Universal Synchronous Asynchronous Receiver Transmitters (USARTs)
- An A/D converter (multi-channel, 10-bit resolution)
- A Synchronous Serial Port (SPI and I<sup>2</sup>C w/ Master mode)

These special features reduce external components, thus reducing cost, enhancing system reliability and reducing power consumption.

There are four oscillator options, of which the single pin RC oscillator provides a low cost solution, the LF oscillator is for low frequency crystals and minimizes power consumption, XT is a standard crystal and the EC is for external clock input.

The SLEEP (power-down) mode offers additional power saving. Wake-up from SLEEP can occur through several external and internal interrupts and device RESETS.

A highly reliable Watchdog Timer with its own on-chip RC oscillator provides protection against software malfunction.

There are four configuration options for the device operational mode:

- Microprocessor
- Microcontroller
- Extended microcontroller
- Protected microcontroller

The microprocessor and extended microcontroller modes allow up to 64K-words of external program memory.

The device also has Brown-out Reset circuitry. This allows a device RESET to occur if the device VDD falls below the Brown-out voltage trip point (BVDD). The chip will remain in Brown-out Reset until VDD rises above BVDD.

A UV erasable, CERQUAD packaged version (compatible with PLCC), is ideal for code development, while the cost-effective One-Time-Programmable (OTP) version is suitable for production in any volume.

The PIC17C7XX fits perfectly in applications that require extremely fast execution of complex software programs. These include applications ranging from precise motor control and industrial process control to automotive, instrumentation, and telecom applications.

The EPROM technology makes customization of application programs (with unique security codes, combinations, model numbers, parameter storage, etc.) fast and convenient. Small footprint package options (including die sales) make the PIC17C7XX ideal for applications with space limitations that require high performance.

High speed execution, powerful peripheral features, flexible I/O, and low power consumption all at low cost make the PIC17C7XX ideal for a wide range of embedded control applications.

### 1.1 Family and Upward Compatibility

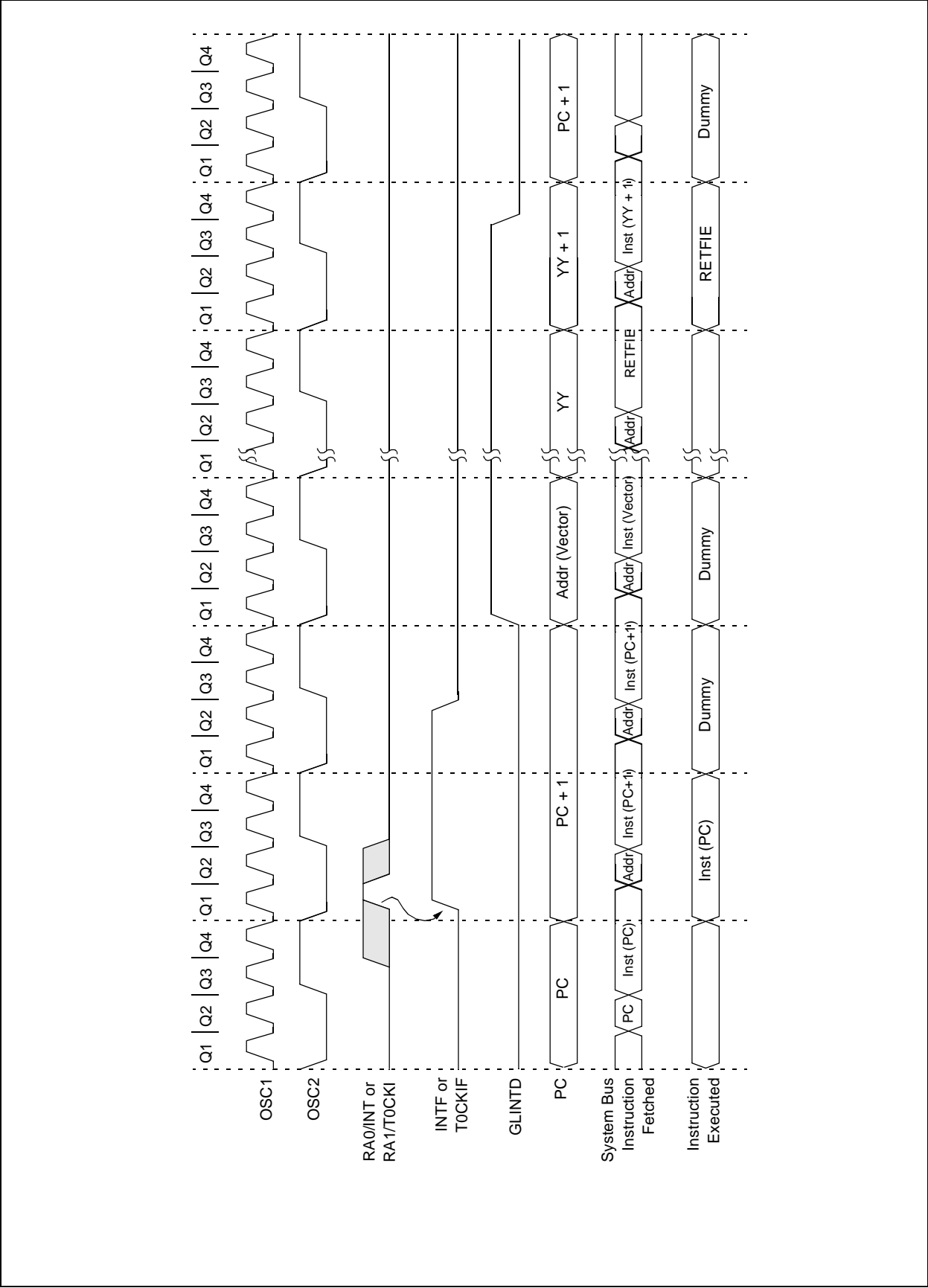
The PIC17CXXX family of microcontrollers have architectural enhancements over the PIC16C5X and PIC16CXX families. These enhancements allow the device to be more efficient in software and hardware requirements. Refer to Appendix A for a detailed list of enhancements and modifications. Code written for PIC16C5X or PIC16CXX can be easily ported to PIC17CXXX devices (Appendix B).

### 1.2 Development Support

The PIC17CXXX family is supported by a full featured macro assembler, a software simulator, an in-circuit emulator, a universal programmer, a "C" compiler and fuzzy logic support tools. For additional information, see Section 19.0.

# PIC17C7XX

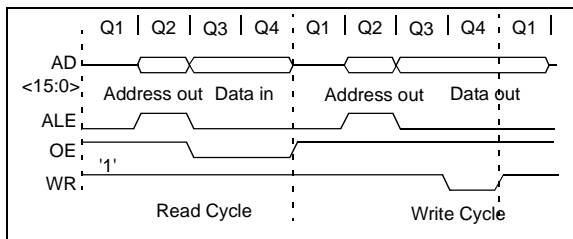
FIGURE 6-2: INT PIN/T0CKI PIN INTERRUPT TIMING



## 7.1.2 EXTERNAL MEMORY INTERFACE

When either Microprocessor or Extended Microcontroller mode is selected, PORTC, PORTD and PORTE are configured as the system bus. PORTC and PORTD are the multiplexed address/data bus and PORTE<2:0> is for the control signals. External components are needed to demultiplex the address and data. This can be done as shown in Figure 7-4. The waveforms of address and data are shown in Figure 7-3. For complete timings, please refer to the electrical specification section.

**FIGURE 7-3: EXTERNAL PROGRAM MEMORY ACCESS WAVEFORMS**



The system bus requires that there is no bus conflict (minimal leakage), so the output value (address) will be capacitively held at the desired value.

As the speed of the processor increases, external EPROM memory with faster access time must be used. Table 7-2 lists external memory speed requirements for a given PIC17C7XX device frequency.

In Extended Microcontroller mode, when the device is executing out of internal memory, the control signals will continue to be active. That is, they indicate the action that is occurring in the internal memory. The external memory access is ignored.

The following selection is for use with Microchip EPROMs. For interfacing to other manufacturers memory, please refer to the electrical specifications of the desired PIC17C7XX device, as well as the desired memory device to ensure compatibility.

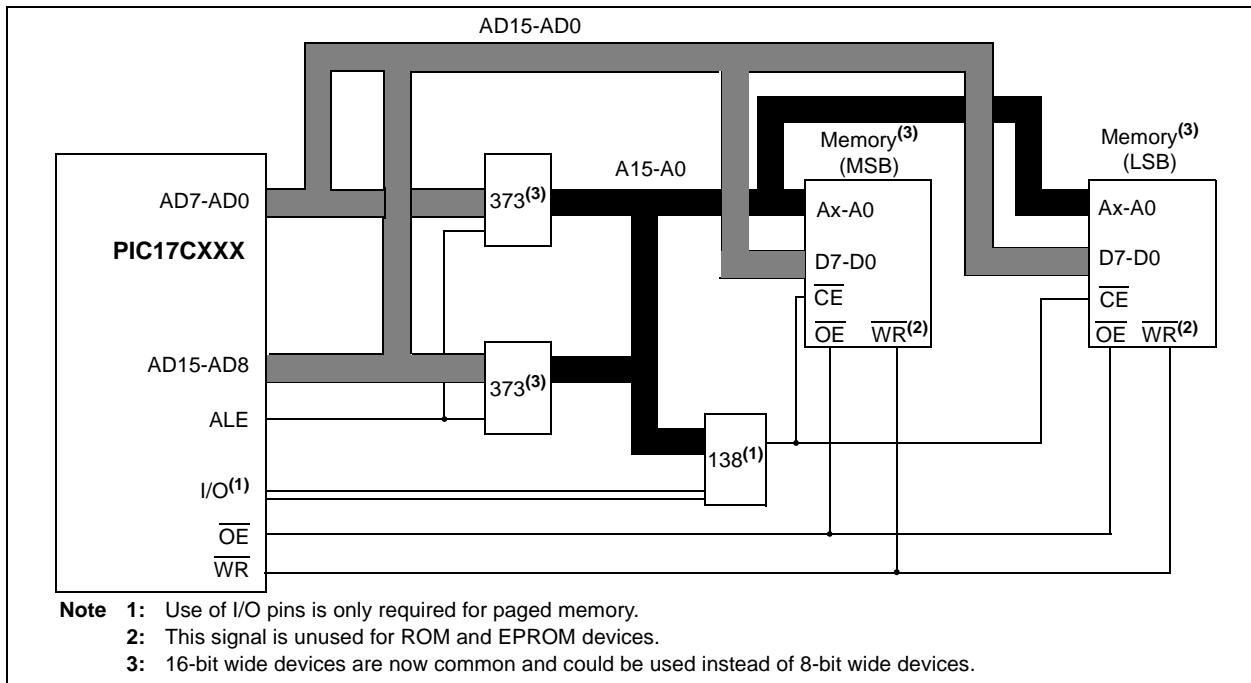
**TABLE 7-2: EPROM MEMORY ACCESS TIME ORDERING SUFFIX**

PIC17C7XX Oscillator Frequency	Instruction Cycle Time (Tcy)	EPROM Suffix
8 MHz	500 ns	-25
16 MHz	250 ns	-15
20 MHz	200 ns	-10
25 MHz	160 ns	-70

**Note:** The access times for this requires the use of fast SRAMs.

The electrical specifications now include timing specifications for the memory interface with PIC17LCXXX devices. These specifications reflect the capability of the device by characterization. Please validate your design with these timings.

**FIGURE 7-4: TYPICAL EXTERNAL PROGRAM MEMORY CONNECTION DIAGRAM**



## 7.7 Program Counter Module

The Program Counter (PC) is a 16-bit register. PCL, the low byte of the PC, is mapped in the data memory. PCL is readable and writable just as is any other register. PCH is the high byte of the PC and is not directly addressable. Since PCH is not mapped in data or program memory, an 8-bit register PCLATH (PC high latch) is used as a holding latch for the high byte of the PC. PCLATH is mapped into data memory. The user can read or write PCH through PCLATH.

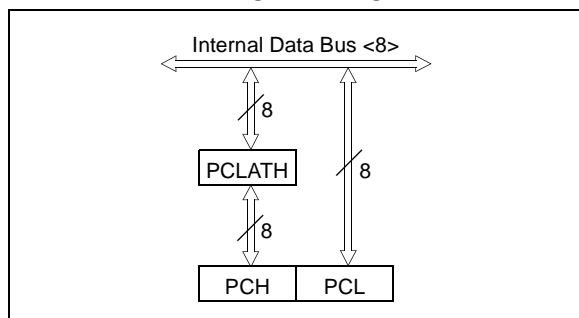
The 16-bit wide PC is incremented after each instruction fetch during Q1 unless:

- Modified by a GOTO, CALL, LCALL, RETURN, RETLW, or RETFIE instruction
- Modified by an interrupt response
- Due to destination write to PCL by an instruction

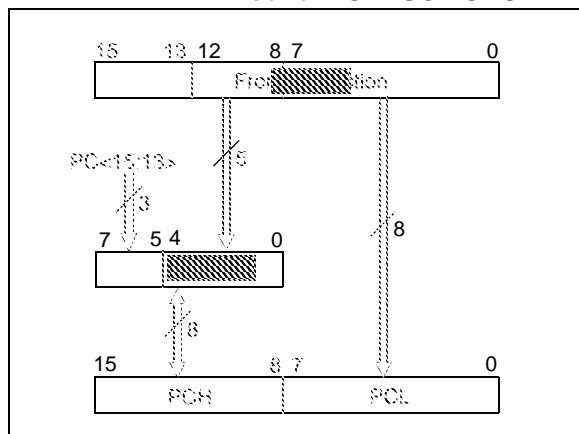
“Skips” are equivalent to a forced NOP cycle at the skipped address.

Figure 7-7 and Figure 7-8 show the operation of the program counter for various situations.

**FIGURE 7-7: PROGRAM COUNTER OPERATION**



**FIGURE 7-8: PROGRAM COUNTER USING THE CALL AND GOTO INSTRUCTIONS**



Using Figure 7-7, the operations of the PC and PCLATH for different instructions are as follows:

- LCALL instructions:**  
An 8-bit destination address is provided in the instruction (opcode). PCLATH is unchanged.  
PCLATH → PCH  
Opcode<7:0> → PCL
- Read instructions on PCL:**  
Any instruction that reads PCL.  
PCL → data bus → ALU or destination  
PCH → PCLATH
- Write instructions on PCL:**  
Any instruction that writes to PCL.  
8-bit data → data bus → PCL  
PCLATH → PCH
- Read-Modify-Write instructions on PCL:**  
Any instruction that does a read-write-modify operation on PCL, such as ADDWF PCL.  
Read: PCL → data bus → ALU  
Write: 8-bit result → data bus → PCL  
PCLATH → PCH
- RETURN instruction:**  
Stack<MRU> → PC<15:0>

Using Figure 7-8, the operation of the PC and PCLATH for GOTO and CALL instructions is as follows:

### CALL, GOTO instructions:

A 13-bit destination address is provided in the instruction (opcode).

Opcode<12:0> → PC<12:0>

PC<15:13> → PCLATH<7:5>

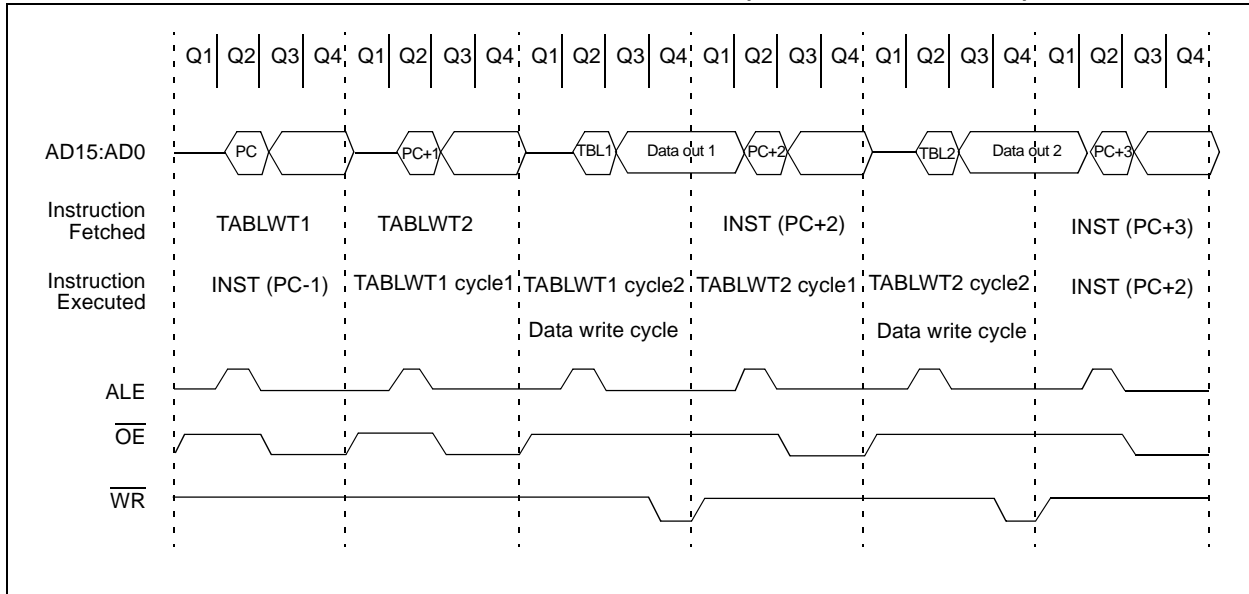
Opcode<12:8> → PCLATH<4:0>

The read-modify-write only affects the PCL with the result. PCH is loaded with the value in the PCLATH. For example, ADDWF PCL will result in a jump within the current page. If PC = 03F0h, WREG = 30h and PCLATH = 03h before instruction, PC = 0320h after the instruction. To accomplish a true 16-bit computed jump, the user needs to compute the 16-bit destination address, write the high byte to PCLATH and then write the low value to PCL.

The following PC related operations do not change PCLATH:

- LCALL, RETLW, and RETFIE instructions.
- Interrupt vector is forced onto the PC.
- Read-modify-write instructions on PCL (e.g. BSF PCL).

**FIGURE 8-6: CONSECUTIVE TABLWT WRITE TIMING (EXTERNAL MEMORY)**



# PIC17C7XX

## 10.2 PORTB and DDRB Registers

PORTB is an 8-bit wide, bi-directional port. The corresponding data direction register is DDRB. A '1' in DDRB configures the corresponding port pin as an input. A '0' in the DDRB register configures the corresponding port pin as an output. Reading PORTB reads the status of the pins, whereas writing to PORTB will write to the port latch.

Each of the PORTB pins has a weak internal pull-up. A single control bit can turn on all the pull-ups. This is done by clearing the RBPU (PORTA<7>) bit. The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are enabled on any RESET.

PORTB also has an interrupt-on-change feature. Only pins configured as inputs can cause this interrupt to occur (i.e., any RB7:RB0 pin configured as an output is excluded from the interrupt-on-change comparison). The input pins (of RB7:RB0) are compared with the value in the PORTB data latch. The "mismatch" outputs of RB7:RB0 are OR'd together to set the PORTB Interrupt Flag bit, RBIF (PIR1<7>).

This interrupt can wake the device from SLEEP. The user, in the Interrupt Service Routine, can clear the interrupt by:

- Read-Write PORTB (such as: `MOVWF PORTB, PORTB`). This will end the mismatch condition.
- Then, clear the RBIF bit.

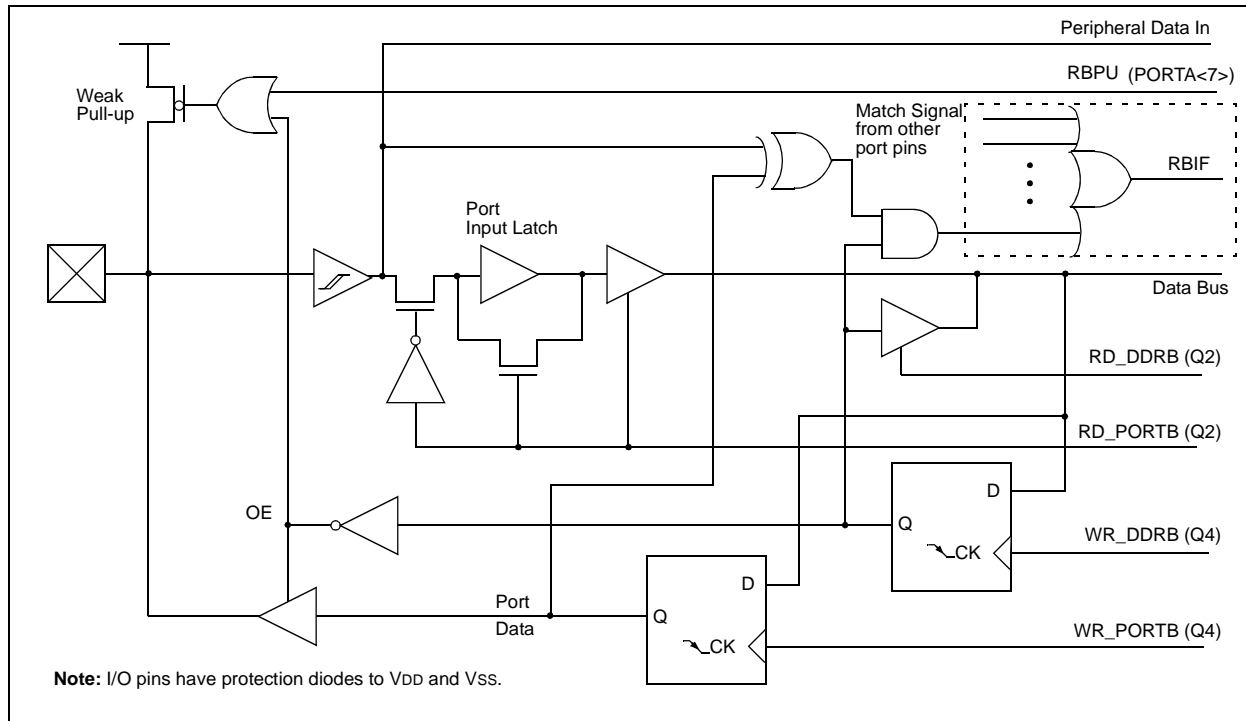
A mismatch condition will continue to set the RBIF bit. Reading, then writing PORTB, will end the mismatch condition and allow the RBIF bit to be cleared.

This interrupt-on-mismatch feature, together with software configurable pull-ups on this port, allows easy interface to a keypad and makes it possible for wake-up on key depression. For an example, refer to Application Note AN552, "Implementing Wake-up on Keystroke."

The interrupt-on-change feature is recommended for wake-up on operations, where PORTB is only used for the interrupt-on-change feature and key depression operations.

**Note:** On a device RESET, the RBIF bit is indeterminate, since the value in the latch may be different than the pin.

**FIGURE 10-5: BLOCK DIAGRAM OF RB5:RB4 AND RB1:RB0 PORT PINS**





## 10.9 PORTJ and DDRJ Registers (PIC17C76X only)

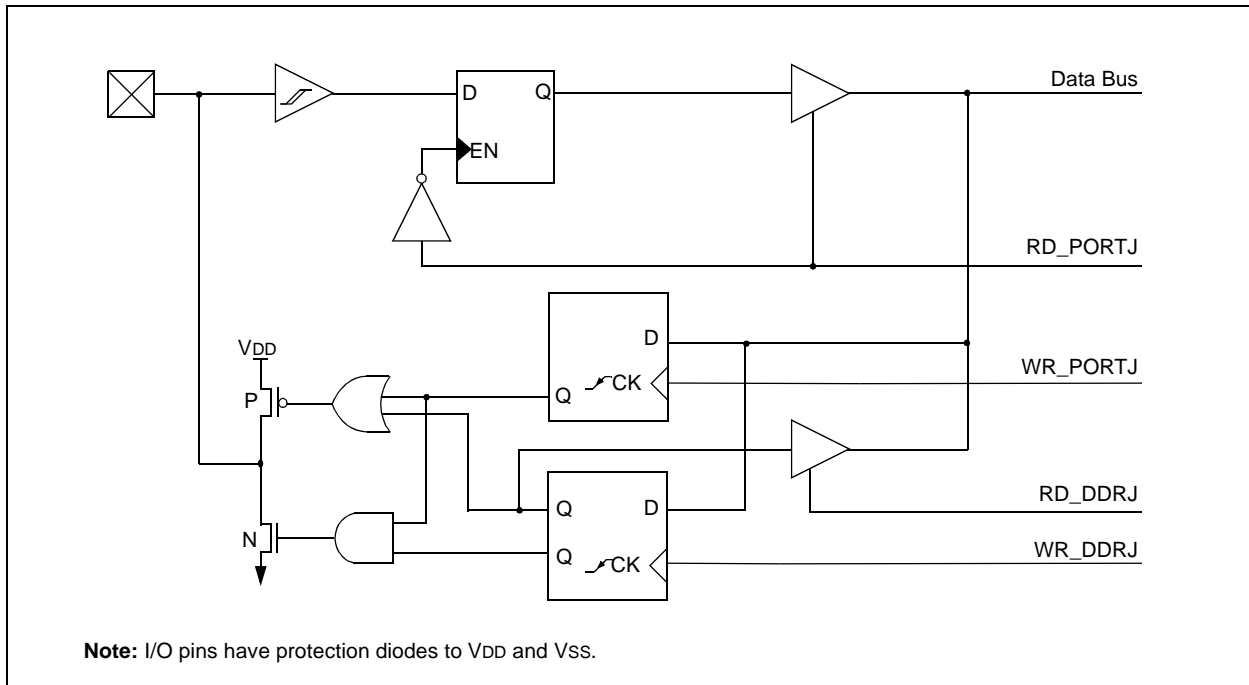
PORTJ is an 8-bit wide, bi-directional port. The corresponding data direction register is DDRJ. A '1' in DDRJ configures the corresponding port pin as an input. A '0' in the DDRJ register configures the corresponding port pin as an output. Reading PORTJ reads the status of the pins, whereas writing to PORTJ will write to the respective port latch.

PORTJ is a general purpose I/O port.

### EXAMPLE 10-9: INITIALIZING PORTJ

```
MOVLB 8      ; Select Bank 8
CLRF  PORTJ, F ; Initialize PORTJ data
               ; latches before setting
               ; the data direction
               ; register
MOVLW  0xCF   ; Value used to initialize
               ; data direction
MOVWF  DDRJ   ; Set RJ<3:0> as inputs
               ; RJ<5:4> as outputs
               ; RJ<7:6> as inputs
```

**FIGURE 10-19: PORTJ BLOCK DIAGRAM**



## 10.10 I/O Programming Considerations

### 10.10.1 BI-DIRECTIONAL I/O PORTS

Any instruction which writes, operates internally as a read, followed by a write operation. For example, the BCF and BSF instructions read the register into the CPU, execute the bit operation and write the result back to the register. Caution must be used when these instructions are applied to a port with both inputs and outputs defined. For example, a BSF operation on bit5 of PORTB, will cause all eight bits of PORTB to be read into the CPU. Then the BSF operation takes place on bit5 and PORTB is written to the output latches. If another bit of PORTB is used as a bi-directional I/O pin (e.g. bit0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and rewritten to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the input mode, no problem occurs. However, if bit0 is switched into output mode later on, the content of the data latch may now be unknown.

Reading a port reads the values of the port pins. Writing to the port register writes the value to the port latch. When using read-modify-write instructions (BCF, BSF, BTG, etc.) on a port, the value of the port pins is read, the desired operation is performed with this value and the value is then written to the port latch.

Example 10-10 shows the possible effect of two sequential read-modify-write instructions on an I/O port.

### EXAMPLE 10-10: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT

```
; Initial PORT settings: PORTB<7:4> Inputs
;                          PORTB<3:0> Outputs
; PORTB<7:6> have pull-ups and are
; not connected to other circuitry
;
;                          PORT latch  PORT pins
;                          -----
;
; BCF  PORTB, 7    ; 01pp pppp   11pp pppp
; BCF  PORTB, 6    ; 10pp pppp   11pp pppp
;
; BCF  DDRB, 7    ; 10pp pppp   11pp pppp
; BCF  DDRB, 6    ; 10pp pppp   10pp pppp
;
; Note that the user may have expected the
; pin values to be 00pp pppp. The 2nd BCF
; caused RB7 to be latched as the pin value
; (High).
```

**Note:** A pin actively outputting a Low or High should not be driven from external devices, in order to change the level on this pin (i.e., “wired-or”, “wired-and”). The resulting high output currents may damage the device.

# PIC17C7XX

## 13.1 Timer1 and Timer2

### 13.1.1 TIMER1, TIMER2 IN 8-BIT MODE

Both Timer1 and Timer2 will operate in 8-bit mode when the T16 bit is clear. These two timers can be independently configured to increment from the internal instruction cycle clock (Tcy), or from an external clock source on the RB4/TCLK12 pin. The timer clock source is configured by the TMRxCS bit (x = 1 for Timer1, or = 2 for Timer2). When TMRxCS is clear, the clock source is internal and increments once every instruction cycle (Fosc/4). When TMRxCS is set, the clock source is the RB4/TCLK12 pin and the counters will increment on every falling edge of the RB4/TCLK12 pin.

The timer increments from 00h until it equals the Period register (PRx). It then resets to 00h at the next increment cycle. The timer interrupt flag is set when the timer is reset. TMR1 and TMR2 have individual interrupt flag bits. The TMR1 interrupt flag bit is latched into TMR1IF and the TMR2 interrupt flag bit is latched into TMR2IF.

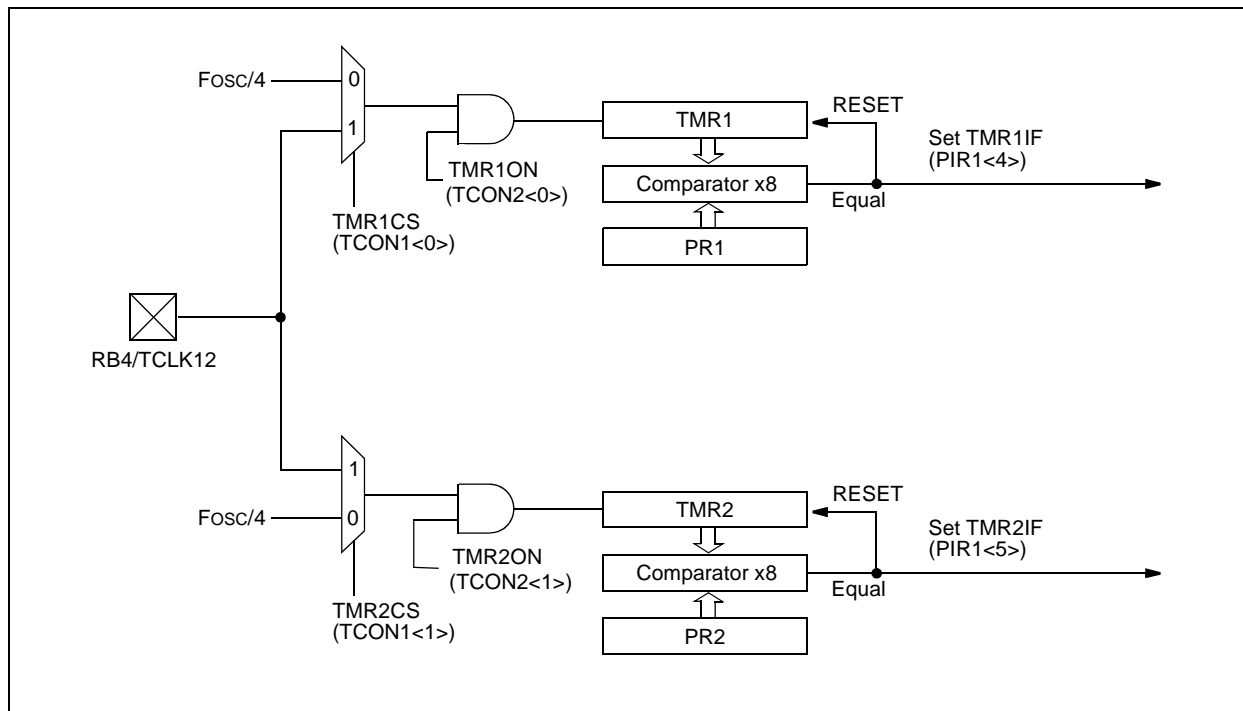
Each timer also has a corresponding interrupt enable bit (TMRxIE). The timer interrupt can be enabled/disabled by setting/clearing this bit. For peripheral interrupts to be enabled, the Peripheral Interrupt Enable bit must be set (PEIE = '1') and global interrupt must be enabled (GLINTD = '0').

The timers can be turned on and off under software control. When the timer on control bit (TMRxON) is set, the timer increments from the clock source. When TMRxON is cleared, the timer is turned off and cannot cause the timer interrupt flag to be set.

#### 13.1.1.1 External Clock Input for Timer1 and Timer2

When TMRxCS is set, the clock source is the RB4/TCLK12 pin, and the counter will increment on every falling edge on the RB4/TCLK12 pin. The TCLK12 input is synchronized with internal phase clocks. This causes a delay from the time a falling edge appears on TCLK12 to the time TMR1 or TMR2 is actually incremented. For the external clock input timing requirements, see the Electrical Specification section.

**FIGURE 13-1: TIMER1 AND TIMER2 IN TWO 8-BIT TIMER/COUNTER MODE**



## 13.1.3.1 PWM Periods

The period of the PWM1 output is determined by Timer1 and its period register (PR1). The period of the PWM2 and PWM3 outputs can be individually software configured to use either Timer1 or Timer2 as the time-base. For PWM2, when TM2PW2 bit (PW2DCL<5>) is clear, the time base is determined by TMR1 and PR1 and when TM2PW2 is set, the time base is determined by Timer2 and PR2. For PWM3, when TM2PW3 bit (PW3DCL<5>) is clear, the time base is determined by TMR1 and PR1, and when TM2PW3 is set, the time base is determined by Timer2 and PR2.

Running two different PWM outputs on two different timers allows different PWM periods. Running all PWMs from Timer1 allows the best use of resources by freeing Timer2 to operate as an 8-bit timer. Timer1 and Timer2 cannot be used as a 16-bit timer if any PWM is being used.

The PWM periods can be calculated as follows:

$$\text{period of PWM1} = [(PR1) + 1] \times 4T_{OSC}$$

$$\text{period of PWM2} = [(PR1) + 1] \times 4T_{OSC} \quad \text{or} \quad [(PR2) + 1] \times 4T_{OSC}$$

$$\text{period of PWM3} = [(PR1) + 1] \times 4T_{OSC} \quad \text{or} \quad [(PR2) + 1] \times 4T_{OSC}$$

The duty cycle of PWMx is determined by the 10-bit value DCx<9:0>. The upper 8-bits are from register PWxDCH and the lower 2-bits are from PWxDCL<7:6> (PWxDCH:PWxDCL<7:6>). Table 13-4 shows the maximum PWM frequency (FPWM), given the value in the period register.

The number of bits of resolution that the PWM can achieve depends on the operation frequency of the device as well as the PWM frequency (FPWM).

Maximum PWM resolution (bits) for a given PWM frequency:

$$= \frac{\log \left( \frac{F_{OSC}}{F_{PWM}} \right)}{\log (2)} \quad \text{bits}$$

where:  $F_{PWM} = 1 / \text{period of PWM}$

The PWMx duty cycle is as follows:

$$\text{PWMx Duty Cycle} = (DCx) \times T_{OSC}$$

where DCx represents the 10-bit value from PWxDCH:PWxDCL.

If  $DCx = 0$ , then the duty cycle is zero. If  $PRx = PWxDCH$ , then the PWM output will be low for one to four Q-clocks (depending on the state of the PWxDCL<7:6> bits). For a duty cycle to be 100%, the PWxDCH value must be greater than the PRx value.

The duty cycle registers for both PWM outputs are double buffered. When the user writes to these registers, they are stored in master latches. When TMR1 (or TMR2) overflows and a new PWM period begins, the master latch values are transferred to the slave latches and the PWMx pin is forced high.

**Note:** For PW1DCH, PW1DCL, PW2DCH, PW2DCL, PW3DCH and PW3DCL registers, a write operation writes to the "master latches", while a read operation reads the "slave latches". As a result, the user may not read back what was just written to the duty cycle registers (until transferred to slave latch).

The user should also avoid any "read-modify-write" operations on the duty cycle registers, such as: `ADDWF PW1DCH`. This may cause duty cycle outputs that are unpredictable.

**TABLE 13-4: PWM FREQUENCY vs. RESOLUTION AT 33 MHz**

PWM Frequency	Frequency (kHz)				
	32.2	64.5	90.66	128.9	515.6
PRx Value	0xFF	0x7F	0x5A	0x3F	0x0F
High Resolution	10-bit	9-bit	8.5-bit	8-bit	6-bit
Standard Resolution	8-bit	7-bit	6.5-bit	6-bit	4-bit

## 13.1.3.2 PWM INTERRUPTS

The PWM modules make use of the TMR1 and/or TMR2 interrupts. A timer interrupt is generated when TMR1 or TMR2 equals its period register and on the following increment is cleared to zero. This interrupt also marks the beginning of a PWM cycle. The user can write new duty cycle values before the timer rollover. The TMR1 interrupt is latched into the TMR1IF bit and the TMR2 interrupt is latched into the TMR2IF bit. These flags must be cleared in software.

# PIC17C7XX

## 15.2.9 I<sup>2</sup>C MASTER MODE START CONDITION TIMING

To initiate a START condition, the user sets the START condition enable bit, SEN (SSPCON2<0>). If the SDA and SCL pins are sampled high, the baud rate generator is reloaded with the contents of SSPADD<6:0> and starts its count. If SCL and SDA are both sampled high when the baud rate generator times out (TBRG), the SDA pin is driven low. The action of the SDA being driven low while SCL is high is the START condition and causes the S bit (SSPSTAT<3>) to be set. Following this, the baud rate generator is reloaded with the contents of SSPADD<6:0> and resumes its count. When the baud rate generator times out (TBRG), the SEN bit (SSPCON2<0>) will be automatically cleared by hardware, the baud rate generator is suspended, leaving the SDA line held low and the START condition is complete.

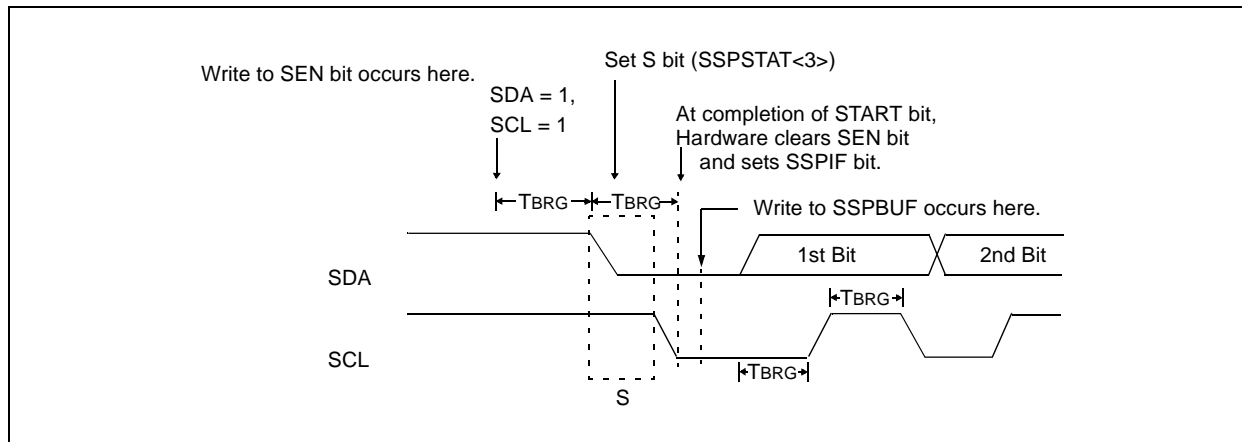
**Note:** If at the beginning of START condition, the SDA and SCL pins are already sampled low, or if during the START condition, the SCL line is sampled low before the SDA line is driven low, a bus collision occurs. The Bus Collision Interrupt Flag (BCLIF) is set, the START condition is aborted and the I<sup>2</sup>C module is reset into its IDLE state.

### 15.2.9.1 WCOL Status Flag

If the user writes the SSPBUF when a START sequence is in progress, then WCOL is set and the contents of the buffer are unchanged (the write doesn't occur).

**Note:** Because queueing of events is not allowed, writing to the lower 5 bits of SSPCON2 is disabled until the START condition is complete.

**FIGURE 15-20: FIRST START BIT TIMING**



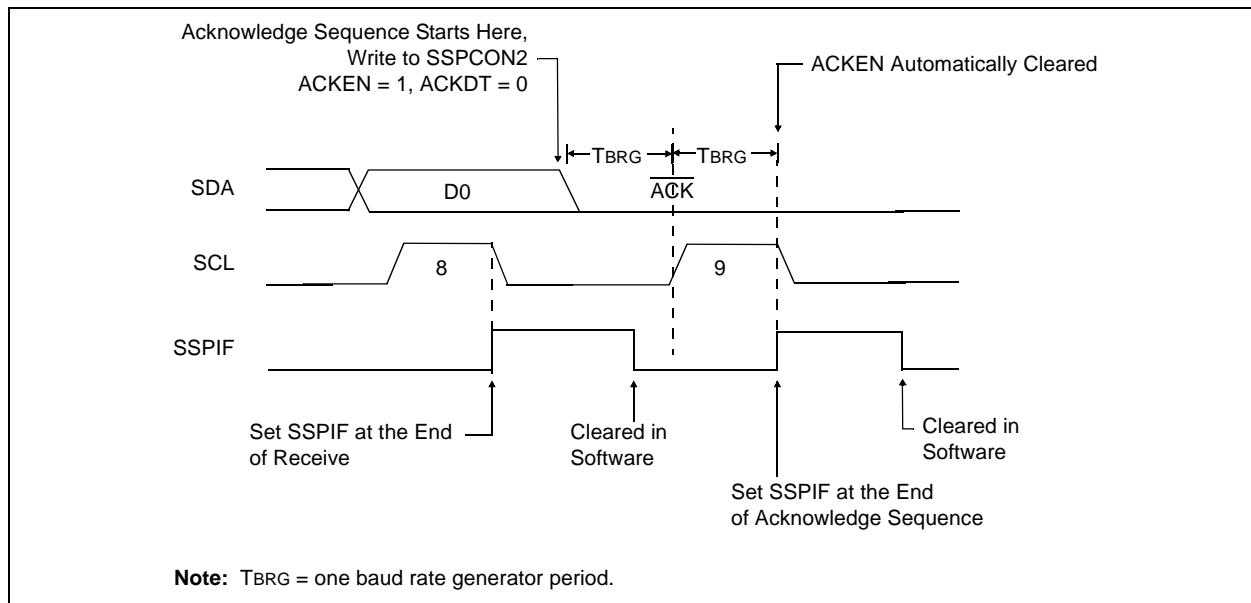
## 15.2.13 ACKNOWLEDGE SEQUENCE TIMING

An acknowledge sequence is enabled by setting the acknowledge sequence enable bit, ACKEN (SSPCON2<4>). When this bit is set, the SCL pin is pulled low and the contents of the acknowledge data bit is presented on the SDA pin. If the user wishes to generate an acknowledge, then the ACKDT bit should be cleared. If not, the user should set the ACKDT bit before starting an acknowledge sequence. The baud rate generator then counts for one rollover period (TBRG), and the SCL pin is de-asserted (pulled high). When the SCL pin is sampled high (clock arbitration), the baud rate generator counts for TBRG. The SCL pin is then pulled low. Following this, the ACKEN bit is automatically cleared, the baud rate generator is turned off and the SSP module then goes into IDLE mode (Figure 15-29).

### 15.2.13.1 WCOL Status Flag

If the user writes the SSPBUF when an acknowledge sequence is in progress, then WCOL is set and the contents of the buffer are unchanged (the write doesn't occur).

**FIGURE 15-29: ACKNOWLEDGE SEQUENCE WAVEFORM**



## 15.3 Connection Considerations for I<sup>2</sup>C Bus

For standard mode I<sup>2</sup>C bus devices, the values of resistors  $R_p$   $R_s$  in Figure 15-42 depends on the following parameters:

- Supply voltage
- Bus capacitance
- Number of connected devices (input current + leakage current)

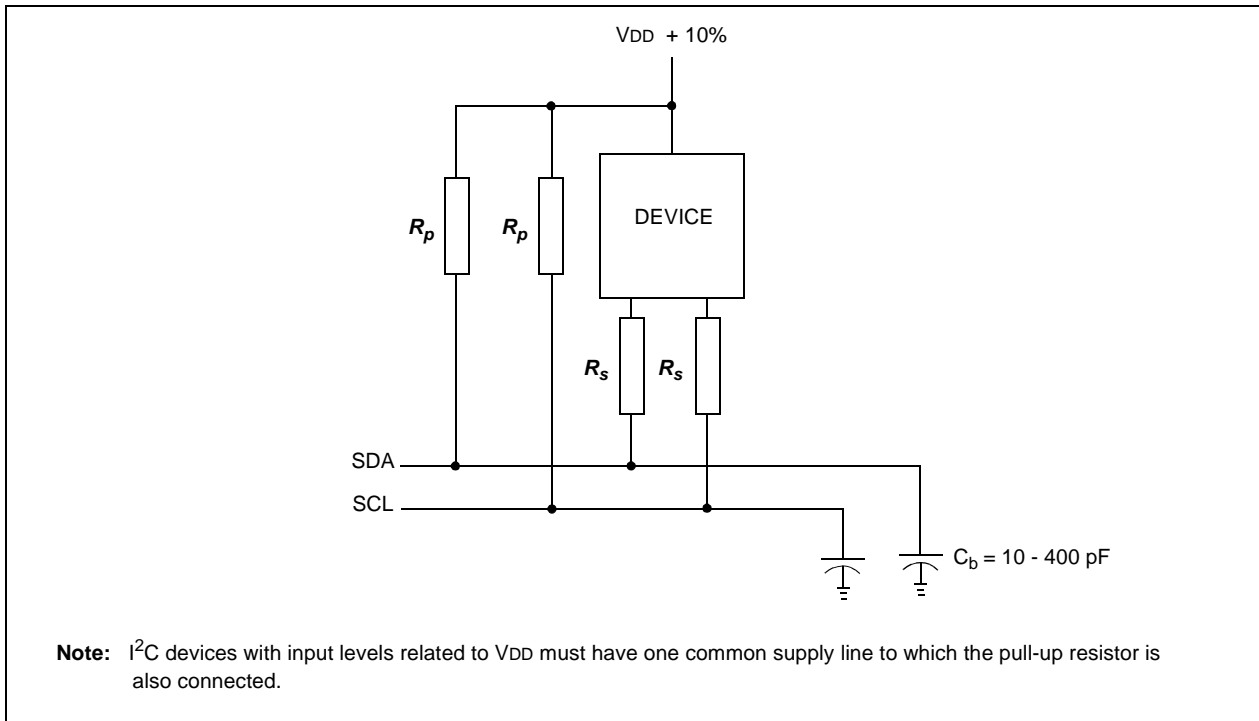
The supply voltage limits the minimum value of resistor  $R_p$  due to the specified minimum sink current of 3 mA at  $V_{OL\ max} = 0.4V$  for the specified output stages. For

example, with a supply voltage of  $V_{DD} = 5V \pm 10\%$  and  $V_{OL\ max} = 0.4V$  at 3 mA,  $R_p\ min = (5.5-0.4)/0.003 = 1.7\ k\Omega$ .  $V_{DD}$  as a function of  $R_p$  is shown in Figure 15-42. The desired noise margin of 0.1  $V_{DD}$  for the low level, limits the maximum value of  $R_s$ . Series resistors are optional and used to improve ESD susceptibility.

The bus capacitance is the total capacitance of wire, connections and pins. This capacitance limits the maximum value of  $R_p$  due to the specified rise time (Figure 15-42).

The SMP bit is the slew rate control enabled bit. This bit is in the SSPSTAT register and controls the slew rate of the I/O pins when in I<sup>2</sup>C mode (master or slave).

**FIGURE 15-42: SAMPLE DEVICE CONFIGURATION FOR I<sup>2</sup>C BUS**



## 17.4 Power-down Mode (SLEEP)

The Power-down mode is entered by executing a `SLEEP` instruction. This clears the Watchdog Timer and postscale (if enabled). The  $\overline{PD}$  bit is cleared and the  $\overline{TO}$  bit is set (in the `CPUSTA` register). In SLEEP mode, the oscillator driver is turned off. The I/O ports maintain their status (driving high, low, or hi-impedance input).

The  $\overline{MCLR}/VPP$  pin must be at a logic high level ( $V_{IHMC}$ ). A WDT time-out RESET does not drive the  $\overline{MCLR}/VPP$  pin low.

### 17.4.1 WAKE-UP FROM SLEEP

The device can wake-up from SLEEP through one of the following events:

- Power-on Reset
- Brown-out Reset
- External RESET input on  $\overline{MCLR}/VPP$  pin
- WDT Reset (if WDT was enabled)
- Interrupt from  $RA0/INT$  pin, RB port change,  $T0CKI$  interrupt, or some peripheral interrupts

The following peripheral interrupts can wake the device from SLEEP:

- Capture interrupts
- USART synchronous slave transmit interrupts
- USART synchronous slave receive interrupts
- A/D conversion complete
- SPI slave transmit/receive complete
- I<sup>2</sup>C slave receive

Other peripherals cannot generate interrupts since during SLEEP, no on-chip Q clocks are present.

Any RESET event will cause a device RESET. Any interrupt event is considered a continuation of program execution. The  $\overline{TO}$  and  $\overline{PD}$  bits in the `CPUSTA` register can be used to determine the cause of a device RESET. The  $\overline{PD}$  bit, which is set on power-up, is cleared when SLEEP is invoked. The  $\overline{TO}$  bit is cleared if WDT time-out occurred (and caused a RESET).

When the `SLEEP` instruction is being executed, the next instruction (`PC + 1`) is pre-fetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up is regardless of the state of the `GLINTD` bit. If the `GLINTD` bit is set (disabled), the device continues execution at the instruction after the `SLEEP` instruction. If the `GLINTD` bit is clear (enabled), the device executes the instruction after the `SLEEP` instruction and then branches to the interrupt vector address. In cases where the execution of the instruction following SLEEP is not desirable, the user should have a `NOP` after the `SLEEP` instruction.

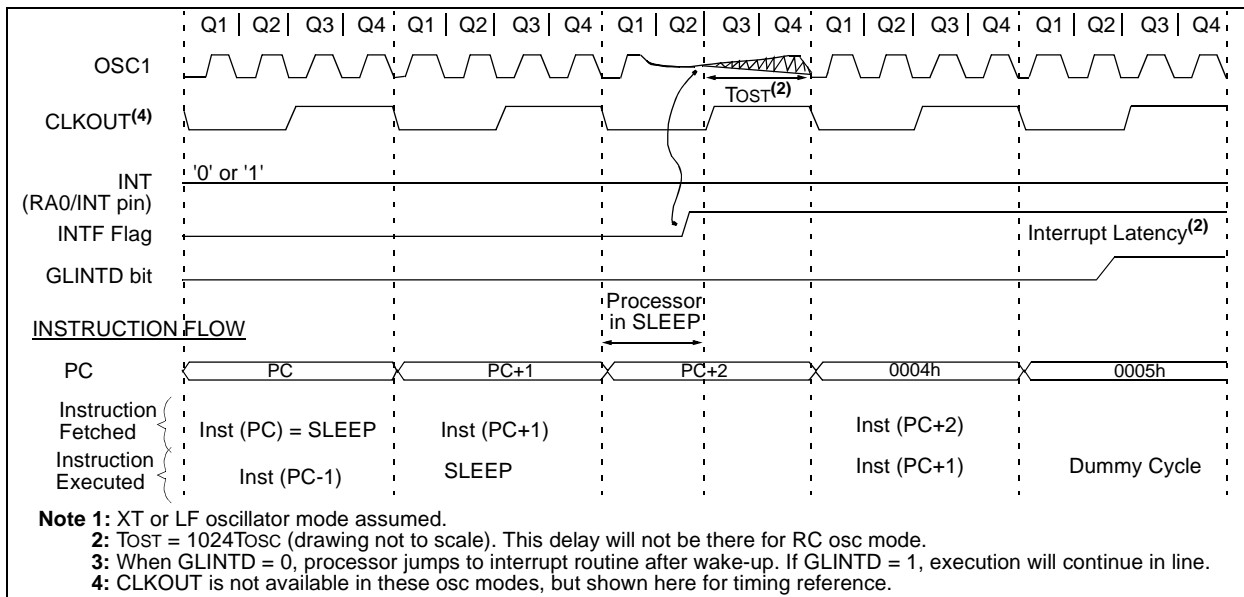
**Note:** If the global interrupt is disabled (`GLINTD` is set), but any interrupt source has both its interrupt enable bit and the corresponding interrupt flag bit set, the device will immediately wake-up from SLEEP. The  $\overline{TO}$  bit is set and the  $\overline{PD}$  bit is cleared.

The WDT is cleared when the device wakes from SLEEP, regardless of the source of wake-up.

#### 17.4.1.1 Wake-up Delay

When the oscillator type is configured in XT or LF mode, the Oscillator Start-up Timer (OST) is activated on wake-up. The OST will keep the device in RESET for  $1024T_{osc}$ . This needs to be taken into account when considering the interrupt response time when coming out of SLEEP.

**FIGURE 17-2: WAKE-UP FROM SLEEP THROUGH INTERRUPT**





XORLW	Exclusive OR Literal with WREG			
Syntax:	[ <i>label</i> ] XORLW k			
Operands:	$0 \leq k \leq 255$			
Operation:	(WREG) .XOR. k $\rightarrow$ (WREG)			
Status Affected:	Z			
Encoding:	1011	0100	kkkk	kkkk
Description:	The contents of WREG are XOR'ed with the 8-bit literal 'k'. The result is placed in WREG.			
Words:	1			
Cycles:	1			
Q Cycle Activity:				
	Q1	Q2	Q3	Q4
	Decode	Read literal 'k'	Process Data	Write to WREG

**Example:** XORLW 0xAF

Before Instruction

WREG = 0xB5

After Instruction

WREG = 0x1A

XORWF		Exclusive OR WREG with f						
Syntax:	[ <i>label</i> ] XORWF    f,d							
Operands:	0 ≤ f ≤ 255 d ∈ [0,1]							
Operation:	(WREG) .XOR. (f) → (dest)							
Status Affected:	Z							
Encoding:	<table><tr><td>0000</td><td>110d</td><td>ffff</td><td>ffff</td></tr></table>				0000	110d	ffff	ffff
0000	110d	ffff	ffff					
Description:	Exclusive OR the contents of WREG with register 'f'. If 'd' is 0, the result is stored in WREG. If 'd' is 1, the result is stored back in the register 'f'.							
Words:	1							
Cycles:	1							
Q Cycle Activity:								
	Q1	Q2	Q3	Q4				
	Decode	Read register 'f'	Process Data	Write to destination				

**Example:** XORWF REG, 1

Before Instruction

REG = 0xAF 1010 1111

WREG = 0xB5 1011 0101

After Instruction

REG = 0x1A 0001 1010

WREG = 0xB5

## 19.0 DEVELOPMENT SUPPORT

The PIC® microcontrollers are supported with a full range of hardware and software development tools:

- Integrated Development Environment
  - MPLAB® IDE Software
- Assemblers/Compilers/Linkers
  - MPASM™ Assembler
  - MPLAB C17 and MPLAB C18 C Compilers
  - MPLINK™ Object Linker/  
MPLIB™ Object Librarian
- Simulators
  - MPLAB SIM Software Simulator
- Emulators
  - MPLAB ICE 2000 In-Circuit Emulator
  - ICEPIC™ In-Circuit Emulator
- In-Circuit Debugger
  - MPLAB ICD for PIC16F87X
- Device Programmers
  - PRO MATE® II Universal Device Programmer
  - PICSTART® Plus Entry-Level Development Programmer
- Low Cost Demonstration Boards
  - PICDEM™ 1 Demonstration Board
  - PICDEM 2 Demonstration Board
  - PICDEM 3 Demonstration Board
  - PICDEM 17 Demonstration Board
  - KEELOQ® Demonstration Board

### 19.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8-bit microcontroller market. The MPLAB IDE is a Windows®-based application that contains:

- An interface to debugging tools
  - simulator
  - programmer (sold separately)
  - emulator (sold separately)
  - in-circuit debugger (sold separately)
- A full-featured editor
- A project manager
- Customizable toolbar and key mapping
- A status bar
- On-line help

The MPLAB IDE allows you to:

- Edit your source files (either assembly or 'C')
- One touch assemble (or compile) and download to PIC MCU emulator and simulator tools (automatically updates all project information)
- Debug using:
  - source files
  - absolute listing file
  - machine code

The ability to use MPLAB IDE with multiple debugging tools allows users to easily switch from the cost-effective simulator to a full-featured emulator with minimal retraining.

### 19.2 MPASM Assembler

The MPASM assembler is a full-featured universal macro assembler for all PIC MCU's.

The MPASM assembler has a command line interface and a Windows shell. It can be used as a stand-alone application on a Windows 3.x or greater system, or it can be used through MPLAB IDE. The MPASM assembler generates relocatable object files for the MPLINK object linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, an absolute LST file that contains source lines and generated machine code, and a COD file for debugging.

The MPASM assembler features include:

- Integration into MPLAB IDE projects.
- User-defined macros to streamline assembly code.
- Conditional assembly for multi-purpose source files.
- Directives that allow complete control over the assembly process.

### 19.3 MPLAB C17 and MPLAB C18 C Compilers

The MPLAB C17 and MPLAB C18 Code Development Systems are complete ANSI 'C' compilers for Microchip's PIC17CXXX and PIC18CXXX family of microcontrollers, respectively. These compilers provide powerful integration capabilities and ease of use not found with other compilers.

For easier source level debugging, the compilers provide symbol information that is compatible with the MPLAB IDE memory display.

## 19.8 MPLAB ICD In-Circuit Debugger

Microchip's In-Circuit Debugger, MPLAB ICD, is a powerful, low cost, run-time development tool. This tool is based on the FLASH PIC16F87X and can be used to develop for this and other PIC microcontrollers from the PIC16CXXX family. The MPLAB ICD utilizes the in-circuit debugging capability built into the PIC16F87X. This feature, along with Microchip's In-Circuit Serial Programming™ protocol, offers cost-effective in-circuit FLASH debugging from the graphical user interface of the MPLAB Integrated Development Environment. This enables a designer to develop and debug source code by watching variables, single-stepping and setting break points. Running at full speed enables testing hardware in real-time.

## 19.9 PRO MATE II Universal Device Programmer

The PRO MATE II universal device programmer is a full-featured programmer, capable of operating in stand-alone mode, as well as PC-hosted mode. The PRO MATE II device programmer is CE compliant.

The PRO MATE II device programmer has programmable VDD and VPP supplies, which allow it to verify programmed memory at VDD min and VDD max for maximum reliability. It has an LCD display for instructions and error messages, keys to enter commands and a modular detachable socket assembly to support various package types. In stand-alone mode, the PRO MATE II device programmer can read, verify, or program PIC MCU devices. It can also set code protection in this mode.

## 19.10 PICSTART Plus Entry Level Development Programmer

The PICSTART Plus development programmer is an easy-to-use, low cost, prototype programmer. It connects to the PC via a COM (RS-232) port. MPLAB Integrated Development Environment software makes using the programmer simple and efficient.

The PICSTART Plus development programmer supports all PIC devices with up to 40 pins. Larger pin count devices, such as the PIC16C92X and PIC17C76X, may be supported with an adapter socket. The PICSTART Plus development programmer is CE compliant.

## 19.11 PICDEM 1 Low Cost PIC MCU Demonstration Board

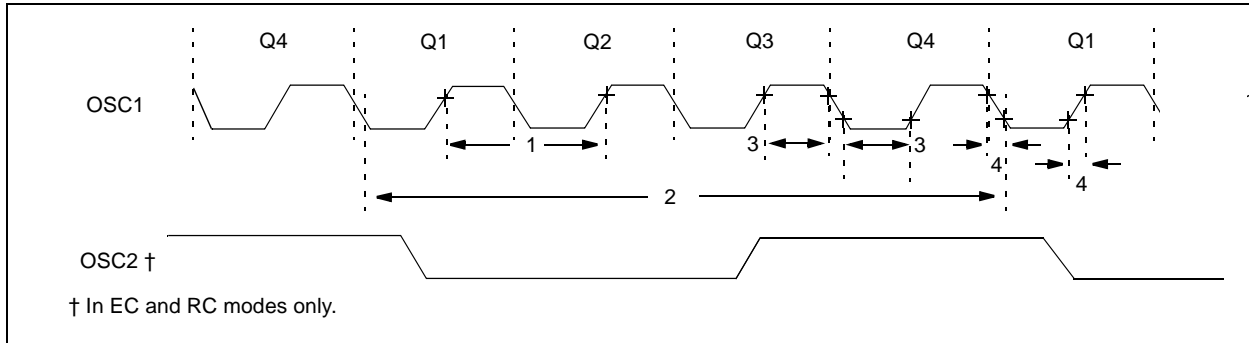
The PICDEM 1 demonstration board is a simple board which demonstrates the capabilities of several of Microchip's microcontrollers. The microcontrollers supported are: PIC16C5X (PIC16C54 to PIC16C58A), PIC16C61, PIC16C62X, PIC16C71, PIC16C8X, PIC17C42, PIC17C43 and PIC17C44. All necessary hardware and software is included to run basic demo programs. The user can program the sample microcontrollers provided with the PICDEM 1 demonstration board on a PRO MATE II device programmer, or a PICSTART Plus development programmer, and easily test firmware. The user can also connect the PICDEM 1 demonstration board to the MPLAB ICE in-circuit emulator and download the firmware to the emulator for testing. A prototype area is available for the user to build some additional hardware and connect it to the microcontroller socket(s). Some of the features include an RS-232 interface, a potentiometer for simulated analog input, push button switches and eight LEDs connected to PORTB.

## 19.12 PICDEM 2 Low Cost PIC16CXX Demonstration Board

The PICDEM 2 demonstration board is a simple demonstration board that supports the PIC16C62, PIC16C64, PIC16C65, PIC16C73 and PIC16C74 microcontrollers. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM 2 demonstration board on a PRO MATE II device programmer, or a PICSTART Plus development programmer, and easily test firmware. The MPLAB ICE in-circuit emulator may also be used with the PICDEM 2 demonstration board to test firmware. A prototype area has been provided to the user for adding additional hardware and connecting it to the microcontroller socket(s). Some of the features include a RS-232 interface, push button switches, a potentiometer for simulated analog input, a serial EEPROM to demonstrate usage of the I<sup>2</sup>C™ bus and separate headers for connection to an LCD module and a keypad.

## 20.4 Timing Diagrams and Specifications

**FIGURE 20-6: EXTERNAL CLOCK TIMING**



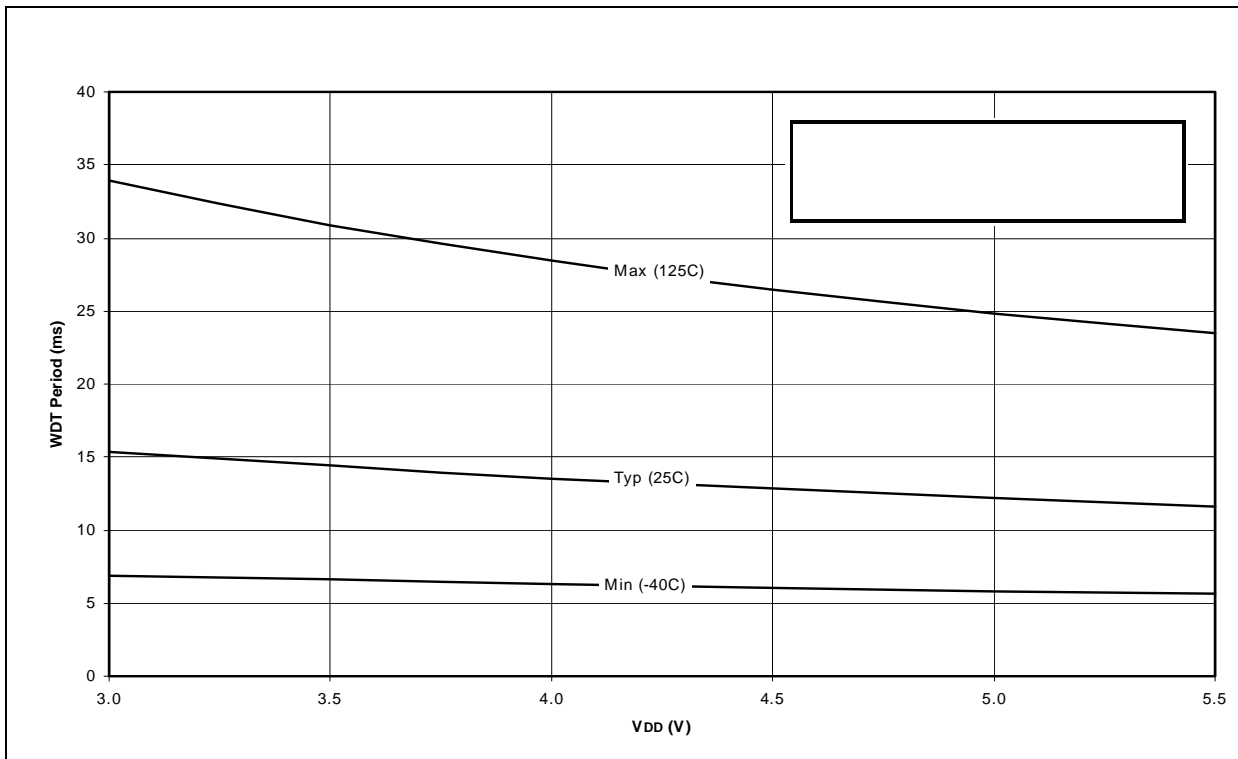
**TABLE 20-1: EXTERNAL CLOCK TIMING REQUIREMENTS**

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	FOSC	<b>External CLKIN Frequency (Note 1)</b>	DC	—	8	MHz	EC osc mode - 08 devices (8 MHz devices)
			DC	—	16	MHz	- 16 devices (16 MHz devices)
			DC	—	33	MHz	- 33 devices (33 MHz devices)
		<b>Oscillator Frequency (Note 1)</b>	DC	—	4	MHz	RC osc mode
			2	—	8	MHz	XT osc mode - 08 devices (8 MHz devices)
			2	—	16	MHz	- 16 devices (16 MHz devices)
			2	—	33	MHz	- 33 devices (33 MHz devices)
			DC	—	2	MHz	LF osc mode
1	TOSC	<b>External CLKIN Period (Note 1)</b>	125	—	—	ns	EC osc mode - 08 devices (8 MHz devices)
			62.5	—	—	ns	- 16 devices (16 MHz devices)
			30.3	—	—	ns	- 33 devices (33 MHz devices)
		<b>Oscillator Period (Note 1)</b>	250	—	—	ns	RC osc mode
			125	—	1,000	ns	XT osc mode - 08 devices (8 MHz devices)
			62.5	—	1,000	ns	- 16 devices (16 MHz devices)
			30.3	—	1,000	ns	- 33 devices (33 MHz devices)
			500	—	—	ns	LF osc mode
2	Tcy	<b>Instruction Cycle Time (Note 1)</b>	121.2	4/FOSC	DC	ns	
3	TosL, TosH	<b>Clock in (OSC1) High or Low Time</b>	10	—	—	ns	EC oscillator
4	TosR, TosF	<b>Clock in (OSC1) Rise or Fall Time</b>	—	—	5	ns	EC oscillator

† Data in "Typ" column is at 5V, 25°C unless otherwise stated.

**Note 1:** Instruction cycle period (Tcy) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKIN pin. When an external clock input is used, the "max." cycle time limit is "DC" (no clock) for all devices.

**FIGURE 21-15: TYPICAL, MINIMUM AND MAXIMUM WDT PERIOD vs.  $V_{DD}$  (-40°C TO +125°C)**



**FIGURE 21-16: TYPICAL WDT PERIOD vs.  $V_{DD}$  OVER TEMPERATURE (-40°C TO +125°C)**

