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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	PIC
Core Size	8-Bit
Speed	8MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	50
Program Memory Size	16KB (8K x 16)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	678 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	68-LCC (J-Lead)
Supplier Device Package	68-PLCC (24.23x24.23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic17lc752t-08i-l

TABLE 1-1: PIC17CXXX FAMILY OF DEVICES

Features		PIC17C42A	PIC17C43	PIC17C44	PIC17C752	PIC17C756A	PIC17C762	PIC17C766
Maximum Frequency of Operation		33 MHz	33 MHz	33 MHz	33 MHz	33 MHz	33 MHz	33 MHz
Operating Voltage Range		2.5 - 6.0V	2.5 - 6.0V	2.5 - 6.0V	3.0 - 5.5V	3.0 - 5.5V	3.0 - 5.5V	3.0 - 5.5V
Program Memory (x16)	(EPROM)	2 K	4 K	8 K	8 K	16 K	8 K	16 K
	(ROM)	—	—	—	—	—	—	—
Data Memory (bytes)		232	454	454	678	902	678	902
Hardware Multiplier (8 x 8)		Yes	Yes	Yes	Yes	Yes	Yes	Yes
Timer0 (16-bit + 8-bit postscaler)		Yes	Yes	Yes	Yes	Yes	Yes	Yes
Timer1 (8-bit)		Yes	Yes	Yes	Yes	Yes	Yes	Yes
Timer2 (8-bit)		Yes	Yes	Yes	Yes	Yes	Yes	Yes
Timer3 (16-bit)		Yes	Yes	Yes	Yes	Yes	Yes	Yes
Capture inputs (16-bit)		2	2	2	4	4	4	4
PWM outputs (up to 10-bit)		2	2	2	3	3	3	3
USART/SCI		1	1	1	2	2	2	2
A/D channels (10-bit)		—	—	—	12	12	16	16
SSP (SPI/I^2C w/Master mode)		—	—	—	Yes	Yes	Yes	Yes
Power-on Reset		Yes	Yes	Yes	Yes	Yes	Yes	Yes
Watchdog Timer		Yes	Yes	Yes	Yes	Yes	Yes	Yes
External Interrupts		Yes	Yes	Yes	Yes	Yes	Yes	Yes
Interrupt Sources		11	11	11	18	18	18	18
Code Protect		Yes	Yes	Yes	Yes	Yes	Yes	Yes
Brown-out Reset		—	—	—	Yes	Yes	Yes	Yes
In-Circuit Serial Programming		—	—	—	Yes	Yes	Yes	Yes
I/O Pins		33	33	33	50	50	66	66
I/O High Current Capability	Source	25 mA	25 mA	25 mA	25 mA	25 mA	25 mA	25 mA
	Sink	25 mA(1)	25 mA(1)	25 mA(1)	25 mA(1)	25 mA(1)	25 mA(1)	25 mA(1)
Package Types		40-pin DIP 44-pin PLCC 44-pin MQFP 44-pin TQFP	40-pin DIP 44-pin PLCC 44-pin MQFP 44-pin TQFP	40-pin DIP 44-pin PLCC 44-pin MQFP 44-pin TQFP	64-pin TQFP 68-pin PLCC	64-pin TQFP 68-pin PLCC	80-pin TQFP 84-pin PLCC	80-pin TQFP 84-pin PLCC

Note 1: Pins RA2 and RA3 can sink up to 60 mA.

6.0 INTERRUPTS

PIC17C7XX devices have 18 sources of interrupt:

- External interrupt from the RA0/INT pin
- Change on RB7:RB0 pins
- TMR0 Overflow
- TMR1 Overflow
- TMR2 Overflow
- TMR3 Overflow
- USART1 Transmit buffer empty
- USART1 Receive buffer full
- USART2 Transmit buffer empty
- USART2 Receive buffer full
- SSP Interrupt
- SSP I^2C bus collision interrupt
- A/D conversion complete
- Capture1
- Capture2
- Capture3
- Capture4
- T0CKI edge occurred

There are six registers used in the control and status of interrupts. These are:

- CPUSTA
- INTSTA
- PIE1
- PIR1
- PIE2
- PIR2

The CPUSTA register contains the GLINTD bit. This is the Global Interrupt Disable bit. When this bit is set, all interrupts are disabled. This bit is part of the controller core functionality and is described in the Section 6.4.

When an interrupt is responded to, the GLINTD bit is automatically set to disable any further interrupts, the return address is pushed onto the stack and the PC is loaded with the interrupt vector address. There are four interrupt vectors. Each vector address is for a specific interrupt source (except the peripheral interrupts, which all vector to the same address). These sources are:

- External interrupt from the RA0/INT pin
- TMR0 Overflow
- T0CKI edge occurred
- Any peripheral interrupt

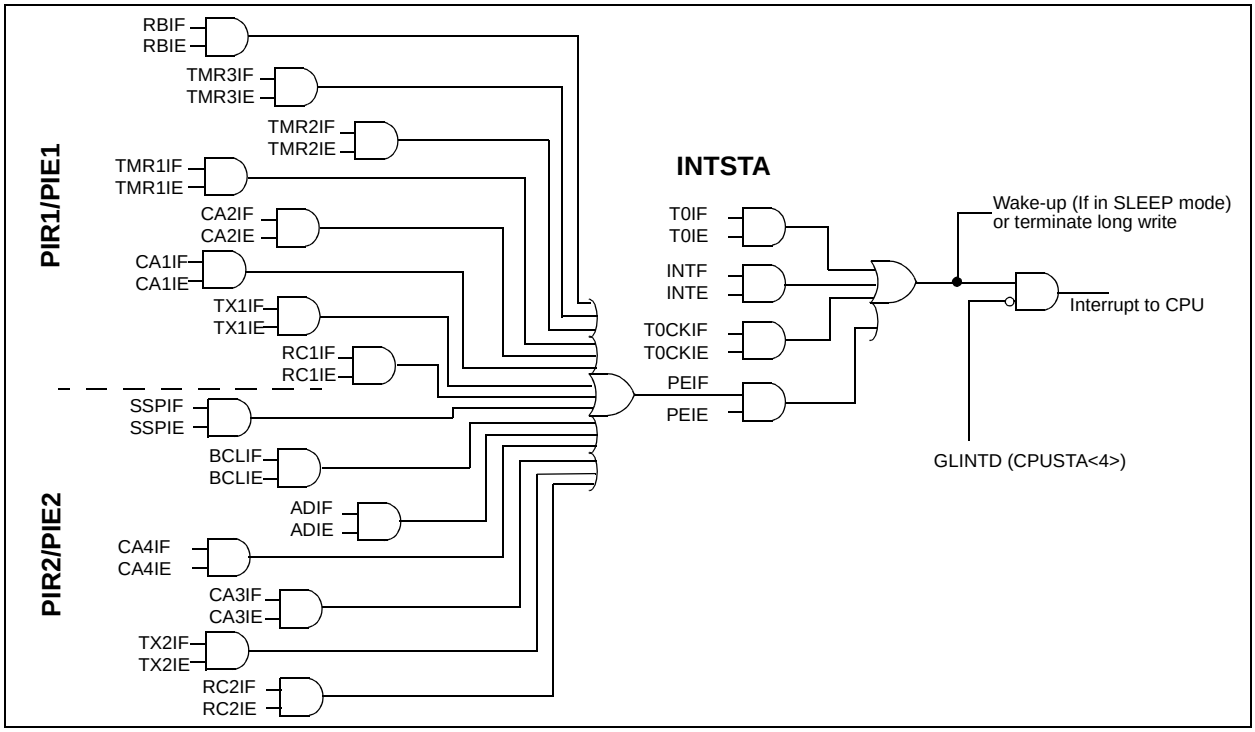
When program execution vectors to one of these interrupt vector addresses (except for the peripheral interrupts), the interrupt flag bit is automatically cleared. Vectoring to the peripheral interrupt vector address does not automatically clear the source of the interrupt. In the peripheral Interrupt Service Routine, the source(s) of the interrupt can be determined by testing the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid infinite interrupt requests.

When an interrupt condition is met, that individual interrupt flag bit will be set, regardless of the status of its corresponding mask bit or the GLINTD bit.

For external interrupt events, there will be an interrupt latency. For two-cycle instructions, the latency could be one instruction cycle longer.

The “return from interrupt” instruction, `RETFIE`, can be used to mark the end of the Interrupt Service Routine. When this instruction is executed, the stack is “POPed” and the GLINTD bit is cleared (to re-enable interrupts).

FIGURE 6-1: INTERRUPT LOGIC



REGISTER 6-3: PIE2 REGISTER (ADDRESS: 11h, BANK 4)

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
SSPIE	BCLIE	ADIE	—	CA4IE	CA3IE	TX2IE	RC2IE
bit 7							bit 0

bit 7 **SSPIE**: Synchronous Serial Port Interrupt Enable bit
1 = Enable SSP interrupt
0 = Disable SSP interrupt

bit 6 **BCLIE**: Bus Collision Interrupt Enable bit
1 = Enable bus collision interrupt
0 = Disable bus collision interrupt

bit 5 **ADIE**: A/D Module Interrupt Enable bit
1 = Enable A/D module interrupt
0 = Disable A/D module interrupt

bit 4 **Unimplemented:** Read as '0'

bit 3 **CA4IE**: Capture4 Interrupt Enable bit
1 = Enable Capture4 interrupt
0 = Disable Capture4 interrupt

bit 2 **CA3IE**: Capture3 Interrupt Enable bit
1 = Enable Capture3 interrupt
0 = Disable Capture3 interrupt

bit 1 **TX2IE**: USART2 Transmit Interrupt Enable bit
1 = Enable USART2 Transmit buffer empty interrupt
0 = Disable USART2 Transmit buffer empty interrupt

bit 0 **RC2IE**: USART2 Receive Interrupt Enable bit
1 = Enable USART2 Receive buffer full interrupt
0 = Disable USART2 Receive buffer full interrupt

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR Reset	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

REGISTER 6-5: PIR2 REGISTER (ADDRESS: 10h, BANK 4)

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R-1	R-0
SSPIF	BCLIF	ADIF	—	CA4IF	CA3IF	TX2IF	RC2IF
bit 7							bit 0

bit 7 **SSPIF**: Synchronous Serial Port (SSP) Interrupt Flag bit
1 = The SSP interrupt condition has occurred and must be cleared in software before returning from the Interrupt Service Routine. The conditions that will set this bit are:

SPI:
A transmission/reception has taken place.

I^2C Slave/Master:
A transmission/reception has taken place.

I^2C Master:
The initiated START condition was completed by the SSP module.
The initiated STOP condition was completed by the SSP module.
The initiated Restart condition was completed by the SSP module.
The initiated Acknowledge condition was completed by the SSP module.
A START condition occurred while the SSP module was idle (Multi-master system).
A STOP condition occurred while the SSP module was idle (Multi-master system).

0 = An SSP interrupt condition has NOT occurred

bit 6 **BCLIF**: Bus Collision Interrupt Flag bit
1 = A bus collision has occurred in the SSP, when configured for I^2C Master mode
0 = No bus collision has occurred

bit 5 **ADIF**: A/D Module Interrupt Flag bit
1 = An A/D conversion is complete
0 = An A/D conversion is not complete

bit 4 **Unimplemented**: Read as '0'

bit 3 **CA4IF**: Capture4 Interrupt Flag bit
1 = Capture event occurred on RE3/CAP4 pin
0 = Capture event did not occur on RE3/CAP4 pin

bit 2 **CA3IF**: Capture3 Interrupt Flag bit
1 = Capture event occurred on RG4/CAP3 pin
0 = Capture event did not occur on RG4/CAP3 pin

bit 1 **TX2IF**:USART2 Transmit Interrupt Flag bit (state controlled by hardware)
1 = USART2 Transmit buffer is empty
0 = USART2 Transmit buffer is full

bit 0 **RC2IF**: USART2 Receive Interrupt Flag bit (state controlled by hardware)
1 = USART2 Receive buffer is full
0 = USART2 Receive buffer is empty

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
- n = Value at POR Reset	’1’ = Bit is set	’0’ = Bit is cleared	x = Bit is unknown

8.1 Table Writes to Internal Memory

A table write operation to internal memory causes a long write operation. The long write is necessary for programming the internal EPROM. Instruction execution is halted while in a long write cycle. The long write will be terminated by any enabled interrupt. To ensure that the EPROM location has been well programmed, a minimum programming time is required (see specification #D114). Having only one interrupt enabled to terminate the long write ensures that no unintentional interrupts will prematurely terminate the long write.

The sequence of events for programming an internal program memory location should be:

1. Disable all interrupt sources, except the source to terminate EPROM program write.
2. Raise $\overline{MCLR}/V_{PP}$ pin to the programming voltage.
3. Clear the WDT.
4. Do the table write. The interrupt will terminate the long write.
5. Verify the memory location (table read).

Note 1: Programming requirements must be met. See timing specification in electrical specifications for the desired device. Violating these specifications (including temperature) may result in EPROM locations that are not fully programmed and may lose their state over time.

2: If the V_{PP} requirement is not met, the table write is a 2-cycle write and the program memory is unchanged.

8.1.1 TERMINATING LONG WRITES

An interrupt source or RESET are the only events that terminate a long write operation. Terminating the long write from an interrupt source requires that the interrupt enable and flag bits are set. The GLINTD bit only enables the vectoring to the interrupt address.

If the T0CKI, RA0/INT, or TMR0 interrupt source is used to terminate the long write, the interrupt flag of the highest priority enabled interrupt, will terminate the long write and automatically be cleared.

Note 1: If an interrupt is pending, the `TABLWT` is aborted (a `NOP` is executed). The highest priority pending interrupt, from the T0CKI, RA0/INT, or TMR0 sources that is enabled, has its flag cleared.

2: If the interrupt is not being used for the program write timing, the interrupt should be disabled. This will ensure that the interrupt is not lost, nor will it terminate the long write prematurely.

If a peripheral interrupt source is used to terminate the long write, the interrupt enable and flag bits must be set. The interrupt flag will not be automatically cleared upon the vectoring to the interrupt vector address.

The GLINTD bit determines whether the program will branch to the interrupt vector when the long write is terminated. If GLINTD is clear, the program will vector, if GLINTD is set, the program will not vector to the interrupt address.

TABLE 8-1: INTERRUPT - TABLE WRITE INTERACTION

Interrupt Source	GLINTD	Enable Bit	Flag Bit	Action
RA0/INT, TMR0, T0CKI	0	1	1	Terminate long table write (to internal program memory), branch to interrupt vector (branch clears flag bit).
	0	1	0	None.
	1	0	x	None.
	1	1	1	Terminate long table write, do not branch to interrupt vector (flag is automatically cleared).
Peripheral	0	1	1	Terminate long table write, branch to interrupt vector.
	0	1	0	None.
	1	0	x	None.
	1	1	1	Terminate long table write, do not branch to interrupt vector (flag remains set).

TABLE 10-7: PORTD FUNCTIONS

Name	Bit	Buffer Type	Function
RD0/AD8	bit0	TTL	Input/output or system bus address/data pin.
RD1/AD9	bit1	TTL	Input/output or system bus address/data pin.
RD2/AD10	bit2	TTL	Input/output or system bus address/data pin.
RD3/AD11	bit3	TTL	Input/output or system bus address/data pin.
RD4/AD12	bit4	TTL	Input/output or system bus address/data pin.
RD5/AD13	bit5	TTL	Input/output or system bus address/data pin.
RD6/AD14	bit6	TTL	Input/output or system bus address/data pin.
RD7/AD15	bit7	TTL	Input/output or system bus address/data pin.

Legend: TTL = TTL input

TABLE 10-8: REGISTERS/BITS ASSOCIATED WITH PORTD

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	$\overline{\text{MCLR}}$, WDT
13h, Bank 1	PORTD	RD7/ AD15	RD6/ AD14	RD5/ AD13	RD4/ AD12	RD3/ AD11	RD2/ AD10	RD1/ AD9	RD0/ AD8	xxxx xxxx	uuuu uuuu
12h, Bank 1	DDRD	Data Direction Register for PORTD								1111 1111	1111 1111

Legend: x = unknown, u = unchanged

10.5 PORTE and DDRE Register

PORTE is a 4-bit bi-directional port. The corresponding data direction register is DDRE. A '1' in DDRE configures the corresponding port pin as an input. A '0' in the DDRE register configures the corresponding port pin as an output. Reading PORTE reads the status of the pins, whereas writing to PORTE will write to the port latch. PORTE is multiplexed with the system bus. When operating as the system bus, PORTE contains the control signals for the address/data bus (AD15:AD0). These control signals are Address Latch Enable (ALE), Output Enable (OE) and Write (WR). The control signals OE and WR are active low signals. The timing for the system bus is shown in the Electrical Specifications section.

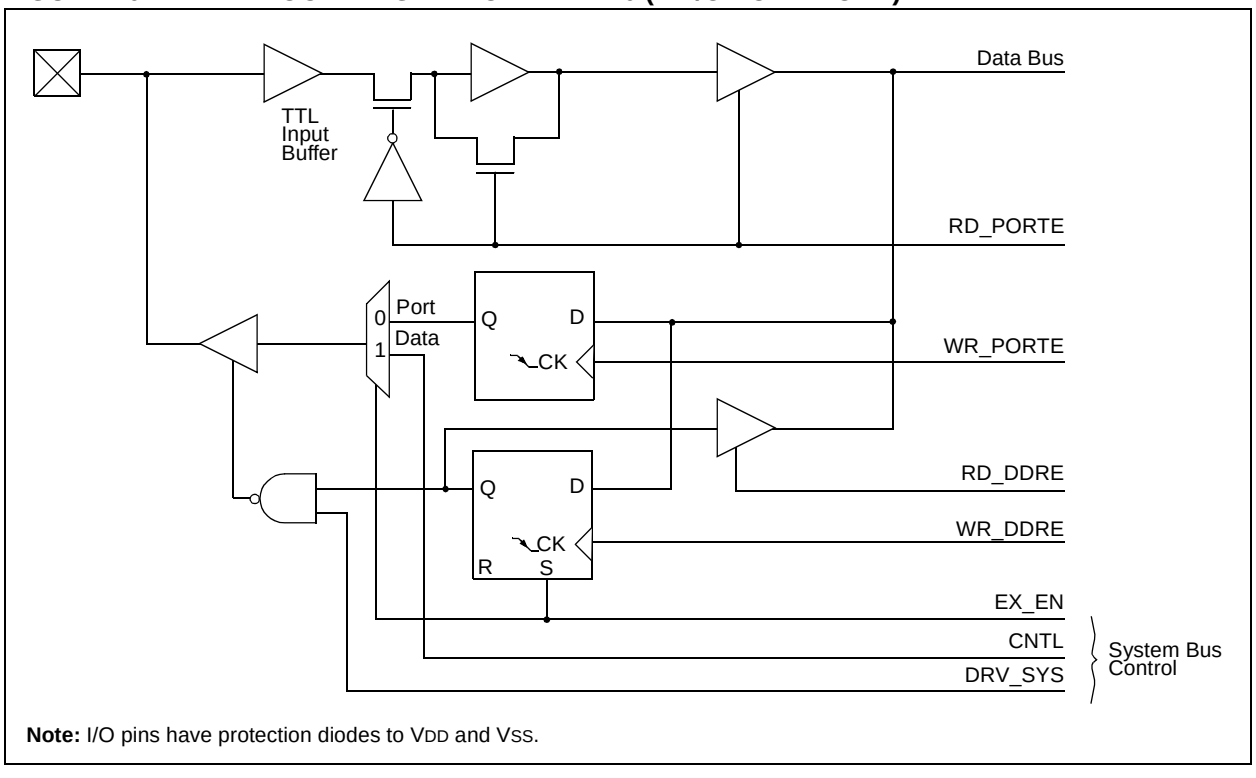
Note:	Three pins of this port are configured as the system bus when the device's configuration bits are selected to Microprocessor or Extended Microcontroller modes. The other pin is a general purpose I/O or Capture4 pin. In the two other microcontroller modes, RE2:RE0 are general purpose I/O pins.

Example 10-5 shows an instruction sequence to initialize PORTE. The Bank Select Register (BSR) must be selected to Bank 1 for the port to be initialized. The following example uses the MOVLB instruction to load the BSR register for bank selection.

EXAMPLE 10-5: INITIALIZING PORTE

```
MOVLB   1          ; Select Bank 1
CLRF    PORTE, F   ; Initialize PORTE data
                   ; latches before setting
                   ; the data direction
                   ; register
MOVLW    0x03      ; Value used to initialize
                   ; data direction
MOVWF    DDRE      ; Set RE<1:0> as inputs
                   ; RE<3:2> as outputs
                   ; RE<7:4> are always
                   ; read as '0'
```

FIGURE 10-11: BLOCK DIAGRAM OF RE2:RE0 (IN I/O PORT MODE)



Note: I/O pins have protection diodes to VDD and VSS.

10.6 PORTF and DDRF Registers

PORTF is an 8-bit wide bi-directional port. The corresponding data direction register is DDRF. A '1' in DDRF configures the corresponding port pin as an input. A '0' in the DDRF register configures the corresponding port pin as an output. Reading PORTF reads the status of the pins, whereas writing to PORTF will write to the respective port latch.

All eight bits of PORTF are multiplexed with 8 channels of the 10-bit A/D converter.

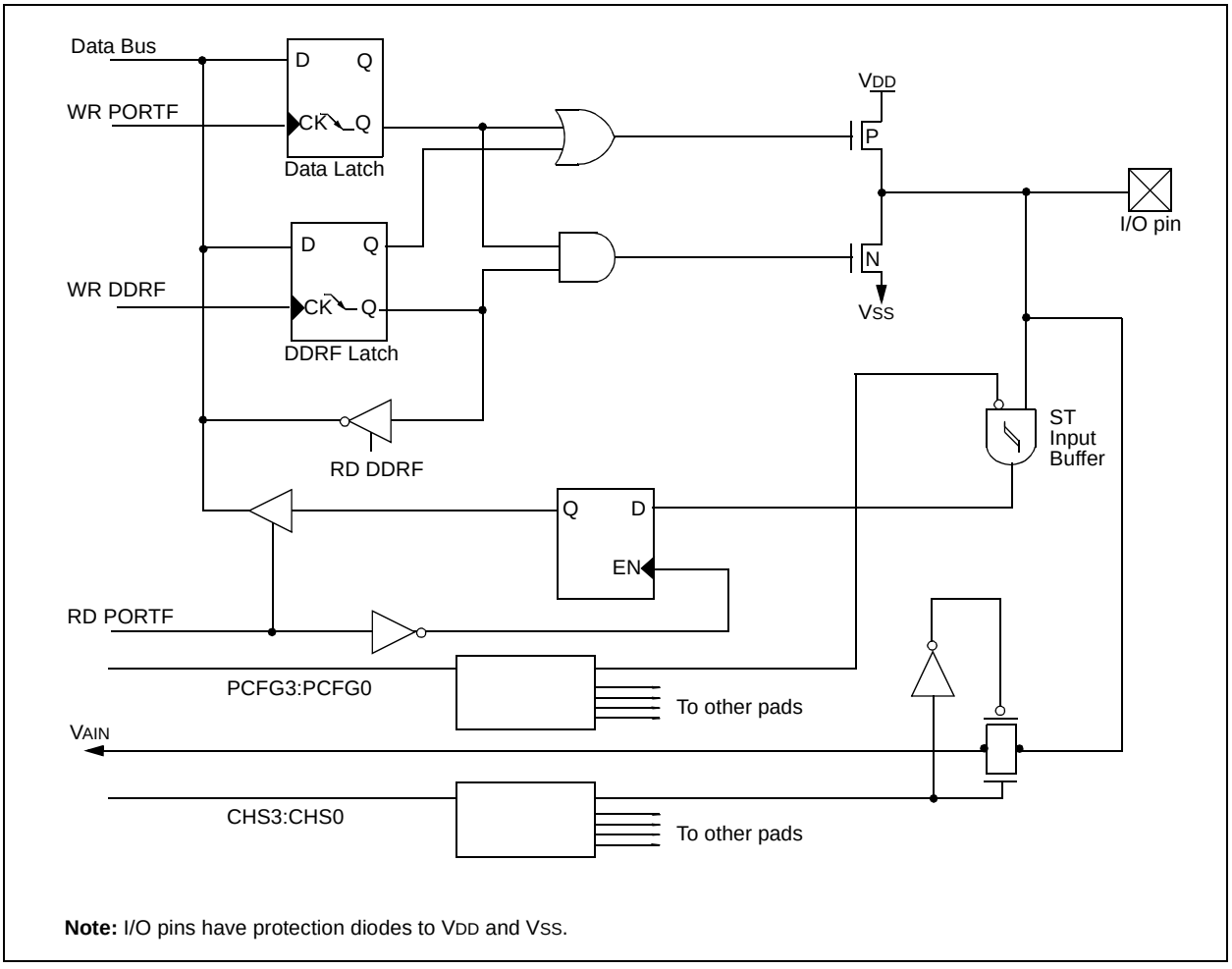
Upon RESET, the entire Port is automatically configured as analog inputs and must be configured in software to be a digital I/O.

Example 10-6 shows an instruction sequence to initialize PORTF. The Bank Select Register (BSR) must be selected to Bank 5 for the port to be initialized. The following example uses the `MOVLB` instruction to load the BSR register for bank selection.

EXAMPLE 10-6: INITIALIZING PORTF

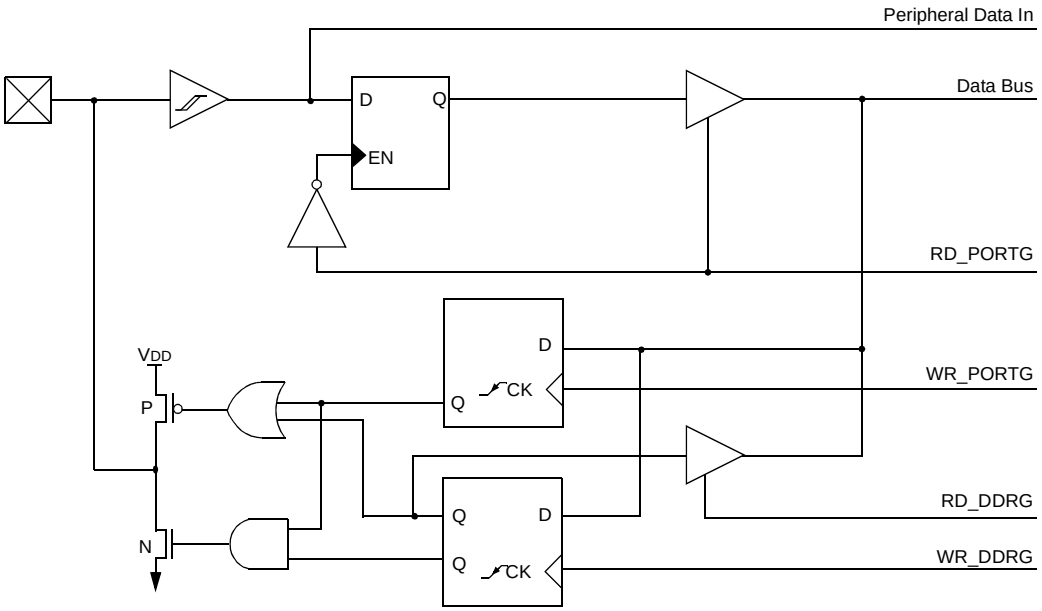
```
MOVLB   5          ; Select Bank 5
MOVWF   0x0E       ; Configure PORTF as
MOVWF   ADCON1     ; Digital
CLRF    PORTF, F   ; Initialize PORTF data
                   ;   latches before
                   ;   the data direction
                   ;   register
MOVLW    0x03      ; Value used to init
                   ;   data direction
MOVWF    DDRF      ; Set RF<1:0> as inputs
                   ;   RF<7:2> as outputs
```

FIGURE 10-13: BLOCK DIAGRAM OF RF7:RF0



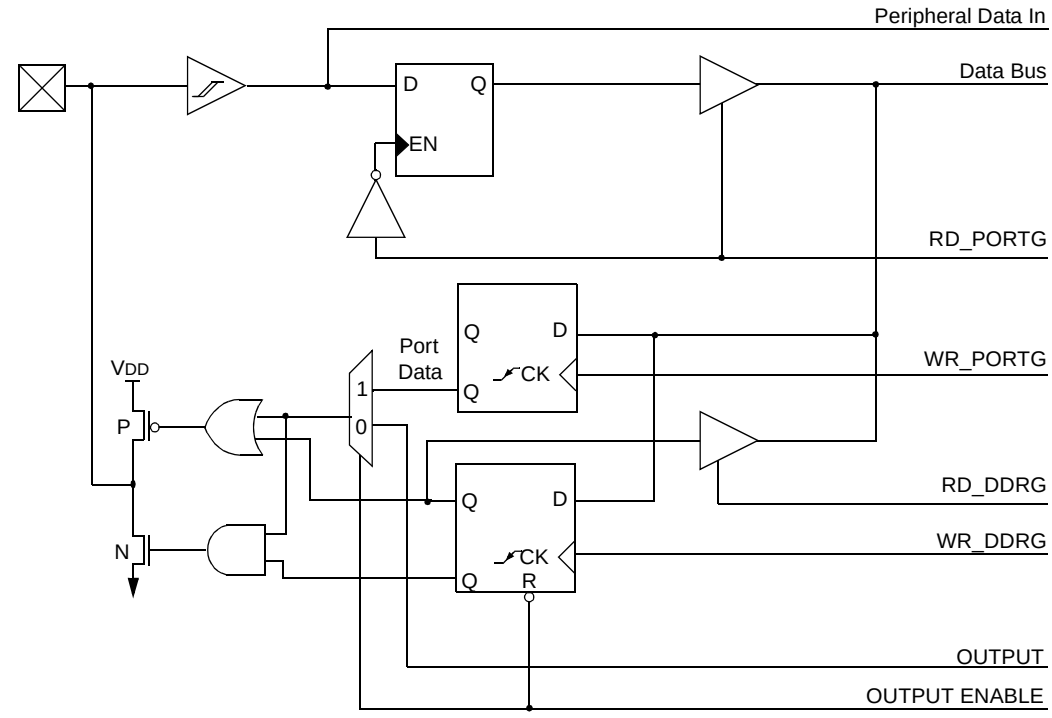
Note: I/O pins have protection diodes to V_{DD} and V_{SS}.

FIGURE 10-15: RG4 BLOCK DIAGRAM



Note: I/O pins have protection diodes to VDD and VSS.

FIGURE 10-16: RG7:RG5 BLOCK DIAGRAM



Note: I/O pins have protection diodes to VDD and VSS.

10.10.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 10-20). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should be such to allow the pin voltage to stabilize (load dependent) before executing the instruction that reads the values on that I/O port. Otherwise, the previous state of that pin may be read into the CPU, rather than the "new" state. When in doubt, it is better to separate these instructions with a `NOP`, or another instruction not accessing this I/O port.

Figure 10-21 shows the I/O model which causes this situation. As the effective capacitance (C) becomes larger, the rise/fall time of the I/O pin increases. As the device frequency increases, or the effective capacitance increases, the possibility of this subsequent PORTx read-modify-write instruction issue increases. This effective capacitance includes the effects of the board traces.

The best way to address this is to add a series resistor at the I/O pin. This resistor allows the I/O pin to get to the desired level before the next instruction.

The use of `NOP` instructions between the subsequent PORTx read-modify-write instructions, is a lower cost solution, but has the issue that the number of `NOP` instructions is dependent on the effective capacitance C and the frequency of the device.

FIGURE 10-20: SUCCESSIVE I/O OPERATION

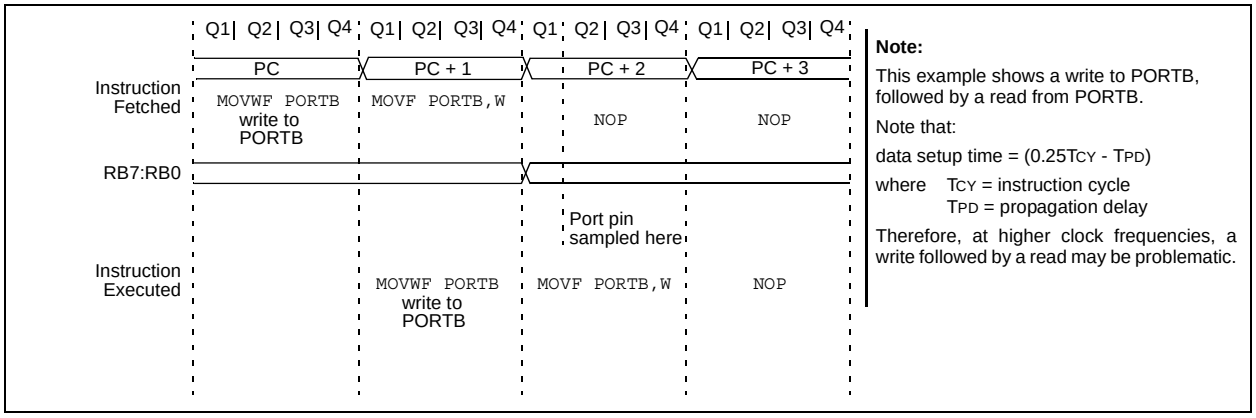
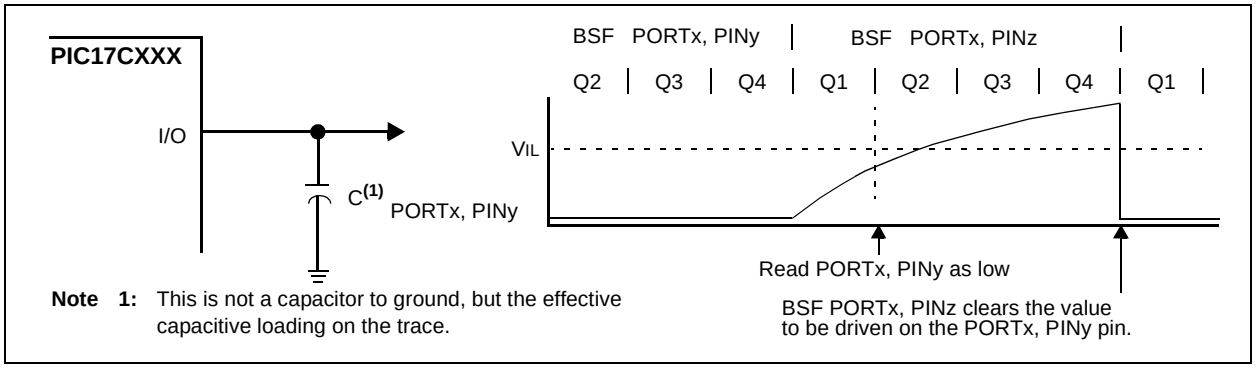


FIGURE 10-21: I/O CONNECTION ISSUES



Note 1: This is not a capacitor to ground, but the effective capacitive loading on the trace.

REGISTER 13-3: TCON3 REGISTER (ADDRESS: 16h, BANK 7)

U-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	CA4OVF	CA3OVF	CA4ED1	CA4ED0	CA3ED1	CA3ED0	PWM3ON
bit 7							bit 0

bit 7 **Unimplemented:** Read as '0'

bit 6 **CA4OVF**: Capture4 Overflow Status bit
This bit indicates that the capture value had not been read from the capture register pair (CA4H:CA4L) before the next capture event occurred. The capture register retains the oldest unread capture value (last capture before overflow). Subsequent capture events will not update the capture register with the TMR3 value until the capture register has been read (both bytes).
1 = Overflow occurred on Capture4 registers
0 = No overflow occurred on Capture4 registers

bit 5 **CA3OVF**: Capture3 Overflow Status bit
This bit indicates that the capture value had not been read from the capture register pair (CA3H:CA3L) before the next capture event occurred. The capture register retains the oldest unread capture value (last capture before overflow). Subsequent capture events will not update the capture register with the TMR3 value until the capture register has been read (both bytes).
1 = Overflow occurred on Capture3 registers
0 = No overflow occurred on Capture3 registers

bit 4-3 **CA4ED1:CA4ED0**: Capture4 Mode Select bits
00 = Capture on every falling edge
01 = Capture on every rising edge
10 = Capture on every 4th rising edge
11 = Capture on every 16th rising edge

bit 2-1 **CA3ED1:CA3ED0**: Capture3 Mode Select bits
00 = Capture on every falling edge
01 = Capture on every rising edge
10 = Capture on every 4th rising edge
11 = Capture on every 16th rising edge

bit 0 **PWM3ON**: PWM3 On bit
1 = PWM3 is enabled (the RG5/PWM3 pin ignores the state of the DDRG<5> bit)
0 = PWM3 is disabled (the RG5/PWM3 pin uses the state of the DDRG<5> bit for data direction)

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR Reset	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

13.1 Timer1 and Timer2

13.1.1 TIMER1, TIMER2 IN 8-BIT MODE

Both Timer1 and Timer2 will operate in 8-bit mode when the T16 bit is clear. These two timers can be independently configured to increment from the internal instruction cycle clock (TCY), or from an external clock source on the RB4/TCLK12 pin. The timer clock source is configured by the TMRxCS bit (x = 1 for Timer1, or = 2 for Timer2). When TMRxCS is clear, the clock source is internal and increments once every instruction cycle (FOSC/4). When TMRxCS is set, the clock source is the RB4/TCLK12 pin and the counters will increment on every falling edge of the RB4/TCLK12 pin.

The timer increments from 00h until it equals the Period register (PRx). It then resets to 00h at the next increment cycle. The timer interrupt flag is set when the timer is reset. TMR1 and TMR2 have individual interrupt flag bits. The TMR1 interrupt flag bit is latched into TMR1IF and the TMR2 interrupt flag bit is latched into TMR2IF.

Each timer also has a corresponding interrupt enable bit (TMRxIE). The timer interrupt can be enabled/disabled by setting/clearing this bit. For peripheral interrupts to be enabled, the Peripheral Interrupt Enable bit must be set (PEIE = '1') and global interrupt must be enabled (GLINTD = '0').

The timers can be turned on and off under software control. When the timer on control bit (TMRxON) is set, the timer increments from the clock source. When TMRxON is cleared, the timer is turned off and cannot cause the timer interrupt flag to be set.

13.1.1.1 External Clock Input for Timer1 and Timer2

When TMRxCS is set, the clock source is the RB4/TCLK12 pin, and the counter will increment on every falling edge on the RB4/TCLK12 pin. The TCLK12 input is synchronized with internal phase clocks. This causes a delay from the time a falling edge appears on TCLK12 to the time TMR1 or TMR2 is actually incremented. For the external clock input timing requirements, see the Electrical Specification section.

FIGURE 13-1: TIMER1 AND TIMER2 IN TWO 8-BIT TIMER/COUNTER MODE

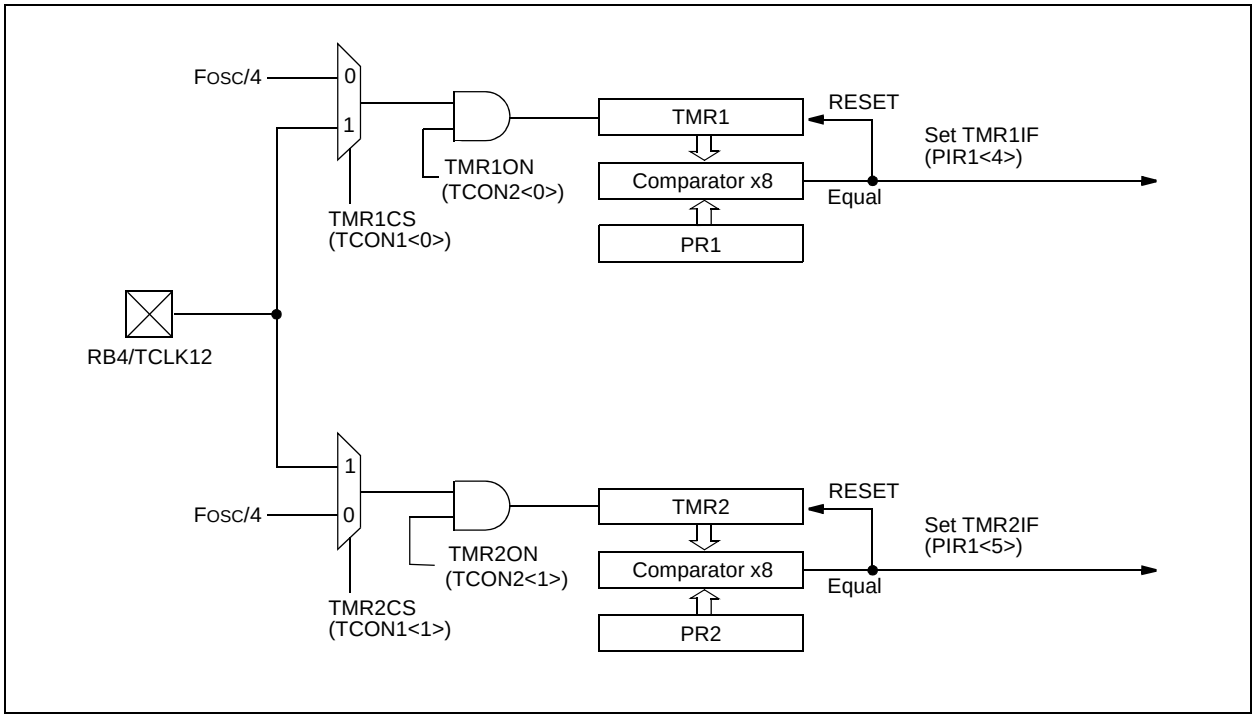


FIGURE 14-1: USART TRANSMIT

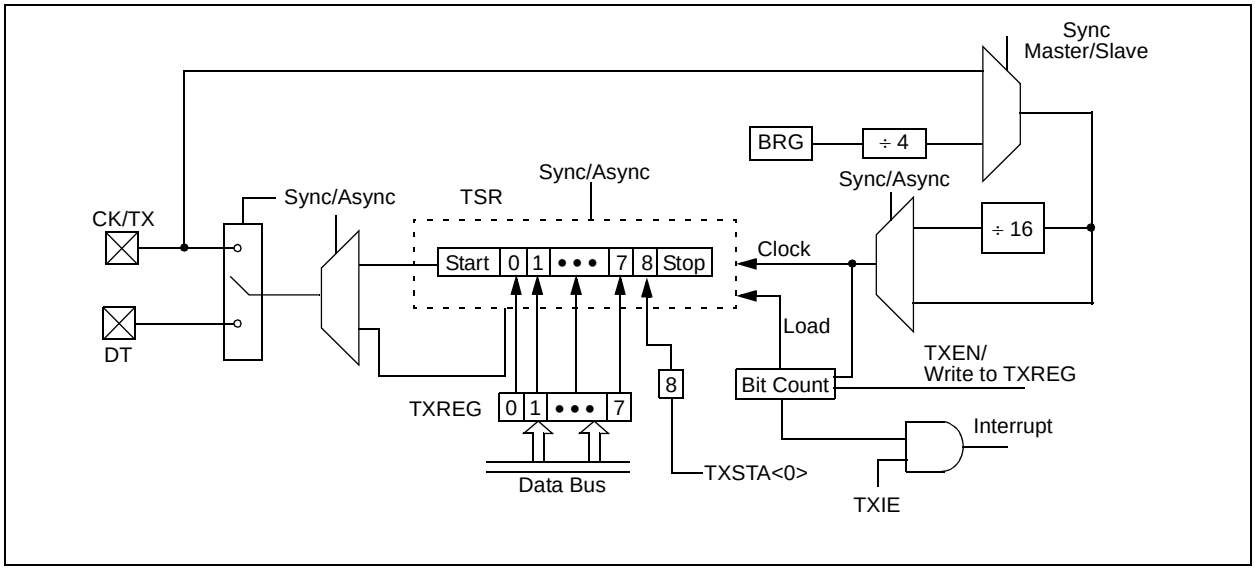
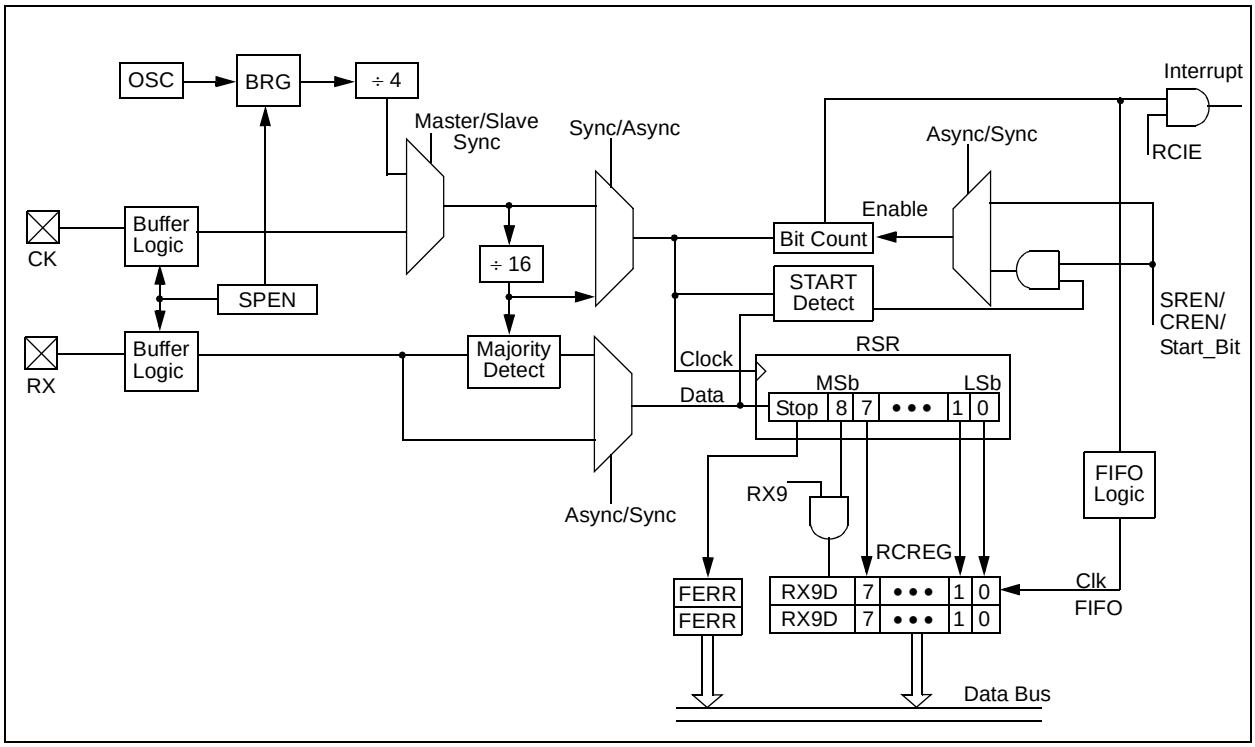


FIGURE 14-2: USART RECEIVE



15.1 SPI Mode

The SPI mode allows 8-bits of data to be synchronously transmitted and received simultaneously. All four modes of SPI are supported. To accomplish communication, typically three pins are used:

- Serial Data Out (SDO)
- Serial Data In (SDI)
- Serial Clock (SCK)

Additionally, a fourth pin may be used when in a Slave mode of operation:

- Slave Select ($\overline{SS}$)

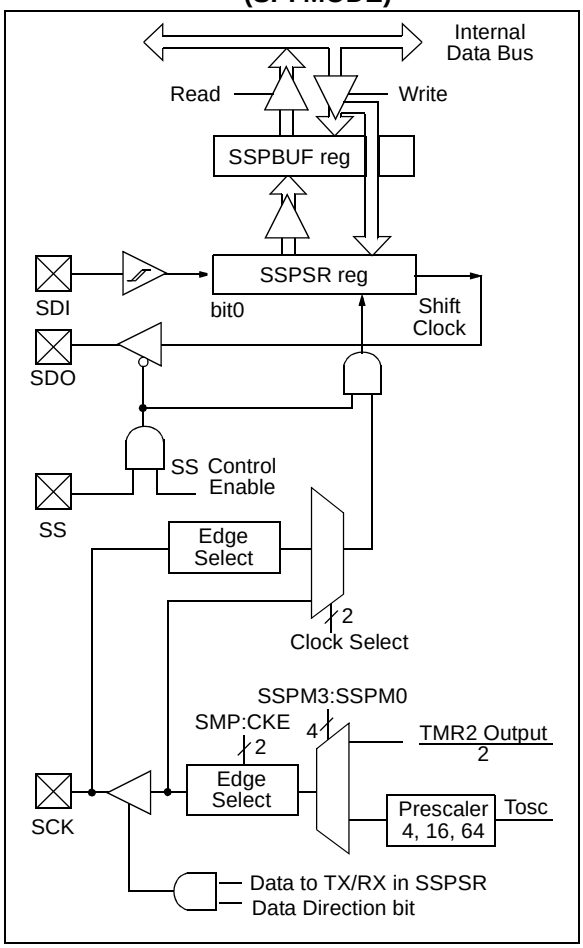
15.1.1 OPERATION

When initializing the SPI, several options need to be specified. This is done by programming the appropriate control bits in the SSPCON1 register (SSPCON1<5:0>) and SSPSTAT<7:6>. These control bits allow the following to be specified:

- Master mode (SCK is the clock output)
- Slave mode (SCK is the clock input)
- Clock Polarity (Idle state of SCK)
- Data Input Sample Phase (middle or end of data output time)
- Clock Edge (output data on rising/falling edge of SCK)
- Clock Rate (Master mode only)
- Slave Select mode (Slave mode only)

Figure 15-4 shows the block diagram of the MSSP module when in SPI mode.

FIGURE 15-4: MSSP BLOCK DIAGRAM (SPI MODE)



The MSSP consists of a transmit/receive Shift Register (SSPSR) and a Buffer register (SSPBUF). The SSPSR shifts the data in and out of the device, MSb first. The SSPBUF holds the data that was written to the SSPSR, until the received data is ready. Once the 8-bits of data have been received, that byte is moved to the SSPBUF register. Then the buffer full detect bit BF (SSPSTAT<0>) and the interrupt flag bit SSPIF (PIR2<7>) are set. This double buffering of the received data (SSPBUF) allows the next byte to start reception before reading the data that was just received. Any write to the SSPBUF register during transmission/reception of data will be ignored, and the write collision detect bit WCOL (SSPCON1<7>) will be set. User software must clear the WCOL bit so that it can be determined if the following write(s) to the SSPBUF register completed successfully.

FIGURE 15-14: I²C SLAVE-TRANSMITTER (10-BIT ADDRESS)

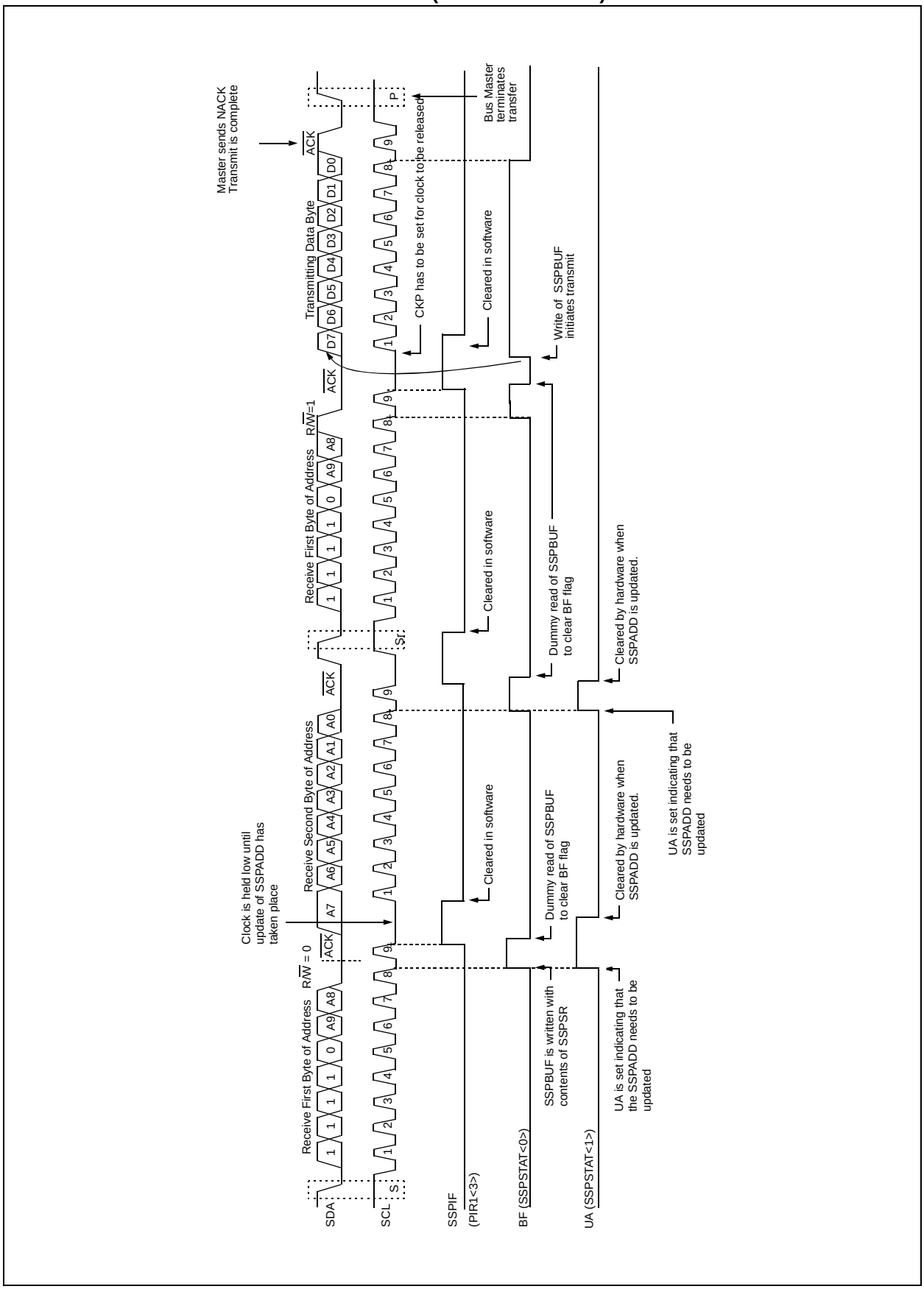
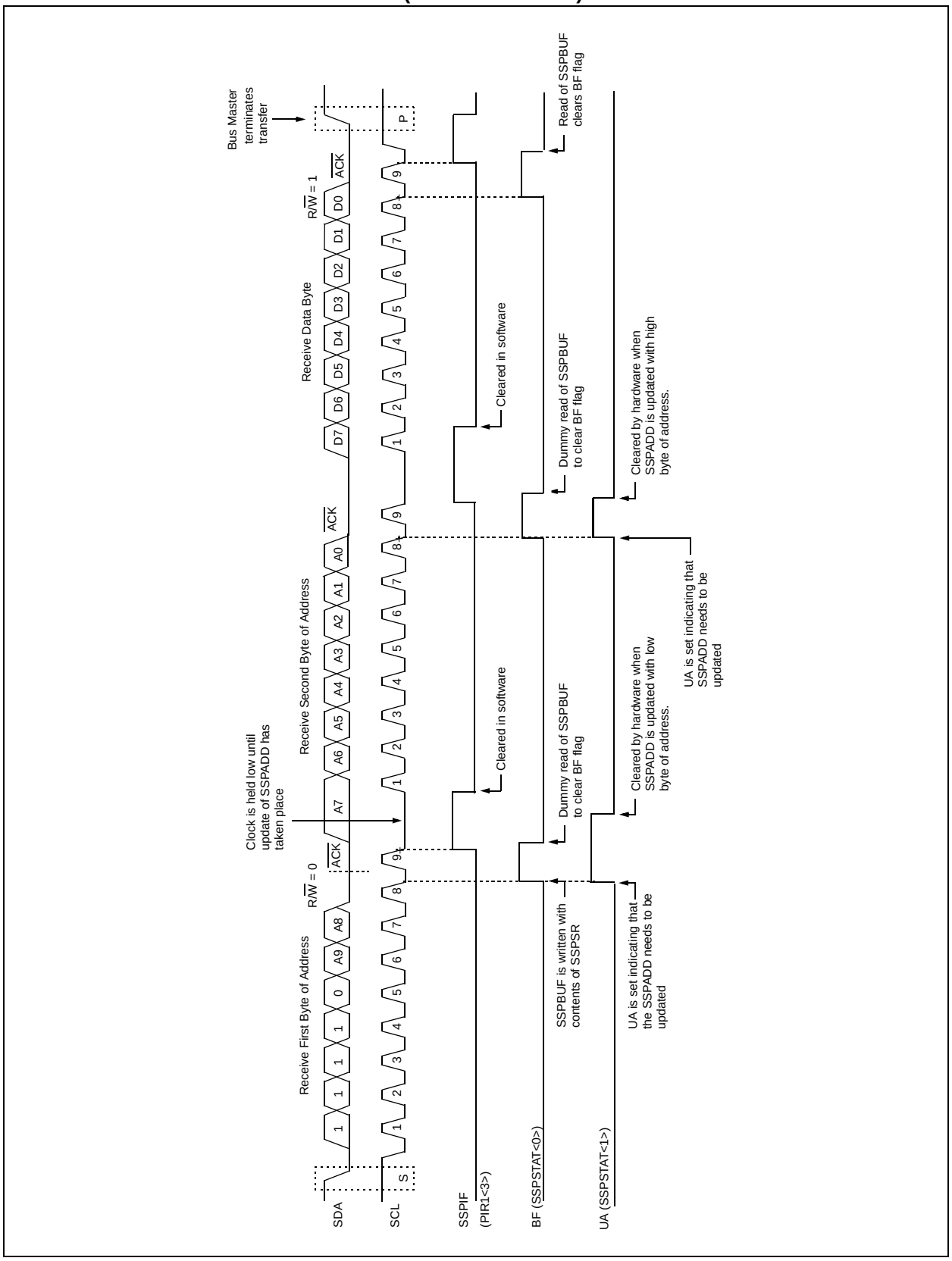


FIGURE 15-15: I^2C SLAVE-RECEIVER (10-BIT ADDRESS)



BTFSS **Bit Test, skip if Set**

Syntax: [*label*] BTFSS f,b

Operands: $0 \le f \le 127$
$0 \le b < 7$

Operation: skip if (f<b>) = 1

Status Affected: None

Encoding:

1001	0bbb	ffff	ffff

Description: If bit 'b' in register 'f' is 1, then the next instruction is skipped.
If bit 'b' is 1, then the next instruction fetched during the current instruction execution is discarded and a NOP is executed instead, making this a two-cycle instruction.

Words: 1

Cycles: 1(2)

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	No operation

If skip:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation

Example:
```
HERE    BTFSS   FLAG,1
FALSE   :
TRUE    :
```

Before Instruction
PC = address (HERE)

After Instruction
If FLAG<1> = 0;
PC = address (FALSE)
If FLAG<1> = 1;
PC = address (TRUE)

BTG **Bit Toggle f**

Syntax: [*label*] BTG f,b

Operands: $0 \le f \le 255$
$0 \le b < 7$

Operation: $(\overline{f<b>}) \rightarrow (f<b>)$

Status Affected: None

Encoding:

0011	1bbb	ffff	ffff

Description: Bit 'b' in data memory location 'f' is inverted.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write register 'f'

Example:
```
BTG     PORTC,  4
```

Before Instruction:
PORTC = 0111 0101 [0x75]

After Instruction:
PORTC = 0110 0101 [0x65]

RETURN **Return from Subroutine**

Syntax: [*label*] RETURN

Operands: None

Operation: TOS → PC;

Status Affected: None

Encoding:

0000	0000	0000	0010

Description: Return from subroutine. The stack is popped and the top of the stack (TOS) is loaded into the program counter.

Words: 1

Cycles: 2

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	No operation	Process Data	POP PC from stack
No operation	No operation	No operation	No operation

Example: `RETURN`

After Interrupt
PC = TOS

RLCF **Rotate Left f through Carry**

Syntax: [*label*] RLCF f,d

Operands: $0 \le f \le 255$
$d \in [0,1]$

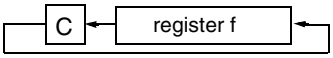
Operation: f<n> → d<n+1>;
f<7> → C;
C → d<0>

Status Affected: C

Encoding:

0001	101d	ffff	ffff

Description: The contents of register 'f' are rotated one bit to the left through the Carry Flag. If 'd' is 0, the result is placed in WREG. If 'd' is 1, the result is stored back in register 'f'.



Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

Example: `RLCF REG,0`

Before Instruction
REG = 1110 0110
C = 0

After Instruction
REG = 1110 0110
WREG = 1100 1100
C = 1

NOTES:

FIGURE 21-19: TYPICAL, MINIMUM AND MAXIMUM VOH vs. IOH (VDD = 3V, -40°C TO +125°C)

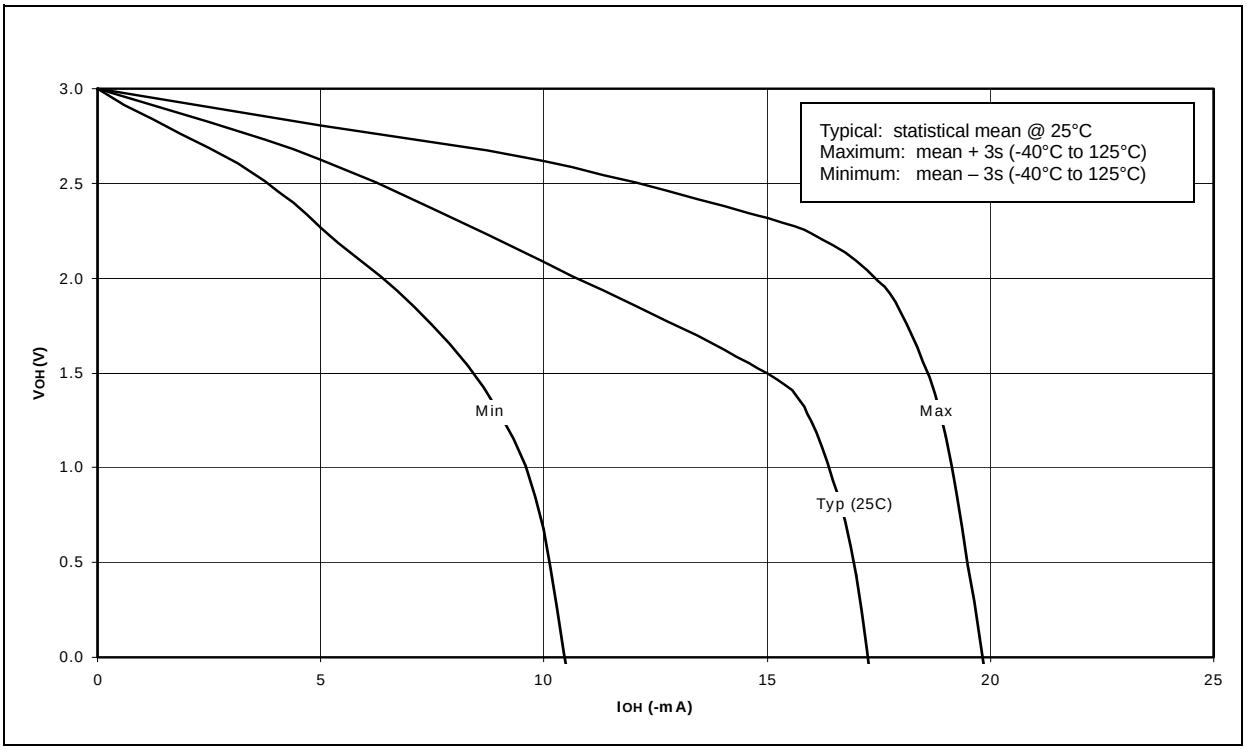


FIGURE 21-20: TYPICAL, MINIMUM AND MAXIMUM VOL vs. IOL (VDD = 3V, -40°C TO +125°C)