Infineon Technologies - TC1167128F133HLADFXUMA1 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	TriCore™
Core Size	32-Bit Single-Core
Speed	133MHz
Connectivity	ASC, CANbus, EBI/EMI, MLI, MSC, SSC
Peripherals	DMA, POR, WDT
Number of I/O	88
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.42V ~ 1.58V
Data Converters	A/D 32x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	PG-LQFP-176-5
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tc1167128f133hladfxuma1

2.1.3 Reserved, Undefined, and Unimplemented Terminology

In tables where register bit fields are defined, the following conventions are used to indicate undefined and unimplemented function. Furthermore, types of bits and bit fields are defined using the abbreviations as shown in **Table 2**.

Table 2 Bit Function Terminology

Function of Bits	Description
Unimplemented, Reserved	Register bit fields named **0** indicate unimplemented functions with the following behavior. • Reading these bit fields returns 0. • These bit fields should be written with 0 if the bit field is defined as r or rh. • These bit fields have to be written with 0 if the bit field is defined as rw. These bit fields are reserved. The detailed description of these bit fields can be found in the register descriptions.
rw	The bit or bit field can be read and written.
rwh	As rw, but bit or bit field can be also set or reset by hardware.
r	The bit or bit field can only be read (read-only).
w	The bit or bit field can only be written (write-only). A read to this register will always give a default value back.
rh	This bit or bit field can be modified by hardware (read-hardware, typical example: status flags). A read of this bit or bit field give the actual status of this bit or bit field back. Writing to this bit or bit field has no effect to the setting of this bit or bit field.
s	Bits with this attribute are “sticky” in one direction. If their reset value is once overwritten by software, they can be switched again into their reset state only by a reset operation. Software cannot switch this type of bit into its reset state by writing the register. This attribute can be combined to “rws” or “rwhs”.
f	Bits with this attribute are readable only when they are accessed by an instruction fetch. Normal data read operations will return other values.

2.1.4 Register Access Modes

Read and write access to registers and memory locations are sometimes restricted. In memory and register access tables, the terms as defined in **Table 3** are used.

2.2 System Architecture of the TC1167

The TC1167 combines three powerful technologies within one silicon die, achieving new levels of power, speed, and economy for embedded applications:

- Reduced Instruction Set Computing (RISC) processor architecture
- Digital Signal Processing (DSP) operations and addressing modes
- On-chip memories and peripherals

DSP operations and addressing modes provide the computational power necessary to efficiently analyze complex real-world signals. The RISC load/store architecture provides high computational bandwidth with low system cost. On-chip memory and peripherals are designed to support even the most demanding high-bandwidth real-time embedded control-systems tasks.

Additional high-level features of the TC1167 include:

- Program Memory Unit – instruction memory and instruction cache
- Serial communication interfaces – flexible synchronous and asynchronous modes
- Peripheral Control Processor – standalone data operations and interrupt servicing
- DMA Controller – DMA operations and interrupt servicing
- General-purpose timers
- High-performance on-chip buses
- On-chip debugging and emulation facilities
- Flexible interconnections to external components
- Flexible power-management

TC1167 clock frequencies:

- Maximum CPU clock frequency: 133 MHz[1)]
- Maximum PCP clock frequency: 133 MHz[2)]
- Maximum SPB frequency: 80 MHz[3)]

The TC1167 is a high-performance microcontroller with TriCore CPU, program and data memories, buses, bus arbitration, an interrupt controller, a peripheral control processor, a DMA controller and several on-chip peripherals. The TC1167 is designed to meet the needs of the most demanding embedded control systems applications where the competing issues of price/performance, real-time responsiveness, computational power, data bandwidth, and power consumption are key design elements.

The TC1167 offers several versatile on-chip peripheral units such as serial controllers, timer units, and Analog-to-Digital converters. Within the TC1167, all these peripheral units are connected to the TriCore CPU/system via the Flexible Peripheral Interconnect (FPI) Bus and the Local Memory Bus (LMB). Several I/O lines on the TC1167 ports are reserved for these peripheral units to communicate with the external world.

1) For CPU frequencies > 80 MHz, 2:1 mode has to be enabled. CPU 2:1 mode means: $f_{SPB} = 0.5 * f_{CPU}$

2) For PCP frequencies > 80 MHz, 2:1 mode has to be enabled. PCP 2:1 mode means: $f_{SPB} = 0.5 * f_{PCP}$

3) CPU 1:1 Mode means: $f_{SPB} = f_{CPU}$. PCP 1:1 mode means: $f_{SPB} = f_{PCP}$

Features

- Free-running 56-bit counter
- All 56 bits can be read synchronously
- Different 32-bit portions of the 56-bit counter can be read synchronously
- Flexible interrupt generation based on compare match with partial STM content
- Driven by maximum 80 MHz (= f_{SYS}, default after reset = $f_{SYS}/2$)
- Counting starts automatically after a reset operation
- STM registers are reset by an application reset if bit ARSTDIS.STMDIS is cleared. If bit ARSTDIS.STMDIS is set, the STM is not reset.
- STM can be halted in debug/suspend mode

Special STM register semantics provide synchronous views of the entire 56-bit counter, or 32-bit subsets at different levels of resolution.

The maximum clock period is $2^{56} \times f_{STM}$. At f_{STM} = 80 MHz, for example, the STM counts 28.56 years before overflowing. Thus, it is capable of continuously timing the entire expected product life time of a system without overflowing.

In case of a power-on reset, a watchdog reset, or a software reset, the STM is reset. After one of these reset conditions, the STM is enabled and immediately starts counting up. It is not possible to affect the content of the timer during normal operation of the TC1167. The timer registers can only be read but not written to.

The STM can be optionally disabled for power-saving purposes, or suspended for debugging purposes via its clock control register. In suspend mode of the TC1167 (initiated by writing an appropriate value to STM_CLC register), the STM clock is stopped but all registers are still readable.

Due to the 56-bit width of the STM, it is not possible to read its entire content with one instruction. It needs to be read with two load instructions. Since the timer would continue to count between the two load operations, there is a chance that the two values read are not consistent (due to possible overflow from the low part of the timer to the high part between the two read operations). To enable a synchronous and consistent reading of the STM content, a capture register (STM_CAP) is implemented. It latches the content of the high part of the STM each time when one of the registers STM_TIM0 to STM_TIM5 is read. Thus, STM_CAP holds the upper value of the timer at exactly the same time when the lower part is read. The second read operation would then read the content of the STM_CAP to get the complete timer value.

The content of the 56-bit System Timer can be compared against the content of two compare values stored in the STM_CMP0 and STM_CMP1 registers. Interrupts can be generated on a compare match of the STM with the STM_CMP0 or STM_CMP1 registers.

Figure 2 provides an overview on the STM module. It shows the options for reading parts of STM content.

- For further operating conditions see data sheet section “Flash Memory Parameters”.

Data Flash Features and Functions

- 64 Kbyte on-chip Flash, configured in two independent Flash banks of equal size.
- 64 bit read interface.
- Erase/program one bank while data read access from the other bank.
- Programming one bank while erasing the other bank using an automatic suspend/resume function.
- Dynamic correction of single-bit errors during read access.
- Sector architecture:
  - Two sectors of equal size.
  - Each sector separately erasable.
- 128 byte pages to be written in one step.
- Operational control per command sequences (unlock sequences, same as those of Program Flash) for protection against unintended operation.
- End-of-busy as well as error reporting with interrupt and bus error trap.
- Write state machine for automatic program and erase.
- Margin check for detection of problematic Flash bits.
- Endurance = 30000 (can be device dependent); i.e. 30000 program/erase cycles per sector are allowed, with a retention of min. 5 years.
- Dedicated DFlash status information.
- Other characteristics: Same as Program Flash.

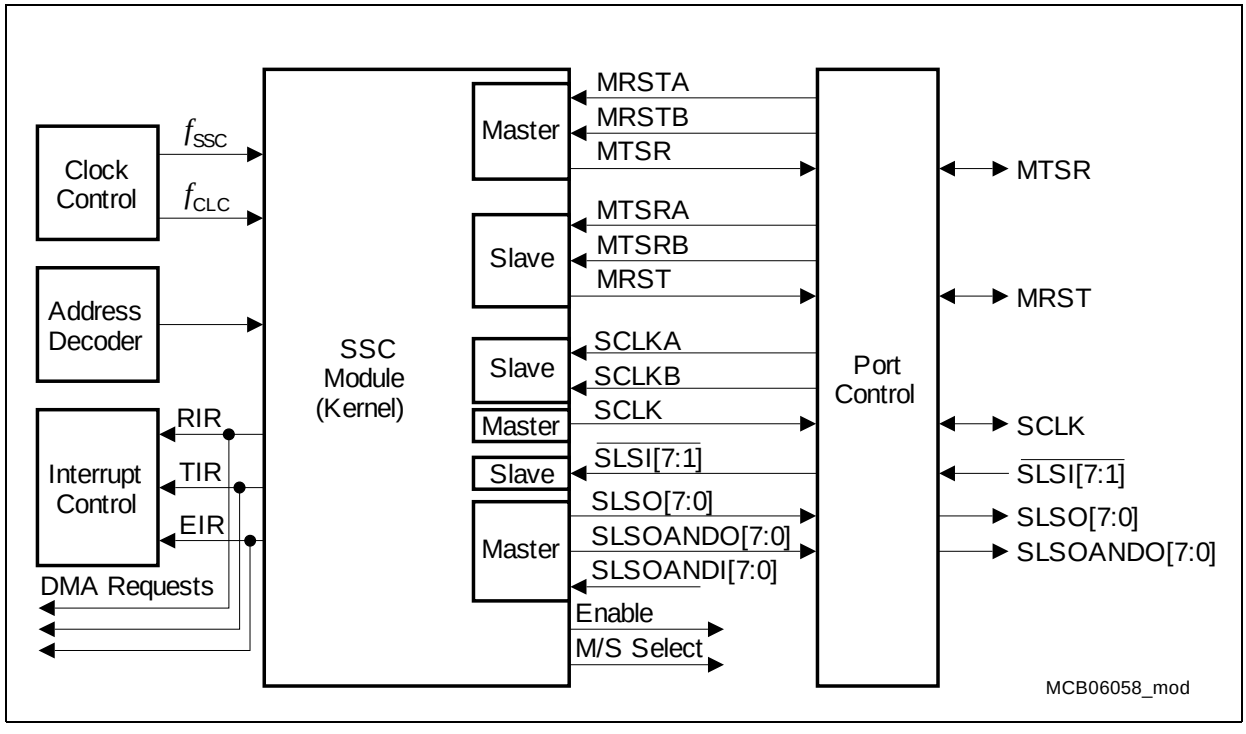

Figure 6 General Block Diagram of the SSC Interface

The SSC supports full-duplex and half-duplex serial synchronous communication up to 40 Mbit/s (@ 80 MHz module clock, Master Mode). The serial clock signal can be generated by the SSC itself (Master Mode) or can be received from an external master (Slave Mode). Data width, shift direction, clock polarity and phase are programmable. This allows communication with SPI-compatible devices. Transmission and reception of data are double-buffered. A shift clock generator provides the SSC with a separate serial clock signal. One slave select input is available for slave mode operation. Eight programmable slave select outputs (chip selects) are supported in Master Mode.

- 32-bit, 16-bit, or 8-bit data transfers supported
- Programmable baud rate: $f_{MLI}/2$ (max. $f_{MLI} = f_{SYS}$)
- Address range protection scheme to block unauthorized accesses
- Multiple receiving devices supported

2.4.6 General Purpose Timer Array (GPTA)

The TC1167 contains the General Purpose Timer Array (GPTA0). **Figure 11** shows a global view of the GPTA module.

The GPTA provides a set of timer, compare, and capture functionalities that can be flexibly combined to form signal measurement and signal generation units. They are optimized for tasks typical of engine, gearbox, and electrical motor control applications, but can also be used to generate simple and complex signal waveforms required for other industrial applications.

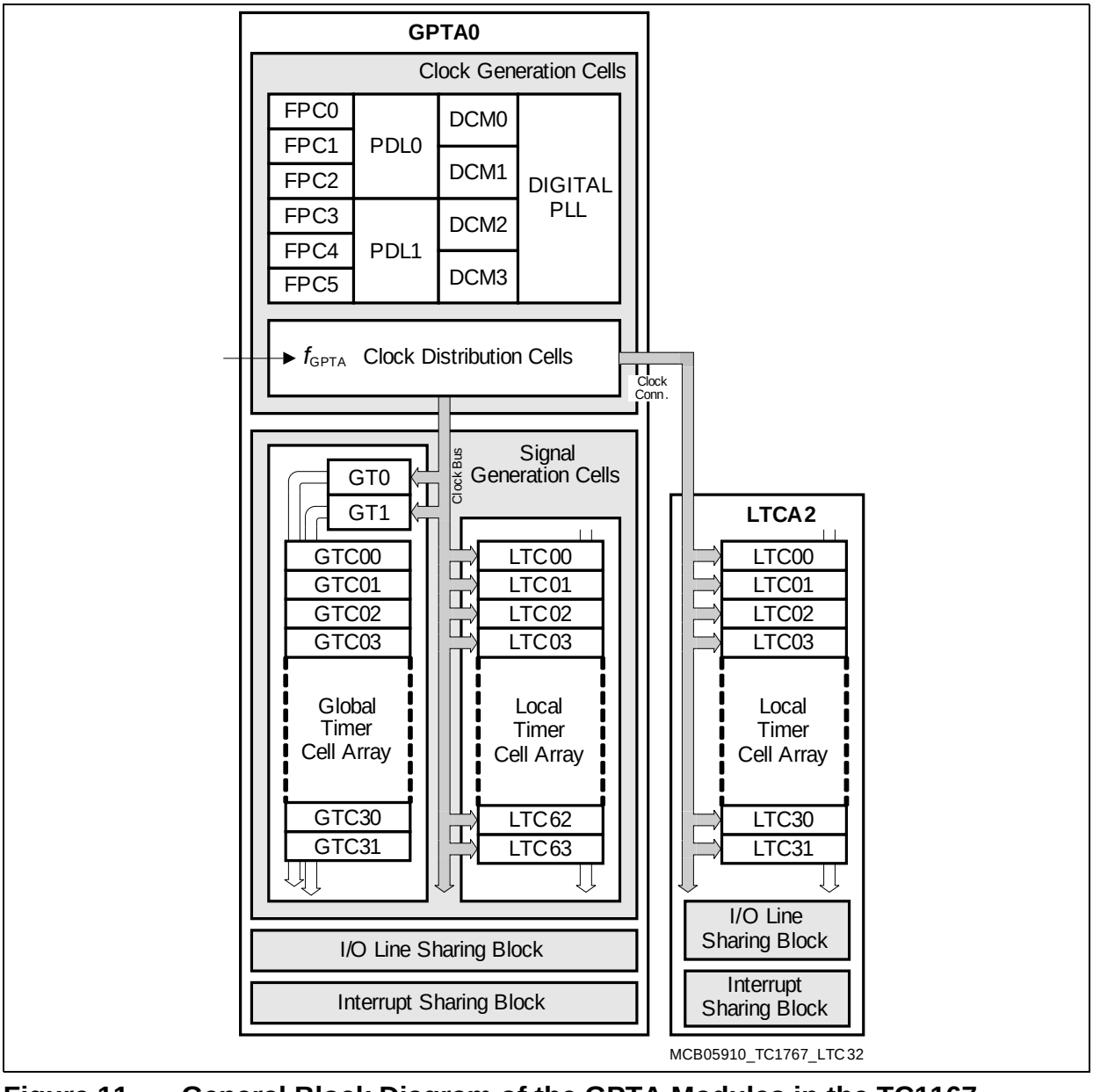

Figure 11 General Block Diagram of the GPTA Modules in the TC1167

On-chip Trigger Unit

- 16 on-chip trigger signals

I/O Sharing Unit

- Interconnecting inputs and outputs from internal clocks, FPC, GTC, LTC, ports, and MSC interface

Table 4 Pin Definitions and Functions (PG-LQFP-176-5 Package[1]) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
97	P1.11	I/O0	A2/ PU	**Port 1 General Purpose I/O Line 11**
	IN27	I		**GPTA0 Input 27**
	IN51	I		**GPTA0 Input 51**
	SCLK1B	I		**SSC1 Clock Input B**
	OUT27	O1		**GPTA0 Output 27**
	OUT51	O2		**GPTA0 Output 51**
	SCLK1B	O3		**SSC1 Clock Output B**
73	P1.12	I/O0	A1/ PU	**Port 1 General Purpose I/O Line 12**
	IN16	I		**LTCA2 Input 16**
	AD0EMUX0	O1		**ADC0 External Multiplexer Control Output 0**
	AD0EMUX0	O2		**ADC0 External Multiplexer Control Output 0**
	OUT16	O3		**LTCA2 Output 16**
72	P1.13	I/O0	A1/ PU	**Port 1 General Purpose I/O Line 13**
	IN17	I		**LTCA2 Input 17**
	AD0EMUX1	O1		**ADC0 External Multiplexer Control Output 1**
	AD0EMUX1	O2		**ADC0 External Multiplexer Control Output 1**
	OUT17	O3		**LTCA2 Output 17**
71	P1.14	I/O0	A1/ PU	**Port 1 General Purpose I/O Line 14**
	IN18	I		**LTCA2 Input 18**
	AD0EMUX2	O1		**ADC0 External Multiplexer Control Output 2**
	AD0EMUX2	O2		**ADC0 External Multiplexer Control Output 2**
	OUT18	O3		**LTCA2 Output 18**
117	P1.15	I/O0	A2/ PU	**Port 1 General Purpose I/O Line 15**
	$\overline{\text{BRKIN}}$	I		**Break Input**
	Reserved	O1		**-**
	Reserved	O2		**-**
	Reserved	O3		**-**
	$\overline{\text{BRKOUT}}$	O		**Break Output (controlled by OCDS module)**

Port 2

Table 4 Pin Definitions and Functions (PG-LQFP-176-5 Package[1]) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
79	P2.5	I/O0	A2/ PU	**Port 2 General Purpose I/O Line 5**
	IN37	I		**GPTA0 Input 37**
	OUT37	O1		**GPTA0 Output 37**
	RREADY0A	O2		**MLI0 Receiver Ready Output A**
	OUT110	O3		**LTCA2 Output 110**
80	P2.6	I/O0	A2/ PU	**Port 2 General Purpose I/O Line 6**
	IN38	I		**GPTA0 Input 38**
	RVALID0A	I		**MLI Receiver Valid Input A**
	OUT38	O1		**GPTA0 Output 38**
	OUT38	O2		**GPTA0 Output 38**
	OUT111	O3		**LTCA2 Output 111**
81	P2.7	I/O0	A2/ PU	**Port 2 General Purpose I/O Line 7**
	IN39	I		**GPTA0 Input 39**
	RDATA0A	I		**MLI Receiver Data Input A**
	OUT39	O1		**GPTA0 Output 39**
	OUT39	O2		**GPTA0 Output 39**
	Reserved	O3		**-**
164	P2.8	I/O0	A2/ PU	**Port 2 General Purpose I/O Line 8**
	SLSO04	O1		**SSC0 Slave Select Output 4**
	SLSO14	O2		**SSC1 Slave Select Output 4**
	EN00	O3		**MSC0 Enable Output 0**
160	P2.9	I/O0	A2/ PU	**Port 2 General Purpose I/O Line 9**
	SLSO05	O1		**SSC0 Slave Select Output 5**
	SLSO15	O2		**SSC1 Slave Select Output 5**
	EN01	O3		**MSC0 Enable Output 1**

Table 4 Pin Definitions and Functions (PG-LQFP-176-5 Package[1]) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
87	P4.1	I/O0	A1/ PU	**Port 4 General Purpose I/O Line 1**
	IN29	I		**GPTA0 Input 29**
	IN53	I		**GPTA0 Input 53**
	OUT29	O1		**GPTA0 Output 29**
	OUT53	O2		**GPTA0 Output 53**
	Reserved	O3		**-**
88	P4.2	I/O0	A2/ PU	**Port 4 General Purpose I/O Line 2**
	IN30	I		**GPTA0 Input 30**
	IN54	I		**GPTA0 Input 54**
	OUT30	O1		**GPTA0 Output 30**
	OUT54	O2		**GPTA0 Output 54**
	EXTCLK1	O3		**External Clock 1 Output**
90	P4.3	I/O0	A2/ PU	**Port 4 General Purpose I/O Line 3**
	IN31	I		**GPTA0 Input 31**
	IN55	I		**GPTA0 Input 55**
	OUT31	O1		**GPTA0 Output 31**
	OUT55	O2		**GPTA0 Output 55**
	EXTCLK0	O3		**External Clock 0 Output**
Port 5				
1	P5.0	I/O0	A1/ PU	**Port 5 General Purpose I/O Line 0**
	IN40	I		**GPTA0 Input 40**
	IN26	I		**LTCA2 Input 26**
	OUT40	O1		**GPTA0 Output 40**
	OUT8	O2		**LTCA2 Output 8**
	Reserved	O3		**-**

Table 4 Pin Definitions and Functions (PG-LQFP-176-5 Package[1]) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
2	P5.1	I/O0	A1/ PU	**Port 5 General Purpose I/O Line 1**
	IN41	I		**GPTA0 Input 41**
	IN27	I		**LTCA2 Input 27**
	OUT41	O1		**GPTA0 Output 41**
	OUT9	O2		**LTCA2 Output 9**
	Reserved	O3		**-**
3	P5.2	I/O0	A1/ PU	**Port 5 General Purpose I/O Line 2**
	IN42	I		**GPTA0 Input 42**
	IN28	I		**LTCA2 Input 28**
	OUT42	O1		**GPTA0 Output 42**
	OUT10	O2		**LTCA2 Output 10**
	Reserved	O3		**-**
4	P5.3	I/O0	A1/ PU	**Port 5 General Purpose I/O Line 3**
	IN43	I		**GPTA0 Input 43**
	OUT43	O1		**GPTA0 Output 43**
	OUT11	O2		**LTCA2 Output 11**
	Reserved	O3		**-**
5	P5.4	I/O0	A1/ PU	**Port 5 General Purpose I/O Line 4**
	IN44	I		**GPTA0 Input 44**
	IN29	I		**LTCA2 Input 29**
	OUT44	O1		**GPTA0 Output 44**
	OUT12	O2		**LTCA2 Output 12**
	Reserved	O3		**-**
6	P5.5	I/O0	A1/ PU	**Port 5 General Purpose I/O Line 5**
	IN45	I		**GPTA0 Input 45**
	IN30	I		**LTCA2 Input 30**
	OUT45	O1		**GPTA0 Output 45**
	OUT13	O2		**LTCA2 Output 13**
	Reserved	O3		**-**

5.1.2 Pad Driver and Pad Classes Summary

This section gives an overview on the different pad driver classes and its basic characteristics. More details (mainly DC parameters) are defined in the **Section 5.2.1**.

Table 6 Pad Driver and Pad Classes Overview

Class	Power Supply	Type	Sub Class	Speed Grade	Load	Leakage[1)]	Termination
A	3.3 V	LVTTL I/O, LVTTL outputs	**A1** (e.g. GPIO)	6 MHz	100 pF	500 nA	No
			A2 (e.g. serial I/Os)	40 MHz	50 pF	6 µA	Series termination recommended
F	3.3 V	LVDS/ CMOS	–	50 MHz	–	–	Parallel termination[2)], 100 Ω ± 10%
D_E	5 V	ADC	–	–	–	–	see **Table 11**

1) Values are for T_{Jmax} = 150 °C.

2) In applications where the LVDSpins are not used (disabled), these pins must be either left unconnected, or properly terminated with the differential parallel termination of 100 Ω ± 10%.

Table 10 Input/Output DC-Characteristics (cont'd)(Operating Conditions apply)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Spike filter pass-through pulse duration	t_{SF2}	CC	100	–	–	ns	
Class A Pads (V_{DDP} = 3.13 to 3.47 V = 3.3V ± 5%)							
Output low voltage [2)3)]	V_{OLA}	CC	–	–	0.4	V	I_{OL} = 2 mA for medium and strong driver mode, I_{OL} = 500 µA for weak driver mode
Output high voltage[2) 3)]	V_{OHA}	CC	2.4	–	–	V	I_{OH} = -2 mA for medium and strong driver mode, I_{OH} = -500 µA for weak driver mode
			V_{DDP} - 0.4	–	–	V	I_{OH} = -1.4 mA for medium and strong driver mode, I_{OH} = -400 µA for weak driver mode
Input low voltage Class A1/2 pins	V_{ILA}	SR	-0.3	–	0.36 × V_{DDP}	V	–
Input high voltage Class A1 pins	V_{IHA1}	SR	0.62 × V_{DDP}	–	V_{DDP}+ 0.3 or max. 3.6	V	Whatever is lower
Ratio V_{IL}/V_{IH}		SR	0.58	–	–	–	–
Input high voltage Class A2 pins	V_{IHA2}	SR	0.60 × V_{DDP}	–	V_{DDP}+ 0.3 or max. 3.6	V	Whatever is lower
Ratio V_{IL}/V_{IH}		CC	0.60	–	–	–	–
Input hysteresis	HYSA	CC	0.1 × V_{DDP}	–	–	V	[4)]
Input leakage current Class A2 pins	I_{OZA2}		–	–	±3000 ±6000	nA	((V_{DDP}/2)-1) < V_{IN} < ((V_{DDP}/2)+1) Otherwise[2)]

3) Maximum resistance of the driver R_{DSON}, defined for P_MOS / N_MOS transistor separately:
25 / 20 Ω for strong driver mode, $I_{OH\,/\,L}$ < 2 mA,
200 / 150 Ω for medium driver mode, $I_{OH\,/\,L}$ < 400 uA,
600 / 400 Ω for weak driver mode, $I_{OH\,/\,L}$ < 100 uA,
verified by design / characterization.

4) Function verified by design, value verified by design characterization.
Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce.
It cannot be guaranteed that it suppresses switching due to external system noise.

5) The following constraint applies to an LVDS pair used in CMOS mode: only one pin of a pair should be used as output, the other should be used as input, or both pins should be used as inputs. Using both pins as outputs is not recommended because of the higher crosstalk between them.

5.3.2 Output Rise/Fall Times

Table 17 Output Rise/Fall Times (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Class A1 Pads						
Rise/fall times[1)]	t_{RA1}, t_{FA1}	–	–	50 140 18000 150 550 65000	ns	Regular (medium) driver, 50 pF Regular (medium) driver, 150 pF Regular (medium) driver, 20 nF Weak driver, 20 pF Weak driver, 150 pF Weak driver, 20 000 pF
Class A2 Pads						
Rise/fall times[1)]	t_{RA2}, t_{FA2}	–	–	3.7 7.5 7 18 50 140 18000 150 550 65000	ns	Strong driver, sharp edge, 50 pF Strong driver, sharp edge, 100pF Strong driver, med. edge, 50 pF Strong driver, soft edge, 50 pF Medium driver, 50 pF Medium driver, 150 pF Medium driver, 20 000 pF Weak driver, 20 pF Weak driver, 150 pF Weak driver, 20 000 pF
Class F Pads						
Rise/fall times	t_{RF1}, t_{FF1}	–	–	2	ns	LVDS Mode
Rise/fall times	t_{RF2}, t_{FF2}	–	–	60	ns	CMOS Mode, 50 pF

1) Not all parameters are subject to production test, but verified by design/characterization and test correlation.

4. The $\overline{\text{PORST}}$ signal may be deactivated after all V_{DD5}, $V_{DD3.3}$, $V_{DD1.5}$, and V_{AREF} power-supplies and the oscillator have reached stable operation, within the normal operating conditions.
5. At normal power down the $\overline{\text{PORST}}$ signal should be activated within the normal operating range, and then the power supplies may be switched off. Care must be taken that all Flash write or delete sequences have been completed.
6. At power fail the $\overline{\text{PORST}}$ signal must be activated at latest when any 3.3 V or 1.5 V power supply voltage falls 12% below the nominal level. The same limit of 3.3 V-12% applies to the 5 V power supply too. If, under these conditions, the PORST is activated during a Flash write, only the memory row that was the target of the write at the moment of the power loss will contain unreliable content. In order to ensure clean power-down behavior, the $\overline{\text{PORST}}$ signal should be activated as close as possible to the normal operating voltage range.
7. In case of a power-loss at any power-supply, all power supplies must be powered-down, conforming at the same time to the rules number 2 and 4.
8. Although not necessary, it is additionally recommended that all power supplies are powered-up/down together in a controlled way, as tight to each other as possible.
9. Aditionally, regarding the ADC reference voltage V_{AREF}:
   – V_{AREF} must power-up at the same time or later than V_{DDM}, and
   – V_{AREF} must power-down eather earlier or at latest to satisfy the condition $V_{AREF} < V_{DDM} + 0.5$ V. This is required in order to prevent discharge of V_{AREF} filter capacitance through the ESD diodes through the V_{DDM} power supply. In case of discharging the reference capacitance through the ESD diodes, the current must be lower than 5 mA.

Table 22 MLI Transmitter/Receiver Timing
(Operating Conditions apply), C_L = 50 pF

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
MLI Transmitter Timing							
TCLK clock period	t_{10}	CC	$2 \times T_{MLI}$	–	–	ns	1)
TCLK high time	t_{11}	CC	$0.45 \times t_{10}$	$0.5 \times t_{10}$	$0.55 \times t_{10}$	ns	2)3)
TCLK low time	t_{12}	CC	$0.45 \times t_{10}$	$0.5 \times t_{10}$	$0.55 \times t_{10}$	ns	2)3)
TCLK rise time	t_{13}	CC	–	–	4)	ns	–
TCLK fall time	t_{14}	CC	–	–	4)	ns	–
TDATA/TVALID output delay time	t_{15}	CC	-3	–	4.4	ns	–
TREADY setup time to TCLK rising edge	t_{16}	SR	18	–	–	ns	–
TREADY hold time from TCLK rising edge	t_{17}	SR	0	–	–	ns	–
MLI Receiver Timing							
RCLK clock period	t_{20}	SR	$1 \times T_{MLI}$	–	–	ns	1)
RCLK high time	t_{21}	SR	–	$0.5 \times t_{20}$	–	ns	5)6)
RCLK low time	t_{22}	SR	–	$0.5 \times t_{20}$	–	ns	5)6)
RCLK rise time	t_{23}	SR	–	–	4	ns	7)
RCLK fall time	t_{24}	SR	–	–	4	ns	7)
RDATA/RVALID setup time to RCLK falling edge	t_{25}	SR	4.2	–	–	ns	–
RDATA/RVALID hold time from RCLK rising edge	t_{26}	SR	2.2	–	–	ns	–
RREADY output delay time	t_{27}	CC	0	–	16	ns	–

1) $T_{MLImin.} = T_{SYS} = 1/f_{SYS}$. When f_{SYS} = 80 MHz, t_{10} = 25 ns and t_{20} = 12.5 ns.

2) The following formula is valid: $t_{11} + t_{12} = t_{10}$

3) The min./max. TCLK low/high times t_{11}/t_{12} include the PLL jitter of f_{SYS}. Fractional divider settings must be regarded additionally to t_{11}/t_{12}.

4) For high-speed MLI interface, strong driver sharp edge selection (class A2 pad) is recommended for TCLK.

5) The following formula is valid: $t_{21} + t_{22} = t_{20}$

6) The min. and max. value of is parameter can be adjusted by considering the other receiver timing parameters.

5.4 Package and Reliability

5.4.1 Package Parameters

Table 25 Thermal Parameters (Operating Conditions apply)

Device	Package	$R_{\Theta JCT}$ 1)	$R_{\Theta JCB}$ 1)	$R_{\Theta JLeads}$ 1)	Unit	Note
TC1167	PG-LQFP-176-5	6.5	5.5	23	K/W	

1) The top and bottom thermal resistances between the case and the ambient (R_{TCAT}, R_{TCAB}) are to be combined with the thermal resistances between the junction and the case given above (R_{TJCT}, R_{TJCB}), in order to calculate the total thermal resistance between the junction and the ambient (R_{TJA}). The thermal resistances between the case and the ambient (R_{TCAT}, R_{TCAB}) depend on the external system (PCB, case) characteristics, and are under user responsibility.
The junction temperature can be calculated using the following equation: $T_J = T_A + R_{TJA} \times P_D$, where the R_{TJA} is the total thermal resistance between the junction and the ambient. This total junction ambient resistance R_{TJA} can be obtained from the upper four partial thermal resistances.
Thermal resistances as measured by the ‘cold plate method’ (MIL SPEC-883 Method 1012.1).

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