Renesas Electronics America Inc - M38039FFLHP#U0 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	740
Core Size	8-Bit
Speed	16.8MHz
Connectivity	SIO, UART/USART
Peripherals	LED, PWM, WDT
Number of I/O	56
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m38039fflhp-u0

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GROUP EXPANSION

Renesas plans to expand the 3803 group (Spec.L) as follows.

Memory Size

- Flash memory size .....60 Kbytes
- Mask ROM size .....60 Kbytes
- RAM size ..... 2048 bytes

Packages

- PRDP0064BA-A (64P4B)
  .....64-pin shrink plastic-molded DIP
- PLQP0064KB-A (64P6Q-A)
  .....0.5 mm-pitch plastic molded LQFP
- PLQP0064GA-A (64P6U-A)
  .....0.8 mm-pitch plastic molded LQFP
- PTLG0064JA-A (64F0G)
  .....0.65 mm-pitch plastic molded FLGA

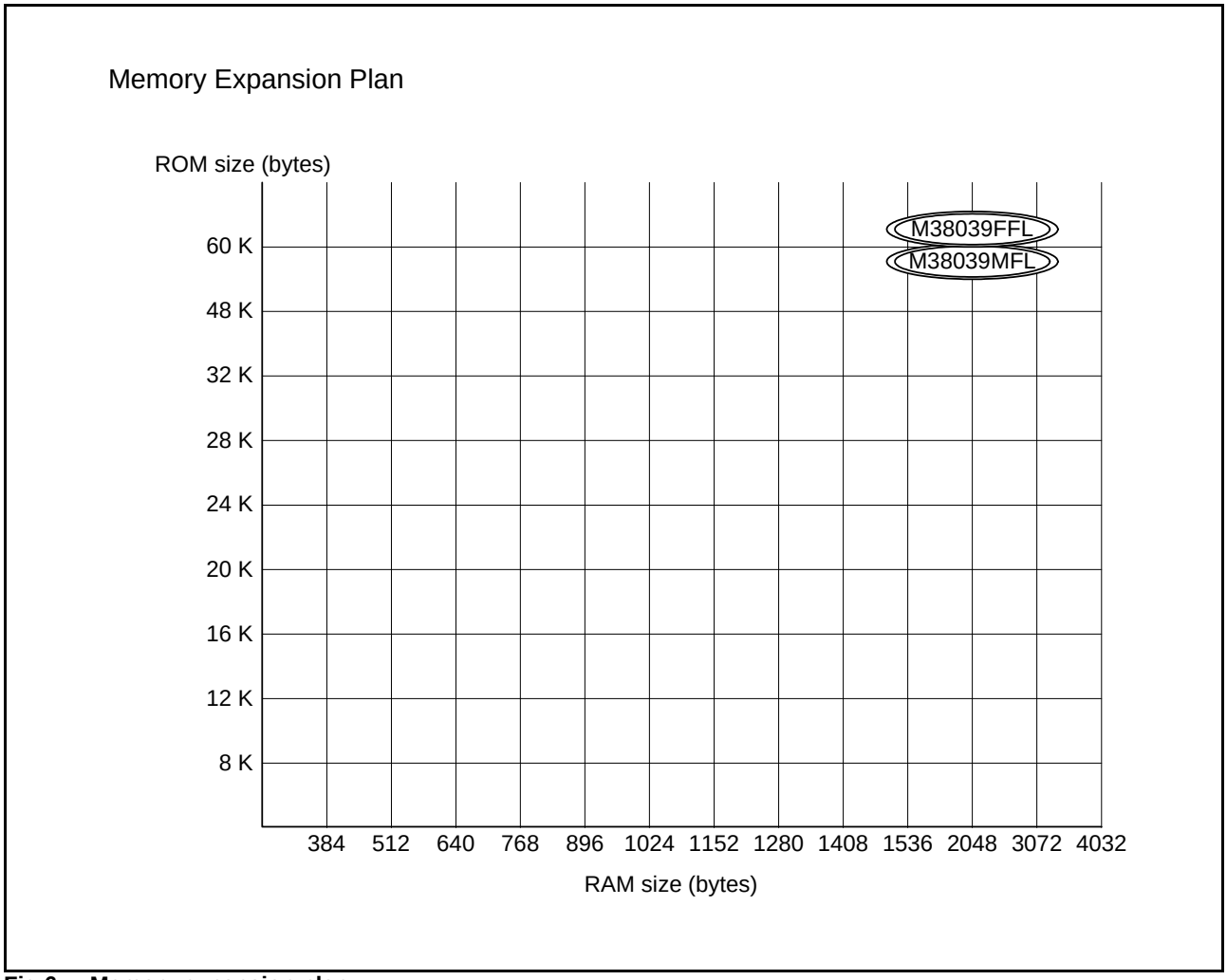


Fig 6. Memory expansion plan

Table 3 Support products

Part No.	ROM size (bytes) ROM size for User in ( )	RAM size (bytes)	Package	Remarks
M38039MFL-XXXSP	61440 (61310)	2048	PRDP0064BA-A (64P4B)	Mask ROM version
M38039MFL-XXXHP			PLQP0064KB-A (64P6Q-A)	
M38039MFL-XXXKP			PLQP0064GA-A (64P6U-A)	
M38039MFL-XXXWG			PTLG0064JA-A (64F0G)	
M38039FFLSP	57344+4096 (NOTE)	2048	PRDP0064BA-A (64P4B)	Flash memory version V_{CC} = 2.7 to 5.5 V
M38039FFLHP			PLQP0064KB-A (64P6Q-A)	
M38039FFLKP			PLQP0064GA-A (64P6U-A)	
M38039FFLWG			PTLG0064JA-A (64F0G)	

NOTE:
1. ROM size includes the ID code area.

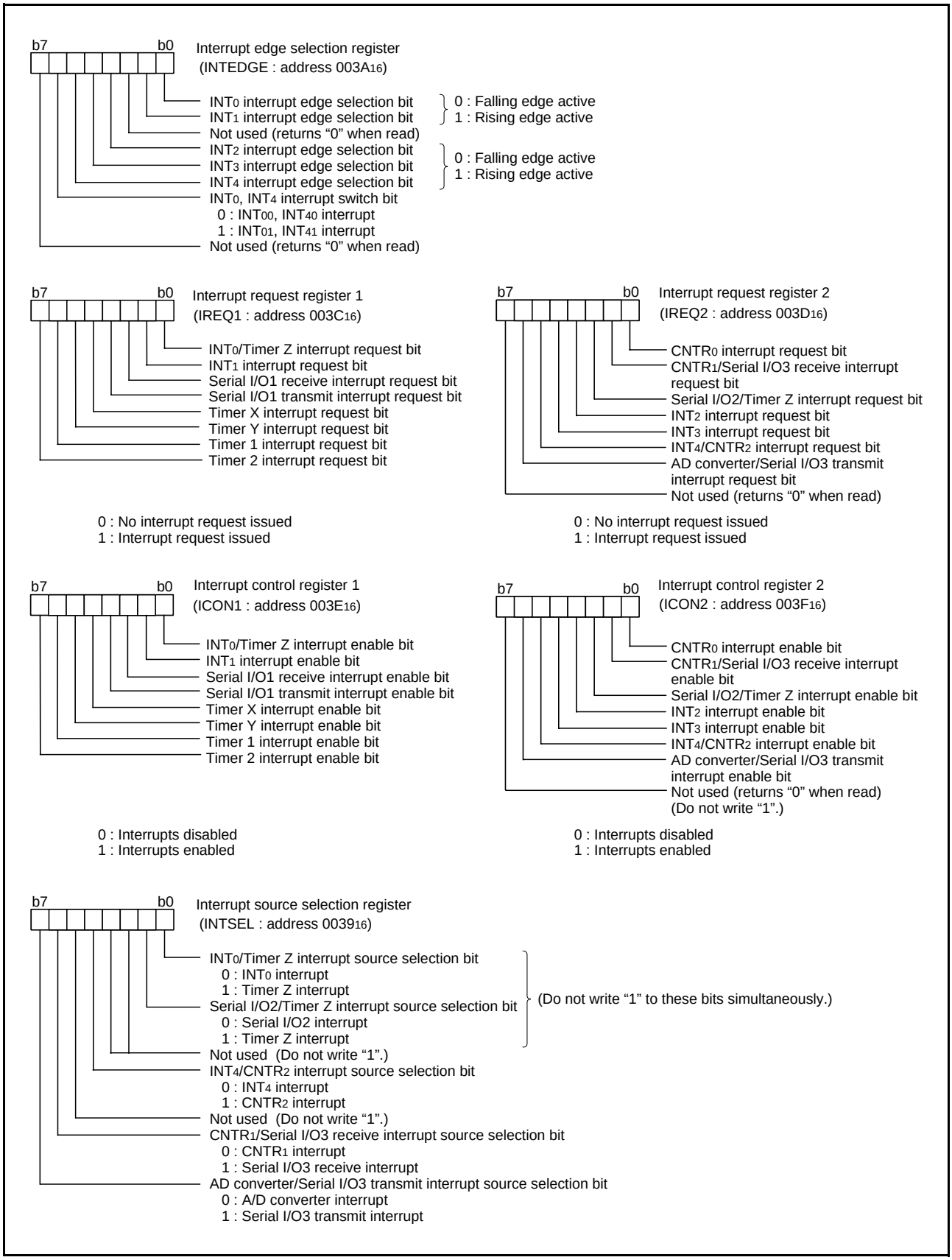


Fig 21. Structure of interrupt-related registers

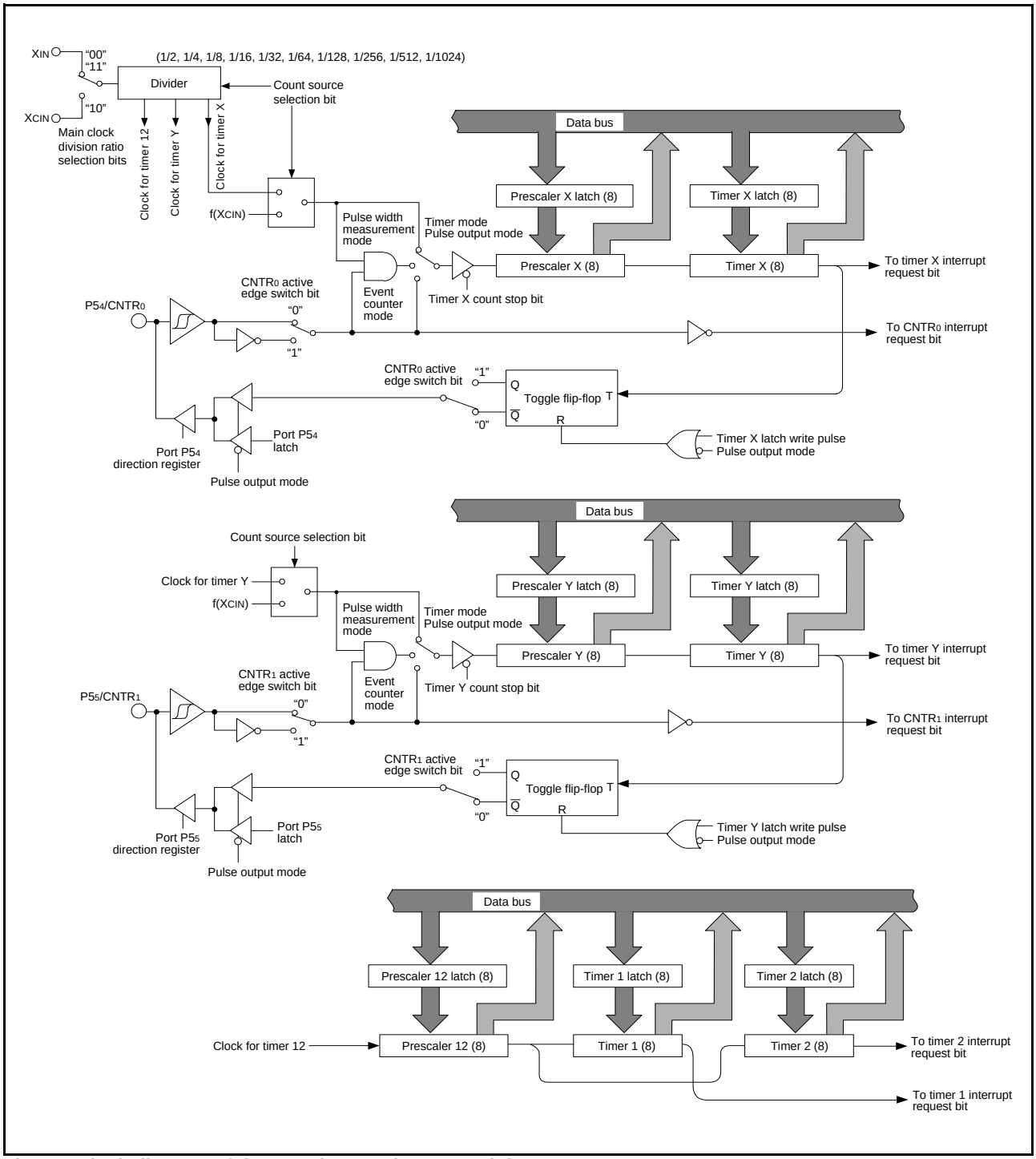


Fig 25. Block diagram of timer X, timer Y, timer 1, and timer 2

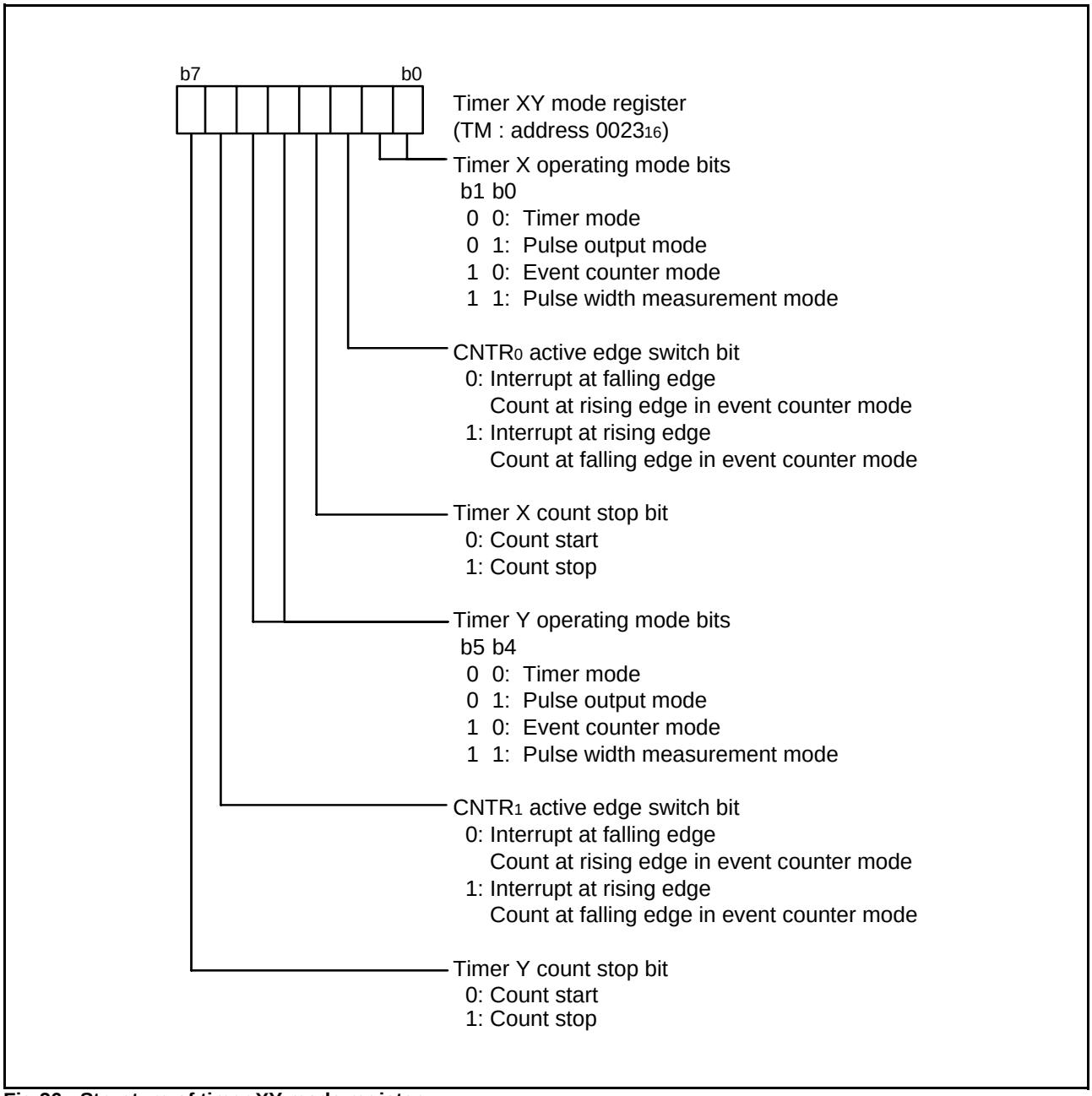


Fig 26. Structure of timer XY mode register

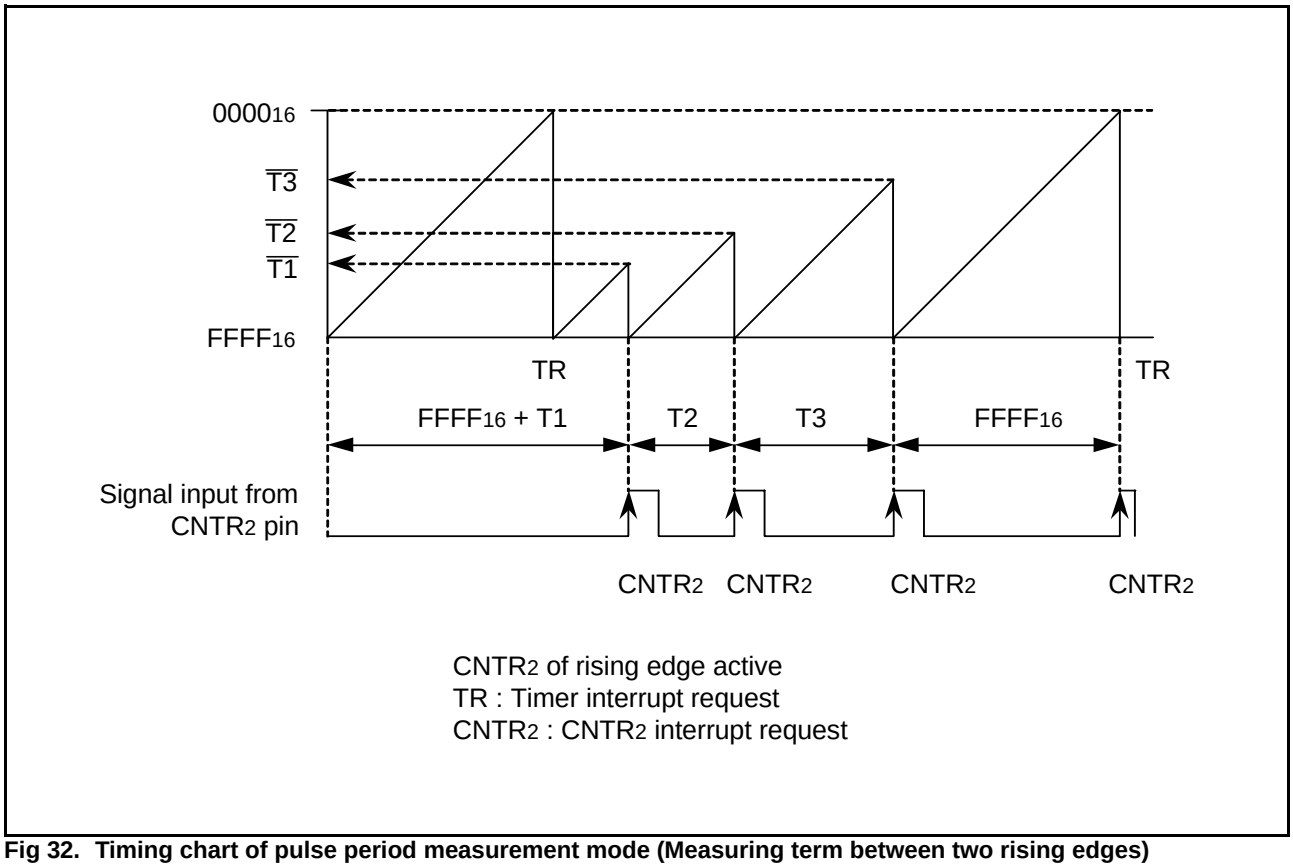


Fig 32. Timing chart of pulse period measurement mode (Measuring term between two rising edges)

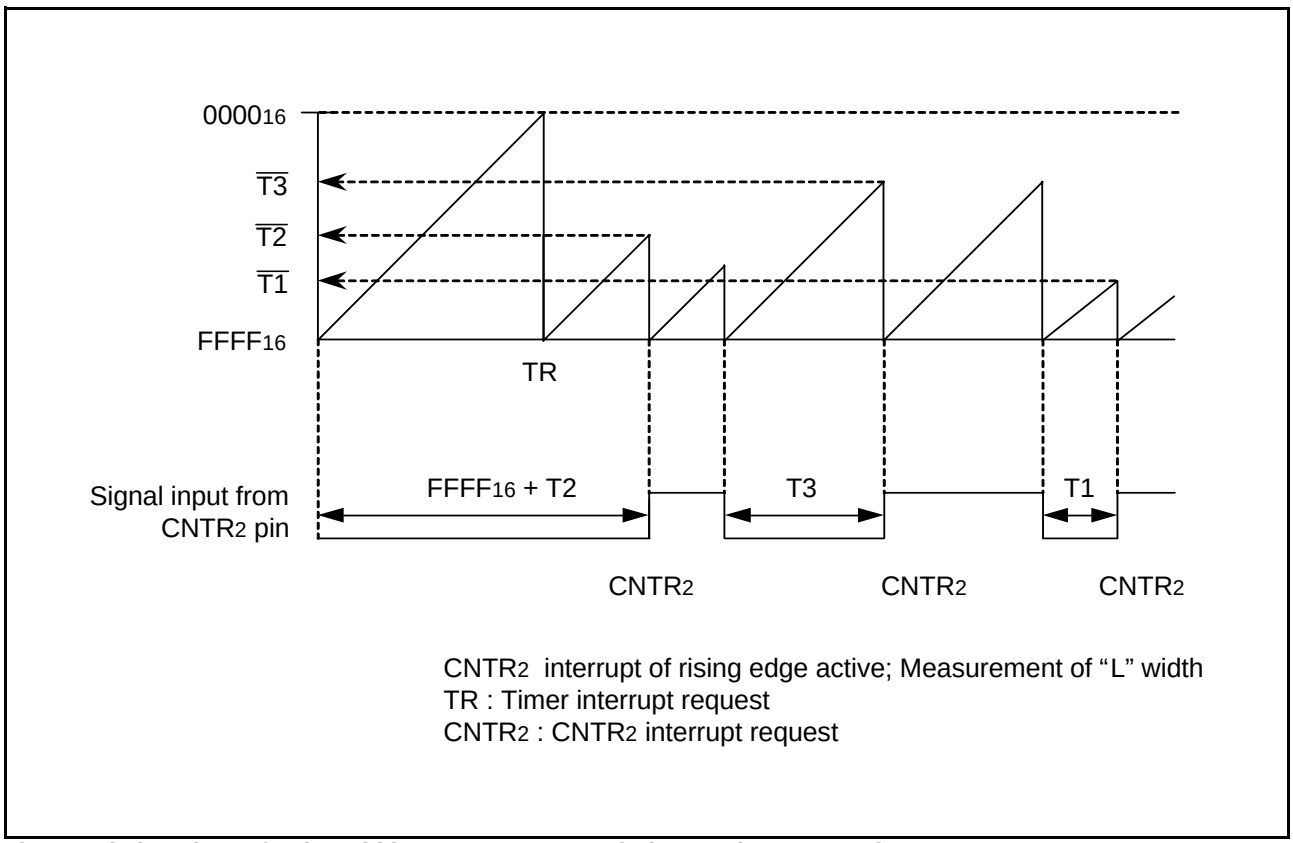


Fig 33. Timing chart of pulse width measurement mode (Measuring “L” term)

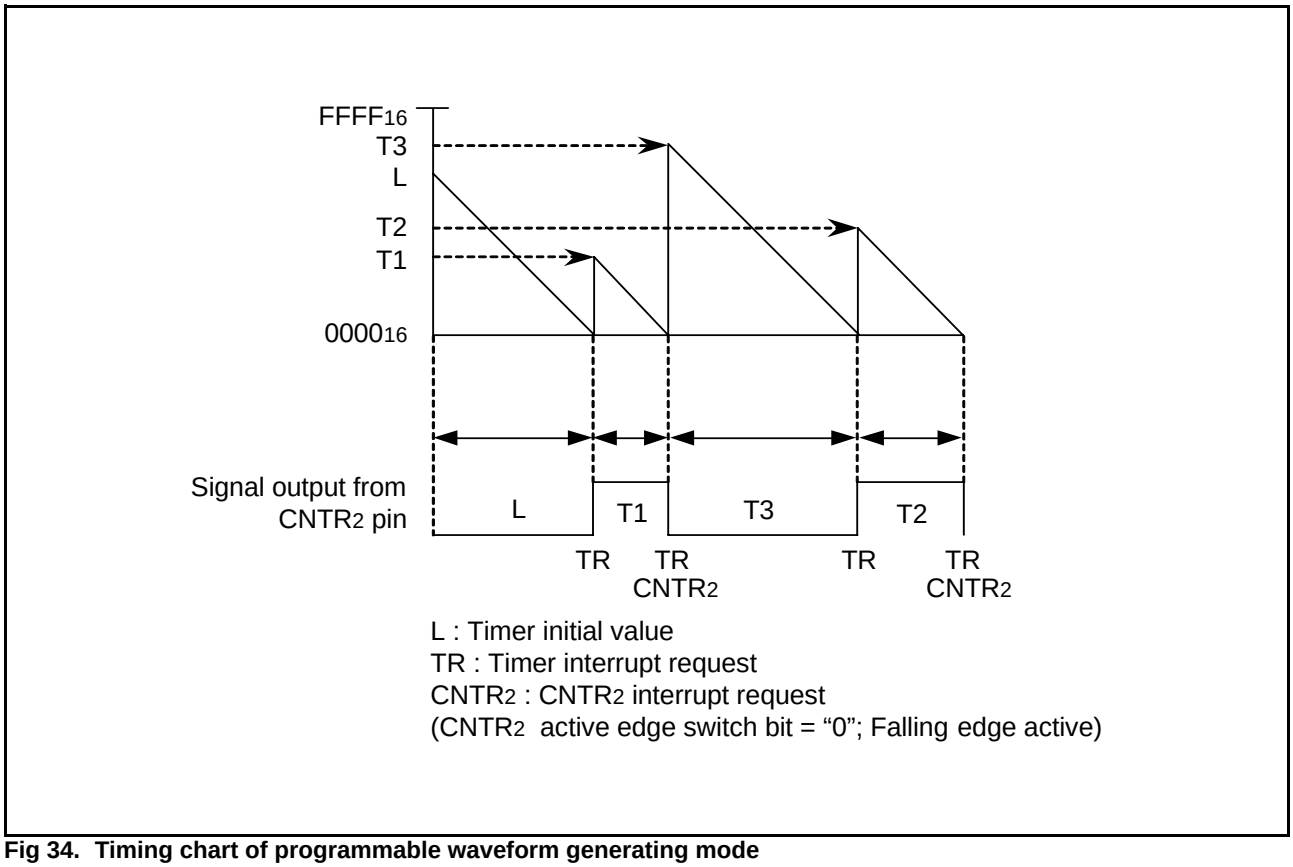


Fig 34. Timing chart of programmable waveform generating mode

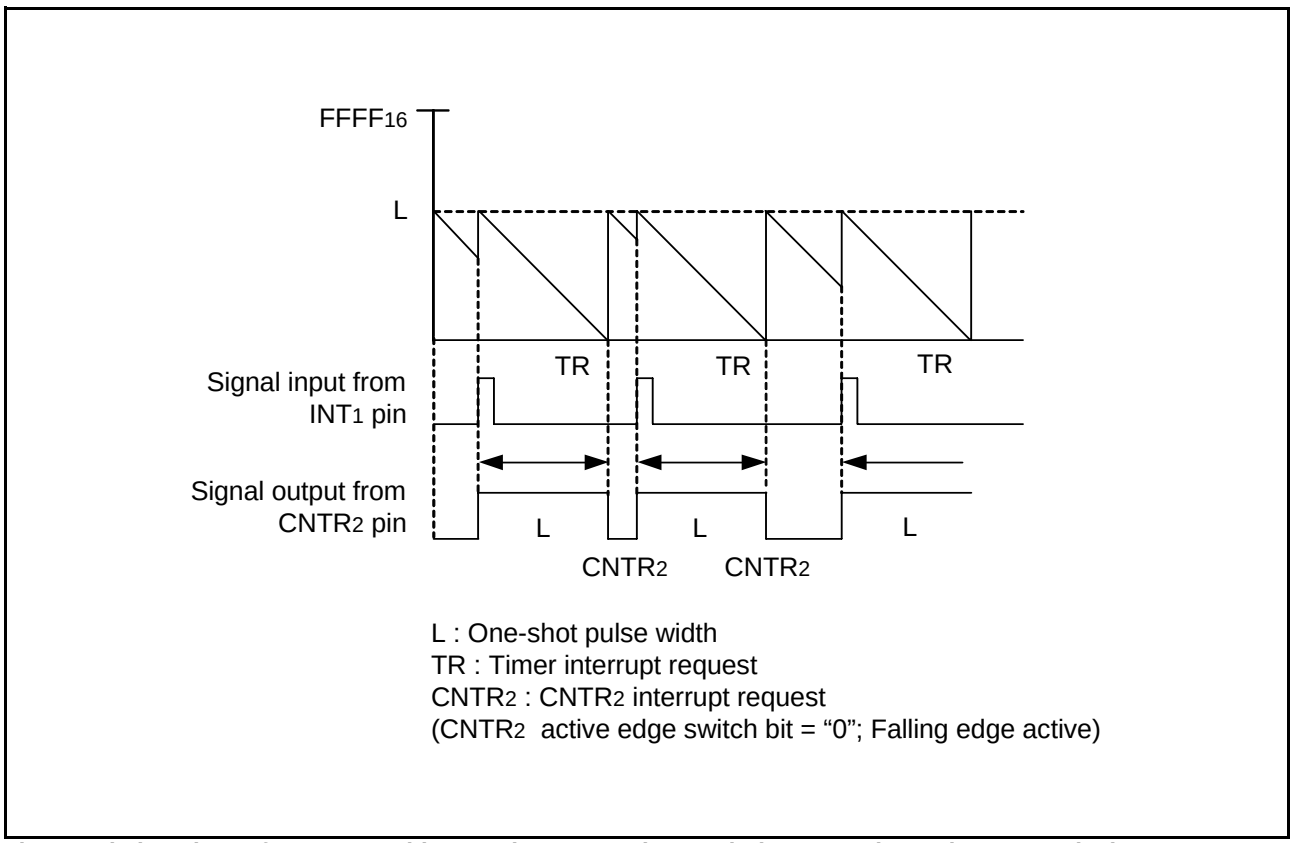
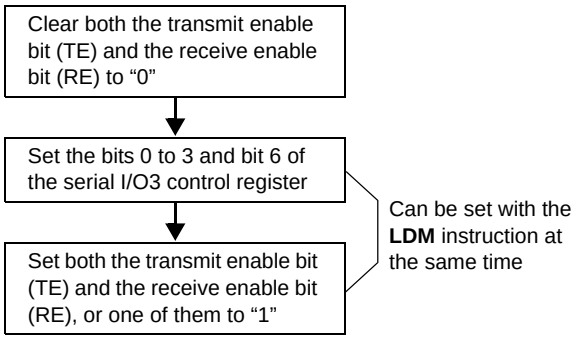


Fig 35. Timing chart of programmable one-shot generating mode (“H” one-shot pulse generating)

3. $\overline{\text{SRDY3}}$ output of reception side
- Note
  When signals are output from the $\overline{\text{SRDY3}}$ pin on the reception side by using an external clock in the clock synchronous serial I/O mode, set all of the receive enable bit, the $\overline{\text{SRDY3}}$ output enable bit, and the transmit enable bit to “1” (transmit enabled).

4. Setting serial I/O3 control register again
- Note
  Set the serial I/O3 control register again after the transmission and the reception circuits are reset by clearing both the transmit enable bit and the receive enable bit to “0”.



5.Data transmission control with referring to transmit shift register completion flag
- Note
  After the transmit data is written to the transmit buffer register, the transmit shift register completion flag changes from “1” to “0” with a delay of 0.5 to 1.5 shift clocks. When data transmission is controlled with referring to the flag after writing the data to the transmit buffer register, note the delay.

6. Transmission control when external clock is selected
- Note
  When an external clock is used as the synchronous clock for data transmission, set the transmit enable bit to “1” at “H” of the SCLK3 input level. Also, write data to the transmit buffer register at “H” of the SCLK input level.

7. Transmit interrupt request when transmit enable bit is set
- Note
  When using the transmit interrupt, take the following sequence.
  1. Set the serial I/O3 transmit interrupt enable bit to “0” (disabled).
  2. Set the transmit enable bit to “1”.
  3. Set the serial I/O3 transmit interrupt request bit to “0” after 1 or more instruction has executed.
  4. Set the serial I/O3 transmit interrupt enable bit to “1” (enabled).

- Reason
  When the transmit enable bit is set to “1”, the transmit buffer empty flag and the transmit shift register shift completion flag are also set to “1”. Therefore, regardless of selecting which timing for the generating of transmit interrupts, the interrupt request is generated and the transmit interrupt request bit is set at this point.

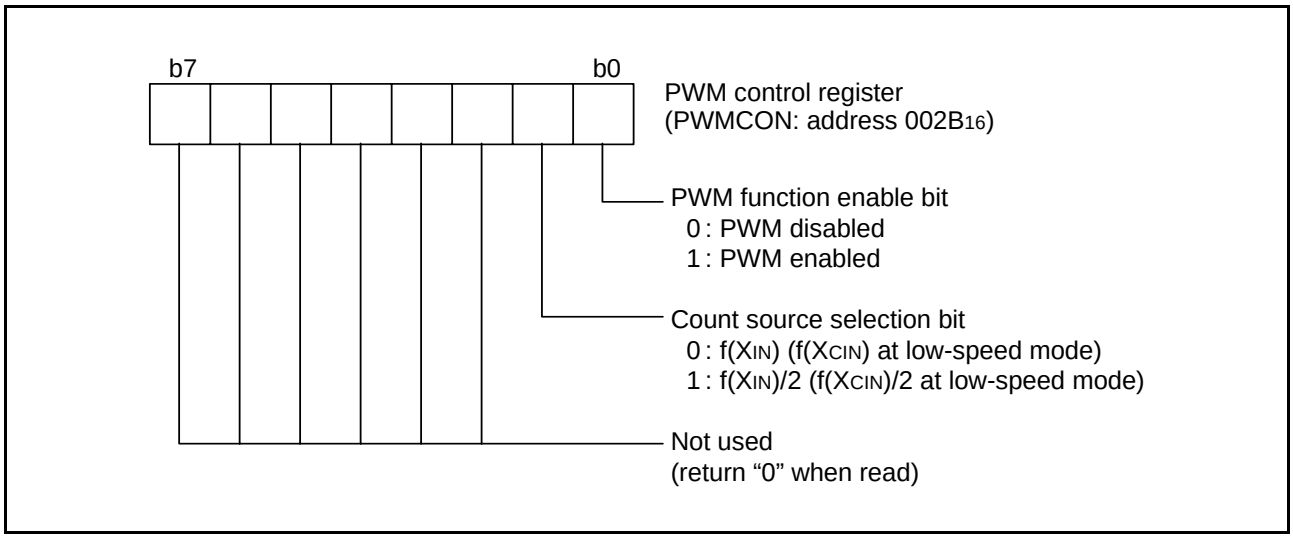


Fig 51. Structure of PWM control register

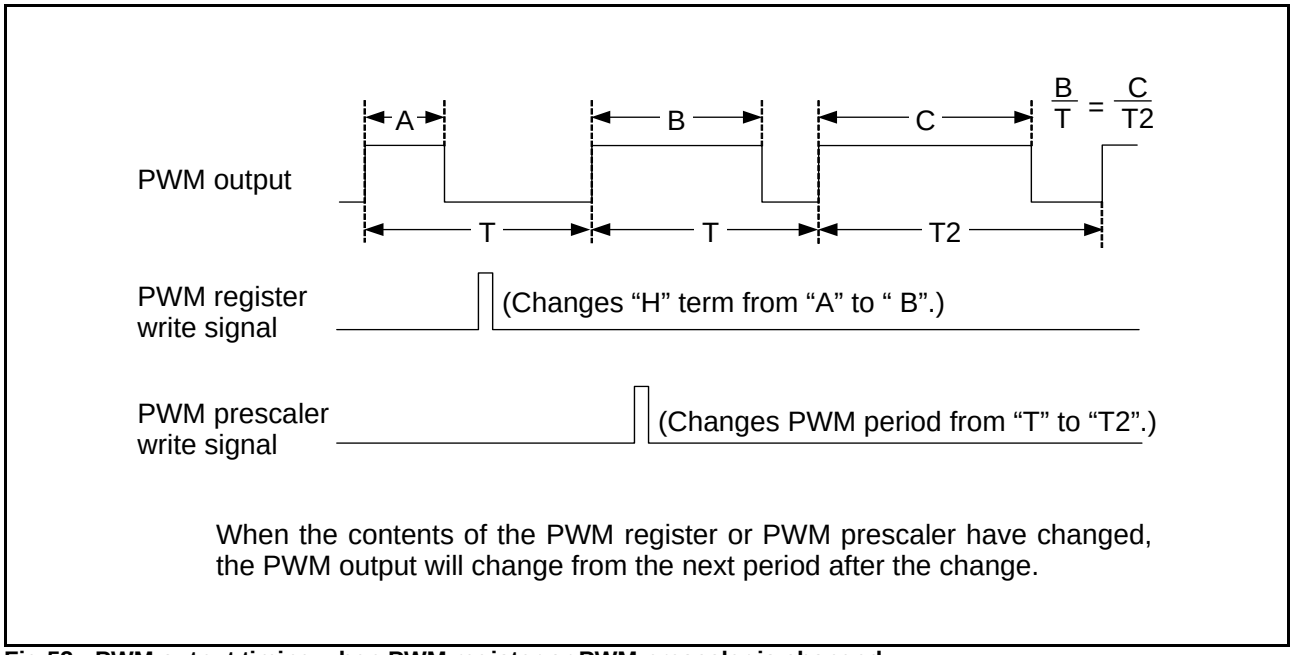


Fig 52. PWM output timing when PWM register or PWM prescaler is changed

<Notes>

The PWM starts after the PWM function enable bit is set to enable and “L” level is output from the PWM pin.
The length of this “L” level output is as follows:

$\frac{n+1}{2 \times f(X_{IN})}$ sec (Count source selection bit = 0, where n is the value set in the prescaler)

$\frac{n+1}{f(X_{IN})}$ sec (Count source selection bit = 1, where n is the value set in the prescaler)

A/D CONVERTER (successive approximation type)

[AD Conversion Register 1, 2 (AD1, AD2)] 0035$_{16}$, 0038$_{16}$

The AD conversion register is a read-only register that stores the result of an A/D conversion. When reading this register during an A/D conversion, the previous conversion result is read.

Bit 7 of the AD conversion register 2 is the conversion mode selection bit. When this bit is set to "0", the A/D converter becomes the 10-bit A/D mode. When this bit is set to "1", that becomes the 8-bit A/D mode. The conversion result of the 8-bit A/D mode is stored in the AD conversion register 1. As for 10-bit A/D mode, not only 10-bit reading but also only high-order 8-bit reading of conversion result can be performed by selecting the reading procedure of the AD conversion registers 1, 2 after A/D conversion is completed (in Figure 54).

As for 10-bit A/D mode, the 8-bit reading inclined to MSB is performed when reading the AD converter register 1 after A/D conversion is started; and when the AD converter register 1 is read after reading the AD converter register 2, the 8-bit reading inclined to LSB is performed.

[AD/DA Control Register (ADCON)] 0034$_{16}$

The AD/DA control register controls the A/D conversion process. Bits 0 to 2 and bit 4 select a specific analog input pin. Bit 3 signals the completion of an A/D conversion. The value of this bit remains at "0" during an A/D conversion, and changes to "1" when an A/D conversion ends. Writing "0" to this bit starts the A/D conversion.

• Comparison Voltage Generator

The comparison voltage generator divides the voltage between AVSS and VREF into 1024, and that outputs the comparison voltage in the 10-bit A/D mode (256 division in 8-bit A/D mode). The A/D converter successively compares the comparison voltage Vref in each mode, dividing the VREF voltage (see below), with the input voltage.

- 10-bit A/D mode (10-bit reading)

$$Vref = \frac{VREF}{1024} \times n \ (n = 0 – 1023)$$

- 10-bit A/D mode (8-bit reading)

$$Vref = \frac{VREF}{256} \times n \ (n = 0 – 255)$$

- 8-bit A/D mode

$$Vref = \frac{VREF}{256} \times (n – 0.5) \ (n = 1 – 255)$$

$$= 0 \qquad (n = 0)$$

• Channel Selector

The channel selector selects one of ports P67/AN7 to P60/AN0 or P07/AN15 to P00/AN8, and inputs the voltage to the comparator.

• Comparator and Control Circuit

The comparator and control circuit compares an analog input voltage with the comparison voltage, and then stores the result in the AD conversion registers 1, 2. When an A/D conversion is completed, the control circuit sets the AD conversion completion bit and the AD interrupt request bit to "1".

Note that because the comparator consists of a capacitor coupling, set f(XIN) to 500 kHz or more during an A/D conversion.

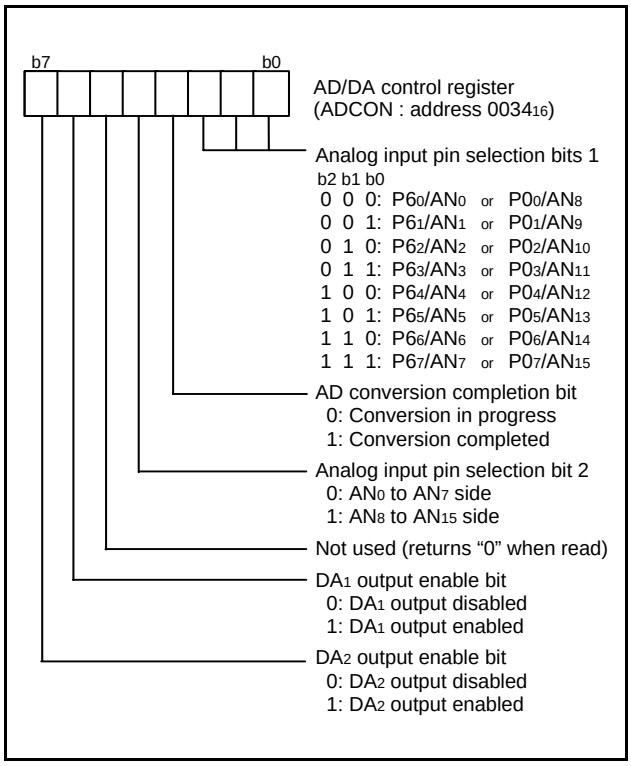


Fig 53. Structure of AD/DA control register

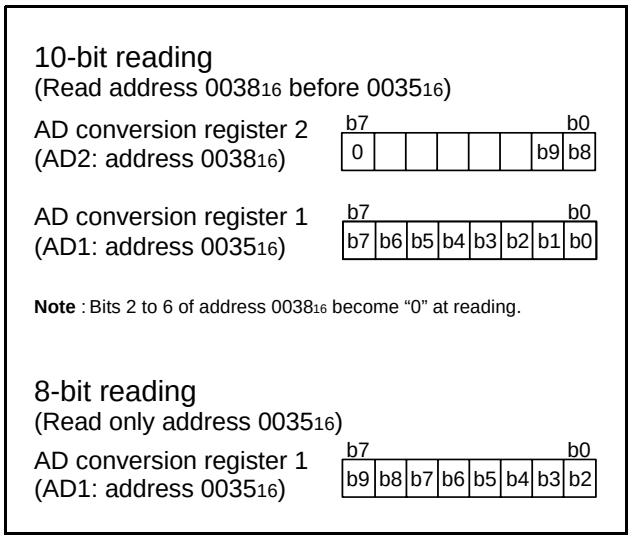


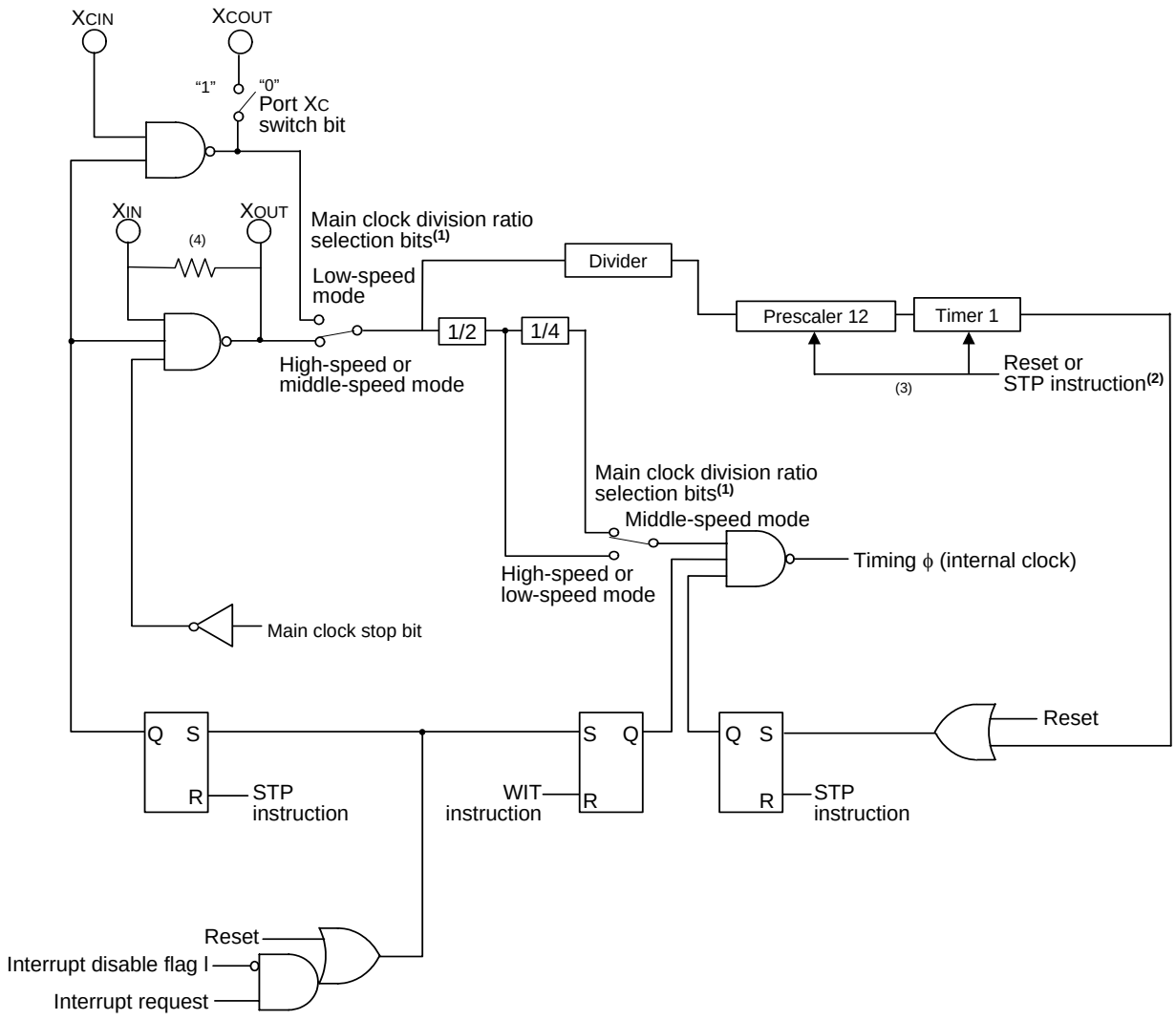
Fig 54. Structure of 10-bit A/D mode reading

		Address	Register contents
(1)	Port P0 (P0)	0000_{16}	00_{16}
(2)	Port P0 direction register (P0D)	0001_{16}	00_{16}
(3)	Port P1 (P1)	0002_{16}	00_{16}
(4)	Port P1 direction register (P1D)	0003_{16}	00_{16}
(5)	Port P2 (P2)	0004_{16}	00_{16}
(6)	Port P2 direction register (P2D)	0005_{16}	00_{16}
(7)	Port P3 (P3)	0006_{16}	00_{16}
(8)	Port P3 direction register (P3D)	0007_{16}	00_{16}
(9)	Port P4 (P4)	0008_{16}	00_{16}
(10)	Port P4 direction register (P4D)	0009_{16}	00_{16}
(11)	Port P5 (P5)	$000A_{16}$	00_{16}
(12)	Port P5 direction register (P5D)	$000B_{16}$	00_{16}
(13)	Port P6 (P6)	$000C_{16}$	00_{16}
(14)	Port P6 direction register (P6D)	$000D_{16}$	00_{16}
(15)	Timer 12, X count source selection register (T12XCSS)	$000E_{16}$	0 0 1 1 0 0 1 1
(16)	Timer Y, Z count source selection register (TYZCSS)	$000F_{16}$	0 0 1 1 0 0 1 1
(17)	MISRG	0010_{16}	00_{16}
(18)	Transmit/Receive buffer register 1 (TB1/RB1)	0018_{16}	X X X X X X X X
(19)	Serial I/O1 status register (SIO1STS)	0019_{16}	1 0 0 0 0 0 0 0
(20)	Serial I/O1 control register (SIO1CON)	$001A_{16}$	00_{16}
(21)	UART1 control register (UART1CON)	$001B_{16}$	1 1 1 0 0 0 0 0
(22)	Baud rate generator 1 (BRG1)	$001C_{16}$	X X X X X X X X
(23)	Serial I/O2 control register (SIO2CON)	$001D_{16}$	00_{16}
(24)	Watchdog timer control register (WDTCON)	$001E_{16}$	0 0 1 1 1 1 1 1
(25)	Serial I/O2 register (SIO2)	$001F_{16}$	X X X X X X X X
(26)	Prescaler 12 (PRE12)	0020_{16}	FF_{16}
(27)	Timer 1 (T1)	0021_{16}	01_{16}
(28)	Timer 2 (T2)	0022_{16}	FF_{16}
(29)	Timer XY mode register (TM)	0023_{16}	00_{16}
(30)	Prescaler X (PREX)	0024_{16}	FF_{16}
(31)	Timer X (TX)	0025_{16}	FF_{16}
(32)	Prescaler Y (PREY)	0026_{16}	FF_{16}
(33)	Timer Y (TY)	0027_{16}	FF_{16}

		Address	Register contents
(34)	Timer Z (low-order) (TZL)	0028_{16}	FF_{16}
(35)	Timer Z (high-order) (TZH)	0029_{16}	FF_{16}
(36)	Timer Z mode register (TZM)	$002A_{16}$	00_{16}
(37)	PWM control register (PWMCON)	$002B_{16}$	00_{16}
(38)	PWM prescaler (PREPWM)	$002C_{16}$	X X X X X X X X
(39)	PWM register (PWM)	$002D_{16}$	X X X X X X X X
(40)	Baud rate generator 3 (BRG3)	$002F_{16}$	X X X X X X X X
(41)	Transmit/Receive buffer register 3 (TB3/RB3)	0030_{16}	X X X X X X X X
(42)	Serial I/O3 status register (SIO3STS)	0031_{16}	1 0 0 0 0 0 0 0
(43)	Serial I/O3 control register (SIO3CON)	0032_{16}	00_{16}
(44)	UART3 control register (UART3CON)	0033_{16}	1 1 1 0 0 0 0 0
(45)	AD/DA control register (ADCON)	0034_{16}	0 0 0 0 1 0 0 0
(46)	AD conversion register 1 (AD1)	0035_{16}	X X X X X X X X
(47)	DA1 conversion register (DA1)	0036_{16}	00_{16}
(48)	DA2 conversion register (DA2)	0037_{16}	00_{16}
(49)	AD conversion register 2 (AD2)	0038_{16}	0 0 0 0 0 0 X X
(50)	Interrupt source selection register (INTSEL)	0039_{16}	00_{16}
(51)	Interrupt edge selection register (INTEDGE)	$003A_{16}$	00_{16}
(52)	CPU mode register (CPUM)	$003B_{16}$	0 1 0 0 1 0 0 0
(53)	Interrupt request register 1 (IREQ1)	$003C_{16}$	00_{16}
(54)	Interrupt request register 2 (IREQ2)	$003D_{16}$	00_{16}
(55)	Interrupt control register 1 (ICON1)	$003E_{16}$	00_{16}
(56)	Interrupt control register 2 (ICON2)	$003F_{16}$	00_{16}
(57)	Flash memory control register 0 (FMCR0)	$0FE0_{16}$	0 0 0 0 0 0 0 1
(58)	Flash memory control register 1 (FMCR1)	$0FE0_{16}$	0 1 0 0 0 0 0 0
(59)	Flash memory control register 2 (FMCR2)	$0FE2_{16}$	0 1 0 0 0 1 0 1
(60)	Port P0 pull-up control register (PULL0)	$0FF0_{16}$	00_{16}
(61)	Port P1 pull-up control register (PULL1)	$0FF1_{16}$	00_{16}
(62)	Port P2 pull-up control register (PULL2)	$0FF2_{16}$	00_{16}
(63)	Port P3 pull-up control register (PULL3)	$0FF3_{16}$	00_{16}
(64)	Port P4 pull-up control register (PULL4)	$0FF4_{16}$	00_{16}
(65)	Port P5 pull-up control register (PULL5)	$0FF5_{16}$	00_{16}
(66)	Port P6 pull-up control register (PULL6)	$0FF6_{16}$	00_{16}
(67)	Processor status register	(PS)	X X X X X 1 X X
(68)	Program counter	(PC_H)	$FFFD_{16}$ contents
		(PC_L)	$FFFC_{16}$ contents

Note : X: Not fixed.
Since the initial values for other than above mentioned registers and RAM contents are indefinite at reset, they must be set.

Fig 62. Internal status at reset



Notes 1: Either high-speed, middle-speed or low-speed mode is selected by bits 7 and 6 of the CPU mode register. When low-speed mode is selected, set port X_C switch bit (b4) to "1".

2: f(X_{IN})/16 is supplied as the count source to the prescaler 12 at reset, the count source before executing the STP instruction is supplied as the count source at executing STP instruction.

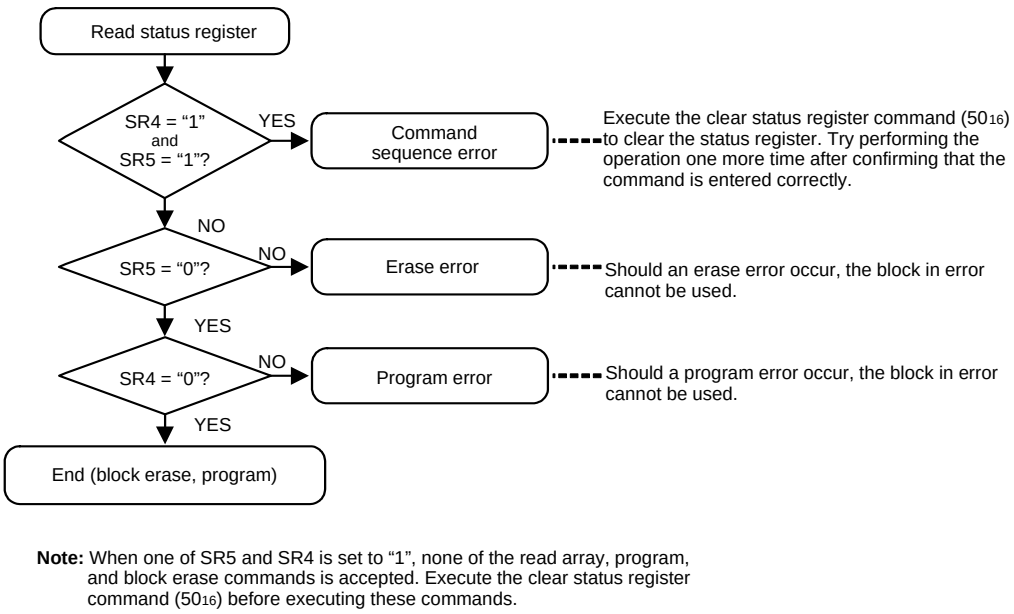
3: When bit 0 of MISRG is "0", timer 1 is set "01_{16}" and prescaler 12 is set "FF_{16}" automatically. When bit 0 of MISRG is "1" , set the appropriate value to them in accordance with oscillation stabilizing time required by the using oscillator because nothing is automatically set into timer 1 and prescaler 12.

4: Although a feed-back resistor exists on-chip, an external feed-back resistor may be needed depending on conditions.

Fig 65. System clock generating circuit block diagram (Single-chip mode)

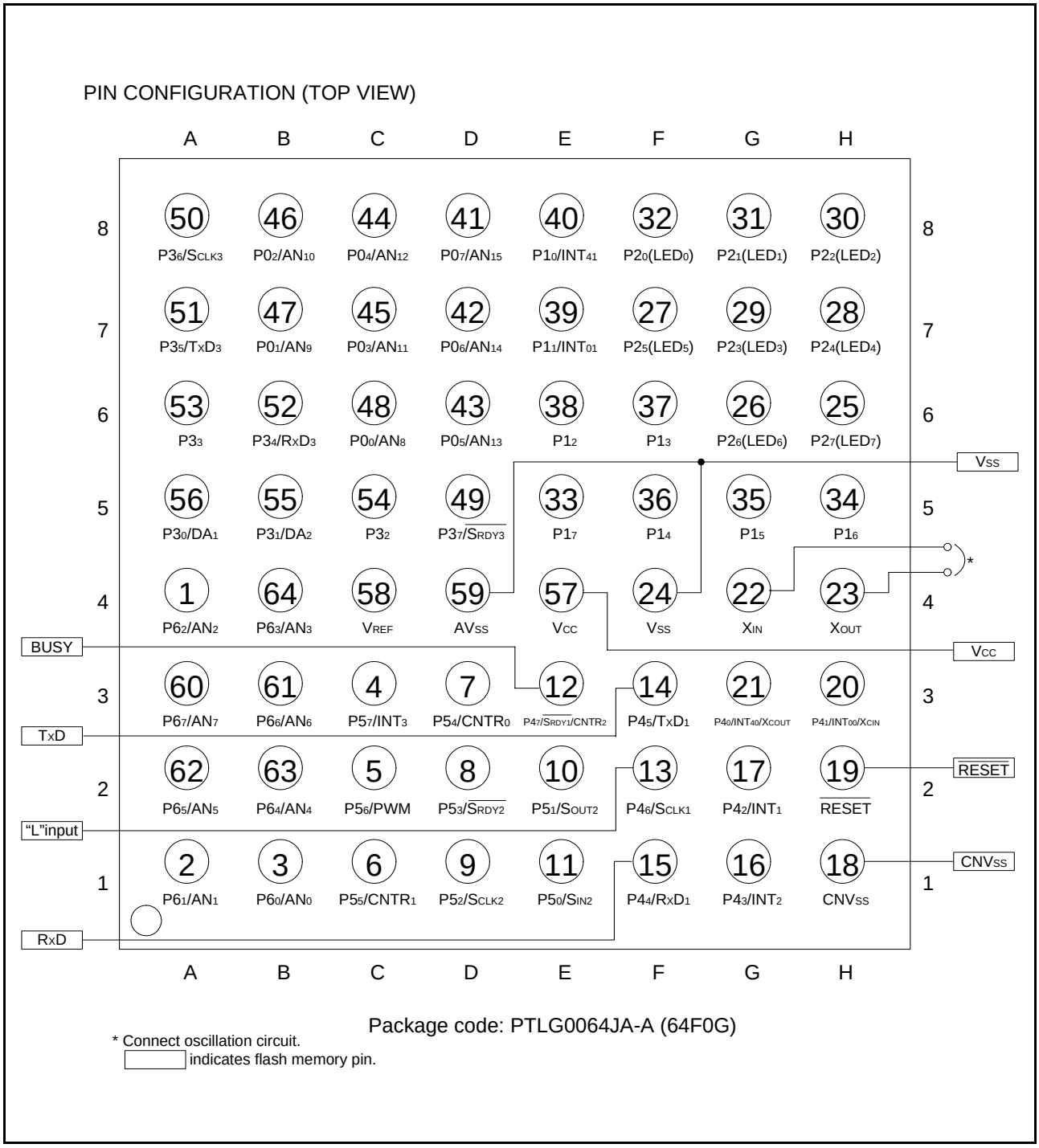
Full Status Check

By performing full status check, it is possible to know the execution results of erase and program operations. Figure 74 shows a full status check flowchart and the action to be taken when each error occurs.



Note: When one of SR5 and SR4 is set to "1", none of the read array, program, and block erase commands is accepted. Execute the clear status register command (50_{16}) before executing these commands.

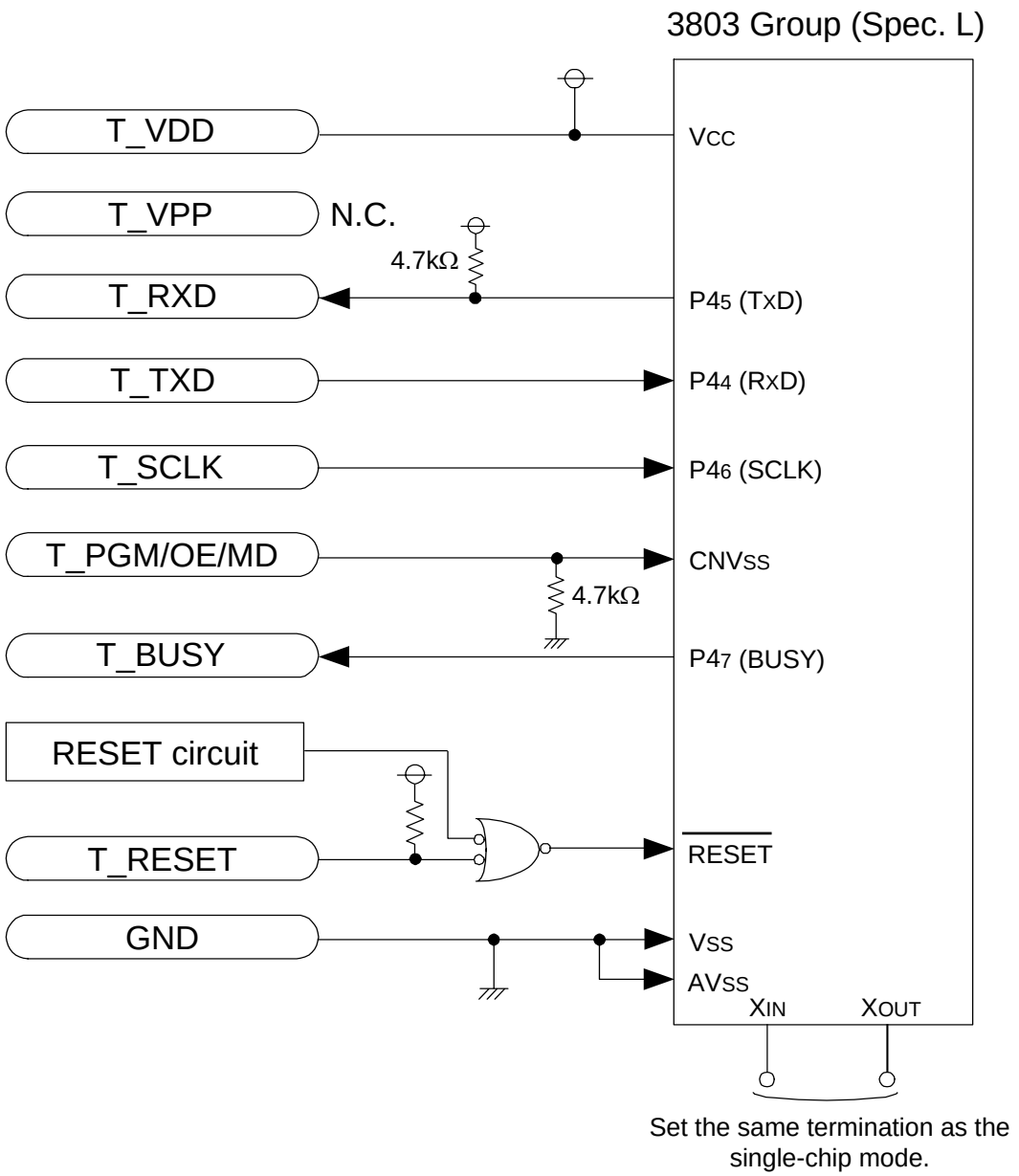
Fig 74. Full status check flowchart and remedial procedure for errors



Package code: PTLG0064JA-A (64F0G)

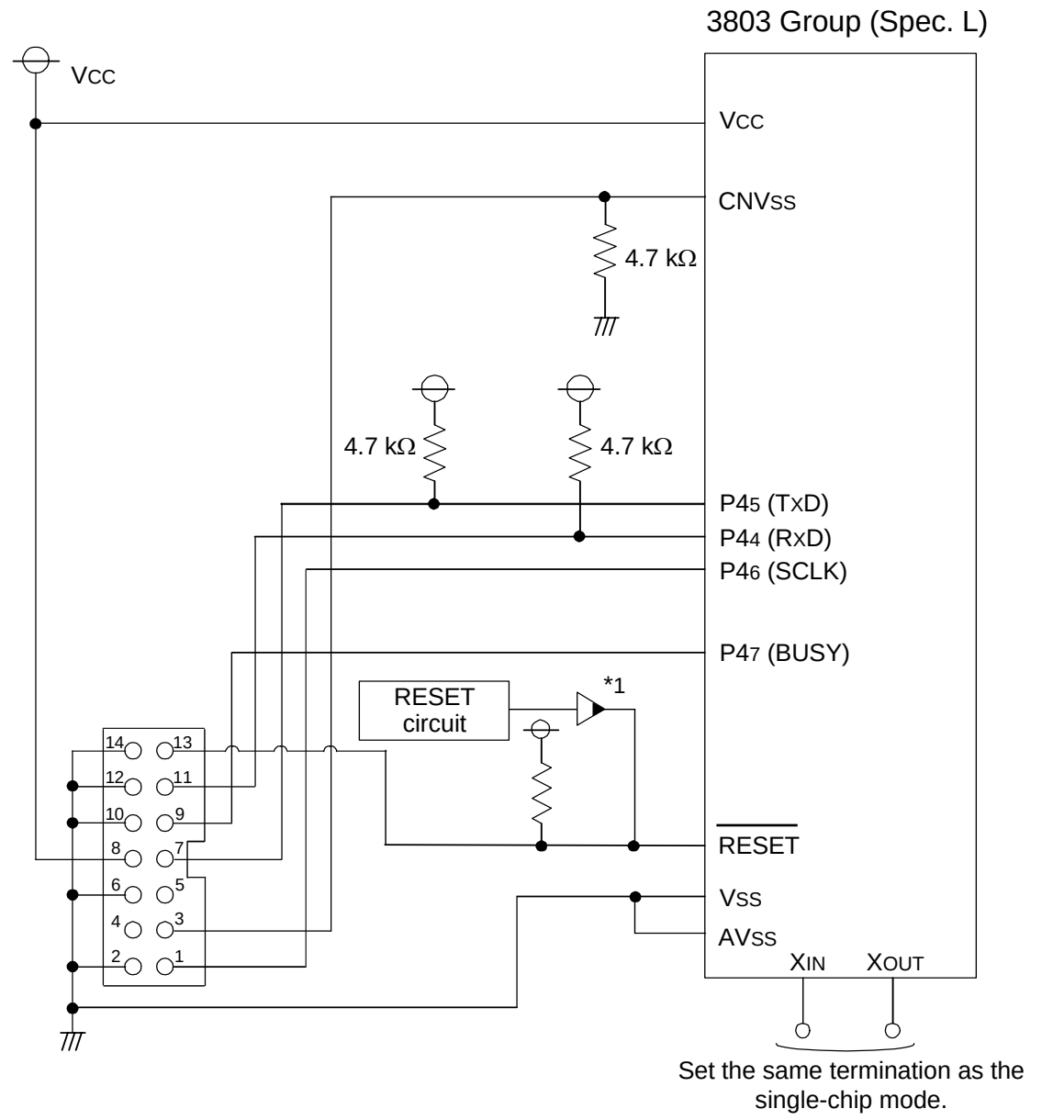
* Connect oscillation circuit.
□ indicates flash memory pin.

Fig 82. Connection for standard serial I/O mode 2 (M38039FFLWG)



Note: For the programming circuit, the wiring capacity of each signal pin must not exceed 47 pF.

Fig 85. When using programmer (in standard serial I/O mode 1) of Suisei Electronics System Co., LTD, connection example



*1 : Open-collector buffer

Note : For the programming circuit, the wiring capacity of each signal pin must not exceed 47 pF.

Fig 86. When using E8 programmer (in standard serial I/O mode 1), connection example

ELECTRICAL CHARACTERISTICS

Absolute maximum ratings

Table 16 Absolute maximum ratings

Symbol	Parameter		Conditions	Ratings	Unit
V_{CC}	Power source voltages		All voltages are based on V_{SS}. When an input voltage is measured, output transistors are cut off.	–0.3 to 6.5	V
V_I	Input voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$, $P3_1$, $P3_4$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, V_{REF}		–0.3 to V_{CC} + 0.3	V
V_I	Input voltage	$P3_2$, $P3_3$		–0.3 to 5.8	V
V_I	Input voltage	$\overline{RESET}$, X_{IN}		–0.3 to V_{CC} + 0.3	V
V_I	Input voltage	CNV_{SS}		–0.3 to V_{CC} + 0.3	V
V_O	Output voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$, $P3_1$, $P3_4$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, X_{OUT}		–0.3 to V_{CC} + 0.3	V
V_O	Output voltage	$P3_2$, $P3_3$		–0.3 to 5.8	V
P_d	Power dissipation		Ta=25 °C	1000(1)	mW
T_{opr}	Operating temperature		—	–20 to 85	°C
T_{stg}	Storage temperature		—	–65 to 125	°C

NOTE:
1. This value is 300 mW except SP package.

Table 19 Recommended operating conditions (3)
(Mask ROM version: V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)
(Flash memory version: V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$\Sigma I_{OH(peak)}$	"H" total peak output current(1)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$, $P3_1$, $P3_4$-$P3_7$			–80	mA
$\Sigma I_{OH(peak)}$	"H" total peak output current(1)	$P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$			–80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current(1)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P3_0$-$P3_7$			80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current(1)	$P2_0$-$P2_7$			80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current(1)	$P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$			80	mA
$\Sigma I_{OH(avg)}$	"H" total average output current(1)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$, $P3_1$, $P3_4$-$P3_7$			–40	mA
$\Sigma I_{OH(avg)}$	"H" total average output current(1)	$P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$			–40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current(1)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P3_0$-$P3_7$			40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current(1)	$P2_0$-$P2_7$			40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current(1)	$P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$			40	mA
$I_{OH(peak)}$	"H" peak output current(2)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$, $P3_1$, $P3_4$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$			–10	mA
$I_{OL(peak)}$	"L" peak output current(2)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$			10	mA
$I_{OL(peak)}$	"L" peak output current(2)	$P2_0$-$P2_7$			20	mA
$I_{OH(avg)}$	"H" average output current(3)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$, $P3_1$, $P3_4$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$			–5	mA
$I_{OL(avg)}$	"L" average output current(3)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$			5	mA
$I_{OL(avg)}$	"L" average output current(3)	$P2_0$-$P2_7$			10	mA

NOTES:
1. The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.
2. The peak output current is the peak current flowing in each port.
3. The average output current I_{OL}(avg), I_{OH}(avg) are average value measured over 100 ms.

A/D converter characteristics

Table 23 A/D converter recommended operating conditions (Mask ROM version)
(V_{CC} = 2.0 to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Power source voltage (When A/D converter is used)	8-bit A/D mode(1)	2.0	5.0	5.5	V
		10-bit A/D mode(2)	2.2	5.0	5.5	
V_{REF}	Analog convert reference voltage		2.0		V_{CC}	V
AV_{SS}	Analog power source voltage			0		V
V_{IA}	Analog input voltage AN_0-AN_{15}		0		V_{CC}	V
f(X_{IN})	Main clock input oscillation frequency (When A/D converter is used)	2.0 ≤ V_{CC} = V_{REF} < 2.2 V	0.5		$\frac{(20 \times V_{CC} - 36) \times 1.05}{2}$	MHz
		2.2 ≤ V_{CC} = V_{REF} < 2.7 V	0.5		$\frac{(24 \times V_{CC} - 40.8) \times 1.05}{3}$	
		2.7 ≤ V_{CC} = V_{REF} < 4.0 V	0.5		$\frac{(9 \times V_{CC} - 0.3) \times 1.05}{3}$	
		4.0 ≤ V_{CC} = V_{REF} < 4.5 V	0.5		$\frac{(24.6 \times V_{CC} - 62.7) \times 1.05}{3}$	
		4.5 ≤ V_{CC} = V_{REF} ≤ 5.5 V	0.5		16.8	

NOTES:
1. 8-bit A/D mode: When the conversion mode selection bit (bit 7 of address 0038_{16}) is “1”.
2. 10-bit A/D mode: When the conversion mode selection bit (bit 7 of address 0038_{16}) is “0”.

Table 24 A/D converter characteristics (Mask ROM version)
(V_{CC} = 2.0 to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits			Unit
					Min.	Typ.	Max.	
–	Resolution		8-bit A/D mode(1)				8	bit
			10-bit A/D mode(2)				10	
–	Absolute accuracy (excluding quantization error)		8-bit A/D mode(1)	2.0 ≤ V_{REF} < 2.2 V			±3	LSB
				2.2 ≤ V_{REF} ≤ 5.5 V			±2	
			10-bit A/D mode(2)	2.2 ≤ V_{REF} < 2.7 V			±5	LSB
				2.7 ≤ V_{REF} ≤ 5.5 V			±4	
t_{CONV}	Conversion time		8-bit A/D mode(1)				50	2tc(X_{IN})
			10-bit A/D mode(2)				61	
R_{LADDER}	Ladder resistor				12	35	100	kΩ
I_{VREF}	Reference power source input current	at A/D converter operated	V_{REF} = 5.0 V		50	150	200	μA
		at A/D converter stopped	V_{REF} = 5.0 V				5.0	μA
$I_{I(AD)}$	A/D port input current						5.0	μA

NOTES:
1. 8-bit A/D mode: When the conversion mode selection bit (bit 7 of address 0038_{16}) is “1”.
2. 10-bit A/D mode: When the conversion mode selection bit (bit 7 of address 0038_{16}) is “0”.

D/A converter characteristics

Table 25 D/A converter characteristics (Mask ROM version)
(V_{CC} = 2.7 to 5.5 V, V_{REF} = 2.7 V to V_{CC}, V_{SS} = AV_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
–	Resolution				8	bit
–	Absolute accuracy	4.0 ≤ V_{REF} ≤ 5.5 V			1.0	%
		2.7 ≤ V_{REF} < 4.0 V			2.5	
tsu	Setting time				3	μs
RO	Output resistor		2	3.5	5	kΩ
I_{VREF}	Reference power source input current(1)				3.2	mA

NOTE:
1. Using one D/A converter, with the value in the DA conversion register of the other D/A converter being “00_{16}”.

Table 32 Switching characteristics (1)
(Mask ROM version: V_{CC} = 2.0 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)
(Flash memory version: V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
$t_{WH}(S_{CLK1})$ $t_{WH}(S_{CLK3})$	Serial I/O1, serial I/O3 clock output “H” pulse width	4.5 ≤ V_{CC} ≤ 5.5 V	Fig.100	$t_C(S_{CLK1})/2-30$, $t_C(S_{CLK3})/2-30$			ns
		4.0 ≤ V_{CC} < 4.5 V		$t_C(S_{CLK1})/2-35$, $t_C(S_{CLK3})/2-35$			
		2.7 ≤ V_{CC} < 4.0 V		$t_C(S_{CLK1})/2-40$, $t_C(S_{CLK3})/2-40$			
		2.2 ≤ V_{CC} < 2.7 V		$t_C(S_{CLK1})/2-45$, $t_C(S_{CLK3})/2-45$			
		2.0 ≤ V_{CC} < 2.2 V		$t_C(S_{CLK1})/2-50$, $t_C(S_{CLK3})/2-50$			
$t_{WL}(S_{CLK1})$ $t_{WL}(S_{CLK3})$	Serial I/O1, serial I/O3 clock output “L” pulse width	4.5 ≤ V_{CC} ≤ 5.5 V		$t_C(S_{CLK1})/2-30$, $t_C(S_{CLK3})/2-30$			ns
		4.0 ≤ V_{CC} < 4.5 V		$t_C(S_{CLK1})/2-35$, $t_C(S_{CLK3})/2-35$			
		2.7 ≤ V_{CC} < 4.0 V		$t_C(S_{CLK1})/2-40$, $t_C(S_{CLK3})/2-40$			
		2.2 ≤ V_{CC} < 2.7 V		$t_C(S_{CLK1})/2-45$, $t_C(S_{CLK3})/2-45$			
		2.0 ≤ V_{CC} < 2.2 V		$t_C(S_{CLK1})/2-50$, $t_C(S_{CLK3})/2-50$			
$t_d(S_{CLK1}\text{-}T_xD_1)$ $t_d(S_{CLK3}\text{-}T_xD_3)$	Serial I/O1, serial I/O3 output delay time(1)	4.5 ≤ V_{CC} ≤ 5.5 V				140	ns
		4.0 ≤ V_{CC} < 4.5 V				200	
		2.7 ≤ V_{CC} < 4.0 V				350	
		2.2 ≤ V_{CC} < 2.7 V				400	
		2.0 ≤ V_{CC} < 2.2 V				420	
$t_v(S_{CLK1}\text{-}T_xD_1)$ $t_v(S_{CLK3}\text{-}T_xD_3)$	Serial I/O1, serial I/O3 output valid time(1)	4.5 ≤ V_{CC} ≤ 5.5 V		–30			ns
		4.0 ≤ V_{CC} < 4.5 V		–30			
		2.7 ≤ V_{CC} < 4.0 V		–30			
		2.2 ≤ V_{CC} < 2.7 V		–30			
		2.0 ≤ V_{CC} < 2.2 V		–30			
$t_r(S_{CLK1})$ $t_r(S_{CLK3})$	Serial I/O1, serial I/O3 rise time of clock output	4.5 ≤ V_{CC} ≤ 5.5 V				30	ns
		4.0 ≤ V_{CC} < 4.5 V				35	
		2.7 ≤ V_{CC} < 4.0 V				40	
		2.2 ≤ V_{CC} < 2.7 V				45	
		2.0 ≤ V_{CC} < 2.2 V				50	
$t_f(S_{CLK1})$ $t_f(S_{CLK3})$	Serial I/O1, serial I/O3 fall time of clock output	4.5 ≤ V_{CC} ≤ 5.5 V				30	ns
		4.0 ≤ V_{CC} < 4.5 V				35	
		2.7 ≤ V_{CC} < 4.0 V				40	
		2.2 ≤ V_{CC} < 2.7 V				45	
		2.0 ≤ V_{CC} < 2.2 V				50	
$t_{WH}(S_{CLK2})$	Serial I/O2 clock output “H” pulse width	4.5 ≤ V_{CC} ≤ 5.5 V		$t_C(S_{CLK2})/2-160$			ns
		4.0 ≤ V_{CC} < 4.5 V		$t_C(S_{CLK2})/2-200$			
		2.7 ≤ V_{CC} < 4.0 V		$t_C(S_{CLK2})/2-240$			
		2.2 ≤ V_{CC} < 2.7 V		$t_C(S_{CLK2})/2-260$			
		2.0 ≤ V_{CC} < 2.2 V		$t_C(S_{CLK2})/2-280$			
$t_{WL}(S_{CLK2})$	Serial I/O2 clock output “L” pulse width	4.5 ≤ V_{CC} ≤ 5.5 V		$t_C(S_{CLK2})/2-160$			ns
		4.0 ≤ V_{CC} < 4.5 V		$t_C(S_{CLK2})/2-200$			
		2.7 ≤ V_{CC} < 4.0 V		$t_C(S_{CLK2})/2-240$			
		2.2 ≤ V_{CC} < 2.7 V		$t_C(S_{CLK2})/2-260$			
		2.0 ≤ V_{CC} < 2.2 V		$t_C(S_{CLK2})/2-280$			
$t_d(S_{CLK2}\text{-}S_{OUT2})$	Serial I/O2 output delay time	4.5 ≤ V_{CC} ≤ 5.5 V				200	ns
		4.0 ≤ V_{CC} < 4.5 V				250	
		2.7 ≤ V_{CC} < 4.0 V				300	
		2.2 ≤ V_{CC} < 2.7 V				350	
		2.0 ≤ V_{CC} < 2.2 V				400	
$t_v(S_{CLK2}\text{-}S_{OUT2})$	Serial I/O2 output valid time	4.5 ≤ V_{CC} ≤ 5.5 V			0		ns
		4.0 ≤ V_{CC} < 4.5 V			0		
		2.7 ≤ V_{CC} < 4.0 V			0		
		2.2 ≤ V_{CC} < 2.7 V			0		
		2.0 ≤ V_{CC} < 2.2 V			0		

NOTE:
1. When the $P4_5/T_xD_1$ P-channel output disable bit of the UART1 control register (bit 4 of address $001B_{16}$) is “0”.