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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	8051
Core Size	8-Bit
Speed	100MHz
Connectivity	EBI/EMI, SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	39
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 17x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f360-c-gqr

2. Absolute Maximum Ratings

Table 2.1. Absolute Maximum Ratings

Parameter	Conditions	Min	Typ	Max	Units
Ambient temperature under bias		–55	—	125	°C
Storage Temperature		–65	—	150	°C
Voltage on any Port I/O Pin or $\overline{\text{RST}}$ with respect to GND		–0.3	—	5.8	V
Voltage on V_{DD} with respect to GND		–0.3	—	4.2	V
Maximum Total current through V_{DD} or GND		—	—	500	mA
Maximum output current sunk by $\overline{\text{RST}}$ or any Port pin		—	—	100	mA

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

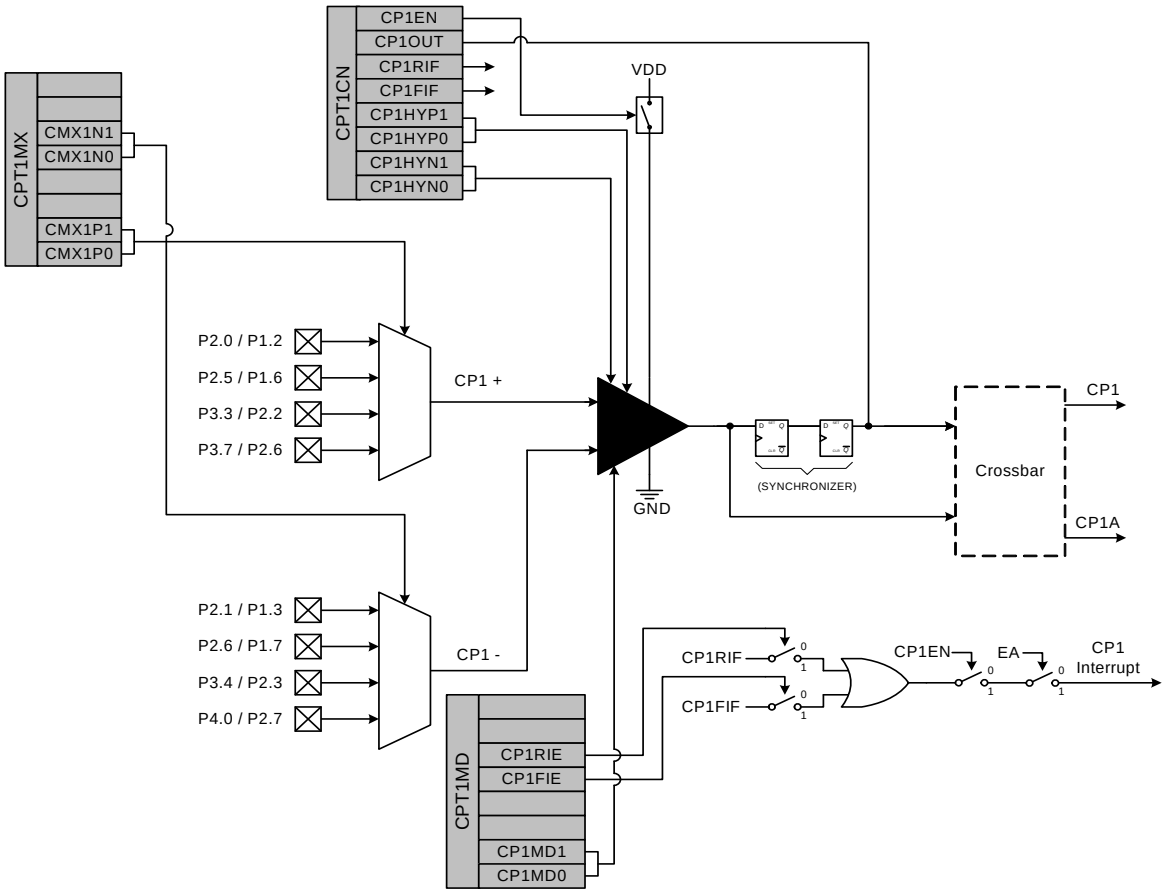


Figure 8.2. Comparator1 Functional Block Diagram

A Comparator output can be polled in software, used as an interrupt source, and/or routed to a Port pin. When routed to a Port pin, the Comparator outputs are available asynchronous or synchronous to the system clock; the asynchronous outputs are available even in STOP mode (with no system clock active). When disabled, the Comparator outputs (if assigned to a Port I/O pin via the Crossbar) default to the logic low state, and their supply current falls to less than 100 nA. See Section “17.1. Priority Crossbar Decoder” on page 184 for details on configuring Comparator outputs via the digital Crossbar. Comparator inputs can be externally driven from –0.25 V to (V_{DD}) + 0.25 V without damage or upset. The complete Comparator electrical specifications are given in Table 8.1.

The Comparator response time may be configured in software via the CPT0MD and CPT1MD registers (see SFR Definition 8.3 and SFR Definition 8.6). Selecting a longer response time reduces the Comparator supply current. See Table 8.1 for complete timing and power consumption specifications.

Table 9.3. Special Function Registers (Continued)

SFRs are listed in alphabetical order. All undefined SFR locations are reserved.

Register	Address	SFR Page	Description	Page No.
P0MAT	0xF3	0	Port 0 Match	page 191
P0MDIN	0xF1	F	Port 0 Input Mode	page 190
P0MDOUT	0xA4	F	Port 0 Output Mode Configuration	page 190
P0SKIP	0xD4	F	Port 0 Skip	page 191
P1	0x90	All Pages	Port 1 Latch	page 192
P1MASK	0xE2	0	Port 1 Mask	page 194
P1MAT	0xE1	0	Port 1 Match	page 193
P1MDIN	0xF2	F	Port 1 Input Mode	page 192
P1MDOUT	0xA5	F	Port 1 Output Mode Configuration	page 193
P1SKIP	0xD5	F	Port 1 Skip	page 193
P2	0xA0	All Pages	Port 2 Latch	page 194
P2MASK	0xB2	0	Port 2 Mask	page 196
P2MAT	0xB1	0	Port 2 Match	page 196
P2MDIN	0xF3	F	Port 2 Input Mode	page 195
P2MDOUT	0xA6	F	Port 2 Output Mode Configuration	page 195
P2SKIP	0xD6	F	Port 2 Skip	page 196
P3	0xB0	All Pages	Port 3 Latch	page 197
P3MDIN	0xF4	F	Port 3 Input Mode	page 197
P3MDOUT	0xAF	F	Port 3 Output Mode Configuration	page 198
P3SKIP	0xD7	F	Port 3 Skip	page 198
P4	0xB5	All Pages	Port 4 Latch	page 199
P4MDOUT	0xAE	F	Port 4 Output Mode Configuration	page 199
PCA0CN	0xD8	All Pages	PCA Control	page 274
PCA0CPH0	0xFC	All Pages	PCA Module 0 Capture/Compare High Byte	page 278
PCA0CPH1	0xEA	All Pages	PCA Module 1 Capture/Compare High Byte	page 278
PCA0CPH2	0xEC	All Pages	PCA Module 2 Capture/Compare High Byte	page 278
PCA0CPH3	0xEE	All Pages	PCA Module 3 Capture/Compare High Byte	page 278
PCA0CPH4	0xFE	All Pages	PCA Module 4 Capture/Compare High Byte	page 278
PCA0CPH5	0xF6	All Pages	PCA Module 5 Capture/Compare High Byte	page 278
PCA0CPL0	0xFB	All Pages	PCA Module 0 Capture/Compare Low Byte	page 277
PCA0CPL1	0xE9	All Pages	PCA Module 1 Capture/Compare Low Byte	page 277

Notes:
1. Refers to a register in the C8051F360/1/2/6/7/8/9 only.
2. Refers to a register in the C8051F360/3 only.

SFR Definition 10.5. EIE2: Extended Interrupt Enable 2

SFR Page: all pages
SFR Address: 0xE7

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
–	–	–	–	–	–	EMAT	–	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7–2: UNUSED. Read = 000000b. Write = don't care.
Bit 1: EMAT: Enable Port Match Interrupt.
This bit sets the masking of the Port Match interrupt.
0: Disable the Port Match interrupt.
1: Enable the Port Match interrupt.
Bit 0: UNUSED. Read = 0b. Write = don't care.

SFR Definition 10.6. EIP2: Extended Interrupt Priority 2

SFR Page: F
SFR Address: 0xCF

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
–	–	–	–	–	–	PMAT	–	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7–2: UNUSED. Read = 000000b. Write = don't care.
Bit 1: PMAT: Port Match Interrupt Priority Control.
This bit sets the priority of the Port Match interrupt.
0: Port Match interrupt set to low priority level.
1: Port Match interrupt set to high priority level.
Bit 0: UNUSED. Read = 0b. Write = don't care.

11.2. Integer and Fractional Math

MAC0 is capable of interpreting the 16-bit inputs stored in MAC0A and MAC0B as signed integers or as signed fractional numbers. When the MAC0FM bit (MAC0CF.1) is cleared to '0', the inputs are treated as 16-bit, 2's complement, integer values. After the operation, the accumulator will contain a 40-bit, 2's complement, integer value. Figure 11.2 shows how integers are stored in the SFRs.

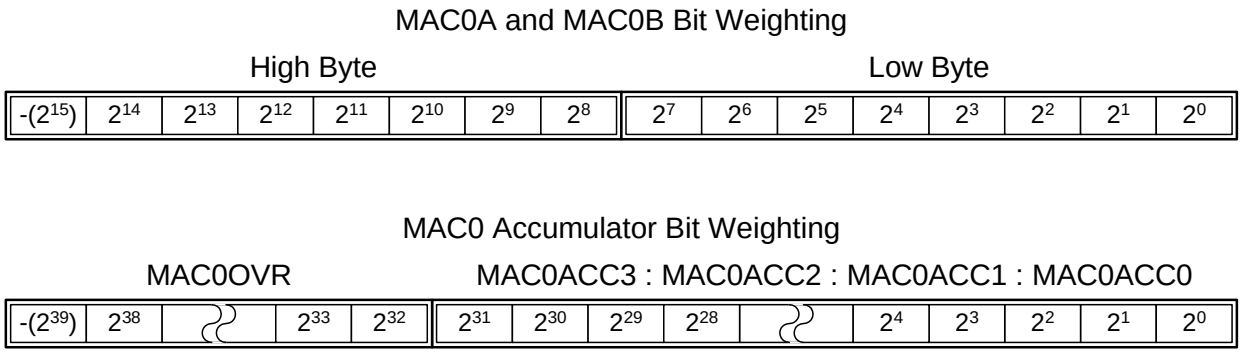
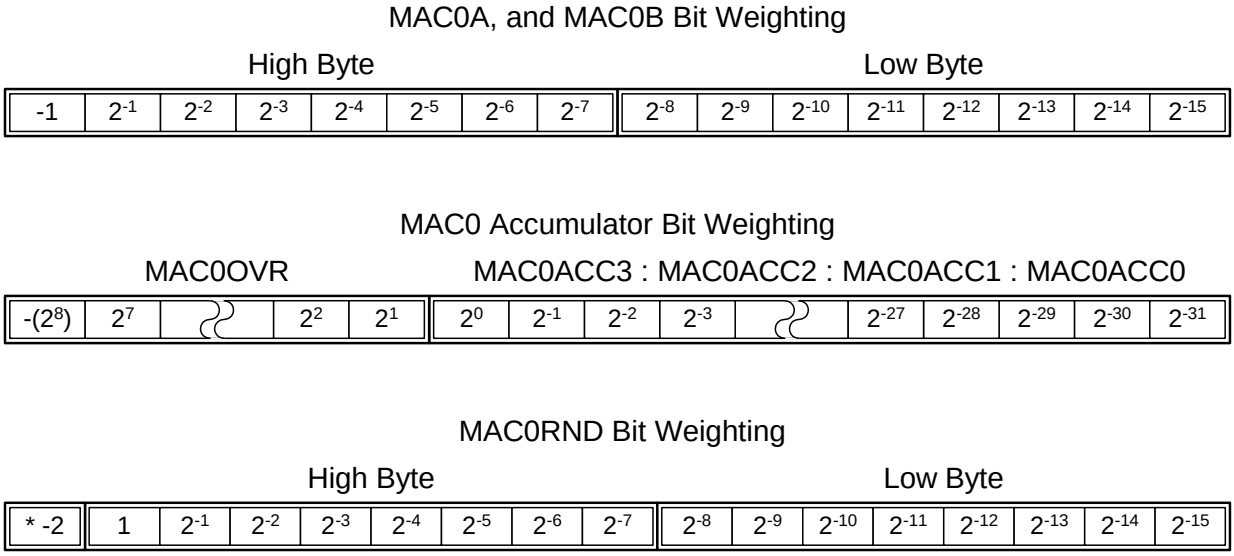


Figure 11.2. Integer Mode Data Representation

When the MAC0FM bit is set to '1', the inputs are treated at 16-bit, 2's complement, fractional values. The decimal point is located between bits 15 and 14 of the data word. After the operation, the accumulator will contain a 40-bit, 2's complement, fractional value, with the decimal point located between bits 31 and 30. Figure 11.3 shows how fractional numbers are stored in the SFRs.



* The MAC0RND register contains the 16 LSBs of a two's complement number. The MAC0N Flag can be used to determine the sign of the MAC0RND register.

Figure 11.3. Fractional Mode Data Representation

11.6. Rounding and Saturation

A Rounding Engine is included, which can be used to provide a rounded result when operating on fractional numbers. MAC0 uses an unbiased rounding algorithm to round the data stored in bits 31–16 of the accumulator, as shown in Table 11.1. Rounding occurs during the third stage of the MAC0 pipeline, after any shift operation, or on a write to the LSB of the accumulator. The rounded results are stored in the rounding registers: MAC0RNDH (SFR Definition 11.12) and MAC0RNDL (SFR Definition 11.13). The accumulator registers are not affected by the rounding engine. Although rounding is primarily used for fractional data, the data in the rounding registers is updated in the same way when operating in integer mode.

Table 11.1. MAC0 Rounding (MAC0SAT = 0)

Accumulator Bits 15–0 (MAC0ACC1:MAC0ACC0)	Accumulator Bits 31–16 (MAC0ACC3:MAC0ACC2)	Rounding Direction	Rounded Results (MAC0RNDH:MAC0RNDL)
Greater Than 0x8000	Anything	Up	(MAC0ACC3:MAC0ACC2) + 1
Less Than 0x8000	Anything	Down	(MAC0ACC3:MAC0ACC2)
Equal To 0x8000	Odd (LSB = 1)	Up	(MAC0ACC3:MAC0ACC2) + 1
Equal To 0x8000	Even (LSB = 0)	Down	(MAC0ACC3:MAC0ACC2)

The rounding engine can also be used to saturate the results stored in the rounding registers. If the MAC0SAT bit is set to ‘1’ and the rounding register overflows, the rounding registers will saturate. When a positive overflow occurs, the rounding registers will show a value of 0x7FFF when saturated. For a negative overflow, the rounding registers will show a value of 0x8000 when saturated. If the MAC0SAT bit is cleared to ‘0’, the rounding registers will not saturate.

11.7. Usage Examples

This section details some software examples for using MAC0. Section 11.7.1 shows a series of two MAC operations using fractional numbers. Section 11.7.2 shows a single operation in Multiply Only mode with integer numbers. The last example, shown in Section 11.7.3, demonstrates how the left-shift and right-shift operations can be used to modify the accumulator. All of the examples assume that all of the flags in the MAC0STA register are initially set to ‘0’.

11.7.1. Multiply and Accumulate Example

The example below implements the equation:

$$(0.5 \times 0.25) + (0.5 \times -0.25) = 0.125 - 0.125 = 0.0$$

```
MOV   MAC0CF, #0Ah    ; Set to Clear Accumulator, Use fractional numbers
MOV   MAC0AH, #40h    ; Load MAC0A register with 4000 hex = 0.5 decimal
MOV   MAC0AL, #00h
MOV   MAC0BH, #20h    ; Load MAC0B register with 2000 hex = 0.25 decimal
MOV   MAC0BL, #00h    ; This line initiates the first MAC operation
MOV   MAC0BH, #E0h    ; Load MAC0B register with E000 hex = -0.25 decimal
MOV   MAC0BL, #00h    ; This line initiates the second MAC operation
NOP
NOP                   ; After this instruction, the Accumulator should be equal to 0,
                      ; and the MAC0STA register should be 0x04, indicating a zero
NOP                   ; After this instruction, the Rounding register is updated
```

SFR Definition 11.4. MAC0AL: MAC0 A Low Byte

SFR Page: 0
SFR Address: 0xA4

R	R	R	R	R	R	R	R	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7–0: Low Byte (bits 7–0) of MAC0 A Register.

SFR Definition 11.5. MAC0BH: MAC0 B High Byte

SFR Page: 0
SFR Address: 0xF2

R	R	R	R	R	R	R	R	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7–0: High Byte (bits 15–8) of MAC0 B Register.

SFR Definition 11.6. MAC0BL: MAC0 B Low Byte

SFR Page: 0
SFR Address: 0xF1

R	R	R	R	R	R	R	R	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7–0: Low Byte (bits 7–0) of MAC0 B Register.
A write to this register initiates a Multiply or Multiply and Accumulate operation.

Note: The contents of this register should not be changed by software during the first MAC0 pipeline stage.

SFR Definition 11.13. MAC0RNDL: MAC0 Rounding Register Low Byte

SFR Page: 0
SFR Address: 0xAE

R	R	R	R	R	R	R	R	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7–0: Low Byte (bits 7–0) of MAC0 Rounding Register.

16.3. External Oscillator Drive Circuit

The external oscillator circuit may drive an external crystal, ceramic resonator, capacitor, or RC network. A CMOS clock may also provide a clock input. For a crystal or ceramic resonator configuration, the crystal/resonator must be wired across the XTAL1 and XTAL2 pins as shown in Option 1 of Figure 16.1. A 10 MΩ resistor also must be wired across the XTAL1 and XTAL2 pins for the crystal/resonator configuration. In RC, capacitor, or CMOS clock configuration, the clock source should be wired to the XTAL2 pin as shown in Option 2, 3, or 4 of Figure 16.1. The type of external oscillator must be selected in the OSCXCN register, and the frequency control bits (XFCN) must be selected appropriately (see SFR Definition 16.5).

Important Note on External Oscillator Usage: Port pins must be configured when using the external oscillator circuit. When the external oscillator drive circuit is enabled in crystal/resonator mode, Port pins P0.5 and P0.6 (C8051F360/3) or P0.2 and P0.3 (C8051F361/2/4/5/6/7/8/9) are used as XTAL1 and XTAL2 respectively. When the external oscillator drive circuit is enabled in capacitor, RC, or CMOS clock mode, Port pin P0.6 (C8051F360/3) or P0.3 (C8051F361/2/4/5/6/7/8/9) is used as XTAL2. The Port I/O Crossbar should be configured to skip the Port pins used by the oscillator circuit; see Section “17.1. Priority Crossbar Decoder” on page 184 for Crossbar configuration. Additionally, when using the external oscillator circuit in crystal/resonator, capacitor, or RC mode, the associated Port pins should be configured as **analog inputs**. In CMOS clock mode, the associated pin should be configured as a **digital input**. See Section “17.2. Port I/O Initialization” on page 186 for details on Port input mode selection.

16.4. System Clock Selection

The internal oscillator requires little start-up time, and may be enabled and selected as the system clock in the same write to OSCICN. External crystals and ceramic resonators typically require a start-up time before they are settled and ready for use as the system clock. The Crystal Valid Flag (XTLVLD in register OSCXCN) is set to ‘1’ by hardware when the external oscillator is settled. To avoid reading a false XTLVLD, in crystal mode software should delay at least 1 ms between enabling the external oscillator and checking XTLVLD. RC and C modes typically require no startup time. The PLL also requires time to lock onto the desired frequency, and the PLL Lock Flag (PLLLCK in register PLL0CN) is set to ‘1’ by hardware once the PLL is locked on the correct frequency.

The CLKSL1-0 bits in register CLKSEL select which oscillator source generates the system clock. CLKSL1-0 must be set to ‘01’ for the system clock to run from the external oscillator; however the external oscillator may still clock certain peripherals, such as the timers and PCA, when the internal oscillator or the PLL is selected as the system clock. The system clock may be switched on-the-fly between the internal and external oscillators or the PLL, so long as the selected oscillator source is enabled and settled.

16.6. External RC Example

If an RC network is used as an external oscillator source for the MCU, the circuit should be configured as shown in Figure 16.1, Option 2. The capacitor should be no greater than 100 pF; however for very small capacitors, the total capacitance may be dominated by parasitic capacitance in the PCB layout. To determine the required External Oscillator Frequency Control value (XFCN) in the OSCXCN Register, first select the RC network value to produce the desired frequency of oscillation. If the frequency desired is 100 kHz, let R = 246 kΩ and C = 50 pF:

$f = 1.23(10^3)/RC = 1.23\ (10^3)/[246 \times 50] = 0.1\ MHz = 100\ kHz$

Referring to the table in SFR Definition 16.5, the required XFCN setting is 010b. Programming XFCN to a higher setting in RC mode will improve frequency accuracy at a slightly increased external oscillator supply current.

16.7. External Capacitor Example

If a capacitor is used as an external oscillator for the MCU, the circuit should be configured as shown in Figure 16.1, Option 3. The capacitor should be no greater than 100 pF; however for very small capacitors, the total capacitance may be dominated by parasitic capacitance in the PCB layout. To determine the required External Oscillator Frequency Control value (XFCN) in the OSCXCN Register, select the capacitor to be used and find the frequency of oscillation from the equations below. Assume V_{DD} = 3.0 V and f = 75 kHz:

$f = KF / (C \times V_{DD})$
$0.075\ MHz = KF / (C \times 3.0)$

Since the frequency of roughly 75 kHz is desired, select the K Factor from the table in SFR Definition 16.5 as KF = 7.7:

$0.075\ MHz = 7.7 / (C \times 3.0)$

$C \times 3.0 = 7.7 / 0.075\ MHz$

$C = 102.6 / 3.0\ pF = 34.2\ pF$

Therefore, the XFCN value to use in this example is 010b.

Table 16.3. PLL Frequency Characteristics

–40 to +85 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Input Frequency (Divided Reference Frequency)		5		30	MHz
PLL Output Frequency		25		100*	MHz
***Note:** The maximum operating frequency of the C8051F366/7/8/9 is 50 MHz.					

Table 16.4. PLL Lock Timing Characteristics

–40 to +85 °C unless otherwise specified

Input Frequency	Multiplier (Pll0mul)	Pll0flt Setting	Output Frequency	Min	Typ	Max	Units
5 MHz	20	0x0F	100 MHz		202		µs
	13	0x0F	65 MHz		115		µs
	16	0x1F	80 MHz		241		µs
	9	0x1F	45 MHz		116		µs
	12	0x2F	60 MHz		258		µs
	6	0x2F	30 MHz		112		µs
	10	0x3F	50 MHz		263		µs
	5	0x3F	25 MHz		113		µs
25 MHz	4	0x01	100 MHz		42		µs
	2	0x01	50 MHz		33		µs
	3	0x11	75 MHz		48		µs
	2	0x11	50 MHz		17		µs
	2	0x21	50 MHz		42		µs
	1	0x21	25 MHz		33		µs
	2	0x31	50 MHz		60		µs
	1	0x31	25 MHz		25		µs

SFR Definition 17.2. XBR1: Port I/O Crossbar Register 1

SFR Page: F
SFR Address: 0xE2

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
WEAKPUD	XBARE	T1E	T0E	ECIE	PCA0ME			00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bit 7: WEAKPUD: Port I/O Weak Pullup Disable.
0: Weak Pullups enabled (except for Ports whose I/O are configured as analog input).
1: Weak Pullups disabled.

Bit 6: XBARE: Crossbar Enable.
0: Crossbar disabled.
1: Crossbar enabled.

Bit 5: T1E: T1 Enable
0: T1 unavailable at Port pin.
1: T1 routed to Port pin.

Bit 4: T0E: T0 Enable
0: T0 unavailable at Port pin.
1: T0 routed to Port pin.

Bit 3: ECIE: PCA0 External Counter Input Enable
0: ECI unavailable at Port pin.
1: ECI routed to Port pin.

Bits 2–0: PCA0ME: PCA Module I/O Enable Bits.
000: All PCA I/O unavailable at Port pins.
001: CEX0 routed to Port pin.
010: CEX0, CEX1 routed to Port pins.
011: CEX0, CEX1, CEX2 routed to Port pins.
100: CEX0, CEX1, CEX2, CEX3 routed to Port pins.
101: CEX0, CEX1, CEX2, CEX3, CEX4 routed to Port pins.
110: CEX0, CEX1, CEX2, CEX3, CEX4, CEX5 routed to Port pins.
111: Reserved.

SFR Definition 17.18. P2SKIP: Port2 Skip

SFR Page: F
SFR Address: 0xD6

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7–0: P2SKIP[7:0]: Port2 Crossbar Skip Enable Bits.
These bits select Port pins to be skipped by the Crossbar Decoder. Port pins used as analog inputs (for ADC or Comparator) or used as special functions (V_{REF} input, external oscillator circuit, CNVSTR input) should be skipped by the Crossbar.
0: Corresponding P2.n pin is not skipped by the Crossbar.
1: Corresponding P2.n pin is skipped by the Crossbar.

SFR Definition 17.19. P2MAT: Port2 Match

SFR Page: 0
SFR Address: 0xB1

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7–0: P2MAT[7:0]: Port2 Match Value.
These bits control the value that unmasked P2 Port pins are compared against. A Port Match event is generated if (P2 & P2MASK) does not equal (P2MAT & P2MASK).

SFR Definition 17.20. P2MASK: Port2 Mask

SFR Page: 0
SFR Address: 0xB2

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7–0: P2MASK[7:0]: Port2 Mask Value.
These bits select which Port pins will be compared to the value stored in P2MAT.
0: Corresponding P2.n pin is ignored and cannot cause a Port Match event.
1: Corresponding P2.n pin is compared to the corresponding bit in P2MAT.

SFR Definition 17.23. P3MDOUT: Port3 Output Mode

SFR Page: F
SFR Address: 0xAF

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7–0: Output Configuration Bits for P3.7-P3.0 (respectively): ignored if corresponding bit in register P3MDIN is logic '0'.
0: Corresponding P3.n Output is open-drain.
1: Corresponding P3.n Output is push-pull.

SFR Definition 17.24. P3SKIP: Port3 Skip

SFR Page: F
SFR Address: 0xD7

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7–0: P3SKIP[7:0]: Port3 Crossbar Skip Enable Bits.
These bits select Port pins to be skipped by the Crossbar Decoder. Port pins used as analog inputs (for ADC or Comparator) or used as special functions (V_{REF} input, external oscillator circuit, CNVSTR input) should be skipped by the Crossbar.
0: Corresponding P3.n pin is not skipped by the Crossbar.
1: Corresponding P3.n pin is skipped by the Crossbar.

SFR Definition 19.2. SBUF0: Serial (UART0) Port Data Buffer

SFR Page: all pages
SFR Address: 0x99

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7–0: SBUF0[7:0]: Serial Data Buffer Bits 7–0 (MSB–LSB)
This SFR accesses two registers; a transmit shift register and a receive latch register. When data is written to SBUF0, it goes to the transmit shift register and is held for serial transmission. Writing a byte to SBUF0 initiates the transmission. A read of SBUF0 returns the contents of the receive latch.

Table 19.2. Timer Settings for Standard Baud Rates Using an External 25.0 MHz Oscillator

	Frequency: 25.0 MHz						
	Target Baud Rate (bps)	Baud Rate % Error	Oscillator Divide Factor	Timer Clock Source	SCA1–SCA0 (pre-scale select)[1]	T1M[1]	Timer 1 Reload Value (hex)
SYSCLK and Timer Clock from External Osc.	230400	–0.47%	108	SYSCLK	XX[2]	1	0xCA
	115200	0.45%	218	SYSCLK	XX	1	0x93
	57600	–0.01%	434	SYSCLK	XX	1	0x27
	28800	0.45%	872	SYSCLK/4	01	0	0x93
	14400	–0.01%	1736	SYSCLK/4	01	0	0x27
	9600	0.15%	2608	EXTCLK/8	11	0	0x5D
	2400	0.45%	10464	SYSCLK/48	10	0	0x93
	1200	–0.01%	20832	SYSCLK/48	10	0	0x27
SYSCLK from Internal Osc., Timer Clock from External Osc.	57600	–0.47%	432	EXTCLK/8	11	0	0xE5
	28800	–0.47%	864	EXTCLK/8	11	0	0xCA
	14400	0.45%	1744	EXTCLK/8	11	0	0x93
	9600	0.15%	2608	EXTCLK/8	11	0	0x5D

Notes:
1. SCA1–SCA0 and T1M bit definitions can be found in Section 21.1.
2. X = Don't care.

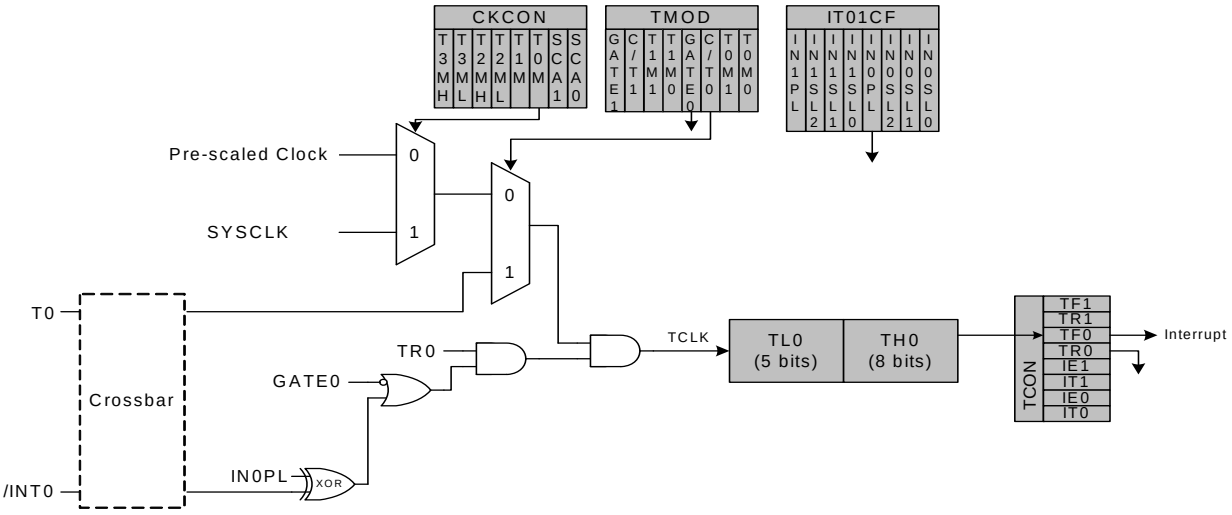


Figure 21.1. T0 Mode 0 Block Diagram

21.1.2. Mode 1: 16-bit Counter/Timer

Mode 1 operation is the same as Mode 0, except that the counter/timer registers use all 16 bits. The counter/timers are enabled and configured in Mode 1 in the same manner as for Mode 0.

21.1.3. Mode 2: 8-bit Counter/Timer with Auto-Reload

Mode 2 configures Timer 0 and Timer 1 to operate as 8-bit counter/timers with automatic reload of the start value. TL0 holds the count and TH0 holds the reload value. When the counter in TL0 overflows from all ones to 0x00, the timer overflow flag TF0 (TCON.5) is set and the counter in TL0 is reloaded from TH0. If Timer 0 interrupts are enabled, an interrupt will occur when the TF0 flag is set. The reload value in TH0 is not changed. TL0 must be initialized to the desired value before enabling the timer for the first count to be correct. When in Mode 2, Timer 1 operates identically to Timer 0.

Both counter/timers are enabled and configured in Mode 2 in the same manner as Mode 0. Setting the TR0 bit (TCON.4) enables the timer when either GATE0 (TMOD.3) is logic ‘0’ or when the input signal /INT0 is active as defined by bit IN0PL in register IT01CF (see Section “10.5. External Interrupts” on page 115 for details on the external input signals /INT0 and /INT1).

21.1.4. Mode 3: Two 8-bit Counter/Timers (Timer 0 Only)

In Mode 3, Timer 0 is configured as two separate 8-bit counter/timers held in TL0 and TH0. The counter/timer in TL0 is controlled using the Timer 0 control/status bits in TCON and TMOD: TR0, C/T0, GATE0 and TF0. TL0 can use either the system clock or an external input signal as its timebase. The TH0 register is restricted to a timer function sourced by the system clock or prescaled clock. TH0 is enabled using the Timer 1 run control bit TR1. TH0 sets the Timer 1 overflow flag TF1 on overflow and thus controls the Timer 1 interrupt.

Timer 1 is inactive in Mode 3. When Timer 0 is operating in Mode 3, Timer 1 can be operated in Modes 0, 1 or 2, but cannot be clocked by external signals nor set the TF1 flag and generate an interrupt. However, the Timer 1 overflow can be used to generate baud rates for the SMBus and/or UART, and/or initiate ADC conversions. While Timer 0 is operating in Mode 3, Timer 1 run control is handled through its mode settings. To run Timer 1 while Timer 0 is in Mode 3, set the Timer 1 Mode as 0, 1, or 2. To disable Timer 1, configure it for Mode 3.

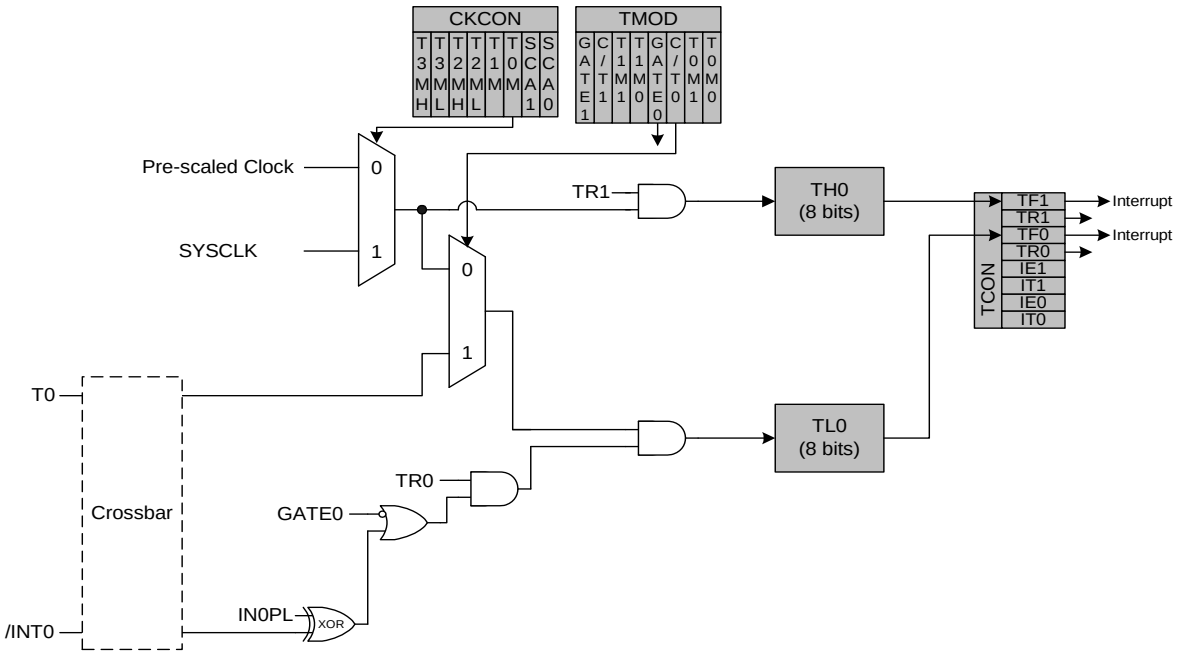


Figure 21.3. T0 Mode 3 Block Diagram

DOCUMENT CHANGE LIST

Revision 0.1 to Revision 0.2

- Updated specification tables with most recently available characterization data.
- Fixed an error with the SYSCLK specification in Table 3.1, “Global Electrical Characteristics,” on page 33.
- Corrected the name of the PMAT bit in SFR Definition 10.2. IP: Interrupt Priority.
- Corrected the reset value for SFR Definition 22.2. PCA0MD: PCA0 Mode.

Revision 0.2 to Revision 1.0

- Updated specification tables with characterization data.
- Fixed Table 1.1, “Product Selection Guide,” on page 19 to reflect the correct number of Port I/O pins for the C8051F361/2/4/5.
- Updated Section “10. Interrupt Handler” on page 107.
  - Added note describing EA change behavior when followed by single cycle instruction.
- Updated SFR Definition 11.1
  - Changed the MAC0SC (MAC0CF.5) bit description to correctly refer to the MAC0SD bit.
- Updated SFR Definition 15.2.
  - Changed the EMI0CF description to properly describe the 1k XRAM boundaries.
- Added Table 16.2, “Internal Low Frequency Oscillator Electrical Characteristics,” on page 171.
- Updated SFR Definition 16.9:
  - Specified that the undefined states for PLLLP3–0 are RESERVED.
- Added Table 19.7 and Table 19.8 on page 231 for UART Baud Rates when using the PLL.
- Updated Table 22.1, “PCA Timebase Input Options,” on page 263:
  - Specified that the undefined states of CPS2–0 are RESERVED.
- Added Revision B to “Revision Specific Behavior” on page 279.

Revision 1.0 to Revision 1.1

- Updated ordering table with Revision C part numbers.
- Updated Figure 17.2. ’Port I/O Cell Block Diagram’ on page 183 to refer to VDD instead of VIO.
- Added Revision C to “Revision Specific Behavior” on page 279.
- Added Revision C to the REVID C2 register in C2 Register Definition 24.3.
- Updated “Digital Supply Current (Stop Mode, shutdown)” typical value in Table 3.1, “Global Electrical Characteristics,” on page 33.
- Updated “Missing Clock Detector Timeout” typical value in Table 12.1, “Reset Electrical Characteristics,” on page 134.

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