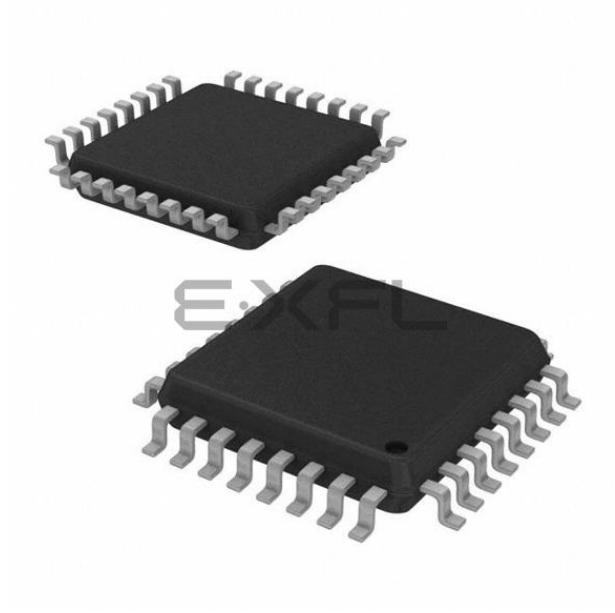

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	8051
Core Size	8-Bit
Speed	100MHz
Connectivity	SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	29
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f364-c-gqr

1.2. On-Chip Memory

The CIP-51 has a standard 8051 program and data address configuration. It includes 256 bytes of data RAM, with the upper 128 bytes dual-mapped. Indirect addressing accesses the upper 128 bytes of general purpose RAM, and direct addressing accesses the 128 byte SFR address space. The lower 128 bytes of RAM are accessible via direct and indirect addressing. The first 32 bytes are addressable as four banks of general purpose registers, and the next 16 bytes can be byte addressable or bit addressable.

Program memory consists of 32/16 kB of Flash. This memory may be reprogrammed in-system in 1024 byte sectors, and requires no special off-chip programming voltage. See Figure 1.6 for the MCU system memory map.

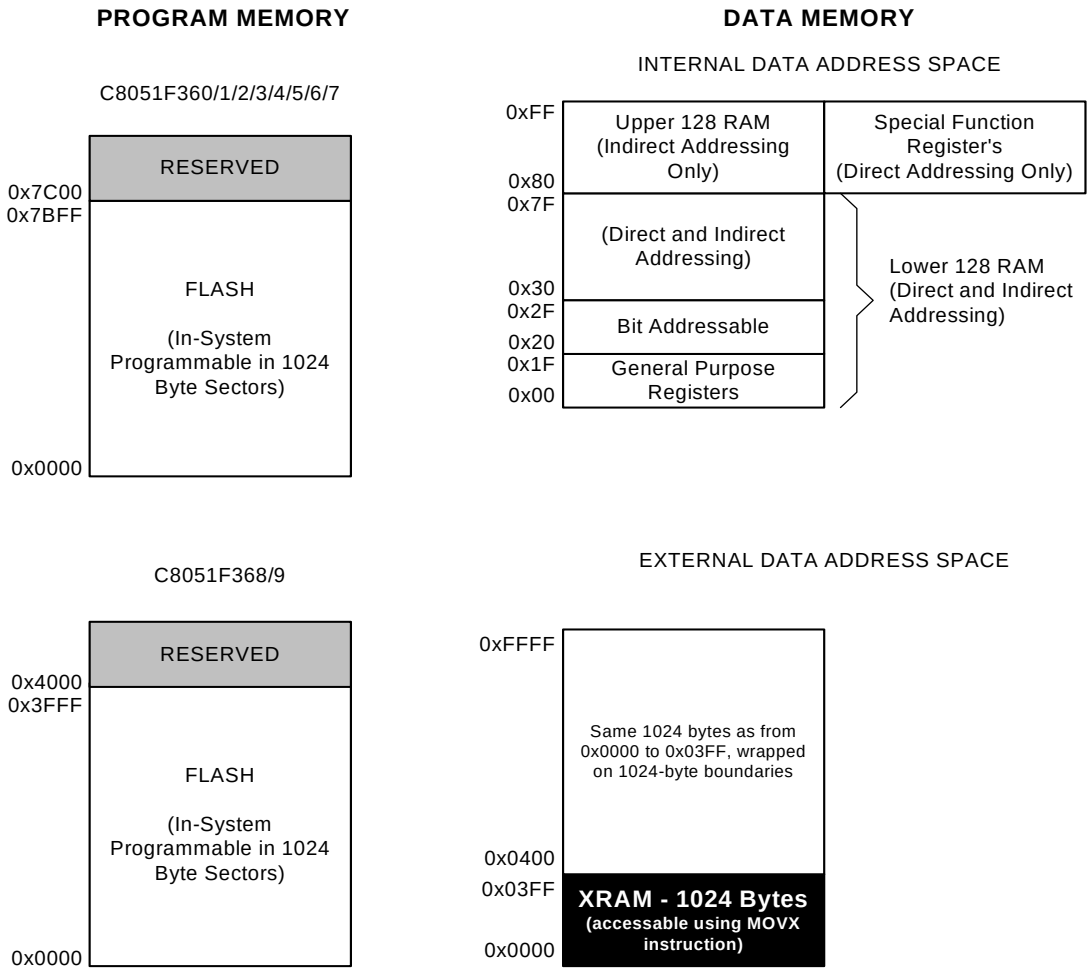

Figure 1.6. On-Board Memory Map

1.3. On-Chip Debug Circuitry

The C8051F36x devices include on-chip Silicon Labs 2-Wire (C2) debug circuitry that provides non-intrusive, full speed, in-circuit debugging of the production part *installed in the end application.*

Silicon Labs' debugging system supports inspection and modification of memory and registers, breakpoints, and single stepping. No additional target RAM, program memory, timers, or communications chan-

Table 3.1. Global Electrical Characteristics (Continued)

–40 to +85 °C, 25 MHz system clock unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Digital Supply Current—CPU Inactive (Idle Mode, not fetching instructions from Flash)					
I_{DD}[2]	V_{DD} = 3.6 V, F = 100 MHz	—	36	40	mA
	V_{DD} = 3.6 V, F = 25 MHz	—	9	12	mA
	V_{DD} = 3.0 V, F = 100 MHz	—	30	35	mA
	V_{DD} = 3.0 V, F = 25 MHz	—	7	9	mA
	V_{DD} = 3.0 V, F = 1 MHz	—	0.24	—	mA
	V_{DD} = 3.0 V, F = 80 kHz	—	19	—	µA
I_{DD} Supply Sensitivity[3]	F = 25 MHz	—	44	—	%/V
	F = 1 MHz	—	43.7	—	%/V
I_{DD} Frequency Sensitivity[3,5]	V_{DD} = 3.0 V, F <= 1 MHz, T = 25 °C	—	0.24	—	mA/MHz
	V_{DD} = 3.0 V, F > 1 MHz, T = 25 °C	—	0.25	—	mA/MHz
	V_{DD} = 3.6 V, F <= 1 MHz, T = 25 °C	—	0.31	—	mA/MHz
	V_{DD} = 3.6 V, F > 1 MHz, T = 25 °C	—	0.32	—	mA/MHz
Digital Supply Current (Stop Mode, shutdown)	Oscillator not running, V_{DD} Monitor Disabled	—	0.5	—	µA

Notes:

1. SYSCLK must be at least 32 kHz to enable debugging.
2. SYSCLK is the internal device clock. For operational speeds in excess of 30 MHz, SYSCLK must be derived from the Phase-Locked Loop (PLL).
3. Based on device characterization data; Not production tested.
4. IDD can be estimated for frequencies ≤ 20 MHz by simply multiplying the frequency of interest by the frequency sensitivity number for that range. When using these numbers to estimate I_{DD} for >20 MHz, the estimate should be the current at 25 MHz minus the difference in current indicated by the frequency sensitivity number. For example: V_{DD} = 3.0 V; F = 20 MHz, I_{DD} = 15.9 mA - (25 MHz - 20 MHz) * 0.38 mA/MHz = 14 mA.
5. Idle IDD can be estimated for frequencies ≤ 1 MHz by simply multiplying the frequency of interest by the frequency sensitivity number for that range. When using these numbers to estimate Idle I_{DD} for >1 MHz, the estimate should be the current at 25 MHz minus the difference in current indicated by the frequency sensitivity number. For example: V_{DD} = 3.0 V; F = 5 MHz, Idle I_{DD} = 7.2 mA - (25 MHz - 5 MHz) * 0.25 mA/MHz = 2.2 mA.

Other electrical characteristics tables are found in the data sheet section corresponding to the associated peripherals. For more information on electrical characteristics for a specific peripheral, refer to the page indicated in Table 3.2.

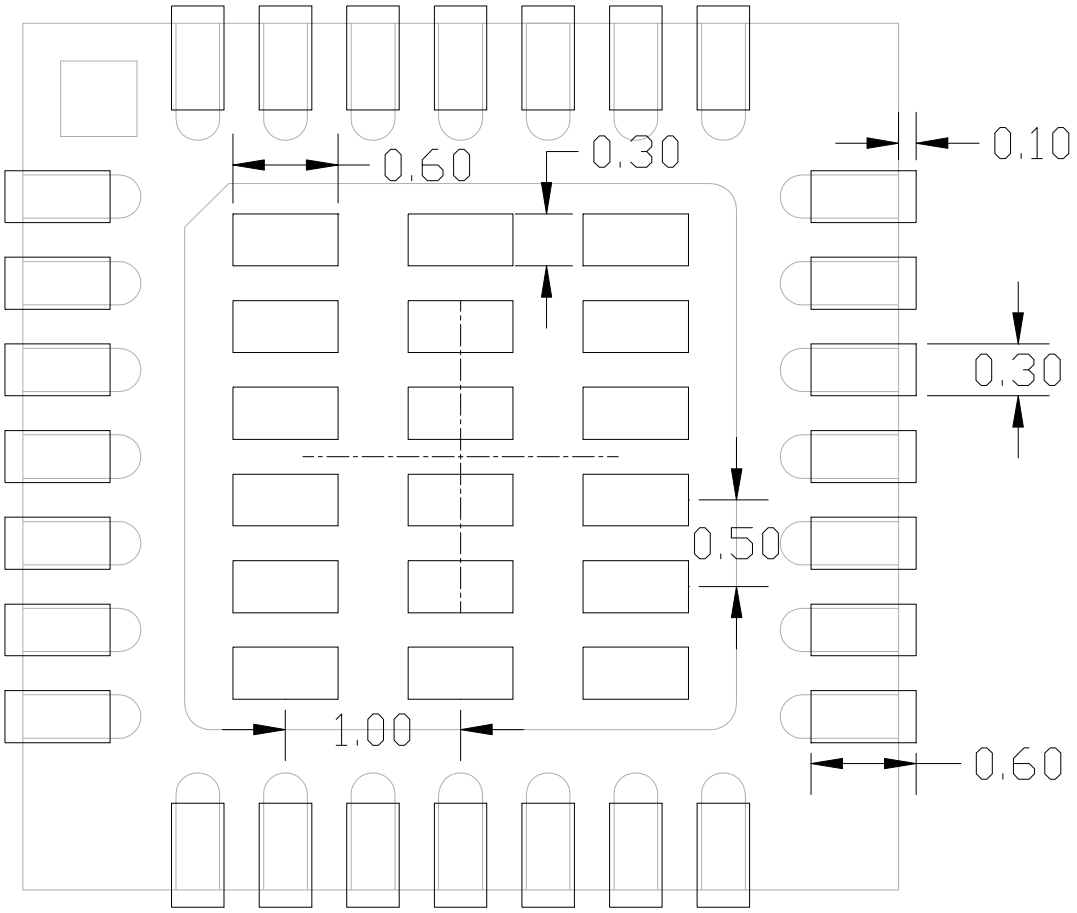

Figure 4.8. QFN-28 Solder Paste Recommendation

5.3.2. Tracking Modes

According to Table 5.1, each ADC0 conversion must be preceded by a minimum tracking time for the converted result to be accurate. The AD0TM bit in register ADC0CN controls the ADC0 track-and-hold mode. In its default state, the ADC0 input is continuously tracked, except when a conversion is in progress. When the AD0TM bit is logic ‘1’, ADC0 operates in low-power track-and-hold mode. In this mode, each conversion is preceded by a tracking period of 3 SAR clocks (after the start-of-conversion signal). When the CNVSTR signal is used to initiate conversions in low-power tracking mode, ADC0 tracks only when CNVSTR is low; conversion begins on the rising edge of CNVSTR (see Figure 5.4). Tracking can also be disabled (shutdown) when the device is in low power standby or sleep modes. Low-power track-and-hold mode is also useful when AMUX settings are frequently changed, due to the settling time requirements described in Section “5.3.3. Settling Time Requirements” on page 53.

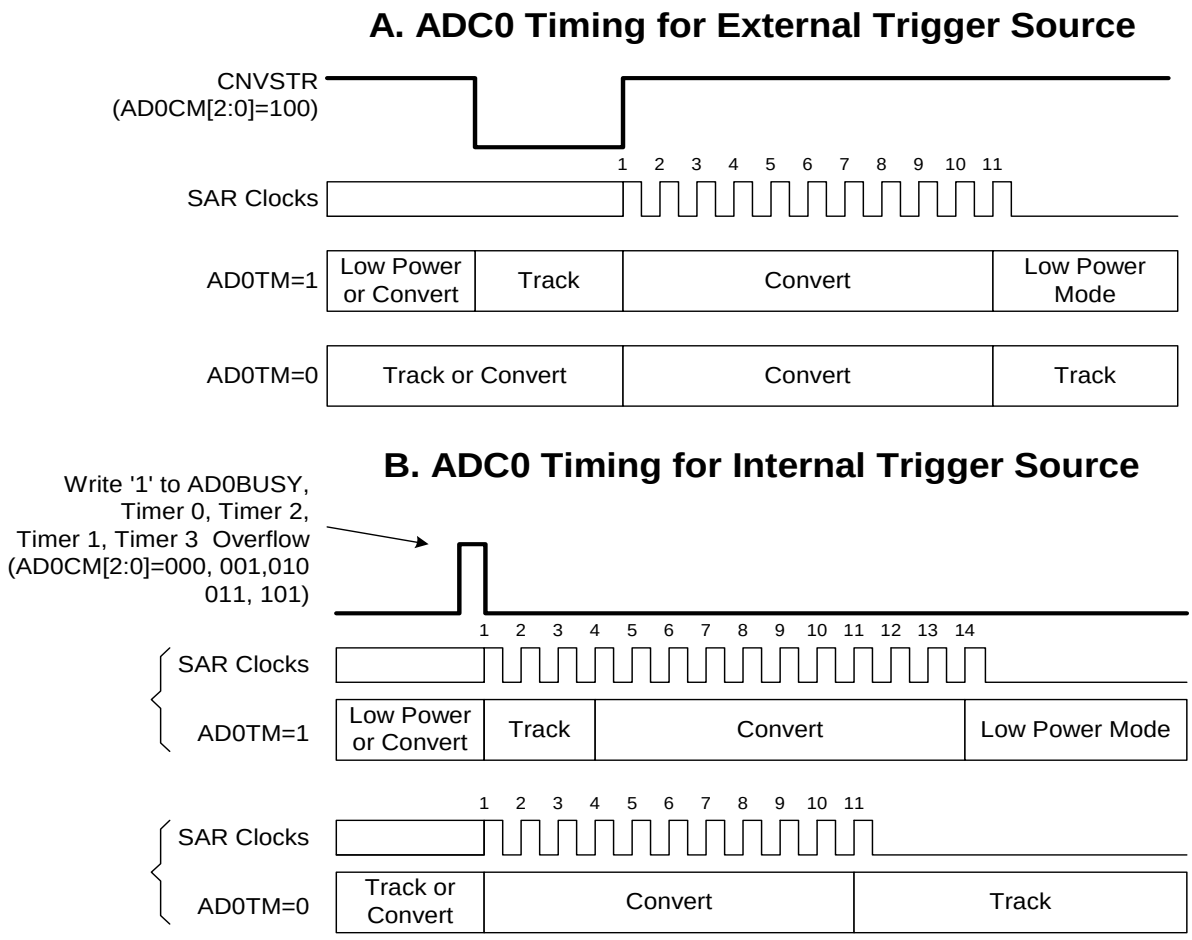

Figure 5.4. 10-Bit ADC Track and Conversion Example Timing

Table 9.3. Special Function Registers

SFRs are listed in alphabetical order. All undefined SFR locations are reserved.

Register	Address	SFR Page	Description	Page No.
ACC	0xE0	All Pages	Accumulator	page 104
ADC0CF	0xBC	All Pages	ADC0 Configuration	page 56[1]
ADC0CN	0xE8	All Pages	ADC0 Control	page 57[1]
ADC0GTH	0xC4	All Pages	ADC0 Greater-Than High Byte	page 58[1]
ADC0GTL	0xC3	All Pages	ADC0 Greater-Than Low Byte	page 58[1]
ADC0H	0xBE	All Pages	ADC0 Data Word High Byte	page 56[1]
ADC0L	0xBD	All Pages	ADC0 Data Word Low Byte	page 56[1]
ADC0LTH	0xC6	All Pages	ADC0 Less-Than High Byte	page 59[1]
ADC0LTL	0xC5	All Pages	ADC0 Less-Than Low Byte	page 59[1]
AMX0N	0xBA	All Pages	AMUX0 Negative Channel Select	page 55[1]
AMX0P	0xBB	All Pages	AMUX0 Positive Channel Select	page 54[1]
B	0xF0	All Pages	B Register	page 104
CCH0CN	0x84	F	Cache Control	page 149
CCH0LC	0xD2	F	Cache Lock	page 151
CCH0MA	0xD3	F	Cache Miss Accumulator	page 152
CCH0TN	0xC9	F	Cache Tuning	page 150
CKCON	0x8E	All Pages	Clock Control	page 252
CLKSEL	0x8F	F	System Clock Select	page 173
CPT0CN	0x9B	All Pages	Comparator0 Control	page 73
CPT0MD	0x9D	All Pages	Comparator0 Configuration	page 75
CPT0MX	0x9F	All Pages	Comparator0 MUX Selection	page 74
CPT1CN	0x9A	All Pages	Comparator1 Control	page 76
CPT1MD	0x9C	All Pages	Comparator1 Configuration	page 78
CPT1MX	0x9E	All Pages	Comparator1 MUX Selection	page 77
DPH	0x83	All Pages	Data Pointer High Byte	page 102
DPL	0x82	All Pages	Data Pointer Low Byte	page 102
EIE1	0xE6	All Pages	Extended Interrupt Enable 1	page 112
EIE2	0xE7	All Pages	Extended Interrupt Enable 2	page 114
EIP1	0xCE	F	Extended Interrupt Priority 1	page 113
EIP2	0xCF	F	Extended Interrupt Priority 2	page 114

Notes:
1. Refers to a register in the C8051F360/1/2/6/7/8/9 only.
2. Refers to a register in the C8051F360/3 only.

12. Reset Sources

Reset circuitry allows the controller to be easily placed in a predefined default condition. On entry to this reset state, the following occur:

- CIP-51 halts program execution
- Special Function Registers (SFRs) are initialized to their defined reset values
- External Port pins are forced to a known state
- Interrupts and timers are disabled.

All SFRs are reset to the predefined values noted in the SFR detailed descriptions. The contents of internal data memory are unaffected during a reset; any previously stored data is preserved. However, since the stack pointer SFR is reset, the stack is effectively lost, even though the data on the stack is not altered.

The Port I/O latches are reset to 0xFF (all logic ones) in open-drain mode. Weak pullups are enabled during and after the reset. For V_{DD} Monitor and power-on resets, the $\overline{RST}$ pin is driven low until the device exits the reset state.

On exit from the reset state, the program counter (PC) is reset, and the system clock defaults to the internal oscillator. Refer to Section “16. Oscillators” on page 168 for information on selecting and configuring the system clock source. The Watchdog Timer is enabled with the system clock divided by 12 as its clock source (Section “22.3. Watchdog Timer Mode” on page 270 details the use of the Watchdog Timer). Program execution begins at location 0x0000.

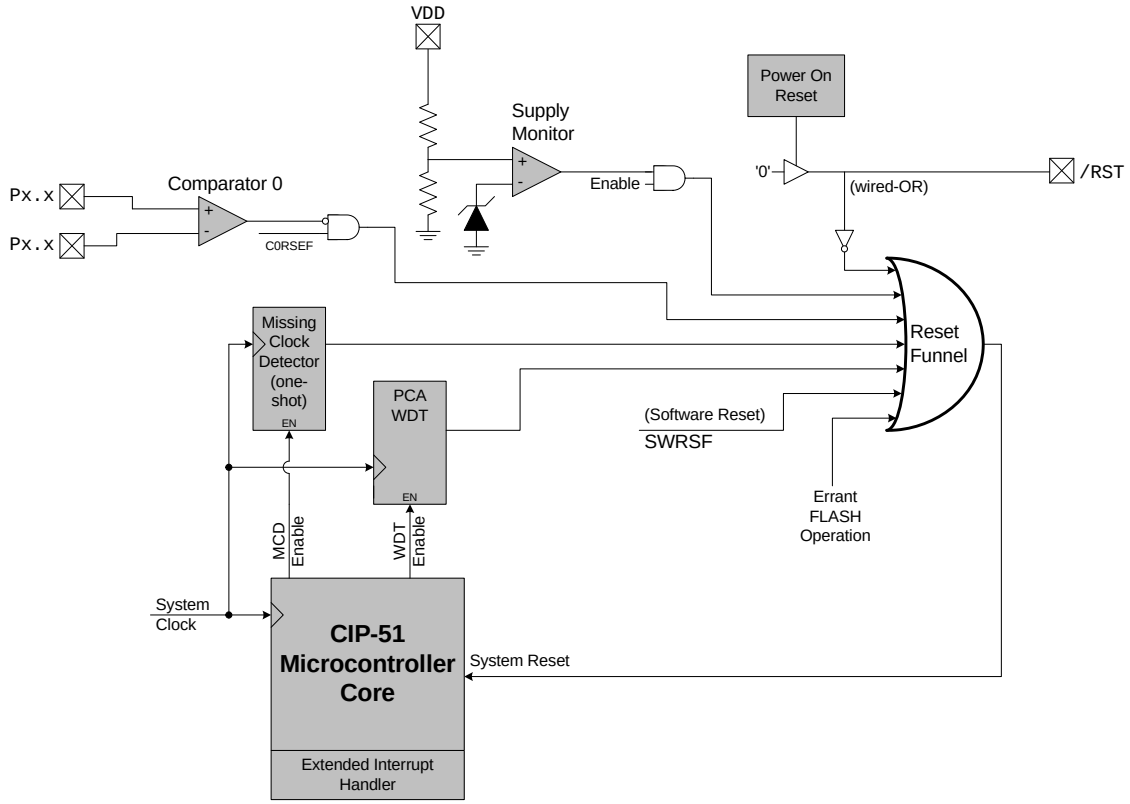

Figure 12.1. Reset Sources

Table 13.2. Flash Electrical Characteristics

V_{DD} = 2.7 to 3.6 V; –40 to +85 °C.

Parameter	Conditions	Min	Typ	Max	Units
Flash Size	C8051F360/1/2/3/4/5/6/7		32768*		Bytes
	C8051F368/9		16384		
Endurance		20 k	250 k		Erase/Write
Erase Cycle Time		8	10	12	ms
Write Cycle Time		37	47	57	µs
***Note:** 1024 Bytes at location 0x7C00 to 0x7FFF are reserved.					

To shut down the PLL, the system clock should be switched to the internal oscillator or a stable external clock source, using the CLKSEL register. Next, disable the PLL by setting PLLEN (PLL0CN.1) to ‘0’. Finally, the PLL can be powered off, by setting PLLPWR (PLL0CN.0) to ‘0’. Note that the PLLEN and PLLPWR bits can be cleared at the same time.

SFR Definition 16.6. PLL0CN: PLL Control

SFR Page: F
SFR Address: 0xB3

R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	Reset Value
–	–	–	PLLLCK	Reserved	PLLSRC	PLLEN	PLLPWR	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7–5: UNUSED. Read = 000b. Write = don’t care.
Bit 4: PLLLCK: PLL Lock Flag.
0: PLL Frequency is not locked.
1: PLL Frequency is locked.
Bit 3: RESERVED. Read = 0b. Must Write 0b.
Bit 2: PLLSRC: PLL Reference Clock Source Select Bit.
0: PLL Reference Clock Source is Internal Oscillator.
1: PLL Reference Clock Source is External Oscillator.
Bit 1: PLLEN: PLL Enable Bit.
0: PLL is held in reset.
1: PLL is enabled. PLLPWR must be ‘1’.
Bit 0: PLLPWR: PLL Power Enable.
0: PLL bias generator is de-activated. No static power is consumed.
1: PLL bias generator is active. Must be set for PLL to operate.

SFR Definition 16.7. PLL0DIV: PLL Pre-divider

SFR Page: F
SFR Address: 0xA9

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
–	–	–	PLLM4	PLLM3	PLLM2	PLLM1	PLLM0	00000001
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7–5: UNUSED. Read = 000b. Write = don’t care.
Bits 4–0: PLLM4–0: PLL Reference Clock Pre-divider.
These bits select the pre-divide value of the PLL reference clock. When set to any non-zero value, the reference clock will be divided by the value in PLLM4–0. When set to ‘00000b’, the reference clock will be divided by 32.

SFR Definition 17.2. XBR1: Port I/O Crossbar Register 1

SFR Page: F
SFR Address: 0xE2

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
WEAKPUD	XBARE	T1E	T0E	ECIE	PCA0ME			00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bit 7: WEAKPUD: Port I/O Weak Pullup Disable.
0: Weak Pullups enabled (except for Ports whose I/O are configured as analog input).
1: Weak Pullups disabled.

Bit 6: XBARE: Crossbar Enable.
0: Crossbar disabled.
1: Crossbar enabled.

Bit 5: T1E: T1 Enable
0: T1 unavailable at Port pin.
1: T1 routed to Port pin.

Bit 4: T0E: T0 Enable
0: T0 unavailable at Port pin.
1: T0 routed to Port pin.

Bit 3: ECIE: PCA0 External Counter Input Enable
0: ECI unavailable at Port pin.
1: ECI routed to Port pin.

Bits 2–0: PCA0ME: PCA Module I/O Enable Bits.
000: All PCA I/O unavailable at Port pins.
001: CEX0 routed to Port pin.
010: CEX0, CEX1 routed to Port pins.
011: CEX0, CEX1, CEX2 routed to Port pins.
100: CEX0, CEX1, CEX2, CEX3 routed to Port pins.
101: CEX0, CEX1, CEX2, CEX3, CEX4 routed to Port pins.
110: CEX0, CEX1, CEX2, CEX3, CEX4, CEX5 routed to Port pins.
111: Reserved.

SFR Definition 17.18. P2SKIP: Port2 Skip

SFR Page: F
SFR Address: 0xD6

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7–0: P2SKIP[7:0]: Port2 Crossbar Skip Enable Bits.
These bits select Port pins to be skipped by the Crossbar Decoder. Port pins used as analog inputs (for ADC or Comparator) or used as special functions (V_{REF} input, external oscillator circuit, CNVSTR input) should be skipped by the Crossbar.
0: Corresponding P2.n pin is not skipped by the Crossbar.
1: Corresponding P2.n pin is skipped by the Crossbar.

SFR Definition 17.19. P2MAT: Port2 Match

SFR Page: 0
SFR Address: 0xB1

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7–0: P2MAT[7:0]: Port2 Match Value.
These bits control the value that unmasked P2 Port pins are compared against. A Port Match event is generated if (P2 & P2MASK) does not equal (P2MAT & P2MASK).

SFR Definition 17.20. P2MASK: Port2 Mask

SFR Page: 0
SFR Address: 0xB2

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7–0: P2MASK[7:0]: Port2 Mask Value.
These bits select which Port pins will be compared to the value stored in P2MAT.
0: Corresponding P2.n pin is ignored and cannot cause a Port Match event.
1: Corresponding P2.n pin is compared to the corresponding bit in P2MAT.

SFR Definition 17.21. P3: Port3

SFR Page: **all pages**
SFR Address: **0xB0** (bit addressable)

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7–0: P3.[7:0]
Write - Output appears on I/O pins per Crossbar Registers.
0: Logic Low Output.
1: Logic High Output (high impedance if corresponding P3MDOUT.n bit = 0).
Read - Always reads ‘0’ if selected as analog input in register P3MDIN. Directly reads Port pin when configured as digital input.
0: P3.n pin is logic low.
1: P3.n pin is logic high.

SFR Definition 17.22. P3MDIN: Port3 Input Mode

SFR Page: **F**
SFR Address: **0xF4**

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7–0: Analog Input Configuration Bits for P3.7-P3.0 (respectively).
Port pins configured as analog inputs have their weak pullup, digital driver, and digital receiver disabled.
0: Corresponding P3.n pin is configured as an analog input.
1: Corresponding P3.n pin is not configured as an analog input.

18.4.2. SMB0CN Control Register

SMB0CN is used to control the interface and to provide status information (see SFR Definition 18.2). The higher four bits of SMB0CN (MASTER, TXMODE, STA, and STO) form a status vector that can be used to jump to service routines. MASTER and TXMODE indicate the master/slave state and transmit/receive modes, respectively.

STA and STO indicate that a START and/or STOP has been detected or generated since the last SMBus interrupt. STA and STO are also used to generate START and STOP conditions when operating as a master. Writing a ‘1’ to STA will cause the SMBus interface to enter Master Mode and generate a START when the bus becomes free (STA is not cleared by hardware after the START is generated). Writing a ‘1’ to STO while in Master Mode will cause the interface to generate a STOP and end the current transfer after the next ACK cycle. If STO and STA are both set (while in Master Mode), a STOP followed by a START will be generated.

As a receiver, writing the ACK bit defines the outgoing ACK value; as a transmitter, reading the ACK bit indicates the value received on the last ACK cycle. ACKRQ is set each time a byte is received, indicating that an outgoing ACK value is needed. When ACKRQ is set, software should write the desired outgoing value to the ACK bit before clearing SI. A NACK will be generated if software does not write the ACK bit before clearing SI. SDA will reflect the defined ACK value immediately following a write to the ACK bit; however SCL will remain low until SI is cleared. If a received slave address is not acknowledged, further slave events will be ignored until the next START is detected.

The ARBLOST bit indicates that the interface has lost an arbitration. This may occur anytime the interface is transmitting (master or slave). A lost arbitration while operating as a slave indicates a bus error condition. ARBLOST is cleared by hardware each time SI is cleared.

The SI bit (SMBus Interrupt Flag) is set at the beginning and end of each transfer, after each byte frame, or when an arbitration is lost; see Table 18.3 for more details.

Important Note About the SI Bit: The SMBus interface is stalled while SI is set; thus SCL is held low, and the bus is stalled until software clears SI.

Table 18.3 lists all sources for hardware changes to the SMB0CN bits. Refer to Table 18.4 for SMBus status decoding using the SMB0CN register.

20.5. Serial Clock Timing

Four combinations of serial clock phase and polarity can be selected using the clock control bits in the SPI0 Configuration Register (SPI0CFG). The CKPHA bit (SPI0CFG.5) selects one of two clock phases (edge used to latch the data). The CKPOL bit (SPI0CFG.4) selects between an active-high or active-low clock. Both master and slave devices must be configured to use the same clock phase and polarity. SPI0 should be disabled (by clearing the SPIEN bit, SPI0CN.0) when changing the clock phase or polarity. The clock and data line relationships for master mode are shown in Figure 20.5. For slave mode, the clock and data relationships are shown in Figure 20.6 and Figure 20.7. Note that CKPHA must be set to '0' on both the master and slave SPI when communicating between two of the following devices: C8051F04x, C8051F06x, C8051F12x, C8051F31x, C8051F32x, C8051F33x, and C8051F36x.

The SPI0 Clock Rate Register (SPI0CKR) as shown in SFR Definition 20.3 controls the master mode serial clock frequency. This register is ignored when operating in slave mode. When the SPI is configured as a master, the maximum data transfer rate (bits/sec) is one-half the system clock frequency or 12.5 MHz, whichever is slower. When the SPI is configured as a slave, the maximum data transfer rate (bits/sec) for full-duplex operation is 1/10 the system clock frequency, provided that the master issues SCK, NSS (in 4-wire slave mode), and the serial input data synchronously with the slave's system clock. If the master issues SCK, NSS, and the serial input data asynchronously, the maximum data transfer rate (bits/sec) must be less than 1/10 the system clock frequency. In the special case where the master only wants to transmit data to the slave and does not need to receive data from the slave (i.e. half-duplex operation), the SPI slave can receive data at a maximum data transfer rate (bits/sec) of 1/4 the system clock frequency. This is provided that the master issues SCK, NSS, and the serial input data synchronously with the slave's system clock.

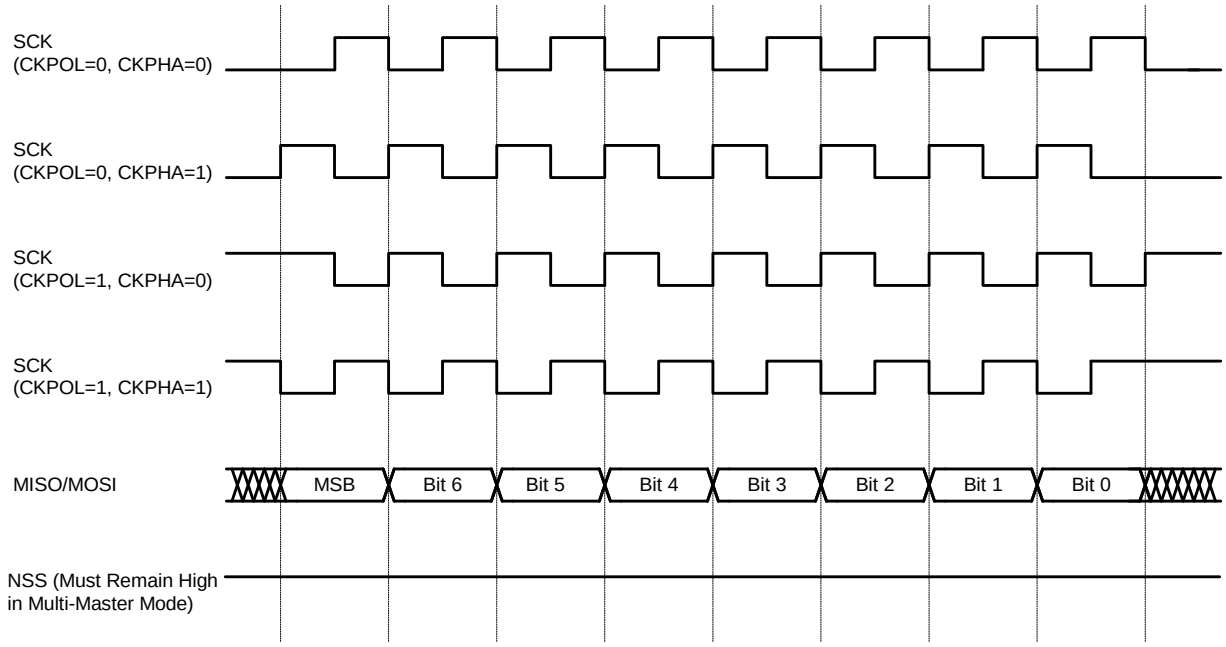

Figure 20.5. Master Mode Data/Clock Timing

21.2. Timer 2

Timer 2 is a 16-bit timer formed by two 8-bit SFRs: TMR2L (low byte) and TMR2H (high byte). Timer 2 may operate in 16-bit auto-reload mode or (split) 8-bit auto-reload mode. The T2SPLIT bit (TMR2CN.3) defines the Timer 2 operation mode.

Timer 2 may be clocked by the system clock, the system clock divided by 12, or the external oscillator source divided by 8. The external clock mode is ideal for real-time clock (RTC) functionality, where the internal oscillator drives the system clock while Timer 2 (and/or the PCA) is clocked by an external precision oscillator. Note that the external oscillator source divided by 8 is synchronized with the system clock.

21.2.1. 16-bit Timer with Auto-Reload

When T2SPLIT (TMR2CN.3) is zero, Timer 2 operates as a 16-bit timer with auto-reload. Timer 2 can be clocked by SYSCLK, SYSCLK divided by 12, or the external oscillator clock source divided by 8. As the 16-bit timer register increments and overflows from 0xFFFF to 0x0000, the 16-bit value in the Timer 2 reload registers (TMR2RLH and TMR2RLL) is loaded into the Timer 2 register as shown in Figure 21.4, and the Timer 2 High Byte Overflow Flag (TMR2CN.7) is set. If Timer 2 interrupts are enabled (if IE.5 is set), an interrupt will be generated on each Timer 2 overflow. Additionally, if Timer 2 interrupts are enabled and the TF2LEN bit is set (TMR2CN.5), an interrupt will be generated each time the lower 8 bits (TMR2L) overflow from 0xFF to 0x00.

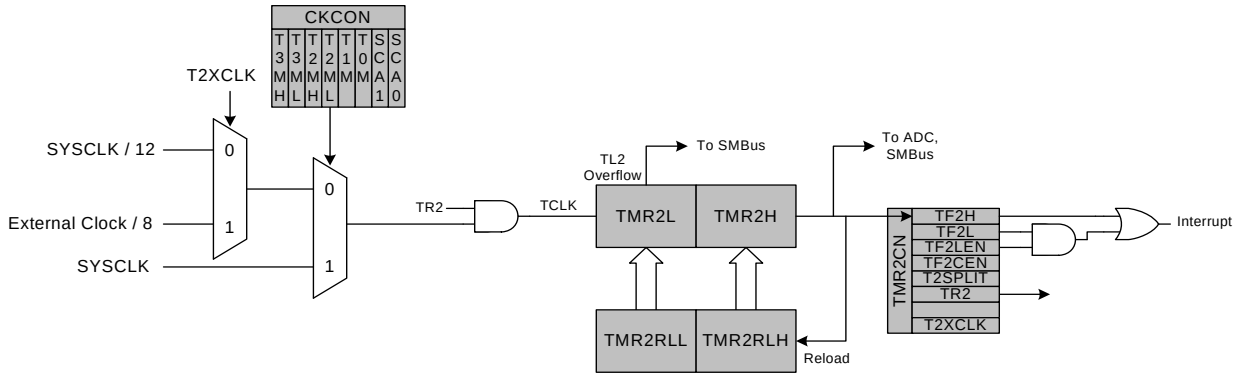

Figure 21.4. Timer 2 16-Bit Mode Block Diagram

22.2.2. Software Timer (Compare) Mode

In Software Timer mode, the PCA0 counter/timer is compared to the module's 16-bit capture/compare register (PCA0CPHn and PCA0CPLn). When a match occurs, the Capture/Compare Flag (CCFn) in PCA0CN is set to logic ‘1’ and an interrupt request is generated if CCF interrupts are enabled. The CCFn bit is not automatically cleared by hardware when the CPU vectors to the interrupt service routine, and must be cleared by software. Setting the ECOMn and MATn bits in the PCA0CPMn register enables Software Timer mode.

Important Note About Capture/Compare Registers: When writing a 16-bit value to the PCA0 Capture/Compare registers, the low byte should always be written first. Writing to PCA0CPLn clears the ECOMn bit to ‘0’; writing to PCA0CPHn sets ECOMn to ‘1’.

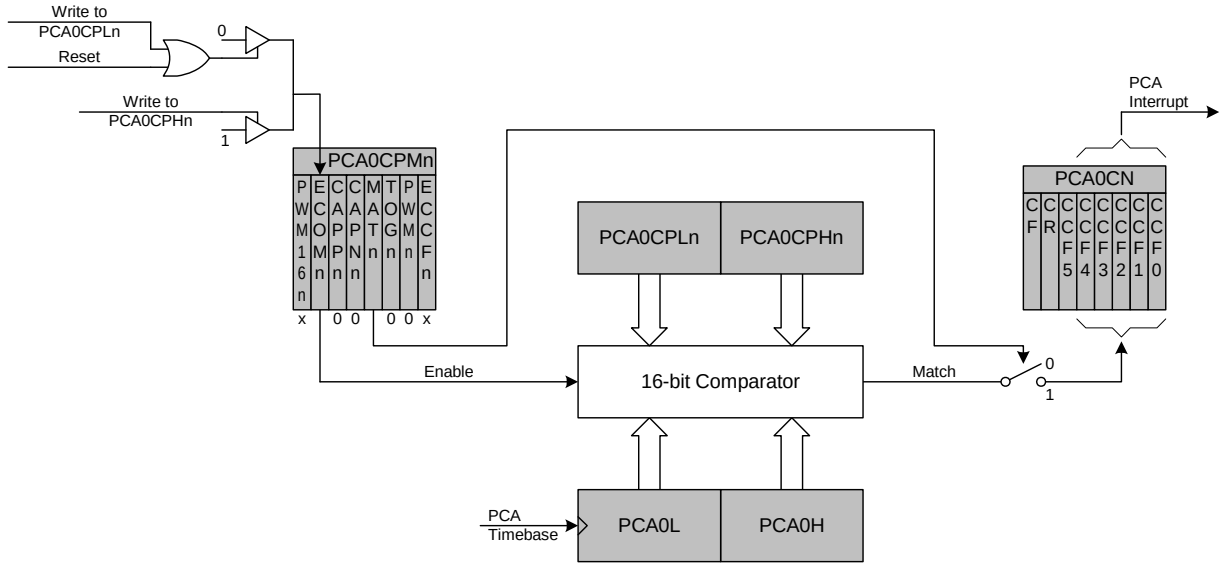

Figure 22.5. PCA Software Timer Mode Diagram

SFR Definition 22.3. PCA0CPMn: PCA0 Capture/Compare Mode

SFR Page: PCA0CPM0: all pages, PCA0CPM1: all pages, PCA0CPM2: all pages, PCA0CPM3: all pages, PCA0CPM4: all pages, PCA0CPM5: all pages

SFR Address: PCA0CPM0: 0xDA, PCA0CPM1: 0xDB, PCA0CPM2: 0xDC, PCA0CPM3: 0xDD, PCA0CPM4: 0xDE, PCA0CPM5: 0xDF

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
PWM16n	ECOMn	CAPPn	CAPNn	MATn	TOGn	PWMn	ECCFn	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bit 7: PWM16n: 16-bit Pulse Width Modulation Enable
This bit selects 16-bit mode when Pulse Width Modulation mode is enabled (PWMn = 1).
0: 8-bit PWM selected.
1: 16-bit PWM selected.

Bit 6: ECOMn: Comparator Function Enable.
This bit enables/disables the comparator function for PCA0 module n.
0: Disabled.
1: Enabled.

Bit 5: CAPPn: Capture Positive Function Enable.
This bit enables/disables the positive edge capture for PCA0 module n.
0: Disabled.
1: Enabled.

Bit 4: CAPNn: Capture Negative Function Enable.
This bit enables/disables the negative edge capture for PCA0 module n.
0: Disabled.
1: Enabled.

Bit 3: MATn: Match Function Enable.
This bit enables/disables the match function for PCA0 module n. When enabled, matches of the PCA0 counter with a module's capture/compare register cause the CCFn bit in PCA0MD register to be set to logic ‘1’.
0: Disabled.
1: Enabled.

Bit 2: TOGn: Toggle Function Enable.
This bit enables/disables the toggle function for PCA0 module n. When enabled, matches of the PCA0 counter with a module's capture/compare register cause the logic level on the CEXn pin to toggle. If the PWMn bit is also set to logic ‘1’, the module operates in Frequency Output Mode.
0: Disabled.
1: Enabled.

Bit 1: PWMn: Pulse Width Modulation Mode Enable.
This bit enables/disables the PWM function for PCA0 module n. When enabled, a pulse width modulated signal is output on the CEXn pin. 8-bit PWM is used if PWM16n is logic ‘0’; 16-bit mode is used if PWM16n logic ‘1’. If the TOGn bit is also set, the module operates in Frequency Output Mode.
0: Disabled.
1: Enabled.

Bit 0: ECCFn: Capture/Compare Flag Interrupt Enable.
This bit sets the masking of the Capture/Compare Flag (CCFn) interrupt.
0: Disable CCFn interrupts.
1: Enable a Capture/Compare Flag interrupt request when CCFn is set.

bit contained a ‘0’ prior to the execution of the “CPL C” opcode, it will properly transition to a 1 when the execution phase of the opcode has completed. This is illustrated in the following table:

Correct operation	Correct operation	Failure case
initial state of C is 1	initial state of C is 0	initial state of C is 1
CPL C	CPL C	CPL C
final state of C is 0	final state of C is 1	final state of C is 1

The instruction order dependency is as follows:

In the failure case, the CPL C opcode must be immediately preceded by a JB, JNB, or JBC opcode.

JB, JNB, and JBC are all conditional branch instructions (JB is “Jump if bit is set”, JNB is “Jump if bit is not set”, and JBC is “Jump if bit is set and clear bit”). Because the branches are conditional, they have both a “branch taken” condition as well as a “branch not taken” condition. Both “branch taken” and “branch not taken” conditions may exhibit the error, as long as the CPL C opcode executes immediately after the branch instruction has executed.

Impacts

The CPL C opcode is often used in math operations, such as address calculations for pointer arithmetic. If present, this behavior can cause undesirable and unpredictable program execution.

The occurrence of this behavior is sensitive to system clock frequency, temperature, and power supply voltage as follows:

JB / JNB / JBC + CPL C opcode sequence present?	VDD	System clock frequency	Temperature range	Failure possible?
No	≥ 3.0 V	≤ 100 MHz	-40 to +85 °C	No
Yes	≥ 3.0 V	≤ 70 MHz	-40 to +85 °C	No

Workaround

The bug can best be addressed by checking to see if the problematic instruction sequence is present in the device firmware and removing it if detected. In most cases, the firmware can be changed to insert a NOP instruction immediately before the CPL C opcode, so that the CPL C instruction does not immediately follow the JB / JNB / JBC opcode in the code execution path.

Silicon Labs has developed a hex file scanner that can be used to determine if a code project contains the instruction sequence above. Instructions for using the scanner, as well as details regarding the scanner’s operation can be found here:

http://community.silabs.com/t5/Silicon-Labs-Knowledge-Base/C8051F360-Rev-B-Erratum-CPU-E101-CPL-C-HEX-Scanner/ta-p/133808

This behavior has been corrected on Revision C of this device.

24. C2 Interface

C8051F36x devices include an on-chip Silicon Laboratories 2-Wire (C2) debug interface to allow Flash programming and in-system debugging with the production part installed in the end application. The C2 interface uses a clock signal (C2CK) and a bi-directional C2 data signal (C2D) to transfer information between the device and a host system. See the C2 Interface Specification for details on the C2 protocol.

24.1. C2 Interface Registers

The following describes the C2 registers necessary to perform Flash programming functions through the C2 interface. All C2 registers are accessed through the C2 interface as described in the C2 Interface Specification.

C2 Register Definition 24.1. C2ADD: C2 Address

Reset Value: 00000000

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

Bits7–0: The C2ADD register is accessed via the C2 interface to select the target Data register for C2 Data Read and Data Write commands.

Address	Description
0x00	Selects the Device ID register for Data Read instructions (DEVICEID)
0x01	Selects the Revision ID register for Data Read instructions (REVID)
0x02	Selects the C2 Flash Programming Control register for Data Read/Write instructions (FPCTL)
0xBF	Selects the C2 Flash Programming Data register for Data Read/Write instructions (FPDAT)

C2 Register Definition 24.2. DEVICEID: C2 Device ID

C2 Address: 0x00

Reset Value: 00010010

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

This read-only register returns the 8-bit device ID: 0x12.

DOCUMENT CHANGE LIST

Revision 0.1 to Revision 0.2

- Updated specification tables with most recently available characterization data.
- Fixed an error with the SYSCLK specification in Table 3.1, “Global Electrical Characteristics,” on page 33.
- Corrected the name of the PMAT bit in SFR Definition 10.2. IP: Interrupt Priority.
- Corrected the reset value for SFR Definition 22.2. PCA0MD: PCA0 Mode.

Revision 0.2 to Revision 1.0

- Updated specification tables with characterization data.
- Fixed Table 1.1, “Product Selection Guide,” on page 19 to reflect the correct number of Port I/O pins for the C8051F361/2/4/5.
- Updated Section “10. Interrupt Handler” on page 107.
  - Added note describing EA change behavior when followed by single cycle instruction.
- Updated SFR Definition 11.1
  - Changed the MAC0SC (MAC0CF.5) bit description to correctly refer to the MAC0SD bit.
- Updated SFR Definition 15.2.
  - Changed the EMI0CF description to properly describe the 1k XRAM boundaries.
- Added Table 16.2, “Internal Low Frequency Oscillator Electrical Characteristics,” on page 171.
- Updated SFR Definition 16.9:
  - Specified that the undefined states for PLLLP3–0 are RESERVED.
- Added Table 19.7 and Table 19.8 on page 231 for UART Baud Rates when using the PLL.
- Updated Table 22.1, “PCA Timebase Input Options,” on page 263:
  - Specified that the undefined states of CPS2–0 are RESERVED.
- Added Revision B to “Revision Specific Behavior” on page 279.

Revision 1.0 to Revision 1.1

- Updated ordering table with Revision C part numbers.
- Updated Figure 17.2. ’Port I/O Cell Block Diagram’ on page 183 to refer to VDD instead of VIO.
- Added Revision C to “Revision Specific Behavior” on page 279.
- Added Revision C to the REVID C2 register in C2 Register Definition 24.3.
- Updated “Digital Supply Current (Stop Mode, shutdown)” typical value in Table 3.1, “Global Electrical Characteristics,” on page 33.
- Updated “Missing Clock Detector Timeout” typical value in Table 12.1, “Reset Electrical Characteristics,” on page 134.