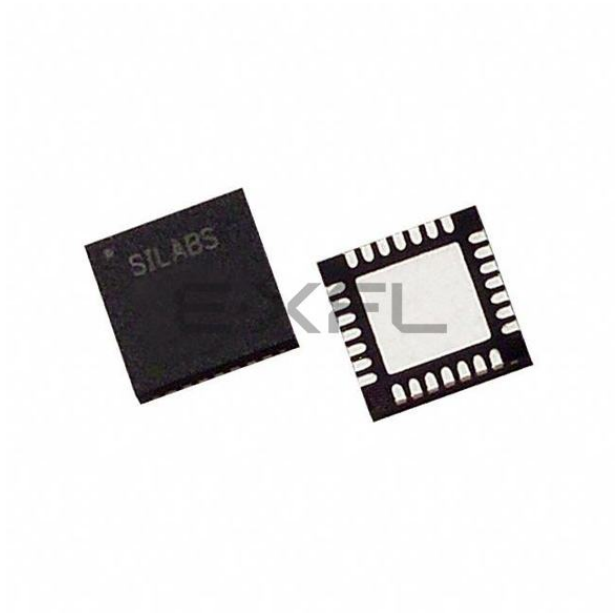

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	25
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 17x10b; D/A 1x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VFQFN Exposed Pad
Supplier Device Package	28-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f367-c-gmr

1.1.3. Additional Features

The C8051F36x SoC family includes several key enhancements to the CIP-51 core and peripherals to improve performance and ease of use in end applications.

The extended interrupt handler provides 16 interrupt sources into the CIP-51 (as opposed to 7 for the standard 8051), allowing numerous analog and digital peripherals to interrupt the controller. An interrupt driven system requires less intervention by the MCU, giving it more effective throughput. The extra interrupt sources are very useful when building multi-tasking, real-time systems.

Eight reset sources are available: power-on reset circuitry (POR), an on-chip V_{DD} Monitor (forces reset when power supply voltage drops below V_{RST} as given in Table 12.1 on page 134), a Watchdog Timer, a Missing Clock Detector, a voltage level detection from Comparator0, a forced software reset, an external reset pin, and an illegal Flash access protection circuit. Each reset source except for the POR, Reset Input Pin, or Flash error may be disabled by the user in software. The WDT may be permanently enabled in software after a power-on reset during MCU initialization.

The internal oscillator factory calibrated to 24.5 MHz ±2%. This internal oscillator period may be user programmed in ~0.5% increments. An additional low-frequency oscillator is also available which facilitates low-power operation. An external oscillator drive circuit is included, allowing an external crystal, ceramic resonator, capacitor, RC, or CMOS clock source to generate the system clock. If desired, the system clock source may be switched on-the-fly between both internal and external oscillator circuits. An external oscillator can also be extremely useful in low power applications, allowing the MCU to run from a slow (power saving) source, while periodically switching to the fast (up to 25 MHz) internal oscillator as needed. Additionally, an on-chip PLL is provided to achieve higher system clock speeds for increased throughput.

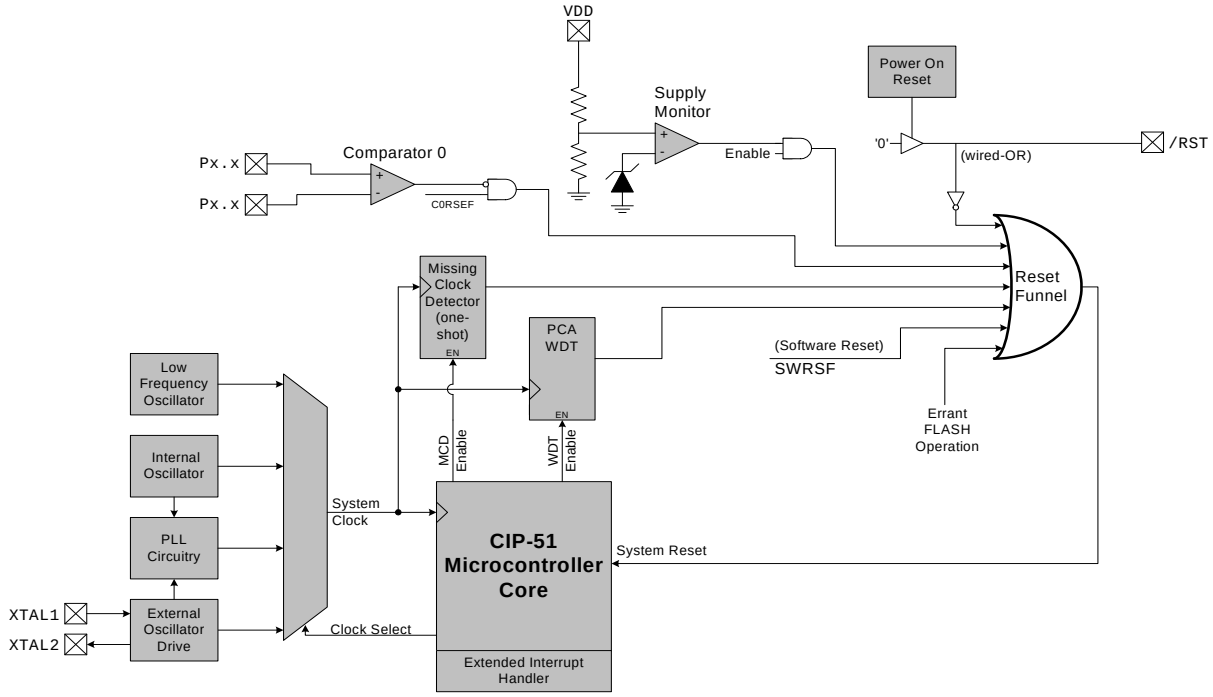

Figure 1.5. On-Chip Clock and Reset

SFR Definition 5.9. ADC0LTH: ADC0 Less-Than Data High Byte

SFR Page: all pages
SFR Address: 0xC6

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7–0: High byte of ADC0 Less-Than Data Word.

SFR Definition 5.10. ADC0LTL: ADC0 Less-Than Data Low Byte

SFR Page: all pages
SFR Address: 0xC5

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7–0: Low byte of ADC0 Less-Than Data Word.

5.4.2. Window Detector In Differential Mode

Figure 5.8 shows two example window comparisons for right-justified, differential data, with ADC0LTH:ADC0LTL = 0x0040 (+64d) and ADC0GTH:ADC0GTH = 0xFFFF (-1d). In differential mode, the measurable voltage between the input pins is between -VREF and VREF*(511/512). Output codes are represented as 10-bit 2's complement signed integers. In the left example, an AD0WINT interrupt will be generated if the ADC0 conversion word (ADC0H:ADC0L) is within the range defined by ADC0GTH:ADC0GTL and ADC0LTH:ADC0LTL (if 0xFFFF (-1d) < ADC0H:ADC0L < 0x0040 (64d)). In the right example, an AD0WINT interrupt will be generated if the ADC0 conversion word is outside of the range defined by the ADC0GT and ADC0LT registers (if ADC0H:ADC0L < 0xFFFF (-1d) or ADC0H:ADC0L > 0x0040 (+64d)). Figure 5.9 shows an example using left-justified data with the same comparison values.

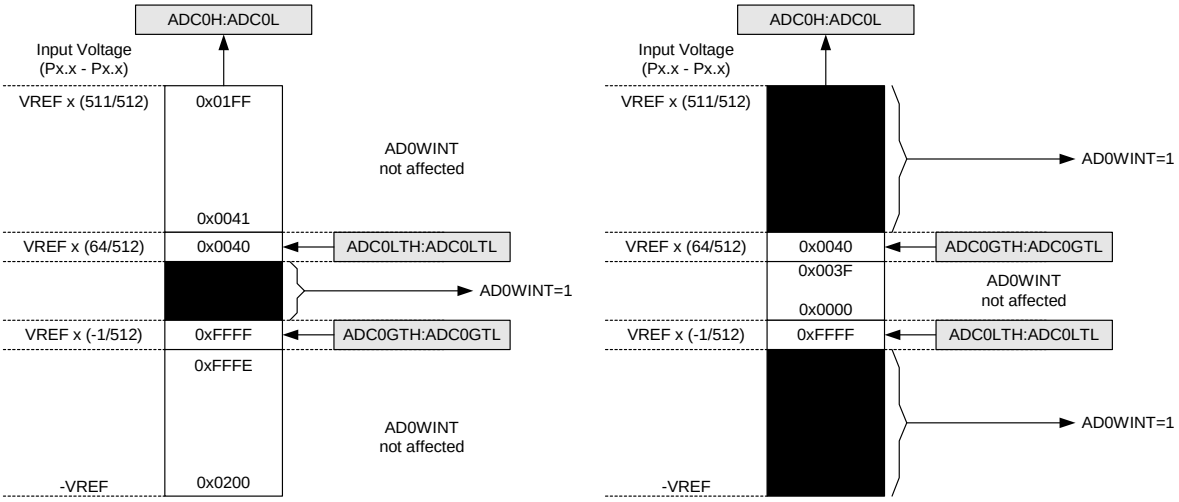

Figure 5.8. ADC Window Compare Example: Right-Justified Differential Data

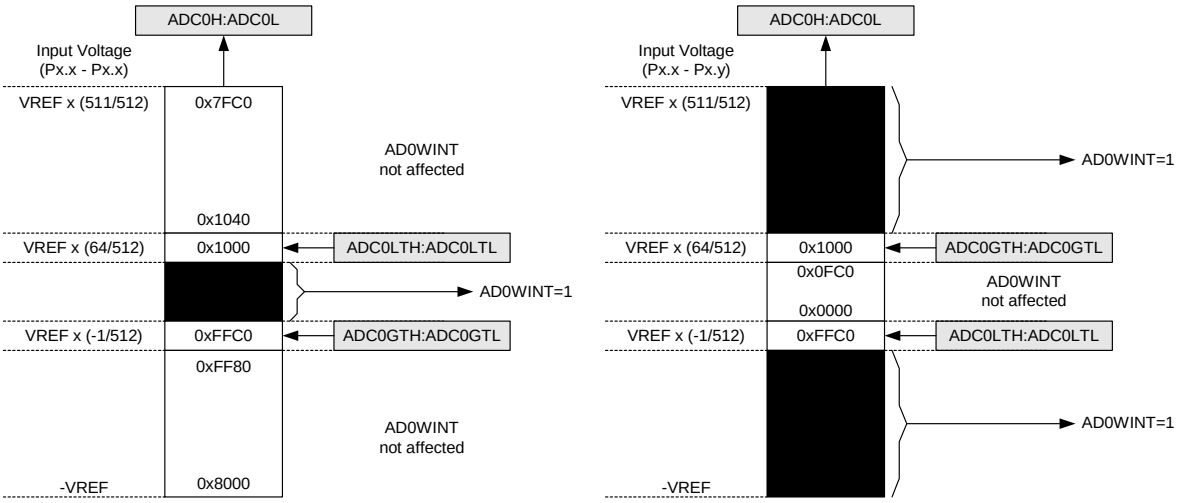

Figure 5.9. ADC Window Compare Example: Left-Justified Differential Data

7. Voltage Reference (C8051F360/1/2/6/7/8/9)

The Voltage reference MUX on the C8051F360/1/2/6/7/8/9 devices is configurable to use an externally connected voltage reference, the internal reference voltage generator, or the V_{DD} power supply voltage (see Figure 7.1). The REFSL bit in the Reference Control register (REF0CN) selects the reference source. For an external source or the internal reference, REFSL should be set to ‘0’. To use V_{DD} as the reference source, REFSL should be set to ‘1’.

The BIASE bit enables the internal voltage bias generator, which is used by the ADC, Temperature Sensor, internal oscillators, and Current DAC. This bias is enabled when any of the aforementioned peripherals are enabled. The bias generator may be enabled manually by writing a ‘1’ to the BIASE bit in register REF0CN; see SFR Definition 7.1 for REF0CN register details. The electrical specifications for the voltage reference circuit are given in Table 7.1.

The internal voltage reference circuit consists of a 1.2 V, temperature stable bandgap voltage reference generator and a gain-of-two output buffer amplifier. The internal voltage reference can be driven out on the VREF pin by setting the REFBE bit in register REF0CN to a ‘1’ (see SFR Definition 7.1). The maximum load seen by the VREF pin must be less than 200 µA to GND. When using the internal voltage reference, bypass capacitors of 0.1 µF and 4.7 µF are recommended from the VREF pin to GND. If the internal reference is not used, the REFBE bit should be cleared to ‘0’. Electrical specifications for the internal voltage reference are given in Table 7.1.

Important Note about the VREF Pin: Port pin P0.3 on the C8051F360 device and P0.0 on C8051F361/2/6/7/89 devices is used as the external VREF input and as an output for the internal VREF. When using either an external voltage reference or the internal reference circuitry, the port pin should be configured as an analog pin, and skipped by the Digital Crossbar. To configure the port pin as an analog pin, set the appropriate bit to ‘0’ in register P0MDIN. To configure the Crossbar to skip the VREF port pin, set the appropriate bit to ‘1’ in register P0SKIP. Refer to Section “17. Port Input/Output” on page 182 for

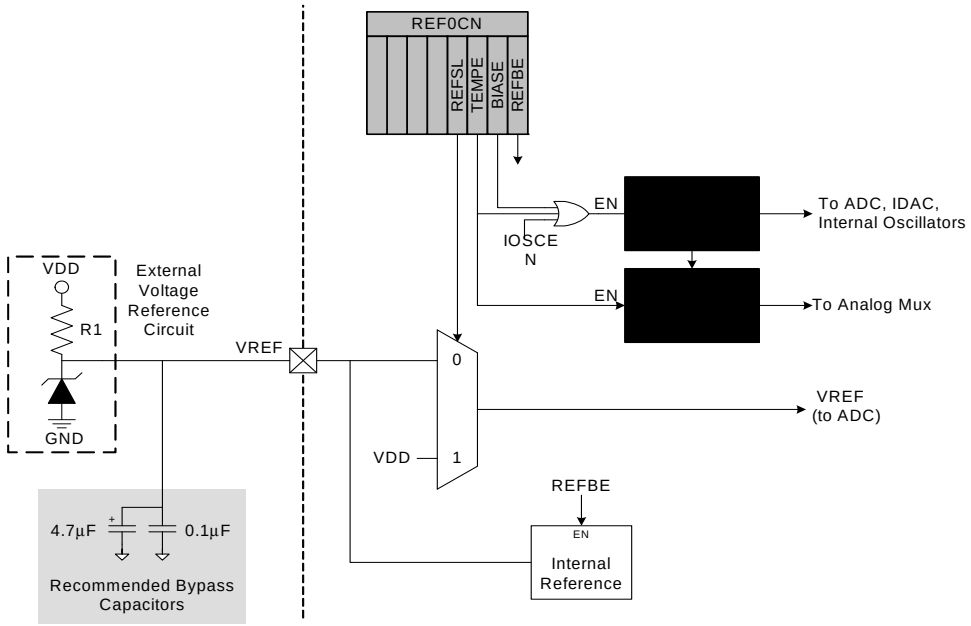

Figure 7.1. Voltage Reference Functional Block Diagram

Table 8.1. Comparator Electrical Characteristics

V_{DD} = 3.0 V, –40 to +85 °C unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Units
Response Time: Mode 0, Vcm* = 1.5 V	CPx+ – CPx– = 100 mV	—	100	—	ns
	CPx+ – CPx– = –100 mV	—	250	—	ns
Response Time: Mode 1, Vcm* = 1.5 V	CPx+ – CPx– = 100 mV	—	175	—	ns
	CPx+ – CPx– = –100 mV	—	500	—	ns
Response Time: Mode 2, Vcm* = 1.5 V	CPx+ – CPx– = 100 mV	—	320	—	ns
	CPx+ – CPx– = –100 mV	—	1100	—	ns
Response Time: Mode 3, Vcm* = 1.5 V	CPx+ – CPx– = 100 mV	—	1050	—	ns
	CPx+ – CPx– = –100 mV	—	5200	—	ns
Common-Mode Rejection Ratio		—	1.26	5	mV/V
Positive Hysteresis 1	CPxHYP1–0 = 00	—	0	1	mV
Positive Hysteresis 2	CPxHYP1–0 = 01	1	5	10	mV
Positive Hysteresis 3	CPxHYP1–0 = 10	6	10	20	mV
Positive Hysteresis 4	CPxHYP1–0 = 11	12	20	30	mV
Negative Hysteresis 1	CPxHYN1–0 = 00	—	0	1	mV
Negative Hysteresis 2	CPxHYN1–0 = 01	1	5	10	mV
Negative Hysteresis 3	CPxHYN1–0 = 10	6	10	20	mV
Negative Hysteresis 4	CPxHYN1–0 = 11	12	20	30	mV
Inverting or Non-Inverting Input Voltage Range		–0.25	—	V_{DD} + 0.25	V
Input Capacitance		—	4	—	pF
Input Bias Current		—	0.001	—	nA
Input Offset Voltage		–5	—	+5	mV
Power Supply					
Power Supply Rejection		—	0.3	—	mV/V
Power-up Time		—	10	—	µs
Supply Current at DC	Mode 0	—	11.4	20	µA
	Mode 1	—	4.6	10	µA
	Mode 2	—	1.9	5	µA
	Mode 3	—	0.4	2.5	µA

***Note:** Vcm is the common-mode voltage on CPx+ and CPx–.

SFR Definition 9.1. SFR0CN: SFR Page Control

SFR Page: F
SFR Address: 0xE5

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SFRPGEN	00000001
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7–1: RESERVED. Read = 0000000b. Must Write 0000000b.
Bit 0: SFRPGEN: SFR Automatic Page Control Enable.
Upon interrupt, the C8051 Core will vector to the specified interrupt service routine and automatically switch to SFR page 0. This bit is used to control this autopaging function.
0: SFR Automatic Paging disabled. C8051 core will not automatically change to SFR page 0.
1: SFR Automatic Paging enabled. Upon interrupt, the C8051 will automatically switch to SFR page 0.

SFR Definition 9.2. SFRPAGE: SFR Page

SFR Page: all pages
SFR Address: 0xA7

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7–0: SFR Page Bits: Byte Represents the SFR Page the C8051 MCU uses when reading or modifying SFR's.
Write: Sets the SFR Page.
Read: Byte is the SFR page the C8051 MCU is using.

When enabled in the SFR Page Control Register (SFR0CN), the C8051 will automatically switch to SFR Page 0x00 and return to the previous SFR page upon return from interrupt (unless SFR Stack was altered before a returning from the interrupt).
SFRPAGE is the top byte of the SFR Page Stack, and push/pop events of this stack are caused by interrupts (and **not** by reading/writing to the SFRPAGE register)

Table 9.3. Special Function Registers (Continued)

SFRs are listed in alphabetical order. All undefined SFR locations are reserved.

Register	Address	SFR Page	Description	Page No.
PCA0CPL2	0xEB	All Pages	PCA Module 2 Capture/Compare Low Byte	page 277
PCA0CPL3	0xED	All Pages	PCA Module 3 Capture/Compare Low Byte	page 277
PCA0CPL4	0xFD	All Pages	PCA Module 4 Capture/Compare Low Byte	page 277
PCA0CPL5	0xF5	All Pages	PCA Module 5 Capture/Compare Low Byte	page 277
PCA0CPM0	0xDA	All Pages	PCA Module 0 Mode	page 276
PCA0CPM1	0xDB	All Pages	PCA Module 1 Mode	page 276
PCA0CPM2	0xDC	All Pages	PCA Module 2 Mode	page 276
PCA0CPM3	0xDD	All Pages	PCA Module 3 Mode	page 276
PCA0CPM4	0xDE	All Pages	PCA Module 4 Mode	page 276
PCA0CPM5	0xDF	All Pages	PCA Module 5 Mode	page 276
PCA0H	0xFA	All Pages	PCA Counter High Byte	page 277
PCA0L	0xF9	All Pages	PCA Counter Low Byte	page 277
PCA0MD	0xD9	All Pages	PCA Mode	page 275
PCON	0x87	All Pages	Power Control	page 106
PLL0CN	0xB3	F	PLL Control	page 179
PLL0DIV	0xA9	F	PLL Divider	page 179
PLL0FLT	0xB2	F	PLL Filter	page 180
PLL0MUL	0xB1	F	PLL Multiplier	page 180
PSCTL	0x8F	0	Flash Write/Erase Control	page 142
PSW	0xD0	All Pages	Program Status Word	page 103
REF0CN	0xD1	All Pages	Voltage Reference Control	page 68[1]
RSTSRC	0xEF	All Pages	Reset Source	page 133
SBUF0	0x99	All Pages	UART 0 Data Buffer	page 224
SCON0	0x98	All Pages	UART 0 Control	page 223
SFR0CN	0xE5	F	SFR Page Control	page 94
SFRLAST	0x86	All Pages	SFR Stack Last Page	page 95
SFRNEXT	0x85	All Pages	SFR Stack Next Page	page 95
SFRPAGE	0xA7	All Pages	SFR Page Select	page 94
SMB0CF	0xC1	All Pages	SMBus Configuration	page 206
SMB0CN	0xC0	All Pages	SMBus Control	page 208
SMB0DAT	0xC2	All Pages	SMBus Data	page 210

Notes:
1. Refers to a register in the C8051F360/1/2/6/7/8/9 only.
2. Refers to a register in the C8051F360/3 only.

SFR Definition 10.5. EIE2: Extended Interrupt Enable 2

SFR Page: all pages
SFR Address: 0xE7

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
–	–	–	–	–	–	EMAT	–	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7–2: UNUSED. Read = 000000b. Write = don't care.
Bit 1: EMAT: Enable Port Match Interrupt.
This bit sets the masking of the Port Match interrupt.
0: Disable the Port Match interrupt.
1: Enable the Port Match interrupt.
Bit 0: UNUSED. Read = 0b. Write = don't care.

SFR Definition 10.6. EIP2: Extended Interrupt Priority 2

SFR Page: F
SFR Address: 0xCF

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
–	–	–	–	–	–	PMAT	–	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7–2: UNUSED. Read = 000000b. Write = don't care.
Bit 1: PMAT: Port Match Interrupt Priority Control.
This bit sets the priority of the Port Match interrupt.
0: Port Match interrupt set to low priority level.
1: Port Match interrupt set to high priority level.
Bit 0: UNUSED. Read = 0b. Write = don't care.

SFR Definition 11.2. MAC0STA: MAC0 Status

SFR Page: 0
SFR Address: 0xCF

R	R	R	R	R/W	R/W	R/W	R/W	Reset Value
–	–	–	–	MAC0HO	MAC0Z	MAC0SO	MAC0N	00000100
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit Addressable

Bits 7–4: UNUSED: Read = 0000b, Write = don't care.

Bit 3: MAC0HO: Hard Overflow Flag.
This bit is set to '1' whenever an overflow out of the MAC0OVR register occurs during a MAC operation (i.e. when MAC0OVR changes from 0x7F to 0x80 or from 0x80 to 0x7F). The hard overflow flag must be cleared in software by directly writing it to '0', or by resetting the MAC logic using the MAC0CA bit in register MAC0CF.

Bit 2: MAC0Z: Zero Flag.
This bit is set to '1' if a MAC0 operation results in an Accumulator value of zero. If the result is non-zero, this bit will be cleared to '0'.

Bit 1: MAC0SO: Soft Overflow Flag.
This bit is set to '1' when a MAC operation causes an overflow into the sign bit (bit 31) of the MAC0 Accumulator. If the overflow condition is corrected after a subsequent MAC operation, this bit is cleared to '0'.

Bit 0: MAC0N: Negative Flag.
If the MAC Accumulator result is negative, this bit will be set to '1'. If the result is positive or zero, this flag will be cleared to '0'.

Note: The contents of this register should not be changed by software during the first two MAC0 pipeline stages.

SFR Definition 11.3. MAC0AH: MAC0 A High Byte

SFR Page: 0
SFR Address: 0xA5

R	R	R	R	R	R	R	R	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7–0: High Byte (bits 15–8) of MAC0 A Register.

12. Reset Sources

Reset circuitry allows the controller to be easily placed in a predefined default condition. On entry to this reset state, the following occur:

- CIP-51 halts program execution
- Special Function Registers (SFRs) are initialized to their defined reset values
- External Port pins are forced to a known state
- Interrupts and timers are disabled.

All SFRs are reset to the predefined values noted in the SFR detailed descriptions. The contents of internal data memory are unaffected during a reset; any previously stored data is preserved. However, since the stack pointer SFR is reset, the stack is effectively lost, even though the data on the stack is not altered.

The Port I/O latches are reset to 0xFF (all logic ones) in open-drain mode. Weak pullups are enabled during and after the reset. For V_{DD} Monitor and power-on resets, the $\overline{RST}$ pin is driven low until the device exits the reset state.

On exit from the reset state, the program counter (PC) is reset, and the system clock defaults to the internal oscillator. Refer to Section “16. Oscillators” on page 168 for information on selecting and configuring the system clock source. The Watchdog Timer is enabled with the system clock divided by 12 as its clock source (Section “22.3. Watchdog Timer Mode” on page 270 details the use of the Watchdog Timer). Program execution begins at location 0x0000.

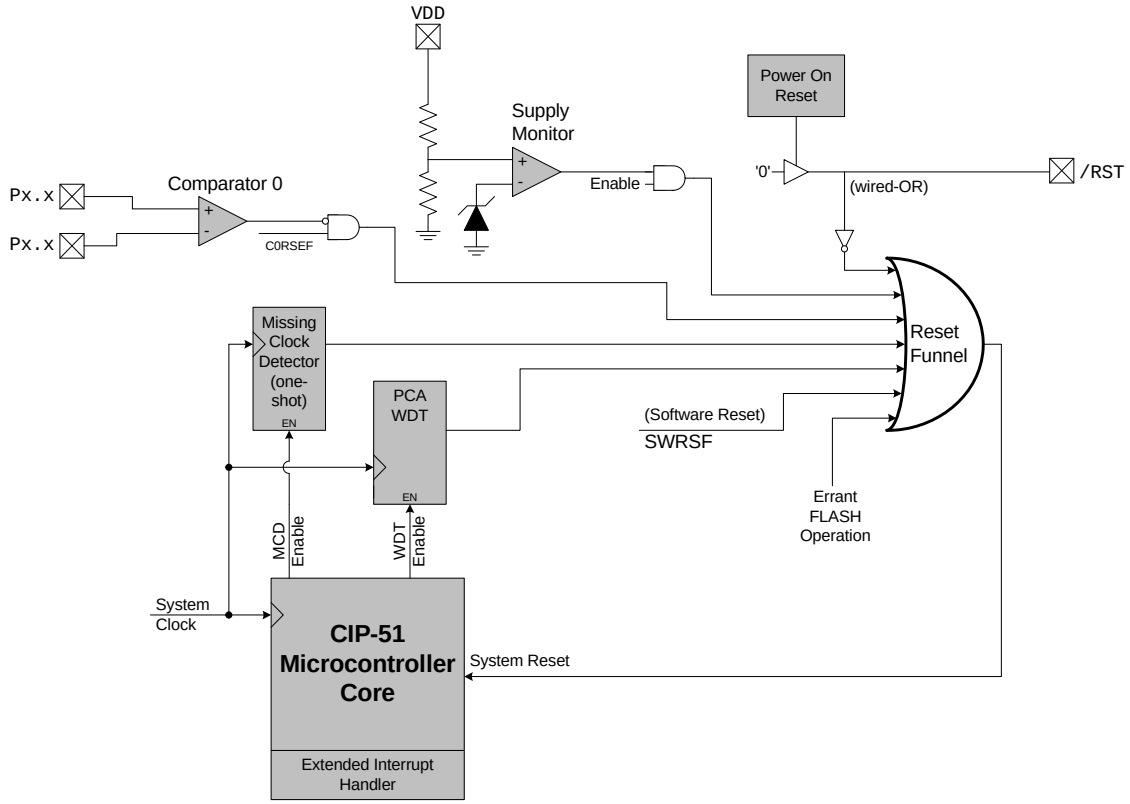

Figure 12.1. Reset Sources

13.4. Flash Read Timing

On reset, the C8051F36x Flash read timing is configured for operation with system clocks up to 25 MHz. If the system clock will not be increased above 25 MHz, then the Flash timing registers may be left at their reset value.

For every Flash read or fetch, the system provides an internal Flash read strobe to the Flash memory. The Flash read strobe lasts for one or two system clock cycles, based on the FLRT bits (FLSCL.4 and FLSCL.5). **If the system clock is greater than 25 MHz, the FLRT bit must be changed to the appropriate setting.** Otherwise, data read or fetched from Flash may not represent the actual contents of Flash. When the Flash read strobe is asserted, Flash memory is active. When it is de-asserted, Flash memory is in a low power state.

The recommended procedure for updating FLRT is:

Step 1. Select SYSCLK to 25 MHz or less.
Step 2. Disable the prefetch engine (CHPFEN = ‘0’ in CCH0CN register).
Step 3. Set the FLRT bits to the appropriate setting for the SYSCLK.
Step 4. Enable the prefetch engine (CHPFEN = ‘1’ in CCH0CN register).

SFR Definition 13.3. FLSCL: Flash Memory Control

SFR Page: 0
SFR Address: 0xB6

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
–	–	FLRT		Reserved	Reserved	Reserved	Reserved	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7–6: UNUSED. Read = 00b. Write = don’t care.
Bits 5–4: FLRT: Flash Read Time.
These bits should be programmed to the smallest allowed value, according to the system clock speed.
00: SYSCLK ≤ 25 MHz.
01: SYSCLK ≤ 50 MHz.
10: SYSCLK ≤ 75 MHz.
11: SYSCLK ≤ 100 MHz.
Bits 3–0: RESERVED. Read = 0000b. Must Write 0000b.

Important Note: When changing the FLRT bits to a lower setting (e.g. when changing from a value of 11b to 00b), cache reads, cache writes, and the prefetch engine should be disabled using the CCH0CN register (see SFR Definition 14.1).

16.1.1. Internal Oscillator Suspend Mode

When software writes a logic ‘1’ to SUSPEND (OSCICN.5), the internal oscillator is suspended. If the system clock is derived from the internal oscillator, the input clock to the peripheral or CIP-51 will be stopped until one of the following events occur:

- Port 0 Match Event.
- Port 1 Match Event.
- Port 2 Match Event.
- Comparator 0 enabled and output is logic ‘0’.
- Comparator 1 enabled and output is logic ‘0’.

When one of the internal oscillator awakening events occur, the internal oscillator, CIP-51, and affected peripherals resume normal operation, regardless of whether the event also causes an interrupt. The CPU resumes execution at the instruction following the write to SUSPEND.

Note: Before entering SUSPEND mode, SYSCLK should be switched to run off of the internal oscillator and not the PLL. When the CPU wakes due to the awakening event, the PLL must be reinitialized before switching back to it as the SYSCLK source.

SFR Definition 16.1. OSCICL: Internal Oscillator Calibration.

SFR Page: F
SFR Address: 0xBF

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								Variable
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7–0: OSCICL: Internal Oscillator Calibration Register.
This register calibrates the internal oscillator period. The reset value for OSCICL defines the internal oscillator base frequency. The reset value is factory calibrated to generate an internal oscillator frequency of 24.5 MHz.

16.8.3. Powering on and Initializing the PLL

To set up and use the PLL as the system clock after power-up of the device, the following procedure should be implemented:

Step 1. Ensure that the reference clock to be used (internal or external) is running and stable.
Step 2. Set the PLLSRC bit (PLL0CN.2) to select the desired clock source for the PLL.
Step 3. Program the Flash read timing bits, FLRT (FLSCL.5–4) to the appropriate value for the new clock rate (see Section “13. Flash Memory” on page 135).
Step 4. Enable power to the PLL by setting PLLPWR (PLL0CN.0) to ‘1’.
Step 5. Program the PLL0DIV register to produce the divided reference frequency to the PLL.
Step 6. Program the PLLLP3–0 bits (PLL0FLT.3–0) to the appropriate range for the divided reference frequency.
Step 7. Program the PLLICO1–0 bits (PLL0FLT.5–4) to the appropriate range for the PLL output frequency.
Step 8. Program the PLL0MUL register to the desired clock multiplication factor.
Step 9. Wait at least 5 µs, to provide a fast frequency lock.
Step 10. Enable the PLL by setting PLLEN (PLL0CN.1) to ‘1’.
Step 11. Poll PLLLCK (PLL0CN.4) until it changes from ‘0’ to ‘1’.
Step 12. Switch the System Clock source to the PLL using the CLKSEL register.

If the PLL characteristics need to be changed when the PLL is already running, the following procedure should be implemented:

Step 1. The system clock should first be switched to either the internal oscillator or an external clock source that is running and stable, using the CLKSEL register.
Step 2. Ensure that the reference clock to be used for the new PLL setting (internal or external) is running and stable.
Step 3. Set the PLLSRC bit (PLL0CN.2) to select the new clock source for the PLL.
Step 4. If moving to a faster frequency, program the Flash read timing bits, FLRT (FLSCL.5–4) to the appropriate value for the new clock rate (see Section “13. Flash Memory” on page 135).
Step 5. Disable the PLL by setting PLLEN (PLL0CN.1) to ‘0’.
Step 6. Program the PLL0DIV register to produce the divided reference frequency to the PLL.
Step 7. Program the PLLLP3–0 bits (PLL0FLT.3–0) to the appropriate range for the divided reference frequency.
Step 8. Program the PLLICO1-0 bits (PLL0FLT.5–4) to the appropriate range for the PLL output frequency.
Step 9. Program the PLL0MUL register to the desired clock multiplication factor.
Step 10. Enable the PLL by setting PLLEN (PLL0CN.1) to ‘1’.
Step 11. Poll PLLLCK (PLL0CN.4) until it changes from ‘0’ to ‘1’.
Step 12. Switch the System Clock source to the PLL using the CLKSEL register.
Step 13. If moving to a slower frequency, program the Flash read timing bits, FLRT (FLSCL.5–4) to the appropriate value for the new clock rate (see Section “13. Flash Memory” on page 135). **Important Note: Cache reads, cache writes, and the prefetch engine should be disabled whenever the FLRT bits are changed to a lower setting.**

17.1. Priority Crossbar Decoder

The Priority Crossbar Decoder (Figure 17.3) assigns a priority to each I/O function, starting at the top with UART0. When a digital resource is selected, the least-significant unassigned Port pin is assigned to that resource (excluding UART0, which will be assigned to specific port pins (P0.1 and P0.2 in the C8051F360/3 devices, P0.4 and P0.5 in the C8051F361/2/4/5/6/7/8/9 devices). If a Port pin is assigned, the Crossbar skips that pin when assigning the next selected resource. Additionally, the Crossbar will skip Port pins whose associated bits in the PnSKIP registers are set. The PnSKIP registers allow software to skip Port pins that are to be used for analog input, dedicated functions, or GPIO.

Important Note on Crossbar Configuration: If a Port pin is claimed by a peripheral without use of the Crossbar, its corresponding PnSKIP bit should be set. This applies to the port pins associated with the external oscillator, V_{REF}, external CNVSTR signal, IDA0, and any selected ADC or comparator inputs. The Crossbar skips selected pins as if they were already assigned, and moves to the next unassigned pin. Figure 17.3 shows the Crossbar Decoder priority with no Port pins skipped (P0SKIP, P1SKIP, P2SKIP, P3SKIP = 0x00); Figure 17.4 shows the Crossbar Decoder priority with the P1.0 and P1.1 pins skipped (P1SKIP = 0x03).

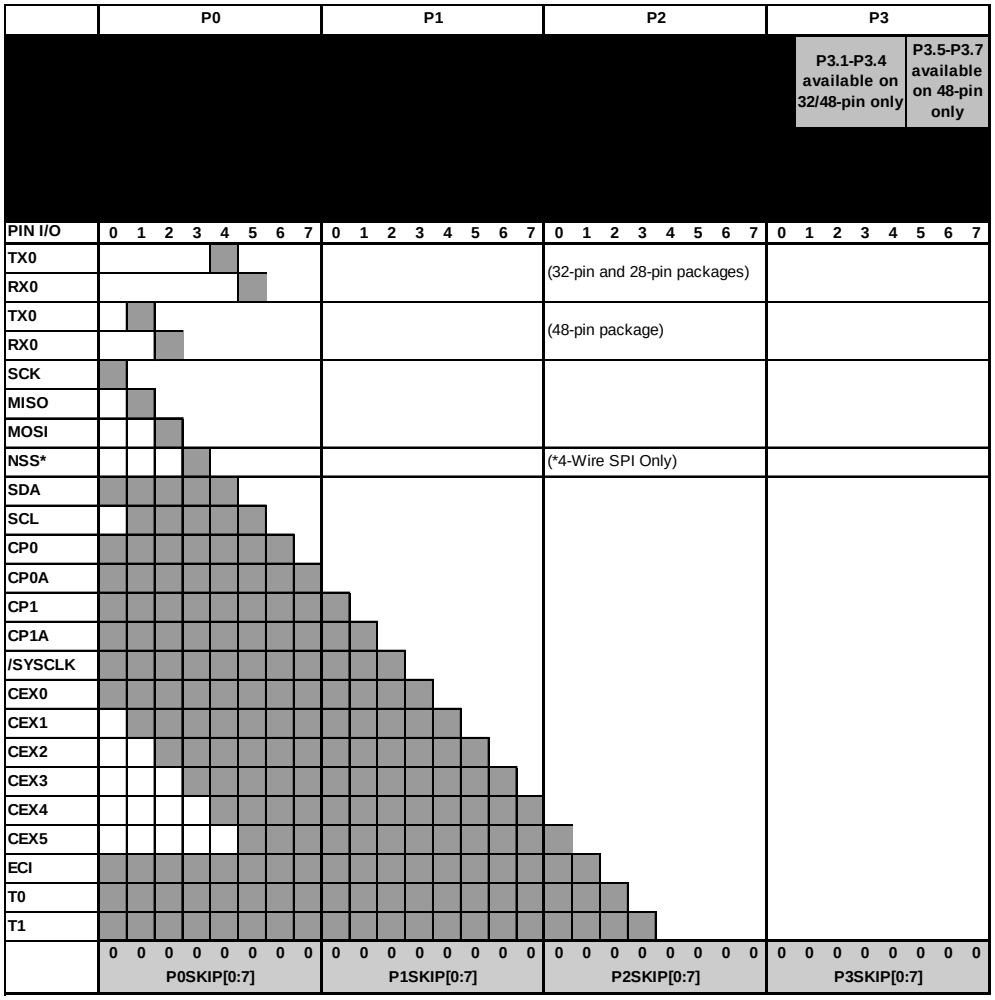

Figure 17.3. Crossbar Priority Decoder with No Pins Skipped

SFR Definition 17.16. P2MDIN: Port2 Input Mode

SFR Page: F
SFR Address: 0xF3

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7–0: Analog Input Configuration Bits for P2.7-P2.0 (respectively).
Port pins configured as analog inputs have their weak pullup, digital driver, and digital receiver disabled.
0: Corresponding P2.n pin is configured as an analog input.
1: Corresponding P2.n pin is not configured as an analog input.

SFR Definition 17.17. P2MDOUT: Port2 Output Mode

SFR Page: F
SFR Address: 0xA6

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7–0: Output Configuration Bits for P2.7-P2.0 (respectively): ignored if corresponding bit in register P2MDIN is logic ‘0’.
0: Corresponding P2.n Output is open-drain.
1: Corresponding P2.n Output is push-pull.

18.5.3. Slave Receiver Mode

Serial data is received on SDA and the clock is received on SCL. When slave events are enabled (INH = 0), the interface enters Slave Receiver Mode when a START followed by a slave address and direction bit (WRITE in this case) is received. Upon entering Slave Receiver Mode, an interrupt is generated and the ACKRQ bit is set. Software responds to the received slave address with an ACK, or ignores the received slave address with a NACK. If the received slave address is ignored, slave interrupts will be inhibited until the next START is detected. If the received slave address is acknowledged, zero or more data bytes are received. Software must write the ACK bit after each received byte to ACK or NACK the received byte. The interface exits Slave Receiver Mode after receiving a STOP. Note that the interface will switch to Slave Transmitter Mode if SMB0DAT is written while an active Slave Receiver. Figure 18.7 shows a typical Slave Receiver sequence. Two received data bytes are shown, though any number of bytes may be received. Notice that the 'data byte transferred' interrupts occur **before** the ACK cycle in this mode.

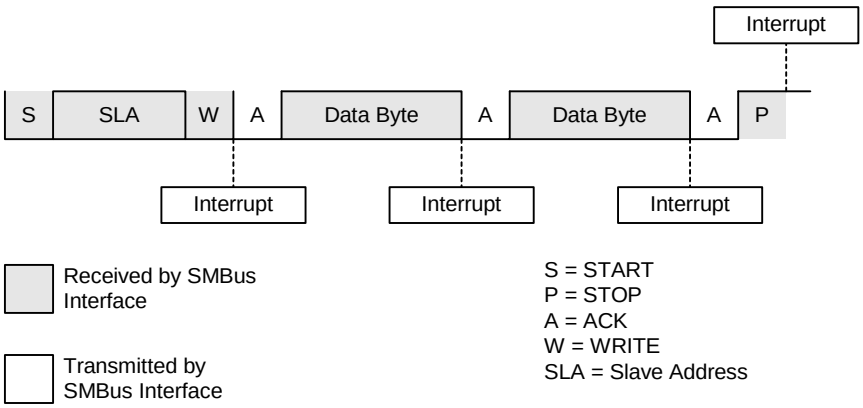

Figure 18.7. Typical Slave Receiver Sequence

21.1.4. Mode 3: Two 8-bit Counter/Timers (Timer 0 Only)

In Mode 3, Timer 0 is configured as two separate 8-bit counter/timers held in TL0 and TH0. The counter/timer in TL0 is controlled using the Timer 0 control/status bits in TCON and TMOD: TR0, C/T0, GATE0 and TF0. TL0 can use either the system clock or an external input signal as its timebase. The TH0 register is restricted to a timer function sourced by the system clock or prescaled clock. TH0 is enabled using the Timer 1 run control bit TR1. TH0 sets the Timer 1 overflow flag TF1 on overflow and thus controls the Timer 1 interrupt.

Timer 1 is inactive in Mode 3. When Timer 0 is operating in Mode 3, Timer 1 can be operated in Modes 0, 1 or 2, but cannot be clocked by external signals nor set the TF1 flag and generate an interrupt. However, the Timer 1 overflow can be used to generate baud rates for the SMBus and/or UART, and/or initiate ADC conversions. While Timer 0 is operating in Mode 3, Timer 1 run control is handled through its mode settings. To run Timer 1 while Timer 0 is in Mode 3, set the Timer 1 Mode as 0, 1, or 2. To disable Timer 1, configure it for Mode 3.

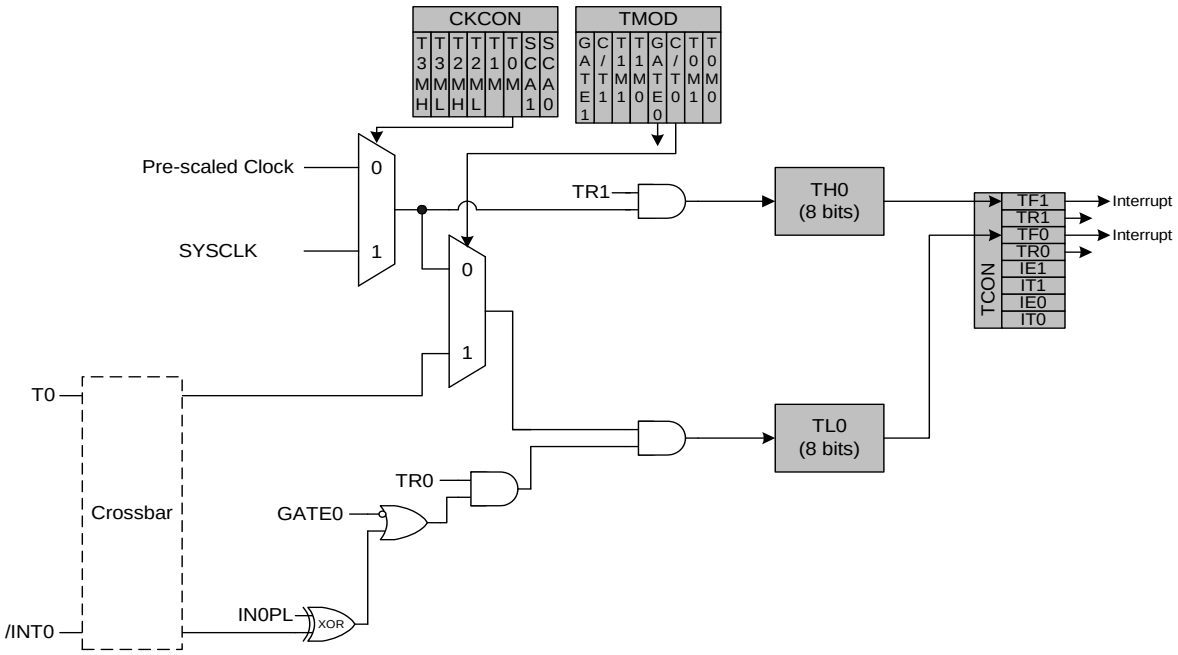

Figure 21.3. T0 Mode 3 Block Diagram

SFR Definition 21.4. TL0: Timer 0 Low Byte

SFR Page: all pages
SFR Address: 0x8A

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7–0: TL0: Timer 0 Low Byte.
The TL0 register is the low byte of the 16-bit Timer 0.

SFR Definition 21.5. TL1: Timer 1 Low Byte

SFR Page: all pages
SFR Address: 0x8B

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7–0: TL1: Timer 1 Low Byte.
The TL1 register is the low byte of the 16-bit Timer 1.

SFR Definition 21.6. TH0: Timer 0 High Byte

SFR Page: all pages
SFR Address: 0x8C

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7–0: TH0: Timer 0 High Byte.
The TH0 register is the high byte of the 16-bit Timer 0.

SFR Definition 21.7. TH1: Timer 1 High Byte

SFR Page: all pages
SFR Address: 0x8D

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:

Bits 7–0: TH1: Timer 1 High Byte.
The TH1 register is the high byte of the 16-bit Timer 1.

SFR Definition 22.4. PCA0L: PCA0 Counter/Timer Low Byte

SFR Page: all pages
SFR Address: 0xF9

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7–0: PCA0L: PCA0 Counter/Timer Low Byte.
The PCA0L register holds the low byte (LSB) of the 16-bit PCA0 Counter/Timer.

SFR Definition 22.5. PCA0H: PCA0 Counter/Timer High Byte

SFR Page: all pages
SFR Address: 0xFA

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7–0: PCA0H: PCA0 Counter/Timer High Byte.
The PCA0H register holds the high byte (MSB) of the 16-bit PCA0 Counter/Timer.

SFR Definition 22.6. PCA0CPLn: PCA0 Capture Module Low Byte

SFR Page: PCA0CPL0: all pages, PCA0CPL1: all pages, PCA0CPL2: all pages, PCA0CPL3: all pages, PCA0CPL4: all pages, PCA0CPL5: all pages
SFR Address: PCA0CPL0: 0xFB, PCA0CPL1: 0xE9, PCA0CPL2: 0xEB, PCA0CPL3: 0xED, PCA0CPL4: 0xFD, PCA0CPL5: 0xF5

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

Bits 7–0: PCA0CPLn: PCA0 Capture Module Low Byte.
The PCA0CPLn register holds the low byte (LSB) of the 16-bit capture module n.

IoT Portfolio
www.silabs.com/IoT

SW/HW
www.silabs.com/simplicity

Quality
www.silabs.com/quality

Support and Community
community.silabs.com

SILICON LABS®

Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
USA

http://www.silabs.com