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Understanding Embedded - Microcontroller, Microprocessor, FPGA Modules

Embedded - Microcontroller, Microprocessor, and FPGA Modules are fundamental components in modern electronic systems, offering a wide range of functionalities and capabilities. Microcontrollers are compact integrated circuits designed to execute specific control tasks within an embedded system. They typically include a processor, memory, and input/output peripherals on a single chip. Microprocessors, on the other hand, are more powerful processing units used in complex computing tasks, often requiring external memory and peripherals. FPGAs (Field Programmable Gate Arrays) are highly flexible devices that can be configured by the user to perform specific logic functions, making them invaluable in applications requiring customization and adaptability.

Applications of Embedded - Microcontroller,

Details	
Product Status	Obsolete
Module/Board Type	FPGA Core
Core Processor	Kintex UltraScale KU40
Co-Processor	-
Speed	-
Flash Size	32MB
RAM Size	4GB
Connector Type	Samtec LSHM
Size / Dimension	1.97" x 1.57" (50mm x 40mm)
Operating Temperature	0°C ~ 70°C
Purchase URL	https://www.e-xfl.com/product-detail/trenz-electronic/te0841-01-040-1c

1 Table of Contents

2.2 Block Diagram

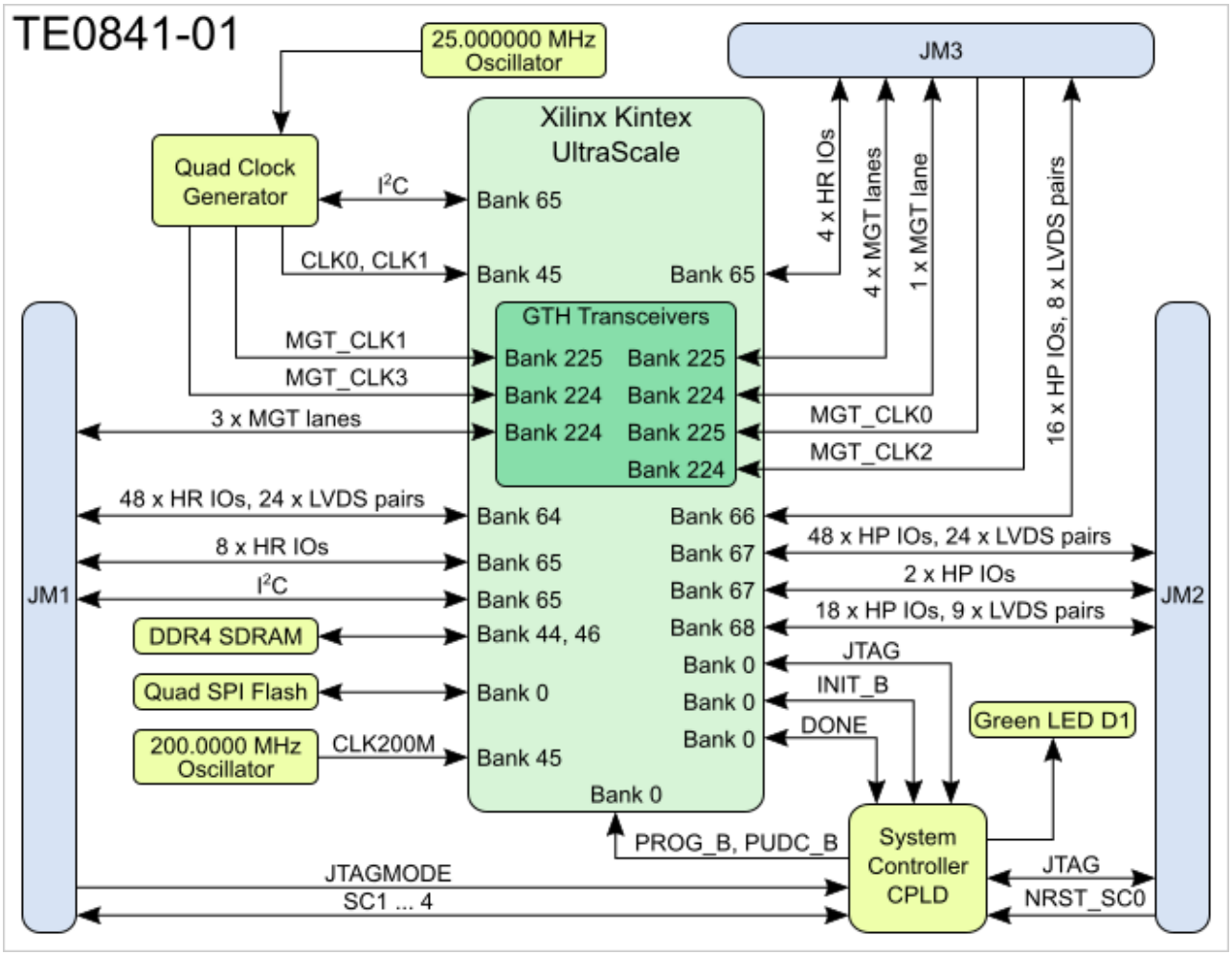

Figure 1: TE0841-01 block diagram.

2.3 Main Components

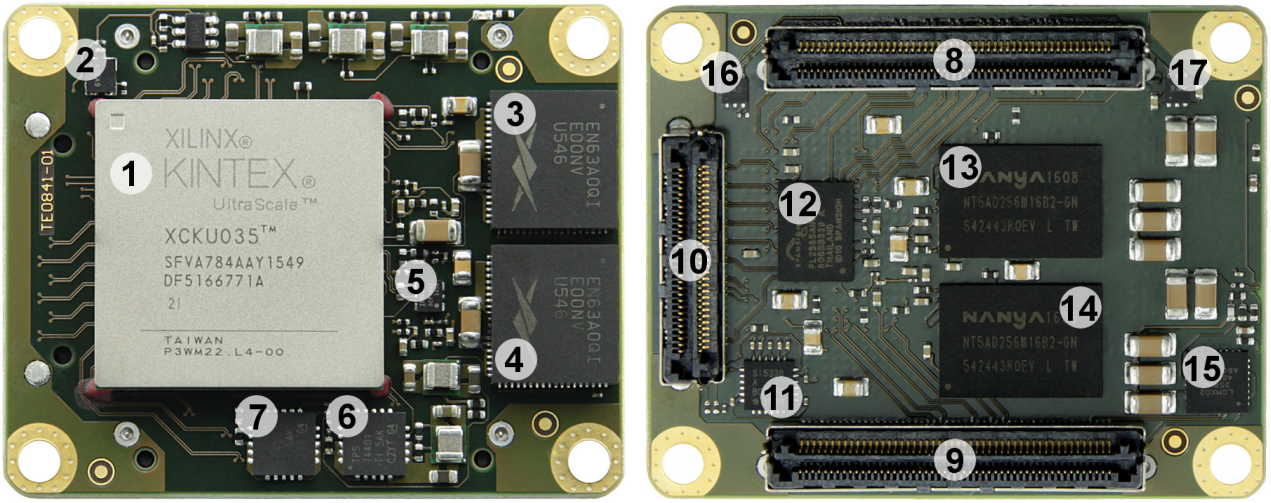

Figure 2: TE0841-01 main components.

1. Xilinx Kintex UltraScale FPGA, U1
2. Ultra performance oscillator @25.000000 MHz, U3
3. 12A PowerSoC DC-DC converter (0.95V), U14
4. 12A PowerSoC DC-DC converter (0.95V), U7
5. Low-jitter precision LVDS oscillator @200.0000 MHz, U11
6. Low-dropout (LDO) linear regulator (MGTAVTT 1.20V), U8
7. Low-dropout (LDO) linear regulator (MGTAVCC 1.02V), U12
8. Samtec Razor Beam™ LSHM-150 B2B connector, JM1
9. Samtec Razor Beam™ LSHM-150 B2B connector, JM2
10. Samtec Razor Beam™ LSHM-130 B2B connector, JM3
11. Programmable quad clock generator, U2
12. 32 MByte QSPI Flash, U6
13. 4 Gbit DDR4 SDRAM, U4
14. 4 Gbit DDR4 SDRAM, U5
15. System Controller CPLD, U18
16. Low-dropout (LDO) linear regulator (MGTAUX), U9
17. Ultra-low power low-dropout (LDO) regulator (VBATT), U19

2.4 Initial Delivery State

Storage device name	Content	Notes
System Controller CPLD	Default firmware	-
Quad SPI Flash OTP area	Empty	Not programmed
Quad clock generator OTP area	Empty	Not programmed

Table 1: TE0841-01 module initial delivery state of programmable on-board devices.

3 Boot Process

By default the configuration mode pins of the FPGA are set to QSPI mode, hence the FPGA is configured from serial NOR flash at system start-up. The JTAG interface of the module is provided for storing the initial FPGA configuration data to the QSPI flash memory.

4 Signals, Interfaces and Pins

4.1 Board to Board (B2B) I/Os

Table below lists bank number, bank type, B2B connection, I/O signal/LVDS pair count and power source for each FPGA PL I/O bank connected to the B2B connectors:

FPGA Bank	Type	B2B Connector	I/O Signal Count	Voltage	Notes
64	HR	JM1	48 IOs, 24 LVDS pairs	B64_VCCO	Supplied by the carrier board
65	HR	JM1	8 IOs	3.3V	On-module power supply
65	HR	JM3	4 IOs, 2 LVDS pairs	3.3V	On-module power supply
66	HP	JM3	16 IOs, 8 LVDS pairs	B66_VCCO	Supplied by the carrier board
67	HP	JM2	48 IOs, 24 LVDS pairs	B67_VCCO	Supplied by the carrier board
67	HP	JM2	2 IOs	B67_VCCO	Supplied by the carrier board
68	HP	JM2	18 IOs, 9 LVDS pairs	B68_VCCO	Supplied by the carrier board

Table 2: General overview of FPGA's PL I/O signals connected to the B2B connectors.

For detailed information about the pin out, please refer to the Pin-out Tables.

4.2 MGT Lanes

MGT (Multi Gigabit Transceiver) lane consists of one transmit and one receive (TX/RX) differential pairs, two signals each or four signals total per one MGT lane. Following table lists lane number, MGT bank number, transceiver type, signal schematic name, board-to-board pin connection and FPGA pin connection information:

Lane	Bank	Type	Signal Name	B2B Pin	FPGA Pin
0	225	GTH	• MGT_RX0_P • MGT_RX0_N • MGT_TX0_P • MGT_TX0_N	• JM3-8 • JM3-10 • JM3-7 • JM3-9	• MGTHRXP0_225, Y2 • MGTHRXN0_225, Y1 • MGTHTXP0_225, AA4 • MGTHTXN0_225, AA3
1	225	GTH	• MGT_RX1_P • MGT_RX1_N • MGT_TX1_P • MGT_TX1_N	• JM3-14 • JM3-16 • JM3-13 • JM3-15	• MGTHRXP1_225, V2 • MGTHRXN1_225, V1 • MGTHTXP1_225, W4 • MGTHTXN1_225, W3
2	225	GTH	• MGT_RX2_P • MGT_RX2_N • MGT_TX2_P • MGT_TX2_N	• JM3-20 • JM3-22 • JM3-19 • JM3-21	• MGTHRXP2_225, T2 • MGTHRXN2_225, T1 • MGTHTXP2_225, U4 • MGTHTXN2_225, U3
3	225	GTH	• MGT_RX3_P • MGT_RX3_N • MGT_TX3_P • MGT_TX3_N	• JM3-26 • JM3-28 • JM3-25 • JM3-27	• MGTHRXP3_225, P2 • MGTHRXN3_225, P1 • MGTHTXP3_225, R4 • MGTHTXN3_225, R3
4	224	GTH	• MGT_RX4_P • MGT_RX4_N • MGT_TX4_P • MGT_TX4_N	• JM1-12 • JM1-10 • JM1-6 • JM1-4	• MGTHRXP0_224, AH2 • MGTHRXN0_224, AH1 • MGTHTXP0_224, AG4 • MGTHTXN0_224, AG3

Lane	Bank	Type	Signal Name	B2B Pin	FPGA Pin
5	224	GTH	• MGT_RX5_P • MGT_RX5_N • MGT_TX5_P • MGT_TX5_N	• JM1-24 • JM1-22 • JM1-18 • JM1-16	• MGTHRXP1_224, AF2 • MGTHRXN1_224, AF1 • MGTHTXP1_224, AF6 • MGTHTXN1_224, AF5
6	224	GTH	• MGT_RX6_P • MGT_RX6_N • MGT_TX6_P • MGT_TX6_N	• JM1-27 • JM1-25 • JM1-19 • JM1-17	• MGTHRXP2_224, AD2 • MGTHRXN2_224, AD1 • MGTHTXP2_224, AE4 • MGTHTXN2_224, AE3
7	224	GTH	• MGT_RX7_P • MGT_RX7_N • MGT_TX7_P • MGT_TX7_N	• JM3-2 • JM3-4 • JM3-1 • JM3-3	• MGTHRXP3_224, AB2 • MGTHRXN3_224, AB1 • MGTHTXP3_224, AC4 • MGTHTXN3_224, AC3

Table 3: FPGA to B2B connectors routed MGT lanes overview.

Below are listed MGT banks reference clock sources.

Clock signal	Bank	Source	FPGA Pin	Notes
MGT_CLK0_P	225	B2B, JM3-33	MGTREFCLK0P_225, Y6	Supplied by the carrier board.
MGT_CLK0_N		B2B, JM3-31	MGTREFCLK0N_225, Y5	
MGT_CLK1_P	225	U2, CLK1B	MGTREFCLK1P_225, V6	On-board Si5338A.
MGT_CLK1_N		U2, CLK1A	MGTREFCLK1N_225, V5	
MGT_CLK2_P	224	B2B, JM3-34	MGTREFCLK2P_224, AD6	Supplied by the carrier board.
MGT_CLK2_N		B2B, JM3-32	MGTREFCLK2N_224, AD5	
MGT_CLK3_P	224	U2, CLK2B	MGTREFCLK3P_224, AB6	On-board Si5338A.
MGT_CLK3_N		U2, CLK2B	MGTREFCLK3N_224, AB5	

Table 4: MGT banks reference clock sources.

4.3 JTAG Interface

JTAG access to the Xilinx Kintex UltraScale FPGA is available through B2B connector JM2.

JTAG Signal	B2B Connector Pin
TMS	JM2-93
TDI	JM2-95
TDO	JM2-97
TCK	JM2-99

Table 5: JTAG interface signals.

⚠ JTAGMODE pin 89 in B2B connector JM1 should be set low or grounded for normal operation. Set this pin high for SC CPLD update via JTAG interface.

4.4 System Controller CPLD I/O Pins

Special purpose pins are connected to the System Controller CPLD and have following default configuration:

Pin Name	Mode	Function	Default Configuration
JTAGMODE	Input	JTAG select	Low for normal operation.
NRST_SC0	Input	Reset	-
SC1	-	-	Not used by default.
SC2	-	-	Not used by default.
SC3	-	-	Not used by default.
SC4	-	-	Not used by default.

Table 6: System Controller CPLD I/O pins.

4.5 Quad SPI Interface

Quad SPI interface is connected to the FPGA configuration bank 0.

Signal Name	QSPI Flash Memory U6 Pin	FPGA Pin
SPI_CS	C2	RDWR_FCS_B_0, AH7
SPI_D0	D3	D00_MOSI_0, AA7
SPI_D1	D2	D01_DIN_0, Y7
SPI_D2	C4	D02_0, U7
SPI_D3	D4	D03_0, V7
SPI_CLK	B2	CCLK_0, V11

Table 7: Quad SPI interface signals and connections.

4.6 I2C Interface

There are two PL bank 65 I/O pins (PLL_SCL and PLL_SDA) reserved as I^2C bus connected to the Si5338 PLL quad clock generator. Default Si5338 PLL chip I^2C bus slave address is 0x70.

Additionally, two PL bank 65 I/O pins (B65_SCL and B65_SDA) connected to the B2B connector JM1 can be used for external I^2C connectivity, otherwise these pins are ordinary I/Os.

5 On-board Peripherals

5.1 System Controller CPLD

The System Controller CPLD (U18) is provided by Lattice Semiconductor LCMXO2-256HC (MachXO2 Product Family). The SC-CPLD is the central system management unit where essential control signals are logically linked by the implemented logic in CPLD firmware, which generates output signals to control the system, the on-board peripherals and the interfaces. Interfaces like JTAG and I^2C between the on-board peripherals and to the FPGA module are by-passed, forwarded and controlled by the System Controller CPLD.

Other tasks of the System Controller CPLD are the monitoring of the power-on sequence and to display the programming state of the FPGA module.

For detailed information, refer to the reference page of the SC CPLD firmware of this module.

5.2 DDR Memory

By default TE0841 module has two NT5AD256M16 DDR4 SDRAM chips arranged into 32-bit wide memory bus providing total of 1 GBytes of on-board RAM. Different memory sizes are available optionally.

5.3 Quad SPI Flash Memory

On-board QSPI flash memory (U6) on the TE0841-01 is provided by Micron Serial NOR Flash Memory N25Q256A with 256-Mbit (32-MByte) storage capacity. This non volatile memory is used to store initial FPGA configuration. Besides FPGA configuration, remaining free flash memory can be used for user application and data storage. All four SPI data lines are connected to the FPGA allowing x1, x2 or x4 data bus widths. Maximum data rate depends on the selected bus width and clock frequency used.

5.4 Programmable Clock Genetraor

There is a Silicon Labs I^2C programmable quad PLL clock generator on-board (Si5338A, U2) to generate several reference clocks for the module.

Si5338A Pin	Signal Name / Description	Connected To	Direction	Note
IN1	-	not connected	Input	not used
IN2	-	GND	Input	not used
IN3	Reference input clock	U3, pin 3	Input	25.000000 MHz oscillator, Si8208AI
IN4	-	GND	Input	I^2C slave device address LSB.
IN5	-	not connected	Input	not used
IN6	-	GND	Input	not used
CLK0A	CLK1_P	U1, R23	Output	FPGA bank 45
CLK0B	CLK1_N	U1, P23		
CLK1A	MGT_CLK1_N	U1, V5	Output	FPGA MGT bank 225 reference clock
CLK1B	MGT_CLK1_P	U1, V6		

Si5338A Pin	Signal Name / Description	Connected To	Direction	Note
CLK2A	MGT_CLK3_N	U1, AB5	Output	FPGA MGT bank 224 reference clock
CLK2B	MGT_CLK3_P	U1, AB6		
CLK3A	CLK0_P	U1, pin T24	Output	FPGA bank 45
CLK3B	CLK0_N	U1, pin T25		

Table 8: Programmable quad PLL clock generator inputs and outputs.

5.5 Oscillators

The FPGA module has following reference clocking signals provided by external baseboard sources and on-board oscillators:

Clock Source	Frequency	Signal Name	Clock Destination
U3, SiT8208AI	25.000000 MHz	CLK	U2, pin 3 (IN3)
U11, DSC1123DL5	200.0000 MHz	CLK200M_P	U1, pin R25
		CLK200M_N	U1, pin R26
B2B, JM3-31	User	MGT_CLK0_N	U1, pin Y5
B2B, JM3-33		MGT_CLK0_P	U1, pin Y6
B2B, JM3-32	User	MGT_CLK2_N	U1, pin AD5
B2B, JM3-34		MGT_CLK2_P	U1, pin AD6

Table 9: Reference clock signals.

5.6 On-board LEDs

LED	Color	Connected to	Description and Notes
D1	Green	System Controller CPLD, bank 3	Exact function is defined by SC CPLD firmware.

Table 10: On-board LEDs.

6 Power and Power-On Sequence

6.1 Power Consumption

The maximum power consumption of a module mainly depends on the design running on the FPGA.

Xilinx provide a power estimator excel sheets to calculate power consumption. It's also possible to evaluate the power consumption of the developed design with Vivado. See also Trenz Electronic Wiki FAQ.

Power Input	Typical Current
VIN	TBD*
3.3VIN	TBD*

Table 11: Typical power consumption.

* TBD - To Be Determined.

Single 3.3V power supply with minimum current capability of 4A for system startup is recommended.

For the lowest power consumption and highest efficiency of the on-board DC-DC regulators it is recommended to power the module from one single 3.3V supply. All input power supplies should have a nominal value of 3.3V. Although the input power supplies can be powered up in any order, it is recommended to power them up simultaneously.

To avoid any damage to the module, check for stabilized on-board voltages should be carried out (i.e. power good and enable signals) before powering up any SoC's I/O bank voltages (B64_VCO, B65_VCO, B66_VCO and B67_VCO). All I/Os should be tri-stated during power-on sequence.

6.2 Power-On Sequence

For the highest efficiency of the on-board DC-DC regulators, it is recommended to use one 3.3V power source for both VIN and 3.3VIN power rails. Although VIN and 3.3VIN can be powered up in any order, it is recommended to power them up simultaneously. It is important that all I/Os of the carrier board are 3-stated at the beginning of the power-on cycle until 3.3V is present on B2B connector JM2 pins 10 and 12, indicating that all on-module PL supply voltages have become stable and Zynq MPSoC module is powered up properly.

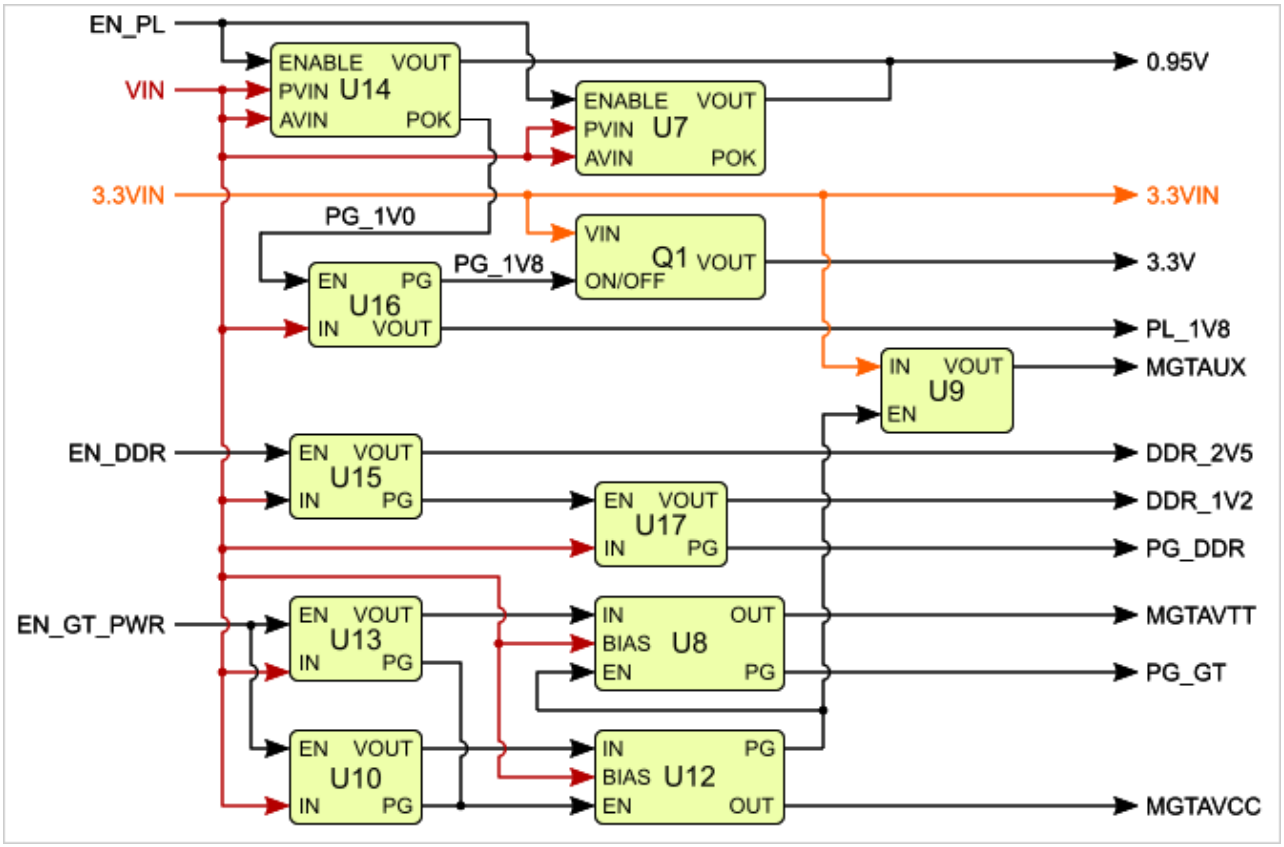

Figure 3: TE0841-01 Power-on sequence.

See also Xilinx datasheet DS892 for additional information. User should also check related baseboard documentation when choosing baseboard design for TE0841 module.

6.3 Power Rails

Power Rail Name	B2B JM1 Pins	B2B JM2 Pins	Input/Output	Notes
VIN	1, 3, 5	2, 4, 6, 8	Input	Supply voltage.
3.3VIN	13, 15	-	Input	Supply voltage.
B64_VCO	9, 11	-	Input	HR (High Range) bank voltage.
B66_VCO	-	1, 3	Input	HP (High Performance) bank voltage.
B67_VCO	-	7, 9	Input	HP (High Performance) bank voltage.
B68_VCO	-	5	Input	HP (High Performance) bank voltage.
VBAT_IN	79	-	Input	RTC battery supply voltage.
3.3V	-	10, 12, 91	Output	Module on-board 3.3V voltage level.

Table 12: Module power rails.

6.4 Bank Voltages

Bank	Schematic Name	Voltage	Voltage Range
0 (config)	PL_1.8V	1.8V	-
44 HP	DDR_1V2	1.2V	HP: 1.2V to 1.8V
45 HP	PL_1.8V	1.8V	HP: 1.2V to 1.8V
46 HP	DDR_1V2	1.2V	HP: 1.2V to 1.8V
64 HR	B64_VCO	user	HR: 1.2V to 3.3V
65 HR	3.3V	3.3V	HR: 1.2V to 3.3V
66 HP	B66_VCO	user	HP: 1.2V to 1.8V
67 HP	B67_VCO	user	HP: 1.2V to 1.8V
68 HP	B68_VCO	user	HP: 1.2V to 1.8V

Table 13: Module's bank voltages.

7 Board to Board Connectors

These connectors are hermaphroditic. Odd pin numbers on the module are connected to even pin numbers on the baseboard and vice versa.

4 x 5 modules use two or three Samtec Razor Beam LSHM connectors on the bottom side.

- 2 x REF-189016-02 (compatible to LSHM-150-04.0-L-DV-A-S-K-TR), (100 pins, "50" per row)
- 1 x REF-189017-02 (compatible to LSHM-130-04.0-L-DV-A-S-K-TR), (60 pins, "30" per row) (depending on module)

7.1 Connector Mating height

When using the same type on baseboard, the mating height is 8mm. Other mating heights are possible by using connectors with a different height

Order number	Connector on baseboard	compatible to	Mating height
23836	REF-189016-01	LSHM-150-02.5-L-DV-A-S-K-TR	6.5 mm
	LSHM-150-03.0-L-DV-A-S-K-TR	LSHM-150-03.0-L-DV-A-S-K-TR	7.0 mm
23838	REF-189016-02	LSHM-150-04.0-L-DV-A-S-K-TR	8.0 mm
	LSHM-150-06.0-L-DV-A-S-K-TR	LSHM-150-06.0-L-DV-A-S-K-TR	10.0mm
26125	REF-189017-01	LSHM-130-02.5-L-DV-A-S-K-TR	6.5 mm
	LSHM-130-03.0-L-DV-A-S-K-TR	LSHM-130-03.0-L-DV-A-S-K-TR	7.0 mm
24903	REF-189017-02	LSHM-130-04.0-L-DV-A-S-K-TR	8.0 mm
	LSHM-130-06.0-L-DV-A-S-K-TR	LSHM-130-06.0-L-DV-A-S-K-TR	10.0mm

The module can be manufactured using other connectors upon request.

7.2 Connector Speed Ratings

The LSHM connector speed rating depends on the stacking height; please see the following table:

Stacking height	Speed rating
12 mm, Single-Ended	7.5 GHz / 15 Gbps
12 mm, Differential	6.5 GHz / 13 Gbps
5 mm, Single-Ended	11.5 GHz / 23 Gbps
5 mm, Differential	7.0 GHz / 14 Gbps

7.3 Current Rating

Current rating of Samtec Razor Beam™ LSHM B2B connectors is 2.0A per pin (2 adjacent pins powered).

7.4 Connector Mechanical Ratings

- Shock: 100G, 6 ms Sine
- Vibration: 7.5G random, 2 hours per axis, 3 axes total

8 Variants Currently In Production

Module Variant	FPGA Chip	Temperature Range
TE0841-01-035-1C	XCKU035-1SFVA784C	Commercial
TE0841-01-035-1I	XCKU035-1SFVA784I	Industrial
TE0841-01-035-2I	XCKU035-2SFVA784I	Industrial
TE0841-01-040-1C	XCKU040-1SFVA784C	Commercial
TE0841-01-040-1I	XCKU040-1SFVA784I	Industrial

Table 14: Module variants in production.

9 Technical Specifications

9.1 Absolute Maximum Ratings

Parameter	Min	Max	Units	Reference Document
VIN supply voltage	-0.3	6.0	V	EN63A0QI, TPS74401RGW datasheets.
3.3VIN supply voltage	-0.1	3.75	V	TPS27082, LCMXO2-256HC datasheets.
Supply voltage for HR I/O banks (VCCO)	-0.500	3.400	V	Xilinx datasheet DS892.
Supply voltage for HP I/O banks (VCCO)	-0.500	2.000	V	Xilinx datasheet DS892.
I/O input voltage for HR I/O banks	-0.400	VCCO + 0.550	V	Xilinx datasheet DS892.
I/O input voltage for HP I/O banks	-0.550	VCCO + 0.550	V	Xilinx datasheet DS892.
GTH and GTY transceiver reference clocks absolute input voltage (MGT_CLK0, MGT_CLK2)	-0.500	1.320	V	Xilinx datasheet DS892.
GTH and GTY transceiver receiver (RXP/RXN) and transmitter (TXP/TXN) absolute input voltage	-0.500	1.260	V	Xilinx datasheet DS892.
Storage temperature	-40	+85	°C	-

Table 15: Module absolute maximum ratings.

⚠ Assembly variants for higher storage temperature range are available on request.

9.2 Recommended Operating Conditions

Parameter	Min	Max	Units	Reference Document
VIN supply voltage	3.3	5.5	V	TPS82085SIL, TPS74401RGW datasheet
3.3VIN supply voltage	2.375	3.6	V	LCMXO2-256HC datasheet
Supply voltage for HR I/O banks (VCCO)	1.140	3.400	V	Xilinx datasheet DS892
Supply voltage for HP I/O banks (VCCO)	0.950	1.890	V	Xilinx datasheet DS892
I/O input voltage	–0.200	VCCO + 0.20	V	Xilinx datasheet DS892

Table 16: Module recommended operating conditions.

> ⚠ Please check also Xilinx datasheet DS892 for complete list of absolute maximum and recommended operating ratings.

9.3 Operating Temperature Ranges

Commercial grade: 0°C to +70°C.

Industrial grade: -40°C to +85°C.

Extended grade: 0°C to +85°C.

Operating temperature range depends also on customer design and cooling solution. Please contact us for options.

9.4 Physical Dimensions

- Module size: 50 mm × 40 mm. Please download the assembly diagram for exact numbers.
- Mating height with standard connectors: 8 mm.
- PCB thickness: 1.6 mm.
- Highest part on PCB: approximately 3 mm. Please download the step model for exact numbers.

All dimensions are given in millimeters.

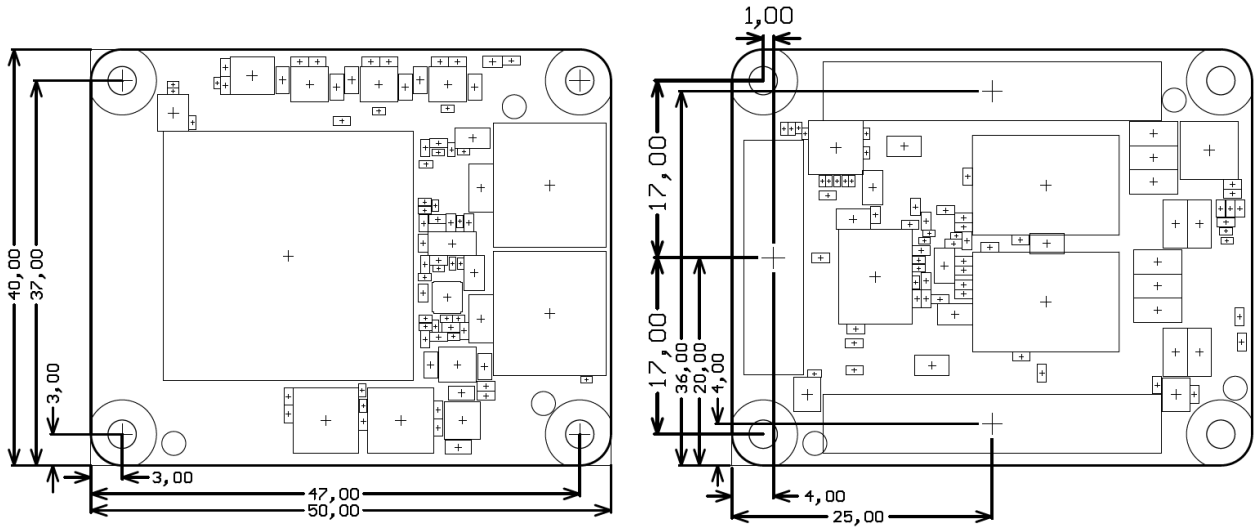

Figure 4: Module physical dimensions.

10 Revision History

10.1 Hardware Revision History

Date	Revision	Notes	PCN	Documentation Link
2015-12-09	01	First production revision	-	TE0841-01

Table 17: Hardware revision history.

Hardware revision number is printed on the PCB board together with the module model number separated by the dash.

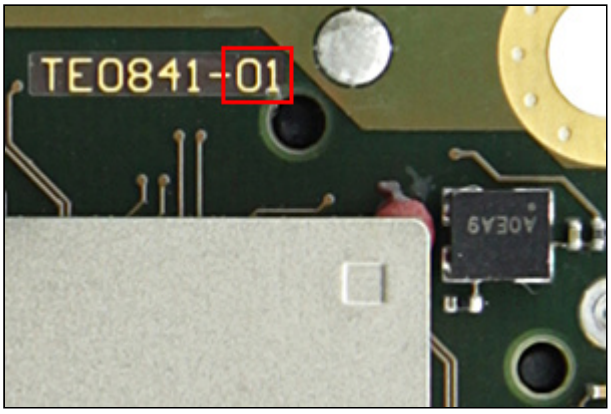

Figure 5: Module hardware revision number.

10.2 Document Change History

Date	Revision	Contributors	Description
2018-07-10	59	John Hartfiel	• update links
13.03.2018	v.57	Jan Kumann, Ali Naseri	Initial document.

Table 18: Document change history.

11 Disclaimer

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Please also note our data protection declaration at https://www.trenz-electronic.de/en/Data-protection-Privacy

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11.7 REACH, RoHS and WEEE

REACH

Trenz Electronic is a manufacturer and a distributor of electronic products. It is therefore a so called downstream user in the sense of REACH. The products we supply to you are solely non-chemical products (goods). Moreover and under normal and reasonably foreseeable circumstances of application, the goods supplied to you shall not release

any substance. For that, Trenz Electronic is obliged to neither register nor to provide safety data sheet. According to present knowledge and to best of our knowledge, no SVHC (Substances of Very High Concern) on the Candidate List are contained in our products. Furthermore, we will immediately and unsolicited inform our customers in compliance with REACH - Article 33 if any substance present in our goods (above a concentration of 0,1 % weight by weight) will be classified as SVHC by the European Chemicals Agency (ECHA).

RoHS

Trenz Electronic GmbH herewith declares that all its products are developed, manufactured and distributed RoHS compliant.

WEEE

Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.