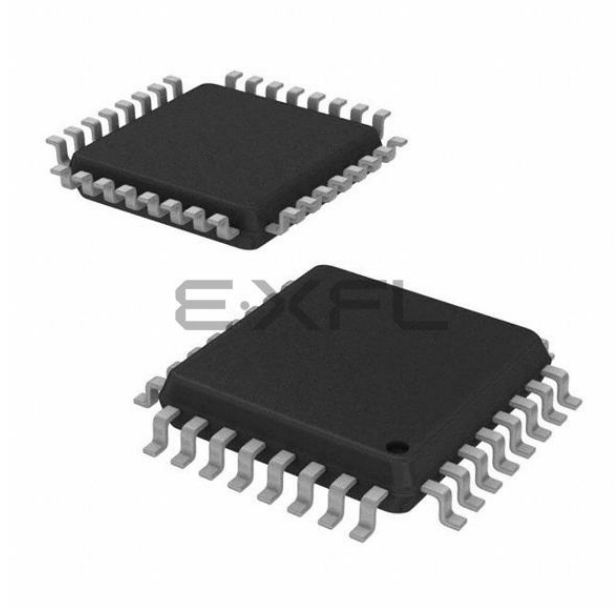

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-8FX
Core Size	8-Bit
Speed	16MHz
Connectivity	I²C, SIO, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	29
Program Memory Size	20KB (20K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	496 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	A/D 17x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb95f434kpmc-g-sne2

(Continued)

Part number / Parameter	MB95F432H	MB95F433H	MB95F434H	MB95F432K	MB95F433K	MB95F434K
I^2C	1 channel					
	• Master/slave transmission and receiving • It has a bus error function, an arbitration function, a transmission direction detection function and a wake-up function. • It also has functions of generating and detecting repeated START conditions.					
16-bit PPG	• PWM mode and single-shot mode are available to use. • Ch. 0 can work with the multi-functional timer or individually.					
Output compare	• 1 channel of 16-bit free-running timer with a compare buffer • 2 channels of 16-bit output compare					
Voltage comparator	4 channels					
OPAMP	• This is an operational amplifier used in an induction heater. It contains 7 software (registers) select close loop gain selections for ground current sensing according to different sense resistor values. The OPAMP can also work as a standalone OPAMP. • It selects closed loop gain for ground current sensing according to different sense resistor values of a standalone OPAMP.					
Watch prescaler	Eight different time intervals can be selected.					
Flash memory	• It supports automatic programming, Embedded Algorithm, and write/erase/erase-suspend/erase-resume commands. • It has a flag indicating the completion of the operation of Embedded Algorithm. • Number of write/erase cycles: 100000 • Data retention time: 20 years • Flash security feature for protecting the content of the Flash memory					
Standby mode	Sleep mode, stop mode, watch mode, time-base timer mode					
Package	FPT-32P-M30 DIP-32P-M06					

(Continued)

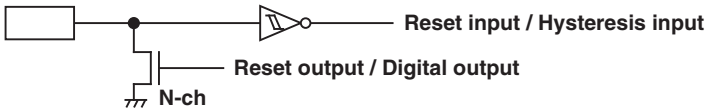
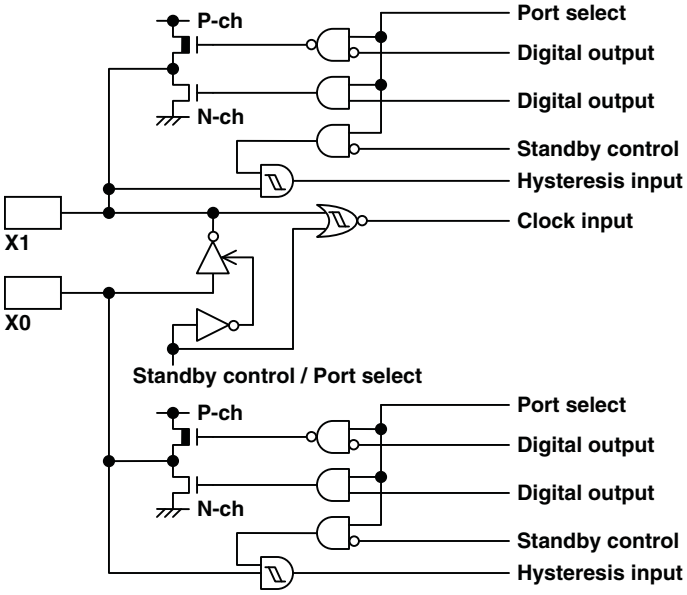
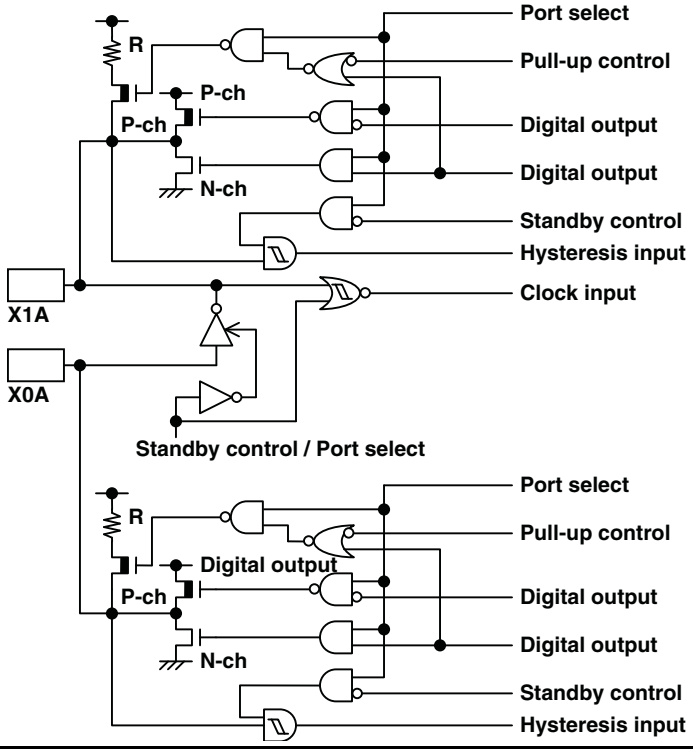
Pin no.		Pin name	I/O circuit type*3	Function
LQFP32*1	SH-DIP32*2			
21	25	P74	I	General-purpose I/O port
		CMP1_P		Comparator ch. 1 positive input pin
		AN10		A/D converter analog input pin
22	26	P75	I	General-purpose I/O port
		CMP1_N		Comparator ch. 1 negative input pin
		AN11		A/D converter analog input pin
23	27	P76	D	General-purpose I/O port
		CMP2_O		Comparator ch. 2 output pin
		UCK		UART/SIO clock I/O pin
24	28	P63	I	General-purpose I/O port
		CMP2_P		Comparator ch. 2 positive input pin
		AN12		A/D converter analog input pin
25	29	P64	I	General-purpose I/O port
		CMP2_N		Comparator ch. 2 negative input pin
		AN13		A/D converter analog input pin
26	30	P65	L	General-purpose I/O port
		CMP3_O		Comparator ch. 3 output pin
		UO		UART/SIO data output pin
		SDA		I^2C data I/O pin
27	31	P66	I	General-purpose I/O port
		CMP3_P		Comparator ch. 3 positive input pin
		AN14		A/D converter analog input pin
28	32	P67	I	General-purpose I/O port
		CMP3_N		Comparator ch. 3 negative input pin
		AN15		A/D converter analog input pin
29	1	PF2	A	General-purpose I/O port
		$\overline{RST}$		Reset pin Dedicated reset pin in MB95F432H/F433H/F434H
30	2	PF0	B	General-purpose I/O port
		X0		Main clock I/O oscillation pin
31	3	PF1	B	General-purpose I/O port
		X1		Main clock I/O oscillation pin
32	4	V_{SS}	—	Power supply pin (GND)

*1: Package code: FPT-32P-M30

*2: Package code: DIP-32P-M06

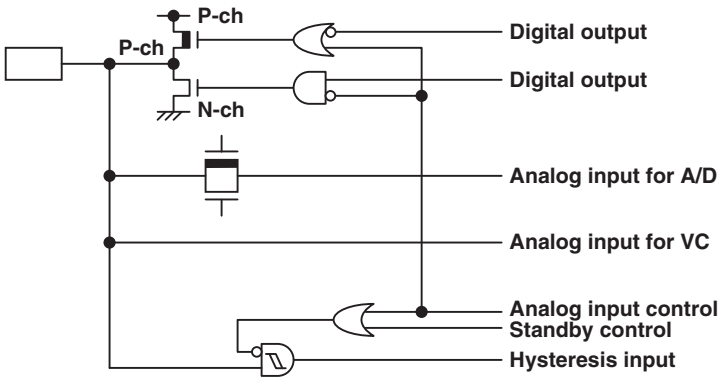
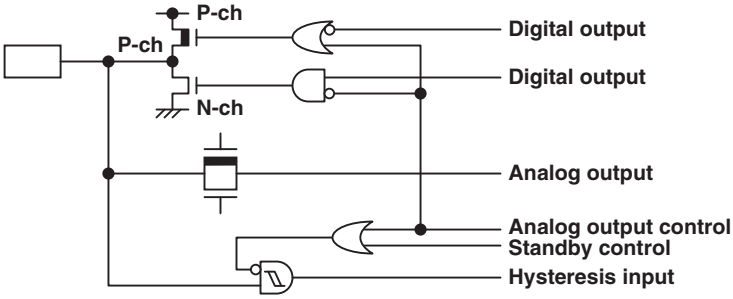
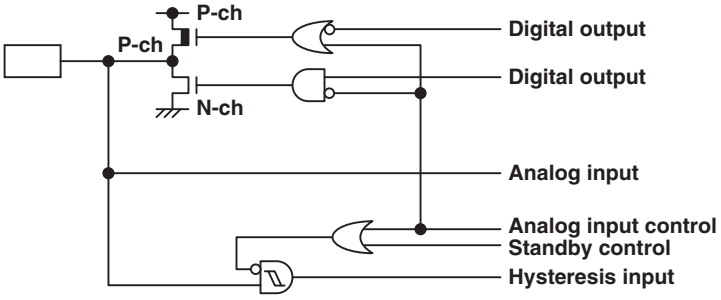
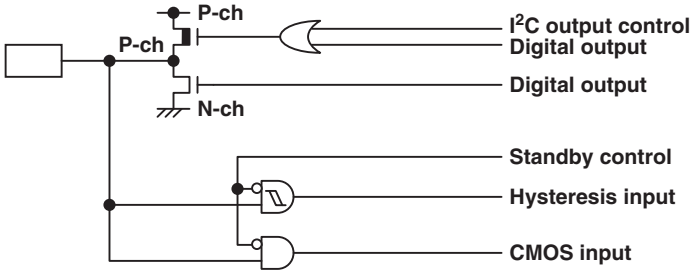
*3: For the I/O circuit types, see "■ I/O CIRCUIT TYPE".

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• N-ch open drain output • Hysteresis input • Reset output
B		• Oscillation circuit • High-speed side Feedback resistance: approx. 1 MΩ • CMOS output • Hysteresis input
C		• Oscillation circuit • Low-speed side Feedback resistance: approx.10 MΩ • CMOS output • Hysteresis input • Pull-up control available

(Continued)

(Continued)

Type	Circuit	Remarks
I		• CMOS output • Hysteresis input
J		• CMOS output • Hysteresis input
K		• CMOS output • Hysteresis input
L		• CMOS output • Hysteresis input • CMOS input • N-ch open drain output (as I²C output)

■ NOTES ON DEVICE HANDLING

• Preventing latch-ups

When using the device, ensure that the voltage applied does not exceed the maximum voltage rating.
In a CMOS IC, if a voltage higher than V_{CC} or a voltage lower than V_{SS} is applied to an input/output pin that is neither a medium-withstand voltage pin nor a high-withstand voltage pin, or if a voltage out of the rating range of power supply voltage mentioned in "1. Absolute Maximum Ratings" of "■ ELECTRICAL CHARACTERISTICS" is applied to the V_{CC} pin or the V_{SS} pin, a latch-up may occur.
When a latch-up occurs, power supply current increases significantly, which may cause a component to be thermally destroyed.

• Stabilizing supply voltage

Supply voltage must be stabilized.
A malfunction may occur when power supply voltage fluctuates rapidly even though the fluctuation is within the guaranteed operating range of the V_{CC} power supply voltage.
As a rule of voltage stabilization, suppress voltage fluctuation so that the fluctuation in V_{CC} ripple (p-p value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the standard V_{CC} value, and the transient fluctuation rate does not exceed 0.1 V/ms at a momentary fluctuation such as switching the power supply.

• Notes on using the external clock

When an external clock is used, oscillation stabilization wait time is required for power-on reset, wake-up from subclock mode or stop mode.

■ PIN CONNECTION

• Treatment of unused pins

If an unused input pin is left unconnected, a component may be permanently damaged due to malfunctions or latch-ups. Always pull up or pull down an unused input pin through a resistor of at least 2 kΩ. Set an unused input/output pin to the output state and leave it unconnected, or set it to the input state and treat it the same as an unused input pin. If there is an unused output pin, leave it unconnected.

• Power supply pins

To reduce unnecessary electro-magnetic emission, prevent malfunctions of strobe signals due to an increase in the ground level, and conform to the total output current standard, always connect the V_{CC} pin and the V_{SS} pin to the power supply and ground outside the device. In addition, connect the current supply source to the V_{CC} pin and the V_{SS} pin with low impedance.
It is also advisable to connect a ceramic capacitor of approximately 0.1 µF as a bypass capacitor between the V_{CC} pin and the V_{SS} pin at a location close to this device.

• DBG pin

Connect the DBG pin directly to an external pull-up resistor.
To prevent the device from unintentionally entering the debug mode due to noise, minimize the distance between the DBG pin and the V_{CC} or V_{SS} pin when designing the layout of the printed circuit board.
The DBG pin should not stay at "L" level after power-on until the reset output is released.

• $\overline{RST}$ pin

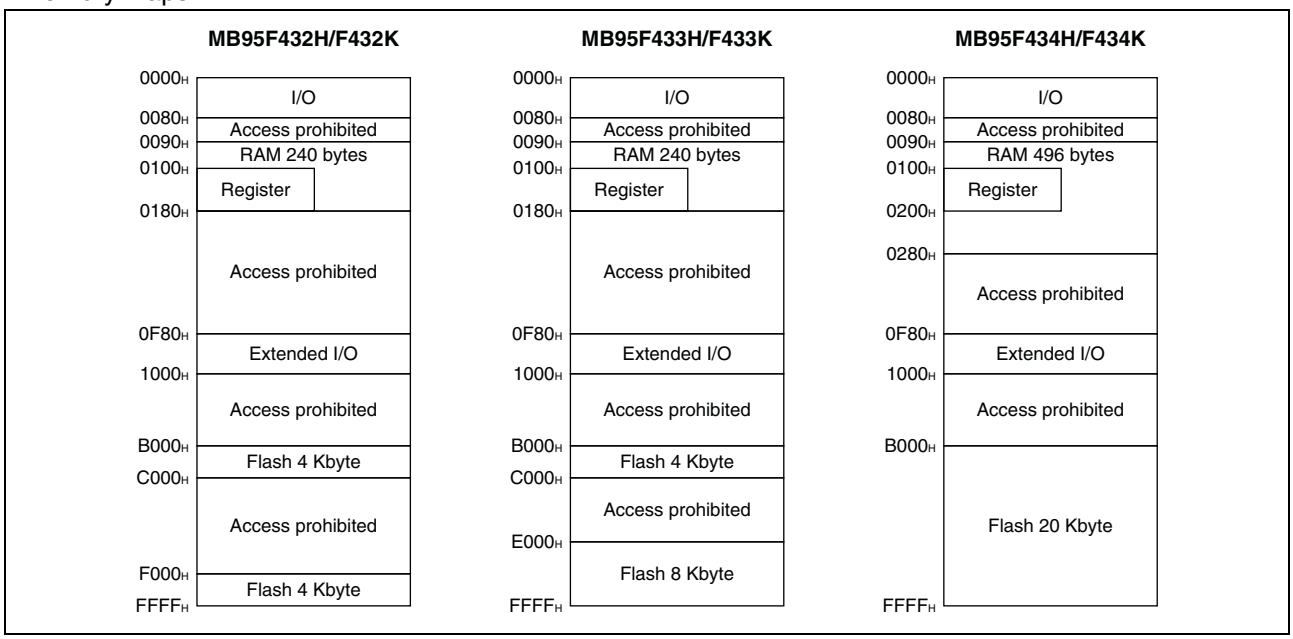
Connect the $\overline{RST}$ pin directly to an external pull-up resistor.
To prevent the device from unintentionally entering the reset mode due to noise, minimize the distance between the $\overline{RST}$ pin and the V_{CC} or V_{SS} pin when designing the layout of the printed circuit board.
The $\overline{RST}$/PF2 pin functions as the reset input/output pin after power-on. In addition, the reset output of the $\overline{RST}$/PF2 pin can be enabled by the RSTOE bit in the SYSC1 register, and the reset input function and the general purpose I/O function can be selected by the RSTEN bit in the SYSC1 register.

■ CPU CORE

• Memory Space

The memory space of the MB95430H Series is 64 Kbyte in size, and consists of an I/O area, a data area, and a program area. The memory space includes areas intended for specific purposes such as general-purpose registers and a vector table. The memory maps of the MB95430H Series are shown below.

• Memory Maps



Address	Register abbreviation	Register name	R/W	Initial value
0F80H	WRARH0	Wild register address setting register (upper) ch. 0	R/W	00000000B
0F81H	WRARL0	Wild register address setting register (lower) ch. 0	R/W	00000000B
0F82H	WRDR0	Wild register data setting register ch. 0	R/W	00000000B
0F83H	WRARH1	Wild register address setting register (upper) ch. 1	R/W	00000000B
0F84H	WRARL1	Wild register address setting register (lower) ch. 1	R/W	00000000B
0F85H	WRDR1	Wild register data setting register ch. 1	R/W	00000000B
0F86H	WRARH2	Wild register address setting register (upper) ch. 2	R/W	00000000B
0F87H	WRARL2	Wild register address setting register (lower) ch. 2	R/W	00000000B
0F88H	WRDR2	Wild register data setting register ch. 2	R/W	00000000B
0F89H	WRARH3	Wild register address setting register (upper) ch. 3	R/W	00000000B
0F8AH	WRARL3	Wild register address setting register (lower) ch. 3	R/W	00000000B
0F8BH	WRDR3	Wild register data setting register ch. 3	R/W	00000000B
0F8CH to 0F91H	—	(Disabled)	—	—
0F92H	T01CR0	8/16-bit composite timer 01 status control register 0 ch. 0	R/W	00000000B
0F93H	T00CR0	8/16-bit composite timer 00 status control register 0 ch. 0	R/W	00000000B
0F94H	T01DR	8/16-bit composite timer 01 data register ch. 0	R/W	00000000B
0F95H	T00DR	8/16-bit composite timer 00 data register ch. 0	R/W	00000000B
0F96H	TMCR0	8/16-bit composite timer 00/01 timer mode control register ch. 0	R/W	00000000B
0F97H to 0FA9H	—	(Disabled)	—	—
0FAAH	PDCRH0	16-bit PPG down counter register (upper) ch. 0	R/W	00000000B
0FABH	PDCRL0	16-bit PPG down counter register (lower) ch. 0	R/W	00000000B
0FACH	PCSRH0	16-bit PPG cycle setting buffer register (upper) ch. 0	R/W	11111111B
0FADH	PCSRL0	16-bit PPG cycle setting buffer register (lower) ch. 0	R/W	11111111B
0FAEH	PDUTH0	16-bit PPG duty setting buffer register (upper) ch. 0	R/W	11111111B
0FAFH	PDUTL0	16-bit PPG duty setting buffer register (lower) ch. 0	R/W	11111111B
0FB0H to 0FBDH	—	(Disabled)	—	—
0FBEH	PSSR0	UART/SIO prescaler select register ch. 0	R/W	00000000B
0FBFH	BRSR0	UART/SIO baud rate setting register ch. 0	R/W	00000000B
0FC0H, 0FC1H	—	(Disabled)	—	—
0FC2H	AIDRH	A/D input disable register (upper)	R/W	00000000B
0FC3H	AIDRL	A/D input disable register (lower)	R/W	00000000B
0FC4H to 0FE3H	—	(Disabled)	—	—

(Continued)

■ INTERRUPT SOURCE TABLE

Interrupt source	Interrupt request number	Vector table address		Bit name of interrupt level setting register	Priority order of interrupt sources of the same level (occurring simultaneously)
		Upper	Lower		
External interrupt ch. 0	IRQ00	FFFA$_H$	FFFB$_H$	L00 [1:0]	High ↑
External interrupt ch. 4					
External interrupt ch. 1	IRQ01	FFF8$_H$	FFF9$_H$	L01 [1:0]	
External interrupt ch. 5					
External interrupt ch. 2	IRQ02	FFF6$_H$	FFF7$_H$	L02 [1:0]	
External interrupt ch. 6					
External interrupt ch. 3	IRQ03	FFF4$_H$	FFF5$_H$	L03 [1:0]	
External interrupt ch. 7					
UART/SIO	IRQ04	FFF2$_H$	FFF3$_H$	L04 [1:0]	
8/16-bit composite timer ch. 0 (lower)	IRQ05	FFF0$_H$	FFF1$_H$	L05 [1:0]	
8/16-bit composite timer ch. 0 (upper)	IRQ06	FFEE$_H$	FFEF$_H$	L06 [1:0]	
Output compare ch. 0 match	IRQ07	FFEC$_H$	FFED$_H$	L07 [1:0]	
Output compare ch. 1 match	IRQ08	FFEA$_H$	FFEB$_H$	L08 [1:0]	
—	IRQ09	FFE8$_H$	FFE9$_H$	L09 [1:0]	
Voltage comparator ch. 0	IRQ10	FFE6$_H$	FFE7$_H$	L10 [1:0]	
Voltage comparator ch. 1	IRQ11	FFE4$_H$	FFE5$_H$	L11 [1:0]	
Voltage comparator ch. 2	IRQ12	FFE2$_H$	FFE3$_H$	L12 [1:0]	
Voltage comparator ch. 3	IRQ13	FFE0$_H$	FFE1$_H$	L13 [1:0]	
16-bit free-running timer (compare match/zero-detect/overflow)	IRQ14	FFDE$_H$	FFDF$_H$	L14 [1:0]	
16-bit PPG	IRQ15	FFDC$_H$	FFDD$_H$	L15 [1:0]	
I^{2}C	IRQ16	FFDA$_H$	FFDB$_H$	L16 [1:0]	
—	IRQ17	FFD8$_H$	FFD9$_H$	L17 [1:0]	
8/10-bit A/D converter	IRQ18	FFD6$_H$	FFD7$_H$	L18 [1:0]	
Time-base timer	IRQ19	FFD4$_H$	FFD5$_H$	L19 [1:0]	
Watch prescaler	IRQ20	FFD2$_H$	FFD3$_H$	L20 [1:0]	
—	IRQ21	FFD0$_H$	FFD1$_H$	L21 [1:0]	
—	IRQ22	FFCE$_H$	FFCF$_H$	L22 [1:0]	
Flash memory	IRQ23	FFCC$_H$	FFCD$_H$	L23 [1:0]	Low

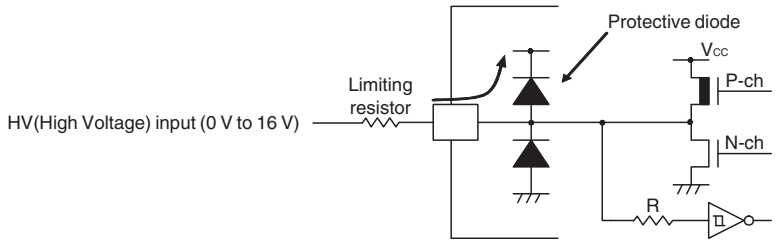
(Continued)

*1: The parameter is based on V_{SS} = 0.0 V.

*2: V_I and V_O must not exceed V_{CC} + 0.3 V. V_I must not exceed the rated voltage. However, if the maximum current to/from an input is limited by means of an external component, the I_{CLAMP} rating is used instead of the V_I rating.

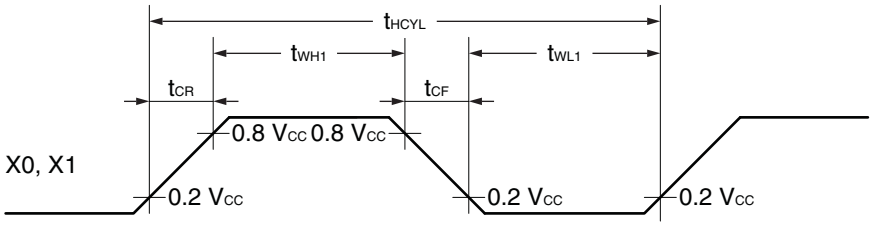
*3: Applicable to the following pins: P00 to P07, P60 to P67, P70 to P76, PF0 and PF1

- Use under recommended operating conditions.
- Use with DC voltage (current).
- The HV (High Voltage) signal is an input signal exceeding the V_{CC} voltage. Always connect a limiting resistor between the HV (High Voltage) signal and the microcontroller before applying the HV (High Voltage) signal.
- The value of the limiting resistor should be set to a value at which the current to be input to the microcontroller pin when the HV (High Voltage) signal is input is below the standard value, irrespective of whether the current is transient current or stationary current.
- When the microcontroller drive current is low, such as in low power consumption modes, the HV (High Voltage) input potential may pass through the protective diode to increase the potential of the V_{CC} pin, affecting other devices.
- If the HV (High Voltage) signal is input when the microcontroller power supply is off (not fixed at 0 V), since power is supplied from the pins, incomplete operations may be executed.
- If the HV (High Voltage) input is input after power-on, since power is supplied from the pins, the voltage of power supply may not be sufficient to enable a power-on reset.
- Do not leave the HV (High Voltage) input pin unconnected.
- Example of a recommended circuit
  - Input/Output equivalent circuit



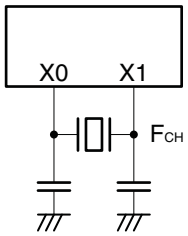
WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

- Input waveform generated when an external clock (main clock) is used

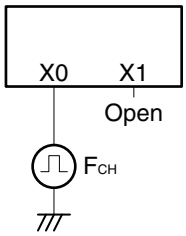


- Figure of main clock input port external connection

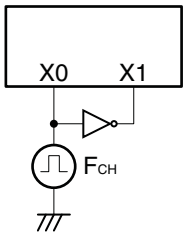
When a crystal oscillator or a ceramic oscillator is used



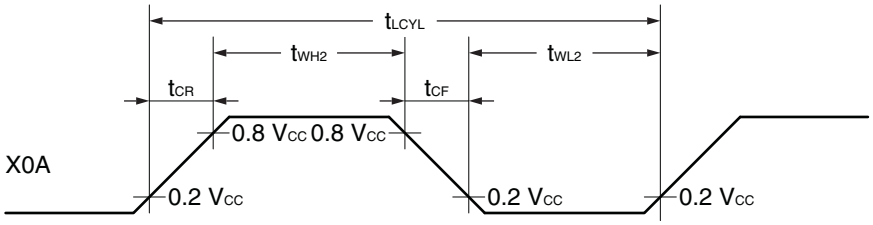
When the external clock is used (X1 is open)



When the external clock is used

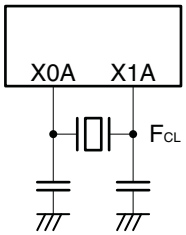


- Input waveform generated when an external clock (subclock) is used

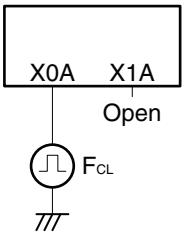


- Figure of subclock input port external connection

When a crystal oscillator or a ceramic oscillator is used



When the external clock is used

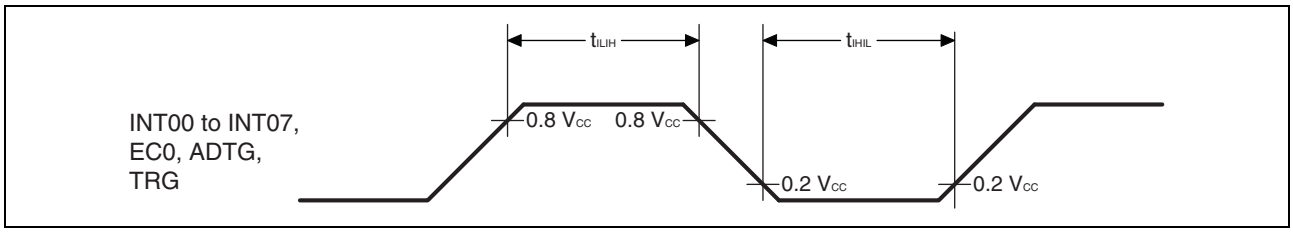


(5) Peripheral Input Timing

(V_{CC} = 5.0 V±10%, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
Peripheral input “H” pulse width	t_{ILIH}	INT00 to INT07, EC0, ADTG, TRG	2 t_{MCLK}*	—	ns
Peripheral input “L” pulse width	t_{IHIL}		2 t_{MCLK}*	—	ns

*: See “(2) Source Clock/Machine Clock” for t_{MCLK}.



(8) I²C Timing

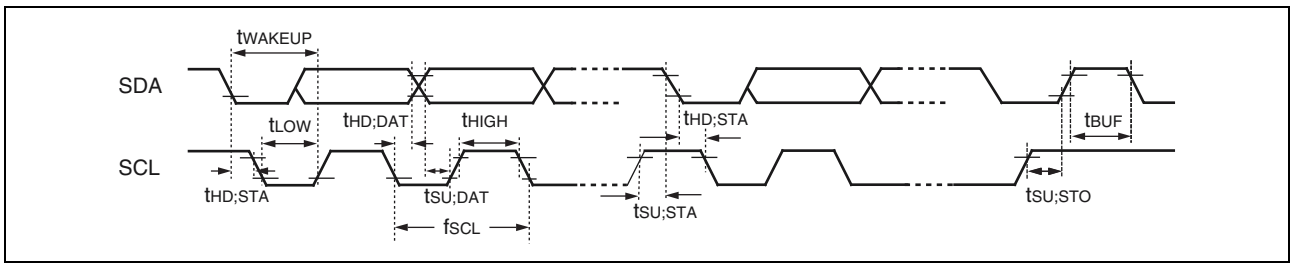
(V_{CC} = 5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value				Unit
				Standard-mode		Fast-mode		
				Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	SCL	R = 1.7 kΩ, C = 50 pF*1	0	100	0	400	kHz
(Repeated) START condition hold time SDA ↓ → SCL ↓	$t_{HD;STA}$	SCL, SDA		4.0	—	0.6	—	µs
SCL clock “L” width	t_{LOW}	SCL		4.7	—	1.3	—	µs
SCL clock “H” width	t_{HIGH}	SCL		4.0	—	0.6	—	µs
(Repeated) START condition setup time SCL ↑ → SDA ↓	$t_{SU;STA}$	SCL, SDA		4.7	—	0.6	—	µs
Data hold time SCL ↓ → SDA ↓↑	$t_{HD;DAT}$	SCL, SDA		0	3.45*2	0	0.9*3	µs
Data setup time SDA ↓↑ → SCL ↑	$t_{SU;DAT}$	SCL, SDA		0.25	—	0.1	—	µs
STOP condition setup time SCL ↑ → SDA ↑	$t_{SU;STO}$	SCL, SDA		4	—	0.6	—	µs
Bus free time between STOP condition and START condition	t_{BUF}	SCL, SDA		4.7	—	1.3	—	µs

*1: R represents the pull-up resistor of the SCL and SDA lines, and C the load capacitor of the SCL and SDA lines.

*2: The maximum $t_{HD;DAT}$ in the Standard-mode is applicable only when the time during which the device is holding the SCL signal at “L” (t_{LOW}) does not extend.

*3: A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system, provided that the condition of $t_{SU;DAT}$ ≥ 250ns is fulfilled.



(Continued)

(V_{CC} = 5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value*2		Unit	Remarks
				Min	Max		
SCL clock “L” width	t_{LOW}	SCL	R = 1.7 kΩ, C = 50 pF*1	$(2 + nm/2)t_{MCLK} – 20$	—	ns	Master mode
SCL clock “H” width	t_{HIGH}	SCL		$(nm/2)t_{MCLK} – 20$	$(nm/2)t_{MCLK} + 20$	ns	Master mode
START condition hold time	$t_{HD;STA}$	SCL, SDA		$(–1 + nm/2)t_{MCLK} – 20$	$(–1 + nm)t_{MCLK} + 20$	ns	Master mode Maximum value is applied when m, n = 1, 8. Otherwise, the minimum value is applied.
STOP condition setup time	$t_{SU;STO}$	SCL, SDA		$(1 + nm/2)t_{MCLK} – 20$	$(1 + nm/2)t_{MCLK} + 20$	ns	Master mode
START condition setup time	$t_{SU;STA}$	SCL, SDA		$(1 + nm/2)t_{MCLK} – 20$	$(1 + nm/2)t_{MCLK} + 20$	ns	Master mode
Bus free time between STOP condition and START condition	t_{BUF}	SCL, SDA		$(2 nm + 4)t_{MCLK} – 20$	—	ns	
Data hold time	$t_{HD;DAT}$	SCL, SDA		$3 t_{MCLK} – 20$	—	ns	Master mode
Data setup time	$t_{SU;DAT}$	SCL, SDA		$(–2 + nm/2)t_{MCLK} – 20$	$(–1 + nm/2)t_{MCLK} + 20$	ns	Master mode When assuming that “L” of SCL is not extended, the minimum value is applied to first bit of continuous data. Otherwise, the maximum value is applied.
Setup time between clearing interrupt and SCL rising	$t_{SU;INT}$	SCL		$(nm/2)t_{MCLK} – 20$	$(1 + nm/2)t_{MCLK} + 20$	ns	Minimum value is applied to interrupt at 9th SCL↓. Maximum value is applied to the interrupt at the 8th SCL↓.

(Continued)

(Continued)

(V_{CC} = 5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Sym-bol	Pin name	Condition	Value*2		Unit	Remarks
				Min	Max		
SCL clock “L” width	t_{LOW}	SCL	R = 1.7 kΩ, C = 50 pF*1	4 t_{MCLK} – 20	—	ns	At reception
SCL clock “H” width	t_{HIGH}	SCL		4 t_{MCLK} – 20	—	ns	At reception
START condition detection	$t_{HD;STA}$	SCL, SDA		2 t_{MCLK} – 20	—	ns	Undetected when 1 t_{MCLK} is used at reception
STOP condition detection	$t_{SU;STO}$	SCL, SDA		2 t_{MCLK} – 20	—	ns	Undetected when 1 t_{MCLK} is used at reception
RESTART condition detection condition	$t_{SU;STA}$	SCL, SDA		2 t_{MCLK} – 20	—	ns	Undetected when 1 t_{MCLK} is used at reception
Bus free time	t_{BUF}	SCL, SDA		2 t_{MCLK} – 20	—	ns	At reception
Data hold time	$t_{HD;DAT}$	SCL, SDA		2 t_{MCLK} – 20	—	ns	At slave transmission mode
Data setup time	$t_{SU;DAT}$	SCL, SDA		t_{LOW} – 3 t_{MCLK} – 20	—	ns	At slave transmission mode
Data hold time	$t_{HD;DAT}$	SCL, SDA		0	—	ns	At reception
Data setup time	$t_{SU;DAT}$	SCL, SDA		t_{MCLK} – 20	—	ns	At reception
SDA↓ → SCL↑ (at wakeup function)	t_{WAKEUP}	SCL, SDA		Oscillation stabilization wait time +2 t_{MCLK} – 20	—	ns	

*1: R represents the pull-up resistor of the SCL and SDA lines, and C the load capacitor of the SCL and SDA lines.

*2:
- See “(2) Source Clock/Machine Clock” for t_{MCLK}.
- m represents the CS4 bit and CS3 bit (bit4 and bit3) in the I²C clock control register (ICCR0).
- n represents the CS2 bit to CS0 bit (bit2 to bit0) in the I²C clock control register (ICCR0).
- The actual timing of I²C is determined by the values of m and n set by the machine clock (t_{MCLK}) and the CS4 to CS0 bits in the ICCR0 register.
- Standard-mode:
  m and n can be set to values in the following range: 0.9 MHz < t_{MCLK} (machine clock) < 16.25 MHz.
  The usable frequencies of the machine clock are determined by the settings of m and n as shown below.
  (m, n) = (1, 8) : 0.9 MHz < t_{MCLK} ≤ 1 MHz
  (m, n) = (1, 22), (5, 4), (6, 4), (7, 4), (8, 4) : 0.9 MHz < t_{MCLK} ≤ 2 MHz
  (m, n) = (1, 38), (5, 8), (6, 8), (7, 8), (8, 8) : 0.9 MHz < t_{MCLK} ≤ 4 MHz
  (m, n) = (1, 98), (5, 22), (6, 22), (7, 22) : 0.9 MHz < t_{MCLK} ≤ 10 MHz
  (m, n) = (8, 22) : 0.9 MHz < t_{MCLK} ≤ 16.25 MHz
- Fast-mode:
  m and n can be set to values in the following range: 3.3 MHz < t_{MCLK} (machine clock) < 16.25 MHz.
  The usable frequencies of the machine clock are determined by the settings of m and n as shown below.
  (m, n) = (1, 8) : 3.3 MHz < t_{MCLK} ≤ 4 MHz
  (m, n) = (1, 22), (5, 4) : 3.3 MHz < t_{MCLK} ≤ 8 MHz
  (m, n) = (1, 22), (6, 4), (7, 4), (8, 4) : 3.3 MHz < t_{MCLK} ≤ 10 MHz
  (m, n) = (5, 8) : 3.3 MHz < t_{MCLK} ≤ 16.25 MHz

5. A/D Converter

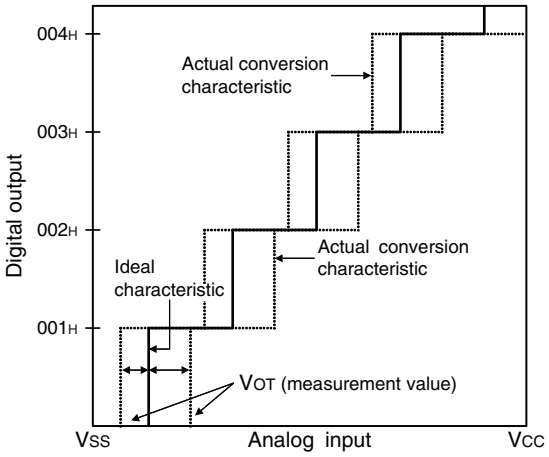
(1) A/D Converter Electrical Characteristics

(V_{CC} = 4.0 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

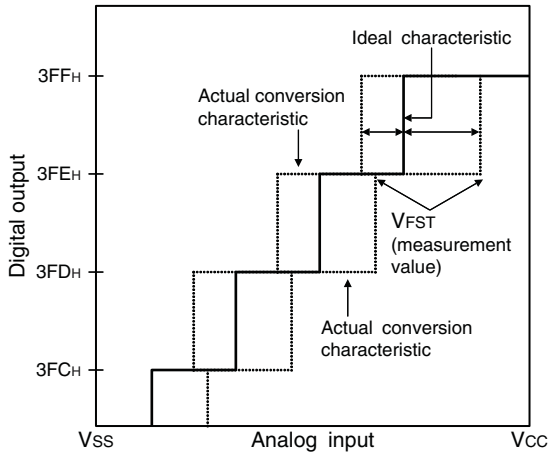
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Resolution	—	—	—	10	bit	
Total error		–3	—	+3	LSB	
Linearity error		–2.5	—	+2.5	LSB	
Differential linear error		–1.9	—	+1.9	LSB	
Zero transition voltage	V_{OT}	V_{SS} – 1.5 LSB	V_{SS} + 0.5 LSB	V_{SS} + 2.5 LSB	V	
Full-scale transition voltage	V_{FST}	V_{CC} – 4.5 LSB	V_{CC} – 2 LSB	V_{CC} + 0.5 LSB	V	
Compare time	—	0.9	—	16500	µs	4.5 V ≤ V_{CC} ≤ 5.5 V
		1.8	—	16500	µs	4.0 V ≤ V_{CC} < 4.5 V
Sampling time	—	0.6	—	∞	µs	4.5 V ≤ V_{CC} ≤ 5.5 V, with external impedance < 5.4 kΩ
		1.2	—	∞	µs	4.0 V ≤ V_{CC} < 4.5 V, with external impedance < 2.4 kΩ
Analog input current	I_{AIN}	–0.3	—	+0.3	µA	
Analog input voltage	V_{AIN}	V_{SS}	—	V_{CC}	V	

(Continued)

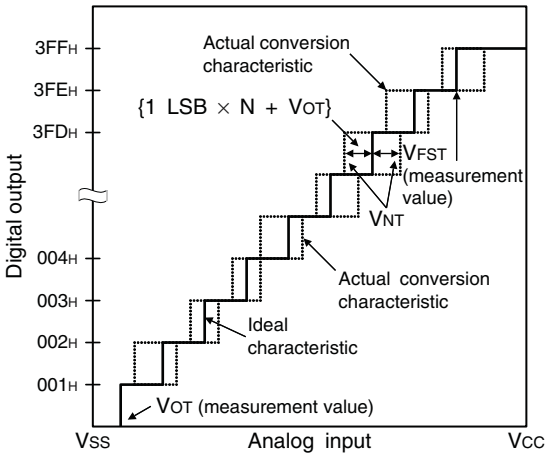
Zero transition error



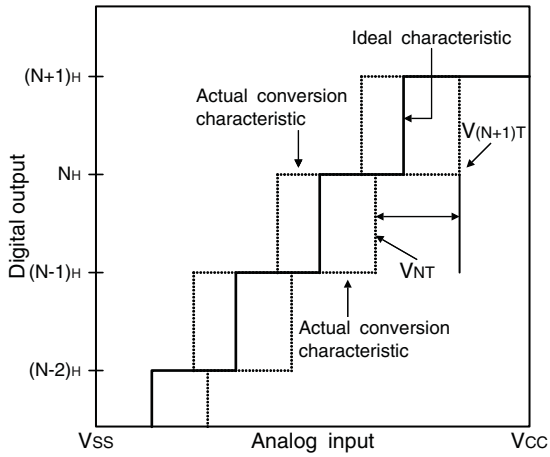
Full-scale transition error



Linearity error



Differential linearity error



$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ LSB \times N + V_{OT}\}}{1\ LSB}$$

$$\text{Differential linear error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ LSB} - 1$$

N : A/D converter digital output value

V_{NT} : Voltage at which the digital output transits from $(N - 1)_H$ to N_H

V_{OT} (ideal value) = V_{SS} + 0.5 LSB [V]

V_{FST} (ideal value) = V_{CC} - 2 LSB [V]

6. Flash Memory Program/Erase Characteristics

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time (2 Kbyte sector)	—	0.2*1	0.5*2	s	The time of writing 00H prior to erasure is excluded.
Sector erase time (16 Kbyte sector)	—	0.5*1	7.5*2	s	The time of writing 00H prior to erasure is excluded.
Byte writing time	—	21	6100*2	µs	System-level overhead is excluded.
Program/erase cycle	100000	—	—	cycle	
Power supply voltage at program/erase	3.0	—	5.5	V	
Flash memory data retention time	20*3	—	—	year	Average T_A = +85°C

*1: T_A = +25°C, V_{CC} = 5.0 V, 100000 cycles

*2: T_A = +85°C, V_{CC} = 3.0 V, 100000 cycles

*3: This value is converted from the result of a technology reliability assessment. (The value is converted from the result of a high temperature accelerated test using the Arrhenius equation with the average temperature being +85°C).

■ MASK OPTIONS

No.	Part Number	MB95F432H MB95F433H MB95F434H	MB95F432K MB95F433K MB95F434K
	Selectable/Fixed	Fixed	
1	Low-voltage detection reset	Without low-voltage detection reset	With low-voltage detection reset
2	Reset	With dedicated reset input	Without dedicated reset input

MEMO

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