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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, Motor Control PWM, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	37
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f103c6t7atr

2 Description

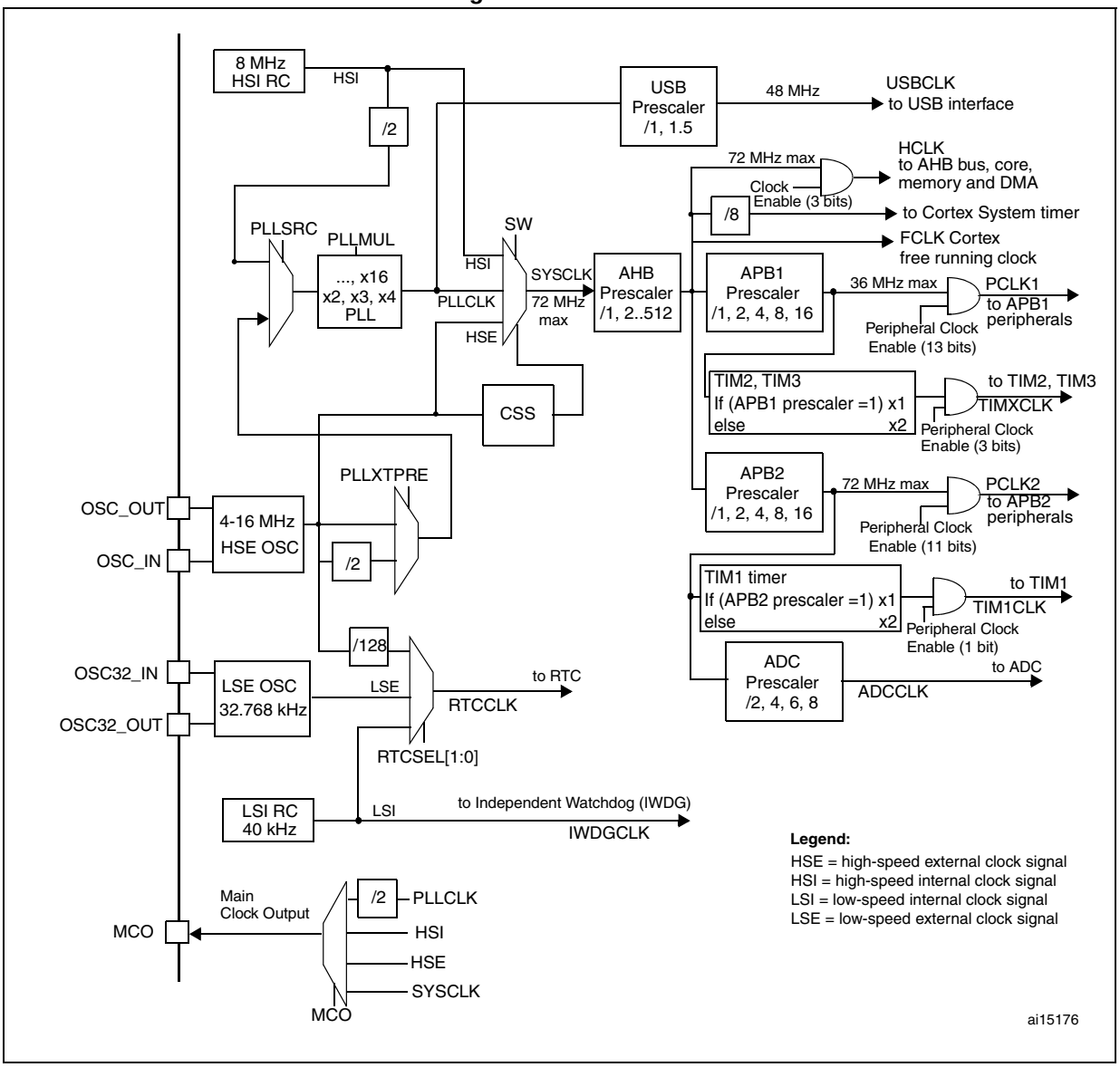
The STM32F103x4 and STM32F103x6 performance line family incorporates the high-performance ARM® Cortex™-M3 32-bit RISC core operating at a 72 MHz frequency, high-speed embedded memories (Flash memory up to 32 Kbytes and SRAM up to 6 Kbytes), and an extensive range of enhanced I/Os and peripherals connected to two APB buses. All devices offer two 12-bit ADCs, three general purpose 16-bit timers plus one PWM timer, as well as standard and advanced communication interfaces: up to two I^2Cs and SPIs, three USARTs, an USB and a CAN.

The STM32F103xx low-density performance line family operates from a 2.0 to 3.6 V power supply. It is available in both the –40 to +85 °C temperature range and the –40 to +105 °C extended temperature range. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F103xx low-density performance line family includes devices in four different package types: from 36 pins to 64 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

These features make the STM32F103xx low-density performance line microcontroller family suitable for a wide range of applications such as motor drives, application control, medical and handheld equipment, PC and gaming peripherals, GPS platforms, industrial applications, PLCs, inverters, printers, scanners, alarm systems, video intercoms, and HVACs.

Figure 2. Clock tree



1. When the HSI is used as a PLL clock input, the maximum system clock frequency that can be achieved is 64 MHz.
2. For the USB function to be available, both HSE and PLL must be enabled, with USBCLK running at 48 MHz.
3. To have an ADC conversion time of 1 µs, APB2 must be at 14 MHz, 28 MHz or 56 MHz.

2.3.13 DMA

The flexible 7-channel general-purpose DMA is able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The DMA controller supports circular buffer management avoiding the generation of interrupts when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C, USART, general-purpose and advanced-control timers TIMx and ADC.

2.3.14 RTC (real-time clock) and backup registers

The RTC and the backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the V_{BAT} pin. The backup registers are ten 16-bit registers used to store 20 bytes of user application data when V_{DD} power is not present.

The real-time clock provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a periodic interrupt. It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low-power RC oscillator or the high-speed external clock divided by 128. The internal low-power RC has a typical frequency of 40 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural crystal deviation. The RTC features a 32-bit programmable counter for long-term measurement using the Compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

2.3.15 Timers and watchdogs

The low-density STM32F103xx performance line devices include an advanced-control timer, two general-purpose timers, two watchdog timers and a SysTick timer.

Table 4 compares the features of the advanced-control and general-purpose timers.

Table 4. Timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TIM1	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	Yes
TIM2, TIM3	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No

Figure 7. STM32F103xx performance line VFQFPN36 pinout

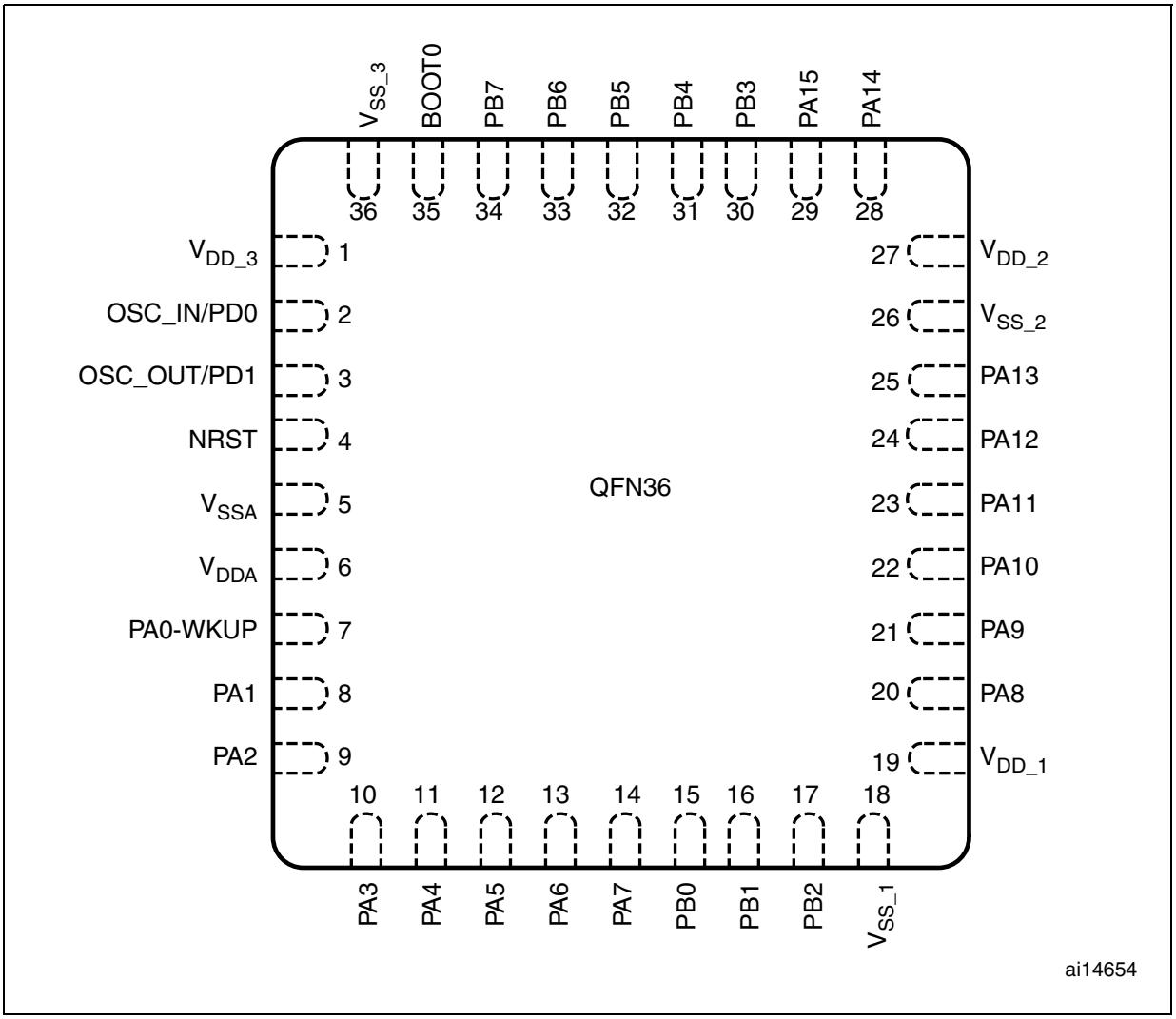


Table 5. Low-density STM32F103xx pin definitions

Pins				Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions(4)	
LQFP48/ UFQFPN48	LQFP64	TFBGA64	VFQFPN36					Default	Remap
1	1	B2	-	V_{BAT}	S	-	V_{BAT}	-	-
2	2	A2	-	PC13-TAMPER-RTC(5)	I/O	-	PC13(6)	TAMPER-RTC	-
3	3	A1	-	PC14-OSC32_IN(5)	I/O	-	PC14(6)	OSC32_IN	-
4	4	B1	-	PC15-OSC32_OUT(5)	I/O	-	PC15(6)	OSC32_OUT	-
5	5	C1	2	OSC_IN	I	-	OSC_IN	-	PD0(7)
6	6	D1	3	OSC_OUT	O	-	OSC_OUT	-	PD1(7)
7	7	E1	4	NRST	I/O	-	NRST		-
-	8	E3	-	PC0	I/O	-	PC0	ADC12_IN10	-
-	9	E2	-	PC1	I/O	-	PC1	ADC12_IN11	-
-	10	F2	-	PC2	I/O	-	PC2	ADC12_IN12	-
-	11	-	-	PC3	I/O	-	PC3	ADC12_IN13	-
-	-	G1	-	V_{REF+}(8)	S	-	V_{REF+}	-	-
8	12	F1	5	V_{SSA}	S	-	V_{SSA}	-	-
9	13	H1	6	V_{DDA}	S	-	V_{DDA}	-	-
10	14	G2	7	PA0-WKUP	I/O	-	PA0	WKUP/USART2_CTS/ ADC12_IN0/ TIM2_CH1_ETR(9)	-
11	15	H2	8	PA1	I/O	-	PA1	USART2_RTS/ ADC12_IN1/ TIM2_CH2(9)	-
12	16	F3	9	PA2	I/O	-	PA2	USART2_TX/ ADC12_IN2/ TIM2_CH3(9)	-
13	17	G3	10	PA3	I/O	-	PA3	USART2_RX/ ADC12_IN3/TIM2_CH4(9)	-
-	18	C2	-	V_{SS_4}	S	-	V_{SS_4}	-	-
-	19	D2	-	V_{DD_4}	S	-	V_{DD_4}	-	-
14	20	H3	11	PA4	I/O	-	PA4	SPI1_NSS(9)/ USART2_CK/ADC12_IN4	-
15	21	F4	12	PA5	I/O	-	PA5	SPI1_SCK(9)/ ADC12_IN5	-
16	22	G4	13	PA6	I/O	-	PA6	SPI1_MISO(9)/ ADC12_IN6/TIM3_CH1(9)	TIM1_BKIN
17	23	H4	14	PA7	I/O	-	PA7	SPI1_MOSI(9)/ ADC12_IN7/TIM3_CH2(9)	TIM1_CH1N
-	24	H5	-	PC4	I/O	-	PC4	ADC12_IN14	-
-	25	H6	-	PC5	I/O	-	PC5	ADC12_IN15	-

Table 5. Low-density STM32F103xx pin definitions (continued)

Pins				Pin name	Type[1]	I / O Level[2]	Main function[3] (after reset)	Alternate functions[4]	
LQFP48/ UFQFPN48	LQFP64	TFBGA64	VFQFPN36					Default	Remap
18	26	F5	15	PB0	I/O	-	PB0	ADC12_IN8/TIM3_CH3[9]	TIM1_CH2N
19	27	G5	16	PB1	I/O	-	PB1	ADC12_IN9/TIM3_CH4[9]	TIM1_CH3N
20	28	G6	17	PB2	I/O	FT	PB2/BOOT1	-	-
21	29	G7	-	PB10	I/O	FT	PB10	-	TIM2_CH3
22	30	H7	-	PB11	I/O	FT	PB11	-	TIM2_CH4
23	31	D6	18	V_{SS_1}	S	-	V_{SS_1}	-	-
24	32	E6	19	V_{DD_1}	S	-	V_{DD_1}	-	-
25	33	H8	-	PB12	I/O	FT	PB12	TIM1_BKIN[9]	-
26	34	G8	-	PB13	I/O	FT	PB13	TIM1_CH1N [9]	-
27	35	F8	-	PB14	I/O	FT	PB14	TIM1_CH2N [9]	-
28	36	F7	-	PB15	I/O	FT	PB15	TIM1_CH3N[9]	-
-	37	F6	-	PC6	I/O	FT	PC6	-	TIM3_CH1
-	38	E7	-	PC7	I/O	FT	PC7	-	TIM3_CH2
-	39	E8	-	PC8	I/O	FT	PC8	-	TIM3_CH3
-	40	D8	-	PC9	I/O	FT	PC9	-	TIM3_CH4
29	41	D7	20	PA8	I/O	FT	PA8	USART1_CK/ TIM1_CH1/MCO	-
30	42	C7	21	PA9	I/O	FT	PA9	USART1_TX[9]/ TIM1_CH2[9]	-
31	43	C6	22	PA10	I/O	FT	PA10	USART1_RX[9]/ TIM1_CH3	-
32	44	C8	23	PA11	I/O	FT	PA11	USART1_CTS/ CAN_RX[9]/ TIM1_CH4 / USBDM	-
33	45	B8	24	PA12	I/O	FT	PA12	USART1_RTS/ CAN_TX[9] / TIM1_ETR / USBDP	-
34	46	A8	25	PA13	I/O	FT	JTMS/SWDIO		PA13
35	47	D5	26	V_{SS_2}	S	-	V_{SS_2}	-	-
36	48	E5	27	V_{DD_2}	S	-	V_{DD_2}	-	-
37	49	A7	28	PA14	I/O	FT	JTCK/SWCLK	-	PA14
38	50	A6	29	PA15	I/O	FT	JTDI	-	TIM2_CH1_ETR/ PA15 / SPI1_NSS
-	51	B7	-	PC10	I/O	FT	PC10	-	-
-	52	B6	-	PC11	I/O	FT	PC11	-	-
-	53	C5	-	PC12	I/O	FT	PC12	-	-
-	-	C1	2	PD0	I/O	FT	PD0	-	-

4 Memory mapping

The memory map is shown in *Figure 8*.

Figure 8. Memory map

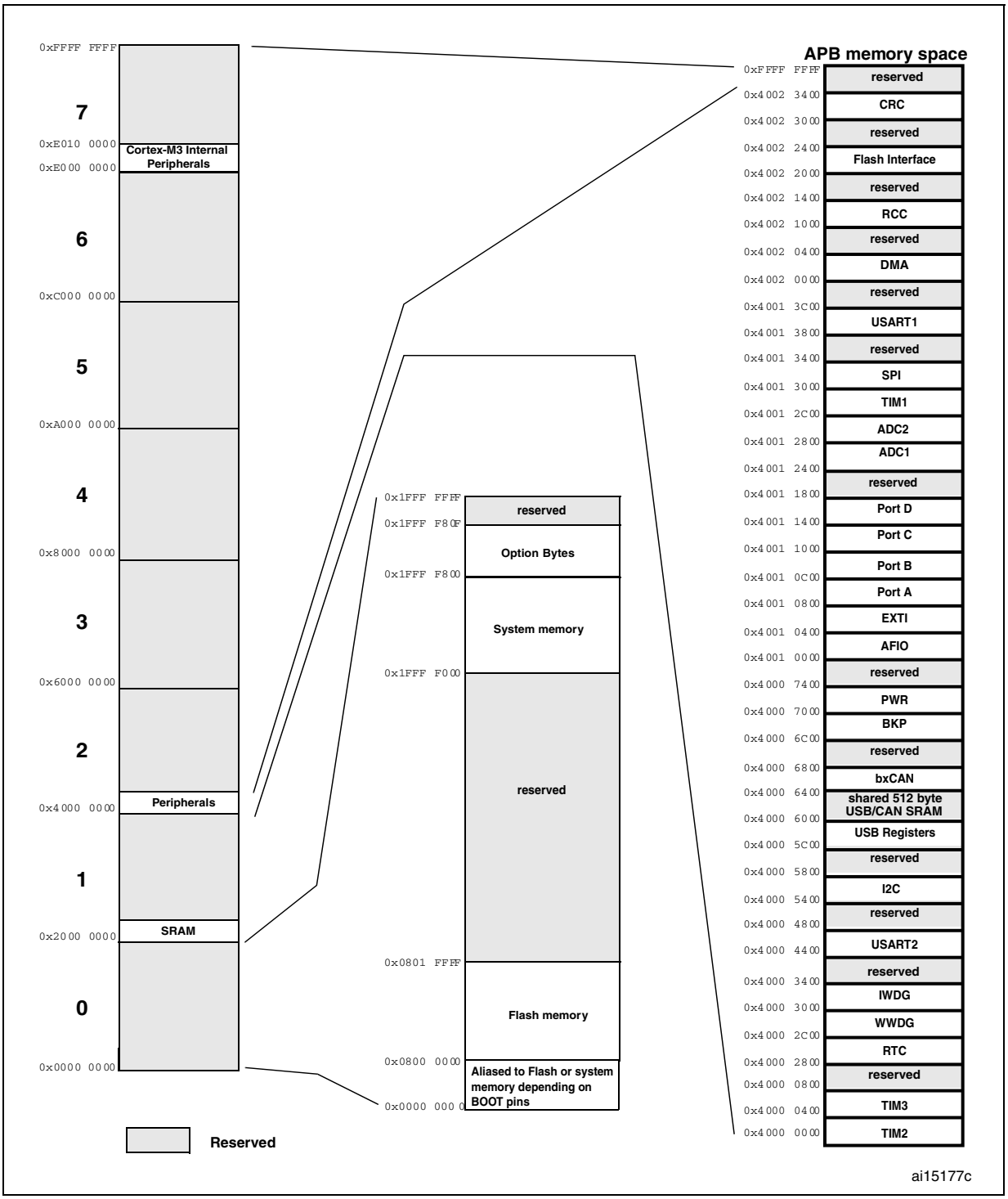


Figure 9. Pin loading conditions

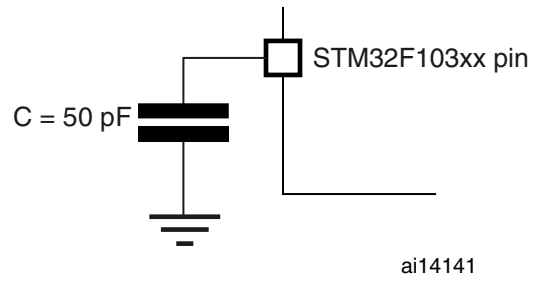
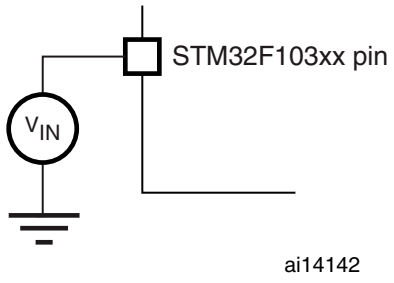
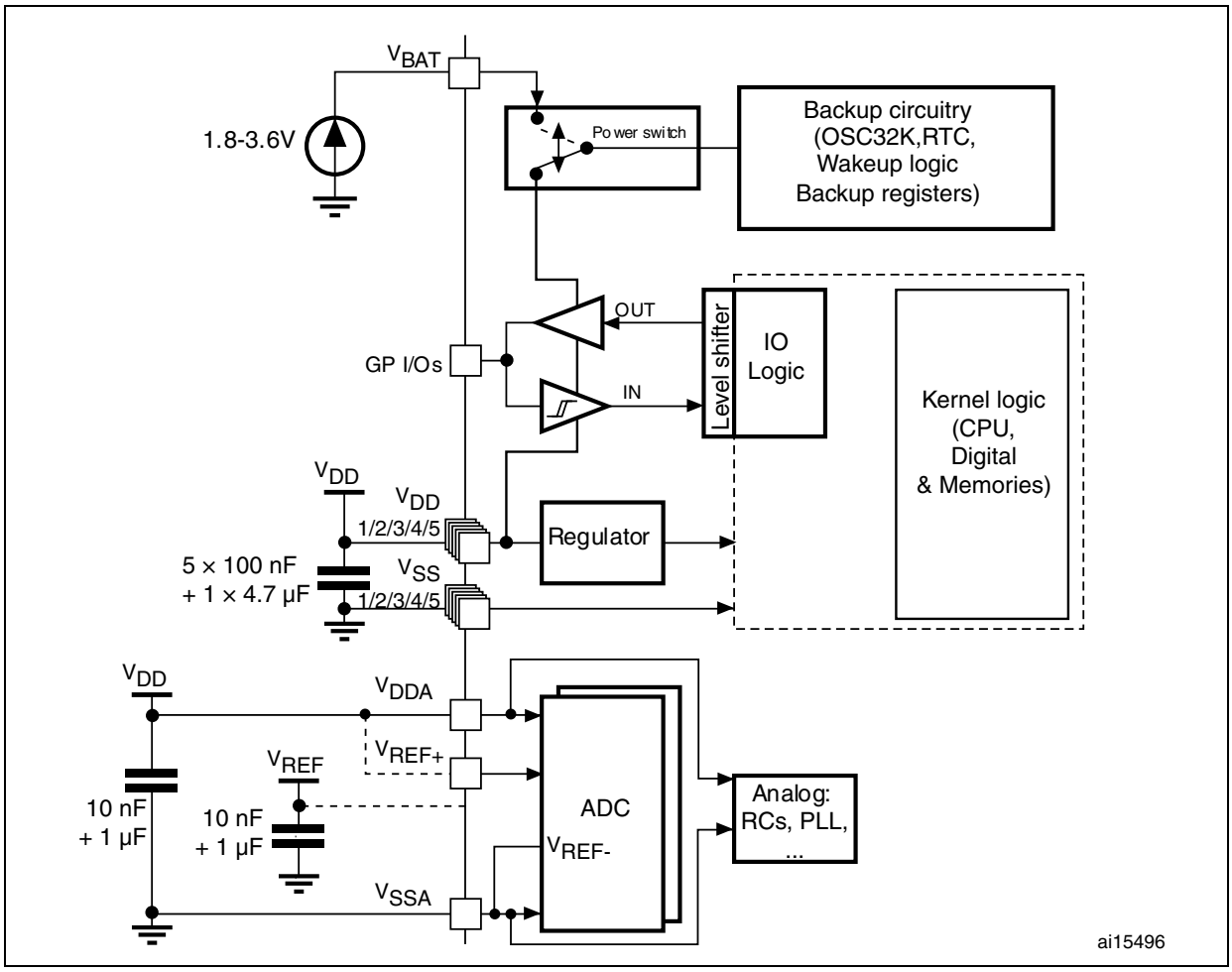


Figure 10. Pin input voltage



5.1.6 Power supply scheme

Figure 11. Power supply scheme



Caution: In *Figure 11*, the 4.7 µF capacitor must be connected to V_{DD3}.

Table 9. General operating conditions (continued)

Symbol	Parameter	Conditions		Min	Max	Unit
V_{IN}	I/O input voltage	Standard IO		–0.3	V_{DD}+ 0.3	V
		FT IO(3)	2 V < V_{DD} ≤ 3.6 V	–0.3	5.5	
			V_{DD} = 2 V	–0.3	5.2	
		BOOT0		0	5.5	
P_D	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7(4)	TFBGA64		-	308	mW
		LQFP64		-	444	
		LQFP48		-	363	
		UFQFPN48		-	624	
		VFQFPN36		-	1000	
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation		–40	85	°C
		Low power dissipation(5)		–40	105	
	Ambient temperature for 7 suffix version	Maximum power dissipation		–40	105	
		Low power dissipation(5)		–40	125	
T_J	Junction temperature range	6 suffix version		–40	105	
		7 suffix version		–40	125	

1. When the ADC is used, refer to *Table 46: ADC characteristics*.
2. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and operation.
3. To sustain a voltage higher than V_{DD}+0.3 V, the internal pull-up/pull-down resistors must be disabled.
4. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed $T_J$max (see *Table 6.6: Thermal characteristics on page 92*).
5. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed $T_J$max (see *Table 6.6: Thermal characteristics on page 92*).

5.3.2 Operating conditions at power-up / power-down

Subject to general operating conditions for T_A.

Table 10. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	¥	µs/V
	V_{DD} fall time rate		20	¥	

5.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 11* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 16. Typical and maximum current consumptions in Stop and Standby modes

Symbol	Parameter	Conditions	Typ(1)			Max		Unit
			V_{DD}/V_{BAT} = 2.0 V	V_{DD}/V_{BAT} = 2.4 V	V_{DD}/V_{BAT} = 3.3 V	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Stop mode	Regulator in Run mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	-	21.3	21.7	160	200	µA
		Regulator in Low Power mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	-	11.3	11.7	145	185	
	Supply current in Standby mode	Low-speed internal RC oscillator and independent watchdog ON	-	2.75	3.4	-	-	
		Low-speed internal RC oscillator ON, independent watchdog OFF	-	2.55	3.2	-	-	
		Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF	-	1.55	1.9	3.2	4.5	
I_{DD_VBAT}	Backup domain supply current	Low-speed oscillator and RTC ON	0.9	1.1	1.4	1.9(2)	2.2	

1. Typical values are measured at T_A = 25 °C.
2. Based on characterization, not tested in production.

Figure 15. Typical current consumption on V_{BAT} with RTC on versus temperature at different V_{BAT} values

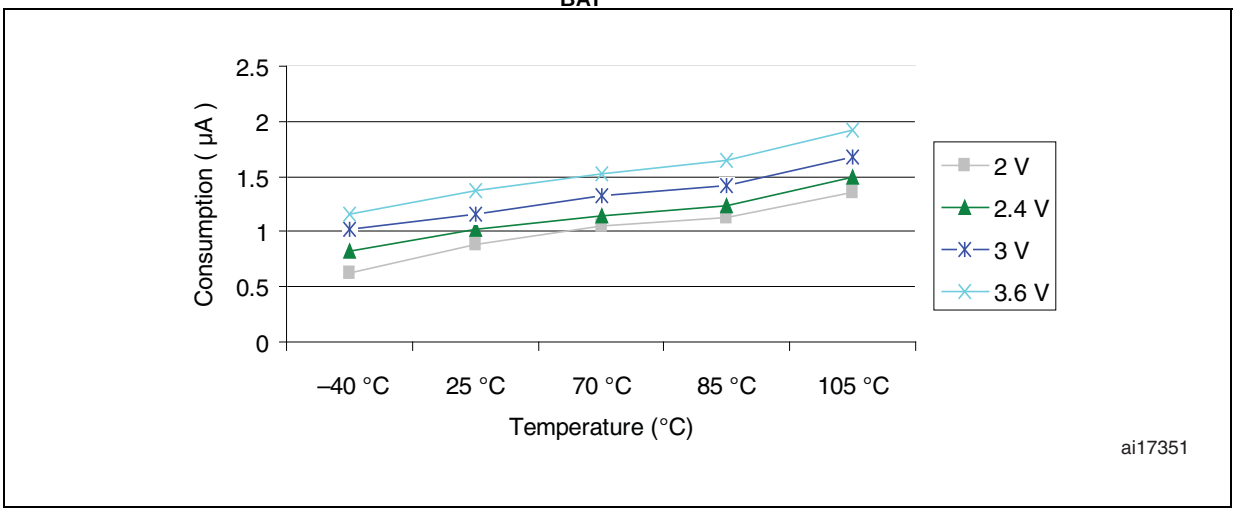


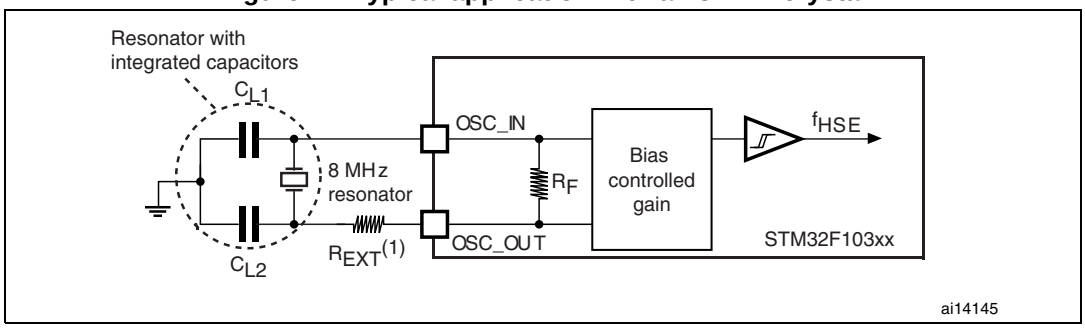
Table 22. HSE 4-16 MHz oscillator characteristics(1) (2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	16	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
C	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)(3)	R_S = 30 Ω	-	30	-	pF
i_2	HSE driving current	V_{DD} = 3.3 V, V_{IN} = V_{SS} with 30 pF load	-	-	1	mA
g_m	Oscillator transconductance	Startup	25	-	-	mA/V
$t_{SU(HSE}$(4)	startup time	V_{DD} is stabilized	-	2	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Based on characterization, not tested in production.
3. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 21*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}. Refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 21. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 23*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization

Low-speed internal (LSI) RC oscillator

Table 25. LSI oscillator characteristics (1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}(2)	Frequency	30	40	60	kHz
$t_{su(LSI)}$(3)	LSI oscillator startup time	-	-	85	µs
$I_{DD(LSI)}$(3)	LSI oscillator power consumption	-	0.65	1.2	µA

1. V_{DD} = 3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Based on characterization, not tested in production.
3. Guaranteed by design, not tested in production.

Wakeup time from low-power mode

The wakeup times given in *Table 26* is measured on a wakeup phase with a 8-MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode.

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

5.3.11 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 32. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C conforming to JESD22-A114	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to JESD22-C101	II	500	

1. Based on characterization results, not tested in production.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 33. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A

5.3.13 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 35* are derived from tests performed under the conditions summarized in *Table 9*. All I/Os are CMOS and TTL compliant.

Table 35. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage	Standard IO input low level voltage	-	-	$0.28*(V_{DD}-2\ V)+0.8\ V$(1)	V
		IO FT(3) input low level voltage	-	-	$0.32*(V_{DD}-2V)+0.75\ V$(1)	
		All I/Os except BOOT0	-	-	$0.35V_{DD}$(2)	
V_{IH}	High level input voltage	Standard IO input high level voltage	$0.41*(V_{DD}-2\ V)+1.3\ V$(1)	-	-	
		IO FT(3) input high level voltage	$0.42*(V_{DD}-2\ V)+1\ V$(1)	-	-	
		All I/Os except BOOT0	$0.65V_{DD}$(2)	-	-	
V_{hys}	Standard IO Schmitt trigger voltage hysteresis(4)	-	200	-	-	mV
	IO FT Schmitt trigger voltage hysteresis(4)	-	5% V_{DD}(5)	-	-	
I_{lkg}	Input leakage current (6)	$V_{SS} \le V_{IN} \le V_{DD}$ Standard I/Os	-	-	±1	µA
		V_{IN} = 5 V I/O FT	-	-	3	
R_{PU}	Weak pull-up equivalent resistor(7)	$V_{IN} = V_{SS}$	30	40	50	kΩ
R_{PD}	Weak pull-down equivalent resistor(7)	$V_{IN} = V_{DD}$	30	40	50	
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Data based on design simulation.
2. Tested in production.
3. FT = Five-volt tolerant. In order to sustain a voltage higher than V_{DD}+0.3 the internal pull-up/pull-down resistors must be disabled.
4. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization, not tested in production.
5. With a minimum of 100 mV.
6. Leakage could be higher than max. if negative current is injected on adjacent pins.
7. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimum (~10% order).

Figure 25. 5 V tolerant I/O input characteristics - CMOS port

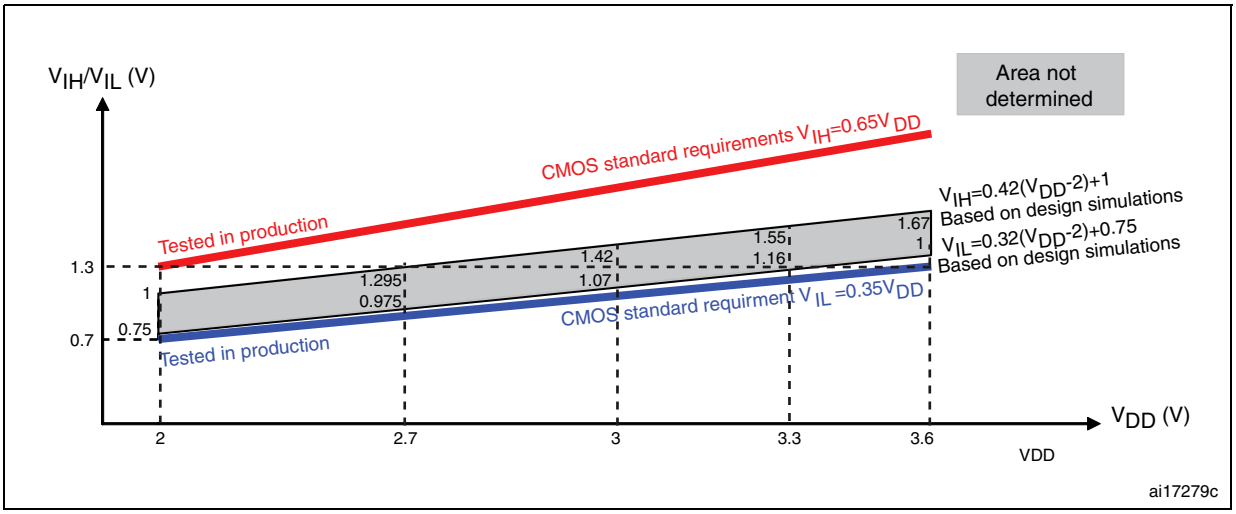
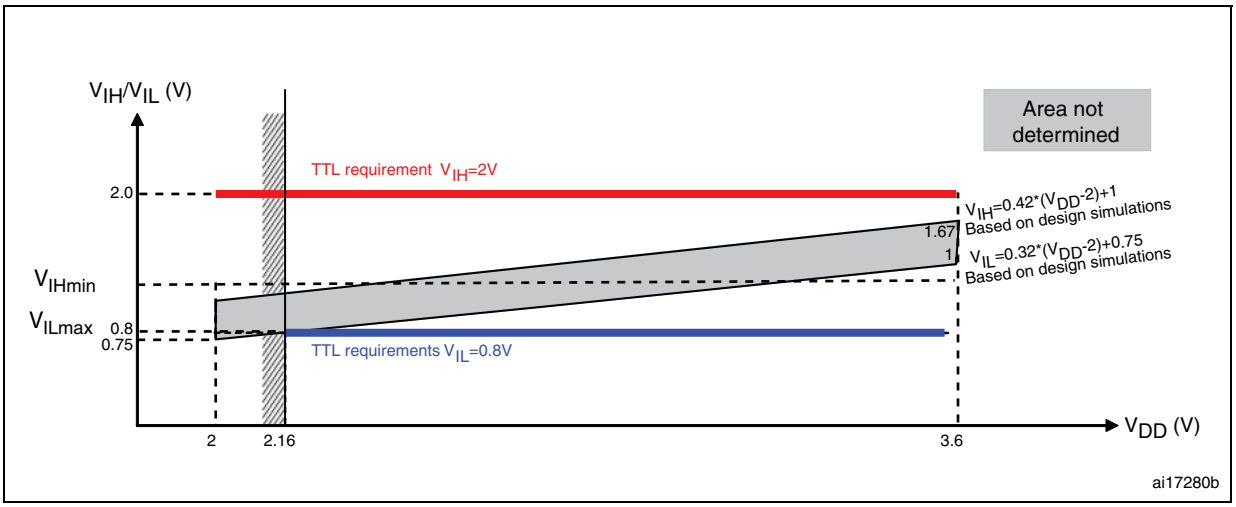


Figure 26. 5 V tolerant I/O input characteristics - TTL port



5.3.16 Communications interfaces

I^2C interface characteristics

The STM32F103xx performance line I^2C interface meets the requirements of the standard I^2C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DD} is disabled, but is still present.

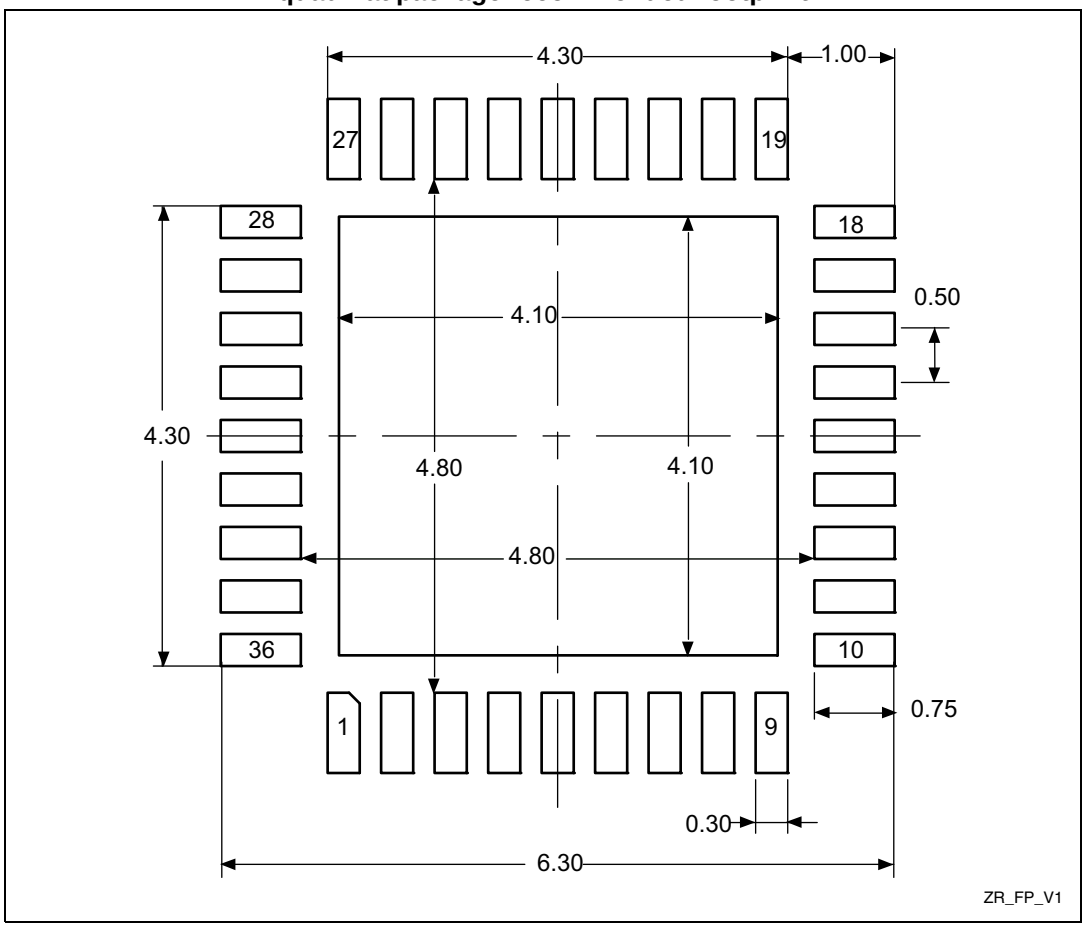
The I^2C characteristics are described in *Table 40*. Refer also to *Section 5.3.12: I/O current injection characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

Table 40. I^2C characteristics

Symbol	Parameter	Standard mode I^2C(1)(2)		Fast mode I^2C(1)(2)		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	-	3450(3)	-	900(3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	-	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	Start condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated Start condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	Stop condition setup time	4.0	-	0.6	-	µs
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7	-	1.3	-	µs
C_b	Capacitive load for each bus line	-	400	-	400	pF

1. Guaranteed by design, not tested in production.
2. f_{PCLK1} must be at least 2 MHz to achieve standard mode I^2C frequencies. It must be at least 4 MHz to achieve fast mode I^2C frequencies. It must be a multiple of 10 MHz to reach the 400 kHz maximum I2C fast mode clock.
3. The maximum Data hold time has only to be met if the interface does not stretch the low period of SCL signal.

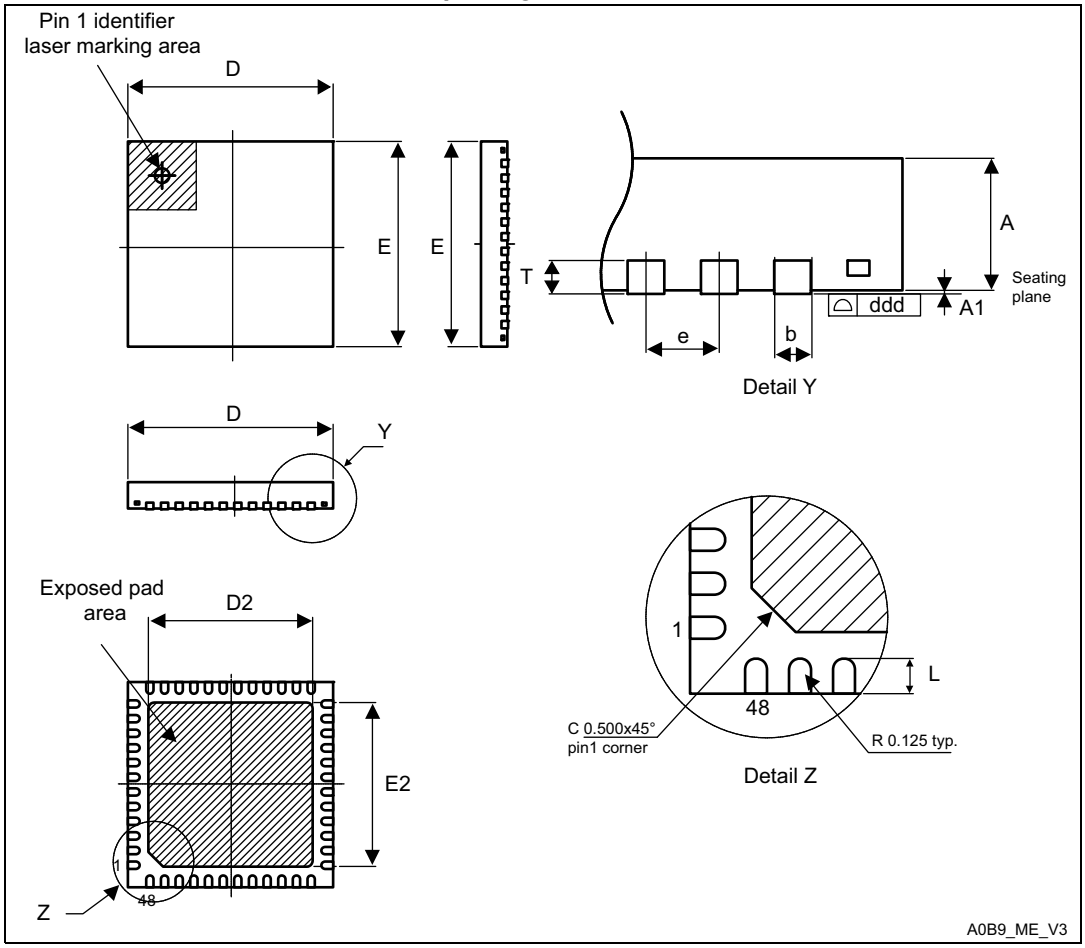
Figure 39. VFQFPN36 - 36-pin, 6x6 mm, 0.5 mm pitch very thin profile fine pitch quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

6.2 UFQFPN48 package information

Figure 41. UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline



1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this back-side pad to PCB ground.

Table 59. Document revision history (continued)

Date	Revision	Changes
20-May-2010	4	Added VFQFPN48 package. Updated note 2 below *Table 40: I^2C characteristics* Updated *Figure 29: I^2C bus AC waveforms and measurement circuit* Updated *Figure 28: Recommended NRST pin protection* Updated *Section 5.3.12: I/O current injection characteristics*
19-Apr-2011	5	Updated footnotes below *Table 6: Voltage characteristics on page 32* and *Table 7: Current characteristics on page 33* Updated tw min in *Table 20: High-speed external user clock characteristics on page 46* Updated startup time in *Table 23: LSE oscillator characteristics (f_{LSE} = 32.768 kHz) on page 49* Added *Section 5.3.12: I/O current injection characteristics* Updated *Section 5.3.13: I/O port characteristics*