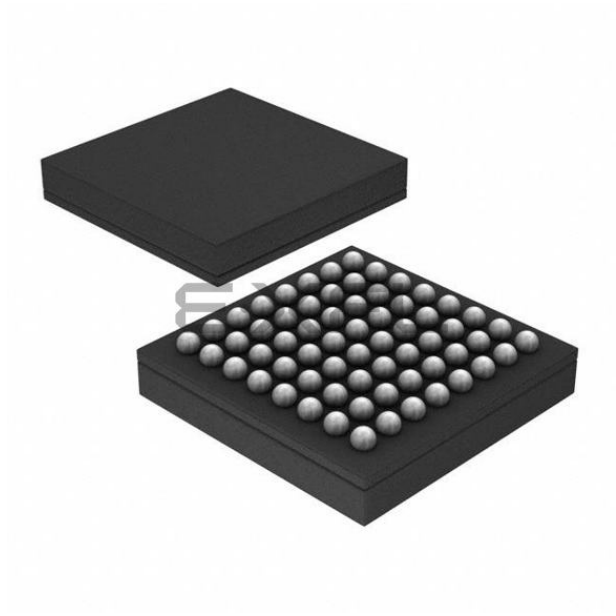

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, Motor Control PWM, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	51
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TFBGA
Supplier Device Package	64-TFBGA (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f103r6h6a

List of figures

2.3.21 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current-capable.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

I/Os on APB2 with up to 18 MHz toggling speed.

2.3.22 ADC (analog-to-digital converter)

Two 12-bit analog-to-digital converters are embedded into STM32F103xx performance line devices and each ADC shares up to 16 external channels, performing conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

- Simultaneous sample and hold
- Interleaved sample and hold
- Single shunt

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TIMx) and the advanced-control timer (TIM1) can be internally connected to the ADC start trigger, injection trigger, and DMA trigger respectively, to allow the application to synchronize A/D conversion and timers.

2.3.23 Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 2 V < V_{DDA} < 3.6 V. The temperature sensor is internally connected to the ADC12_IN16 input channel which is used to convert the sensor output voltage into a digital value.

2.3.24 Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP Interface is embedded. and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target. The JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3 Pinouts and pin description

Figure 3. STM32F103xx performance line LQFP64 pinout

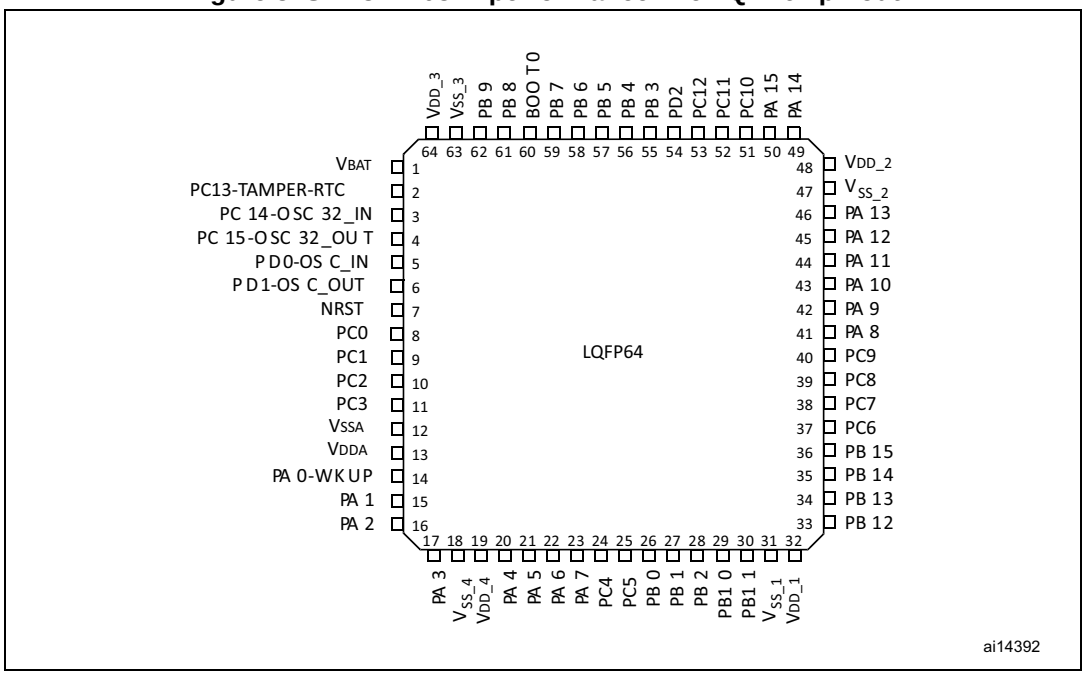


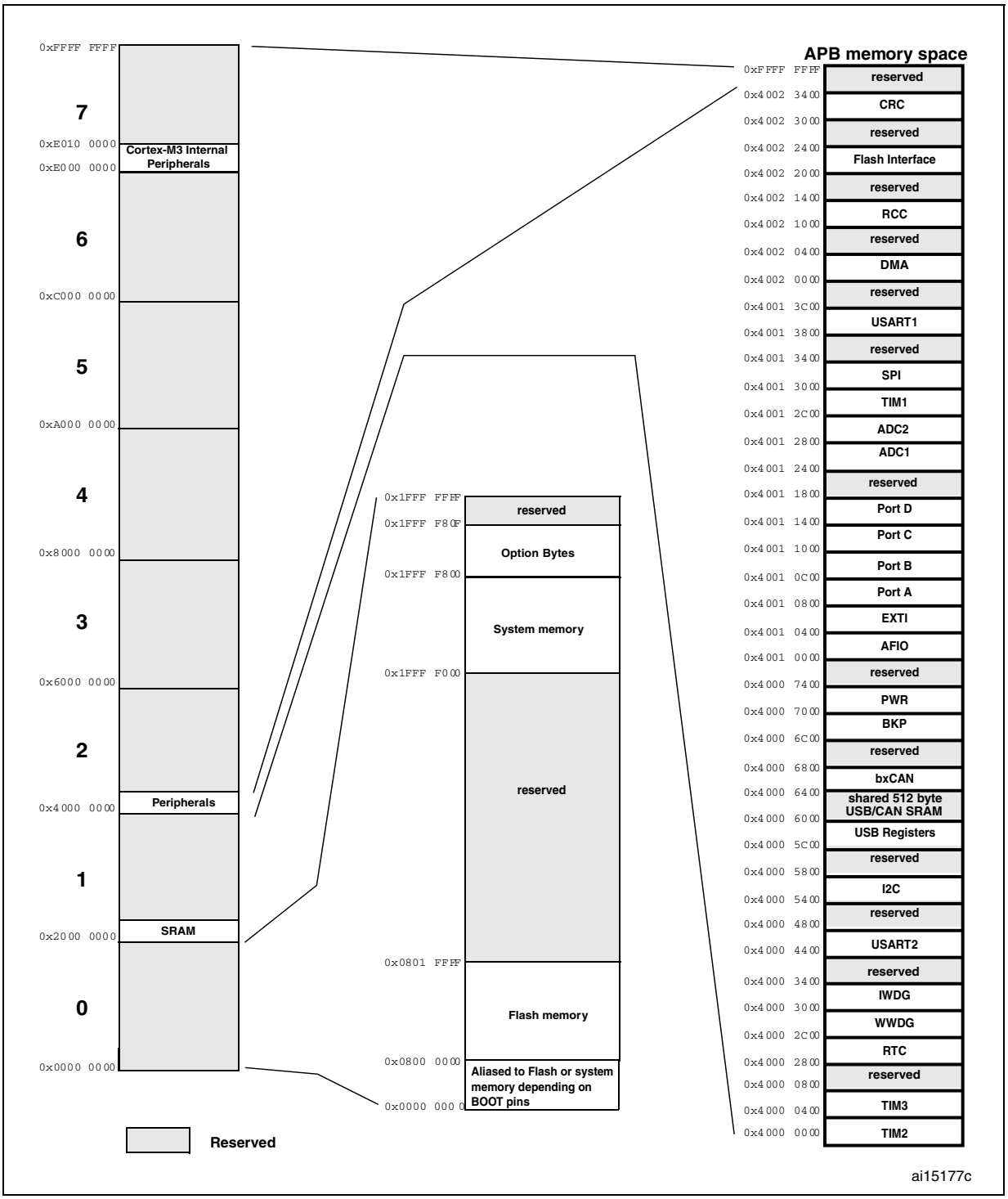
Table 5. Low-density STM32F103xx pin definitions

Pins				Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions(4)	
LQFP48/ UFQFPN48	LQFP64	TFBGA64	VFQFPN36					Default	Remap
1	1	B2	-	V_{BAT}	S	-	V_{BAT}	-	-
2	2	A2	-	PC13-TAMPER-RTC(5)	I/O	-	PC13(6)	TAMPER-RTC	-
3	3	A1	-	PC14-OSC32_IN(5)	I/O	-	PC14(6)	OSC32_IN	-
4	4	B1	-	PC15-OSC32_OUT(5)	I/O	-	PC15(6)	OSC32_OUT	-
5	5	C1	2	OSC_IN	I	-	OSC_IN	-	PD0(7)
6	6	D1	3	OSC_OUT	O	-	OSC_OUT	-	PD1(7)
7	7	E1	4	NRST	I/O	-	NRST		-
-	8	E3	-	PC0	I/O	-	PC0	ADC12_IN10	-
-	9	E2	-	PC1	I/O	-	PC1	ADC12_IN11	-
-	10	F2	-	PC2	I/O	-	PC2	ADC12_IN12	-
-	11	-	-	PC3	I/O	-	PC3	ADC12_IN13	-
-	-	G1	-	V_{REF+}(8)	S	-	V_{REF+}	-	-
8	12	F1	5	V_{SSA}	S	-	V_{SSA}	-	-
9	13	H1	6	V_{DDA}	S	-	V_{DDA}	-	-
10	14	G2	7	PA0-WKUP	I/O	-	PA0	WKUP/USART2_CTS/ ADC12_IN0/ TIM2_CH1_ETR(9)	-
11	15	H2	8	PA1	I/O	-	PA1	USART2_RTS/ ADC12_IN1/ TIM2_CH2(9)	-
12	16	F3	9	PA2	I/O	-	PA2	USART2_TX/ ADC12_IN2/ TIM2_CH3(9)	-
13	17	G3	10	PA3	I/O	-	PA3	USART2_RX/ ADC12_IN3/TIM2_CH4(9)	-
-	18	C2	-	V_{SS_4}	S	-	V_{SS_4}	-	-
-	19	D2	-	V_{DD_4}	S	-	V_{DD_4}	-	-
14	20	H3	11	PA4	I/O	-	PA4	SPI1_NSS(9)/ USART2_CK/ADC12_IN4	-
15	21	F4	12	PA5	I/O	-	PA5	SPI1_SCK(9)/ ADC12_IN5	-
16	22	G4	13	PA6	I/O	-	PA6	SPI1_MISO(9)/ ADC12_IN6/TIM3_CH1(9)	TIM1_BKIN
17	23	H4	14	PA7	I/O	-	PA7	SPI1_MOSI(9)/ ADC12_IN7/TIM3_CH2(9)	TIM1_CH1N
-	24	H5	-	PC4	I/O	-	PC4	ADC12_IN14	-
-	25	H6	-	PC5	I/O	-	PC5	ADC12_IN15	-

4 Memory mapping

The memory map is shown in *Figure 8*.

Figure 8. Memory map



5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.3 V (for the 2 V ≤ V_{DD} ≤ 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 9*.

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 10*.

Table 9. General operating conditions (continued)

Symbol	Parameter	Conditions		Min	Max	Unit
V_{IN}	I/O input voltage	Standard IO		–0.3	V_{DD}+ 0.3	V
		FT IO(3)	2 V < V_{DD} ≤ 3.6 V	–0.3	5.5	
			V_{DD} = 2 V	–0.3	5.2	
		BOOT0		0	5.5	
P_D	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7(4)	TFBGA64		-	308	mW
		LQFP64		-	444	
		LQFP48		-	363	
		UFQFPN48		-	624	
		VFQFPN36		-	1000	
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation		–40	85	°C
		Low power dissipation(5)		–40	105	
	Ambient temperature for 7 suffix version	Maximum power dissipation		–40	105	
		Low power dissipation(5)		–40	125	
T_J	Junction temperature range	6 suffix version		–40	105	
		7 suffix version		–40	125	

1. When the ADC is used, refer to *Table 46: ADC characteristics*.
2. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and operation.
3. To sustain a voltage higher than V_{DD}+0.3 V, the internal pull-up/pull-down resistors must be disabled.
4. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed $T_J$max (see *Table 6.6: Thermal characteristics on page 92*).
5. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed $T_J$max (see *Table 6.6: Thermal characteristics on page 92*).

5.3.2 Operating conditions at power-up / power-down

Subject to general operating conditions for T_A.

Table 10. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	¥	µs/V
	V_{DD} fall time rate		20	¥	

5.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 11* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 15. Maximum current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Max(1)		Unit
				T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Sleep mode	External clock(2), all peripherals enabled	72 MHz	26	27	mA
			48 MHz	17	18	
			36 MHz	14	15	
			24 MHz	10	11	
			16 MHz	7	8	
			8 MHz	4	5	
		External clock(2), all peripherals disabled	72 MHz	7.5	8	
			48 MHz	6	6.5	
			36 MHz	5	5.5	
			24 MHz	4.5	5	
			16 MHz	4	4.5	
			8 MHz	3	4	

1. based on characterization, tested in production at $V_{DD\ max}$, f_{HCLK} max with peripherals enabled.
2. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 17. Typical current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1)		Unit
				All peripherals enabled(2)	All peripherals disabled	
I_{DD}	Supply current in Run mode	External clock(3)	72 MHz	31.3	24.5	mA
			48 MHz	21.9	17.4	
			36 MHz	17.2	13.8	
			24 MHz	11.2	8.9	
			16 MHz	8.1	6.6	
			8 MHz	5	4.2	
			4 MHz	3	2.6	
			2 MHz	2	1.8	
			1 MHz	1.5	1.4	
			500 kHz	1.2	1.2	
			125 kHz	1.05	1	
		Running on high speed internal RC (HSI), AHB prescaler used to reduce the frequency	64 MHz	27.6	21.6	mA
			48 MHz	21.2	16.7	
			36 MHz	16.5	13.1	
			24 MHz	10.5	8.2	
			16 MHz	7.4	5.9	
			8 MHz	4.3	3.6	
			4 MHz	2.4	2	
			2 MHz	1.5	1.3	
			1 MHz	1	0.9	
			500 kHz	0.7	0.65	
			125 kHz	0.5	0.45	

1. Typical values are measures at T_A = 25 °C, V_{DD} = 3.3 V.
2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 18. Typical current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1)		Unit
				All peripherals enabled(2)	All peripherals disabled	
I_{DD}	Supply current in Sleep mode	External clock(3)	72 MHz	12.6	5.3	mA
			48 MHz	8.7	3.8	
			36 MHz	6.7	3.1	
			24 MHz	4.8	2.3	
			16 MHz	3.4	1.8	
			8 MHz	2	1.2	
			4 MHz	1.5	1.1	
			2 MHz	1.25	1	
			1 MHz	1.1	0.98	
			500 kHz	1.05	0.96	
			125 kHz	1	0.95	
		Running on high speed internal RC (HSI), AHB prescaler used to reduce the frequency	64 MHz	10.6	4.2	
			48 MHz	8.1	3.2	
			36 MHz	6.1	2.5	
			24 MHz	4.2	1.7	
			16 MHz	2.8	1.2	
			8 MHz	1.4	0.55	
			4 MHz	0.9	0.5	
			2 MHz	0.7	0.45	
			1 MHz	0.55	0.42	
			500 kHz	0.48	0.4	
			125 kHz	0.4	0.38	

1. Typical values are measures at T_A = 25 °C, V_{DD} = 3.3 V.
2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Low-speed internal (LSI) RC oscillator

Table 25. LSI oscillator characteristics (1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}(2)	Frequency	30	40	60	kHz
$t_{su(LSI)}$(3)	LSI oscillator startup time	-	-	85	µs
$I_{DD(LSI)}$(3)	LSI oscillator power consumption	-	0.65	1.2	µA

1. V_{DD} = 3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Based on characterization, not tested in production.
3. Guaranteed by design, not tested in production.

Wakeup time from low-power mode

The wakeup times given in *Table 26* is measured on a wakeup phase with a 8-MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode.

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 30. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 72 MHz conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, T_A = +25 °C, f_{HCLK} = 72 MHz conforms to IEC 61000-4-4	4A

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

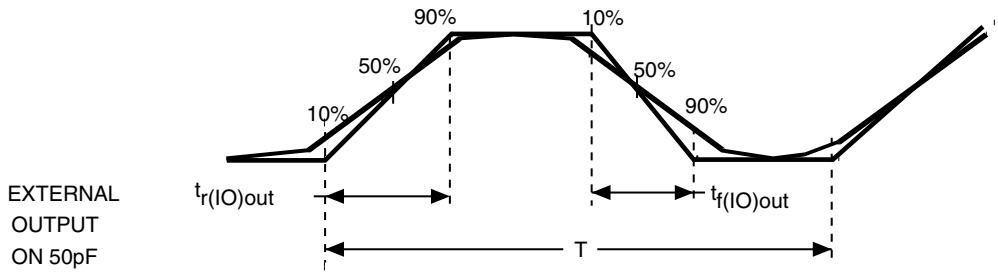
Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 31. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]		Unit
				8/48 MHz	8/72 MHz	
S_{EMI}	Peak level	V_{DD} = 3.3 V, T_A = 25 °C	0.1 to 30 MHz	12	12	dBµV
			30 to 130 MHz	22	19	
			130 MHz to 1GHz	23	29	
			SAE EMI Level	4	4	-

Figure 27. I/O AC characteristics definition



Maximum frequency is achieved if $(t_r + t_f) \leq 2/3)T$ and if the duty cycle is (45-55%)
when loaded by 50pF

5.3.14 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 35*).

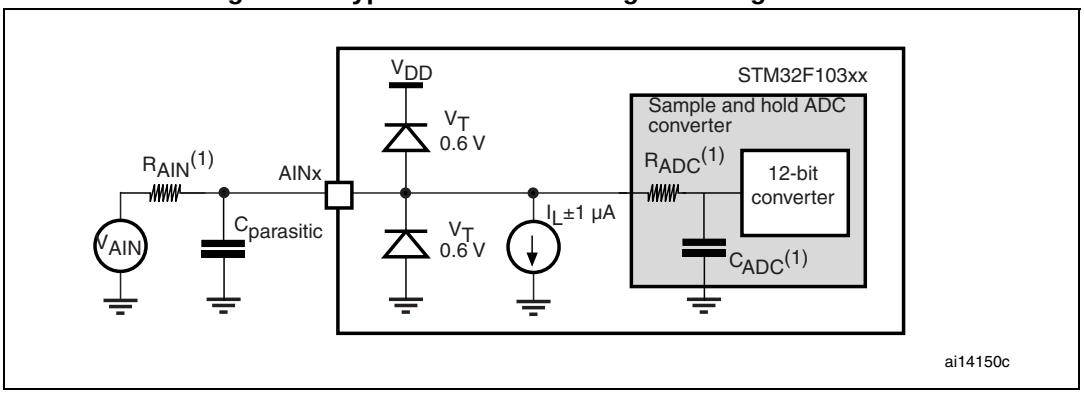
Unless otherwise specified, the parameters given in *Table 38* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 38. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST Input low level voltage	-	–0.5	-	0.8	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage	-	2	-	V_{DD}+0.5	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$(1)	NRST Input filtered pulse	-	-	-	100	ns
$V_{NF(NRST)}$(1)	NRST Input not filtered pulse	-	300	-	-	ns

1. Guaranteed by design, not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

Figure 35. Typical connection diagram using the ADC

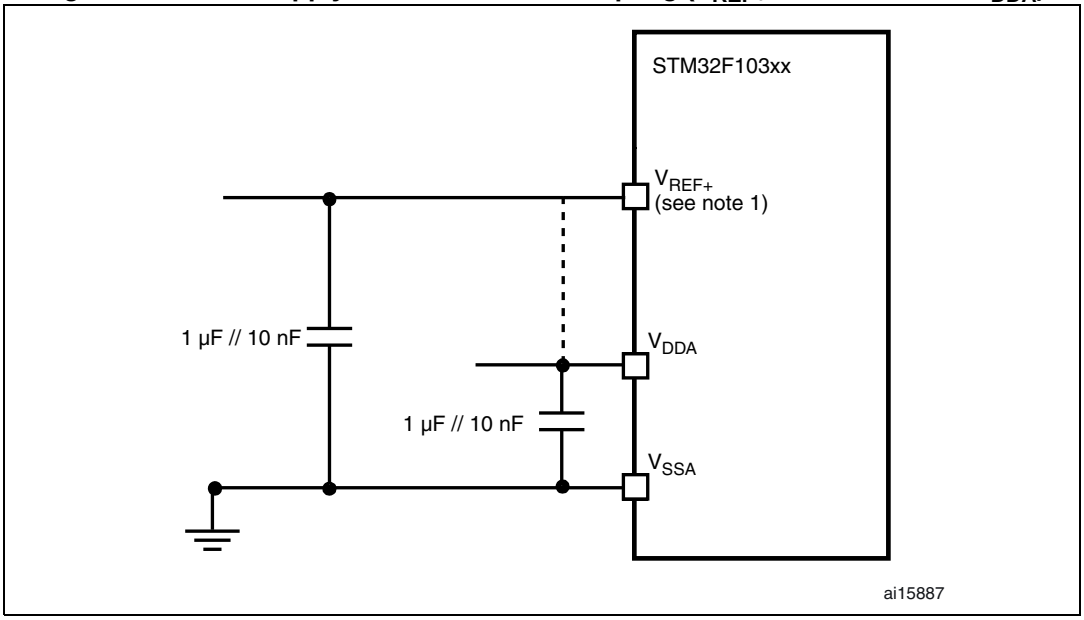


1. Refer to *Table 46* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

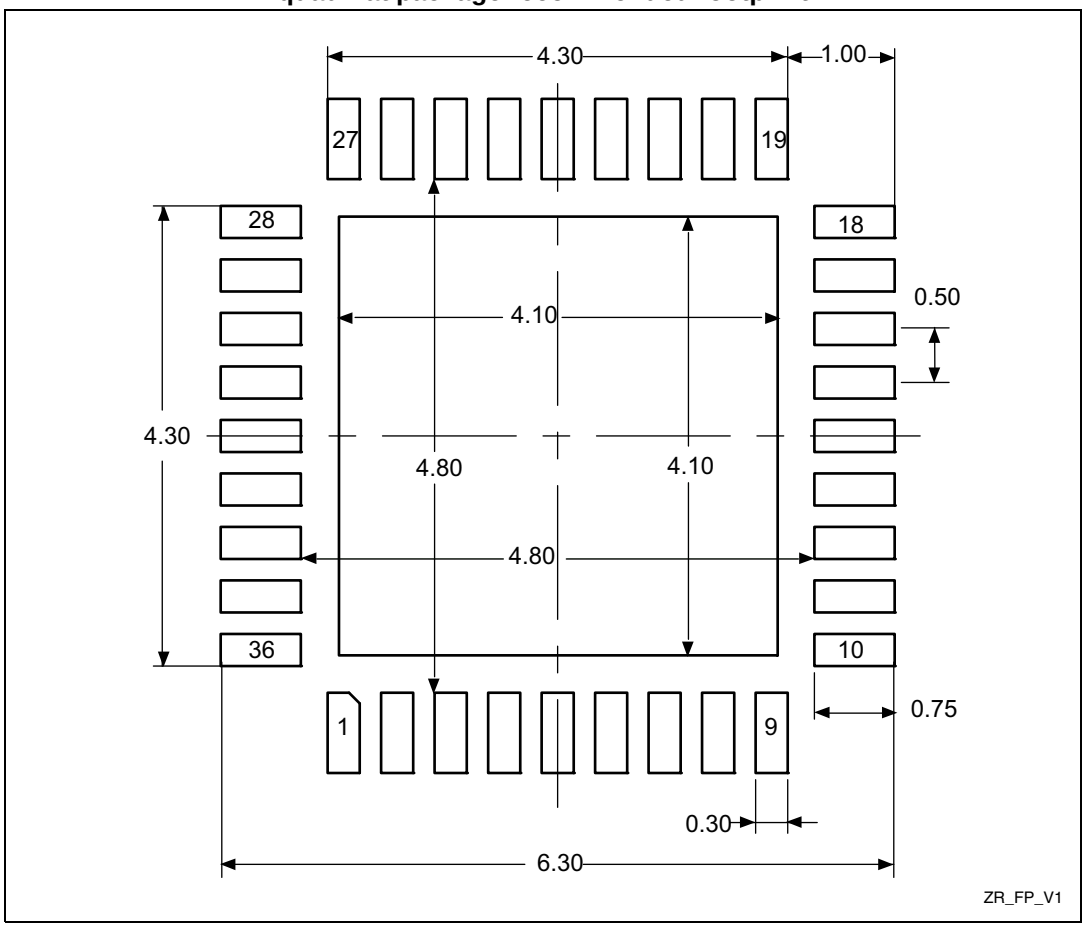
Power supply decoupling should be performed as shown in*Figure 36* or *Figure 37*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

Figure 36. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



1. The V_{REF+} input is available only on the TFBGA64 package.

Figure 39. VFQFPN36 - 36-pin, 6x6 mm, 0.5 mm pitch very thin profile fine pitch quad flat package recommended footprint

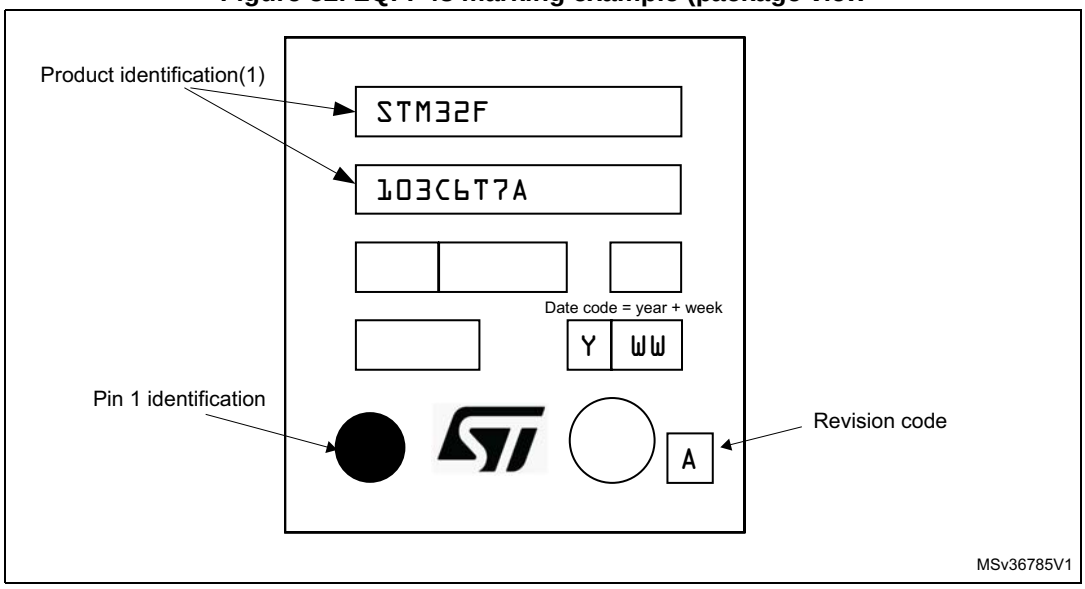


1. Dimensions are expressed in millimeters.

Device Marking for LQFP48

The following figure gives an example of topside marking orientation versus ball 1 identifier location.

Figure 52. LQFP48 marking example (package view



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7 Ordering information scheme

Table 58. Ordering information scheme

Example: STM32 F 103 C 4 T 7 A xxx

Device family

STM32 = ARM®-based 32-bit microcontroller

Product type

F = general-purpose

Device subfamily

103 = performance line

Pin count

T = 36 pins

C = 48 pins

R = 64 pins

Flash memory size

4 = 16 Kbytes of Flash memory

6 = 32 Kbytes of Flash memory

Package

H = BGA

T = LQFP

U = VFQFPN or UFQFPN

Temperature range

6 = Industrial temperature range, –40 to 85 °C.

7 = Industrial temperature range, –40 to 105 °C.

Internal code

“A” or blank

Options

xxx = programmed parts

TR = tape and real

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.