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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, Motor Control PWM, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	51
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f103r6t6

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2 Description

The STM32F103x4 and STM32F103x6 performance line family incorporates the high-performance ARM® Cortex™-M3 32-bit RISC core operating at a 72 MHz frequency, high-speed embedded memories (Flash memory up to 32 Kbytes and SRAM up to 6 Kbytes), and an extensive range of enhanced I/Os and peripherals connected to two APB buses. All devices offer two 12-bit ADCs, three general purpose 16-bit timers plus one PWM timer, as well as standard and advanced communication interfaces: up to two I²Cs and SPIs, three USARTs, an USB and a CAN.

The STM32F103xx low-density performance line family operates from a 2.0 to 3.6 V power supply. It is available in both the –40 to +85 °C temperature range and the –40 to +105 °C extended temperature range. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F103xx low-density performance line family includes devices in four different package types: from 36 pins to 64 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

These features make the STM32F103xx low-density performance line microcontroller family suitable for a wide range of applications such as motor drives, application control, medical and handheld equipment, PC and gaming peripherals, GPS platforms, industrial applications, PLCs, inverters, printers, scanners, alarm systems, video intercoms, and HVACs.

2.1 Device overview

Table 2. STM32F103xx low-density device features and peripheral counts

Peripheral		STM32F103Tx		STM32F103Cx		STM32F103Rx	
Flash - Kbytes		16	32	16	32	16	32
SRAM - Kbytes		6	10	6	10	6	10
Timers	General-purpose	2	2	2	2	2	2
	Advanced-control	1		1		1	
Communication	SPI	1	1	1	1	1	1
	I ² C	1	1	1	1	1	1
	USART	2	2	2	2	2	2
	USB	1	1	1	1	1	1
	CAN	1	1	1	1	1	1
GPIOs		26		37		51	
12-bit synchronized ADC Number of channels		2 10 channels		2 10 channels		2 16 channels ⁽¹⁾	
CPU frequency		72 MHz					
Operating voltage		2.0 to 3.6 V					
Operating temperatures		Ambient temperatures: −40 to +85 °C /−40 to +105 °C (see Table 9) Junction temperature: −40 to + 125 °C (see Table 9)					
Packages		VFQFPN36		LQFP48, UFQFPN48		LQFP64, TFBGA64	

1. On the TFBGA64 package only 15 channels are available (one analog input pin has been replaced by 'Vref+').

SysTick timer

This timer is dedicated for OS, but could also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

2.3.16 I²C bus

The I²C bus interface can operate in multimaster and slave modes. It can support standard and fast modes.

It supports dual slave addressing (7-bit only) and both 7/10-bit addressing in master mode. A hardware CRC generation/verification is embedded.

It can be served by DMA and they support SM Bus 2.0/PM Bus.

2.3.17 Universal synchronous/asynchronous receiver transmitter (USART)

One of the USART interfaces is able to communicate at speeds of up to 4.5 Mbit/s. The other available interface communicates at up to 2.25 Mbit/s. They provide hardware management of the CTS and RTS signals, IrDA SIR ENDEC support, are ISO 7816 compliant and have LIN Master/Slave capability.

All USART interfaces can be served by the DMA controller.

2.3.18 Serial peripheral interface (SPI)

The SPI interface is able to communicate up to 18 Mbits/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

The SPI interface can be served by the DMA controller.

2.3.19 Controller area network (CAN)

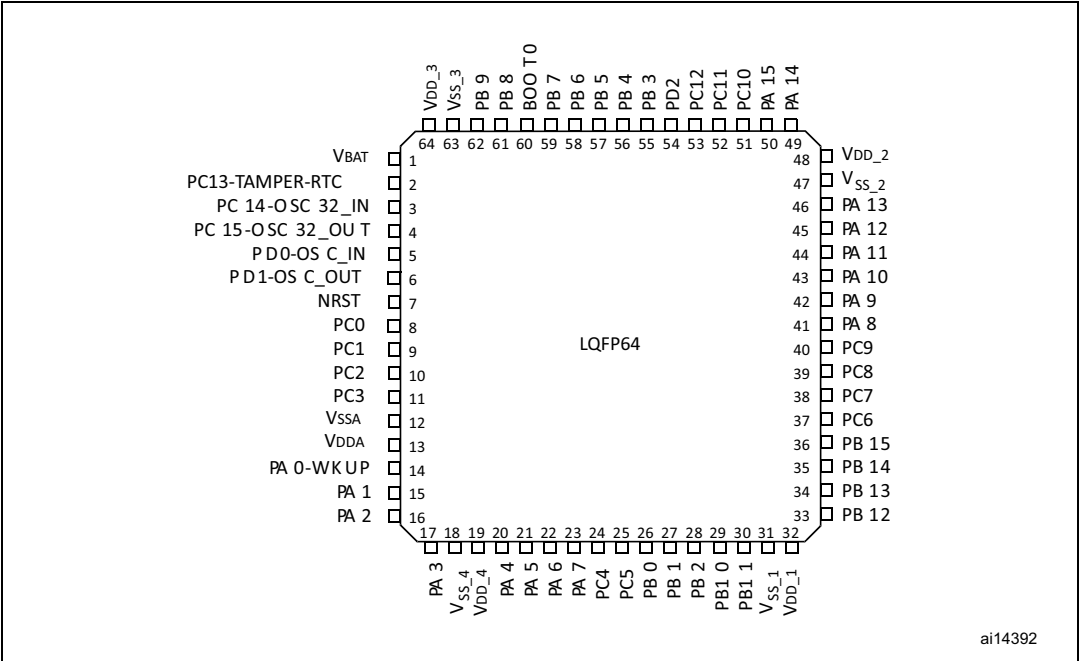
The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

2.3.20 Universal serial bus (USB)

The STM32F103xx performance line embeds a USB device peripheral compatible with the USB full-speed 12 Mbs. The USB interface implements a full-speed (12 Mbit/s) function interface. It has software-configurable endpoint setting and suspend/resume support. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator).

3 Pinouts and pin description

Figure 3. STM32F103xx performance line LQFP64 pinout



On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in [Table 19](#). The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
 - with all peripherals clocked off
 - with only one peripheral clocked on
- ambient operating temperature and V_{DD} supply voltage conditions summarized in [Table 6](#)

Table 19. Peripheral current consumption⁽¹⁾

Peripheral		Typical consumption at 25 °C	Unit
AHB (up to 72MHz)	DMA1	15.97	μA/MHz
	CRC	1.67	
	BusMatrix ⁽²⁾	8.33	
APB1(up to 36MHz)	APB1 Bridge	7.22	μA/MHz
	TIM2	33.33	
	TIM3	33.61	
	USART2	12.78	
	I2C1	10.83	
	USB	16.94	
	CAN1	17.50	
	WWDG	3.33	
	PWR	1.94	
	BKP	2.78	
	IWDG	1.39	
APB2 (up to 72MHz)	APB2-Bridge	3.33	μA/MHz
	GPIO A	7.50	
	GPIO B	6.81	
	GPIO C	7.22	
	GPIO D	6.94	
	ADC1 ⁽³⁾ (4)	15.54	
	ADC2	14.64	
	TIM1	21.53	
	SPI	4.86	
	USART1	12.78	

1. $f_{HCLK} = 72\text{ MHz}$, $f_{APB1} = f_{HCLK}/2$, $f_{APB2} = f_{HCLK}$, default prescaler value for each peripheral.

2. The BusMatrix is automatically active when at least one master is ON.

3. Specific conditions for ADC: $f_{HCLK} = 56\text{ MHz}$, $f_{APB1} = f_{HCLK}/2$, $f_{APB2} = f_{HCLK}$, $f_{ADCCLK} = f_{APB2}/4$. When ADON bit in the ADC_CR2 register is set to 1, we have a consumption added equal to 0.68 mA.

4. When we enable the ADC, a current consumption is added equal to 0,06 mA.

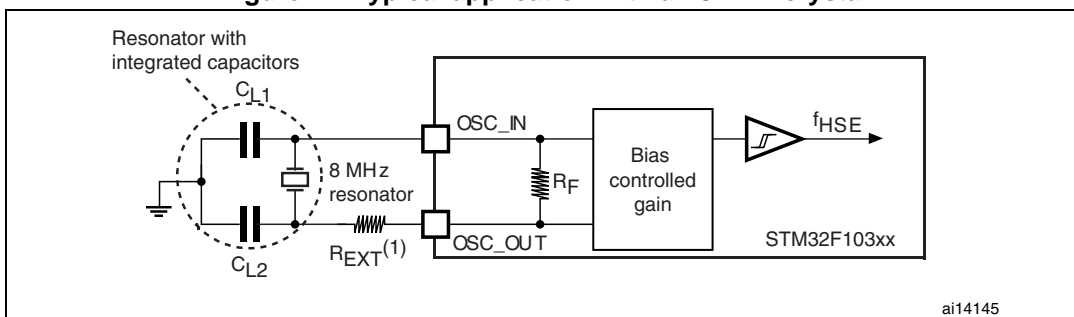
Table 22. HSE 4-16 MHz oscillator characteristics^{(1) (2)}

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	16	MHz
R_F	Feedback resistor	-	-	200	-	k Ω
C	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S) ⁽³⁾	$R_S = 30 \Omega$	-	30	-	pF
i_2	HSE driving current	$V_{DD} = 3.3 V$, $V_{IN} = V_{SS}$ with 30 pF load	-	-	1	mA
g_m	Oscillator transconductance	Startup	25	-	-	mA/V
$t_{SU(HSE)}$ ⁽⁴⁾	startup time	V_{DD} is stabilized	-	2	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Based on characterization, not tested in production.
3. The relatively low value of the RF resistor offers a good protection against issues resulting from use in a humid environment, due to the induced leakage and the bias condition change. However, it is recommended to take this point into account if the MCU is used in tough humidity conditions.
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2} , it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see [Figure 21](#)). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2} . PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2} . Refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 21. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in [Table 23](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization

5.3.12 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DD} (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of spec current injection on adjacent pins or other functional failure (for example reset, oscillator frequency deviation).

The test results are given in [Table 34](#)

Table 34. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on OSC_IN32, OSC_OUT32, PA4, PA5, PC13	-0	+0	mA
	Injected current on all FT pins	-5	+0	
	Injected current on any other pin	-5	+5	

5.3.13 I/O port characteristics

General input/output characteristics

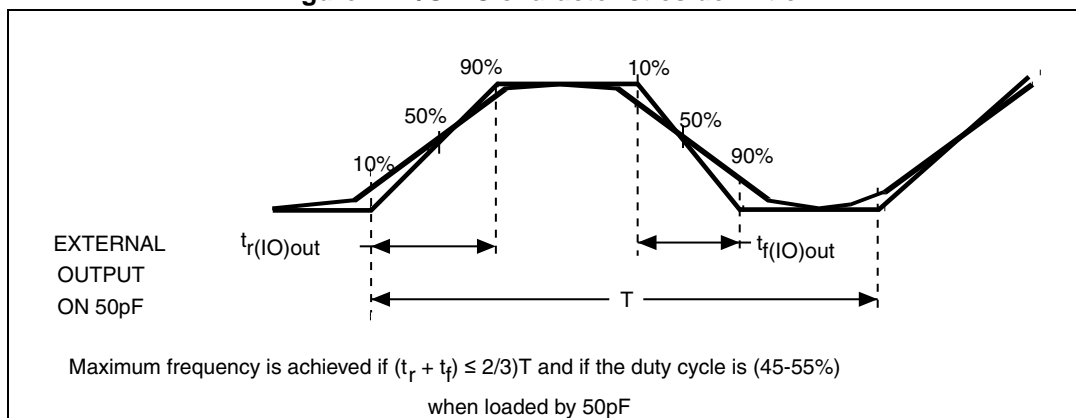
Unless otherwise specified, the parameters given in [Table 35](#) are derived from tests performed under the conditions summarized in [Table 9](#). All I/Os are CMOS and TTL compliant.

Table 35. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage	Standard IO input low level voltage	-	-	$0.28 \cdot (V_{DD} - 2 \text{ V}) + 0.8 \text{ V}^{(1)}$	V
		IO FT ⁽³⁾ input low level voltage	-	-	$0.32 \cdot (V_{DD} - 2 \text{ V}) + 0.75 \text{ V}^{(1)}$	
		All I/Os except BOOT0	-	-	$0.35 V_{DD}^{(2)}$	
V_{IH}	High level input voltage	Standard IO input high level voltage	$0.41 \cdot (V_{DD} - 2 \text{ V}) + 1.3 \text{ V}^{(1)}$	-	-	V
		IO FT ⁽³⁾ input high level voltage	$0.42 \cdot (V_{DD} - 2 \text{ V}) + 1 \text{ V}^{(1)}$	-	-	
		All I/Os except BOOT0	$0.65 V_{DD}^{(2)}$	-	-	
V_{hys}	Standard IO Schmitt trigger voltage hysteresis ⁽⁴⁾	-	200	-	-	mV
	IO FT Schmitt trigger voltage hysteresis ⁽⁴⁾	-	$5\% V_{DD}^{(5)}$	-	-	
I_{lkg}	Input leakage current ⁽⁶⁾	$V_{SS} \leq V_{IN} \leq V_{DD}$ Standard I/Os	-	-	± 1	μA
		$V_{IN} = 5 \text{ V}$ I/O FT	-	-	3	
R_{PU}	Weak pull-up equivalent resistor ⁽⁷⁾	$V_{IN} = V_{SS}$	30	40	50	$k\Omega$
R_{PD}	Weak pull-down equivalent resistor ⁽⁷⁾	$V_{IN} = V_{DD}$	30	40	50	
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Data based on design simulation.
2. Tested in production.
3. FT = Five-volt tolerant. In order to sustain a voltage higher than $V_{DD} + 0.3$ the internal pull-up/pull-down resistors must be disabled.
4. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization, not tested in production.
5. With a minimum of 100 mV.
6. Leakage could be higher than max. if negative current is injected on adjacent pins.
7. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimum (~10% order).

Figure 27. I/O AC characteristics definition



5.3.14 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see [Table 35](#)).

Unless otherwise specified, the parameters given in [Table 38](#) are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in [Table 9](#).

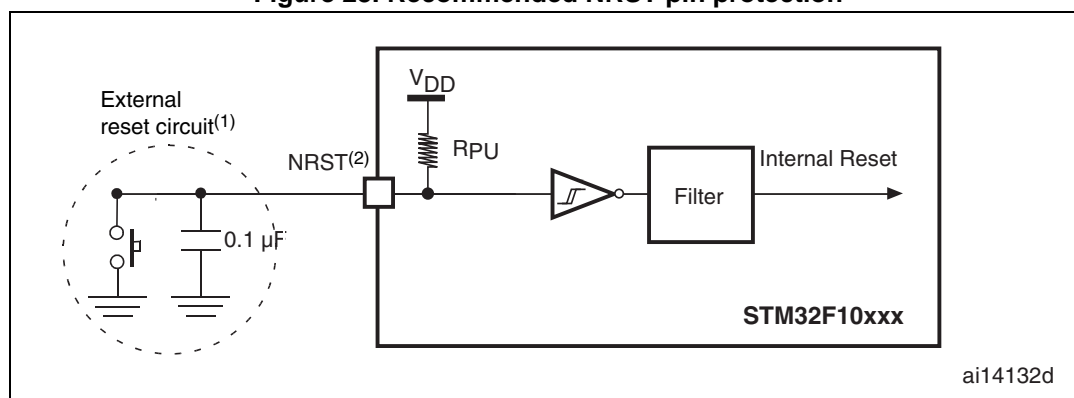
Table 38. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}^{(1)}$	NRST Input low level voltage	-	-0.5	-	0.8	V
$V_{IH(NRST)}^{(1)}$	NRST Input high level voltage	-	2	-	$V_{DD}+0.5$	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor ⁽²⁾	$V_{IN} = V_{SS}$	30	40	50	k Ω
$V_{F(NRST)}^{(1)}$	NRST Input filtered pulse	-	-	-	100	ns
$V_{NF(NRST)}^{(1)}$	NRST Input not filtered pulse	-	300	-	-	ns

1. Guaranteed by design, not tested in production.

2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

Figure 28. Recommended NRST pin protection



2. The reset network protects the device against parasitic resets.
3. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in [Table 38](#). Otherwise the reset will not be taken into account by the device.

5.3.15 TIM timer characteristics

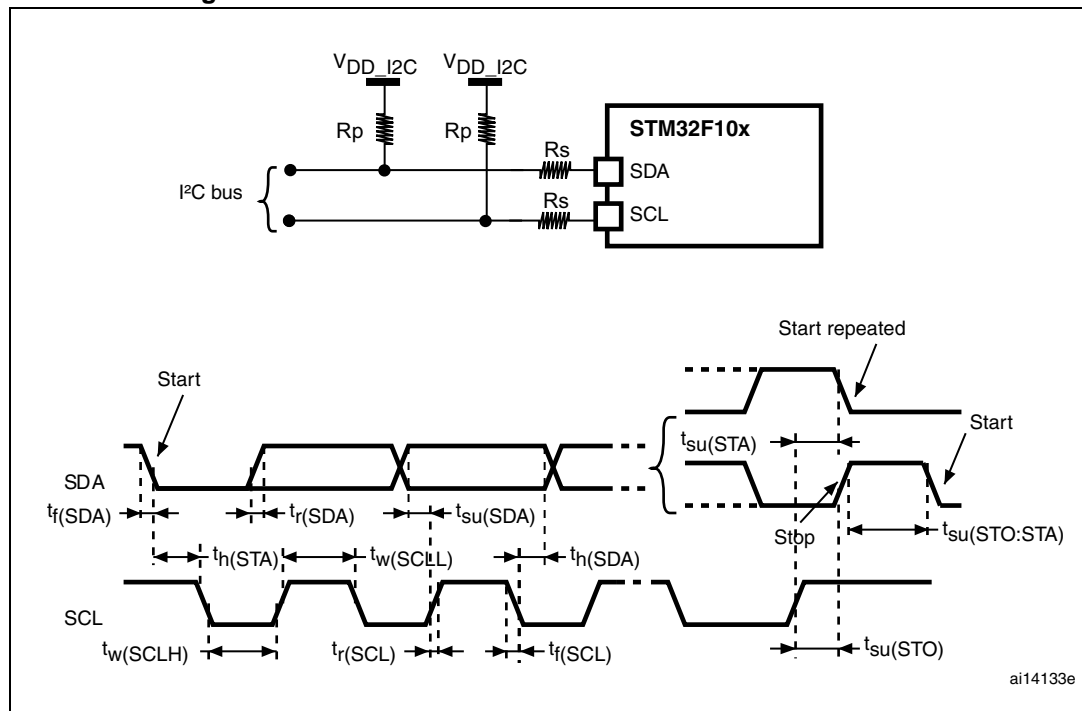
The parameters given in [Table 39](#) are guaranteed by design.

Refer to [Section 5.3.12: I/O current injection characteristics](#) for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 39. TIMx⁽¹⁾ characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 72 \text{ MHz}$	13.9	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK} = 72 \text{ MHz}$	0	36	MHz
Res_{TIM}	Timer resolution	-	-	16	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 72 \text{ MHz}$	0.0139	910	μs
t_{MAX_COUNT}	Maximum possible count	-	-	65536×65536	$t_{TIMxCLK}$
		$f_{TIMxCLK} = 72 \text{ MHz}$	-	59.6	s

1. TIMx is used as a general term to refer to the TIM1, TIM2, TIM3 and TIM4 timers.

Figure 29. I²C bus AC waveforms and measurement circuit

1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.
2. R_s = Series protection resistors, R_p = Pull-up resistors, V_{DD_I2C} = I2C bus supply.

Table 41. SCL frequency ($f_{CLK1} = 36 \text{ MHz}$, $V_{DD_I2C} = 3.3 \text{ V}$)⁽¹⁾⁽²⁾

f_{SCL} (kHz)	I2C_CCR value
	$R_p = 4.7 \text{ k}\Omega$
400	0x801E
300	0x8028
200	0x803C
100	0x00B4
50	0x0168
20	0x0384

1. R_p = External pull-up resistance, f_{SCL} = I²C speed,
2. For speeds around 200 kHz, the tolerance on the achieved speed is of $\pm 5\%$. For other speed ranges, the tolerance on the achieved speed $\pm 2\%$. These variations depend on the accuracy of the external components used to design the application.

Table 51. VFQFPN36 - 36-pin, 6x6 mm, 0.5 mm pitch very thin profile fine pitch quad flat package mechanical data

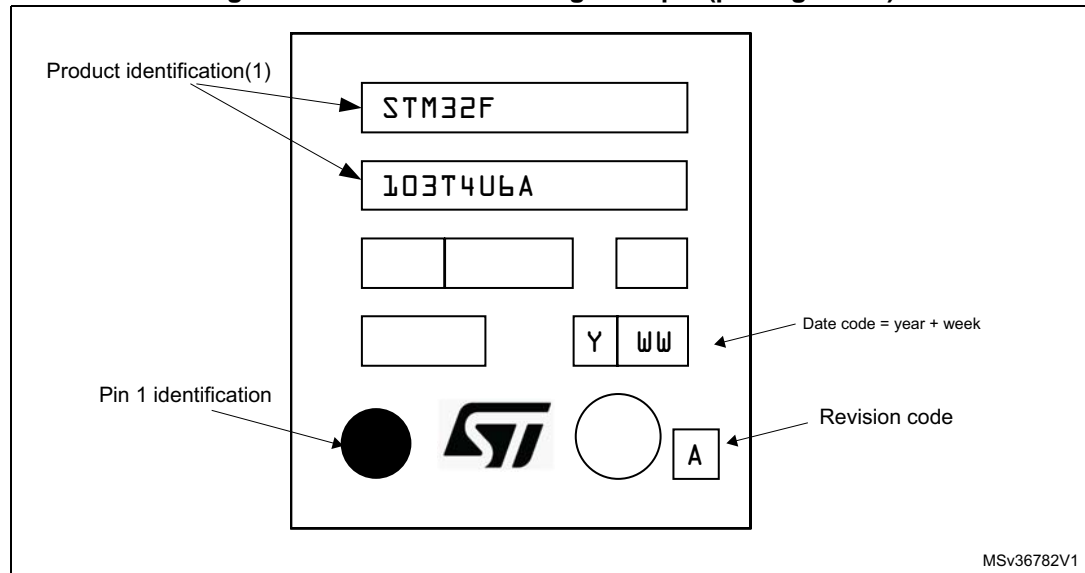
Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	0.800	0.900	1.000	0.0315	0.0354	0.0394
A1	-	0.020	0.050	-	0.0008	0.0020
A2	-	0.650	1.000	-	0.0256	0.0394
A3	-	0.200	-	-	0.0079	-
b	0.180	0.230	0.300	0.0071	0.0091	0.0118
D	5.875	6.000	6.125	0.2313	0.2362	0.2411
D2	1.750	3.700	4.250	0.0689	0.1457	0.1673
E	5.875	6.000	6.125	0.2313	0.2362	0.2411
E2	1.750	3.700	4.250	0.0689	0.1457	0.1673
e	0.450	0.500	0.550	0.0177	0.0197	0.0217
L	0.350	0.550	0.750	0.0138	0.0217	0.0295
K	0.250	-	-	0.0098	-	-
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Device Marking for VFQFPN36

The following figure gives an example of topside marking orientation versus ball 1 identifier location.

Figure 40. VFQFPN36 marking example (package view)

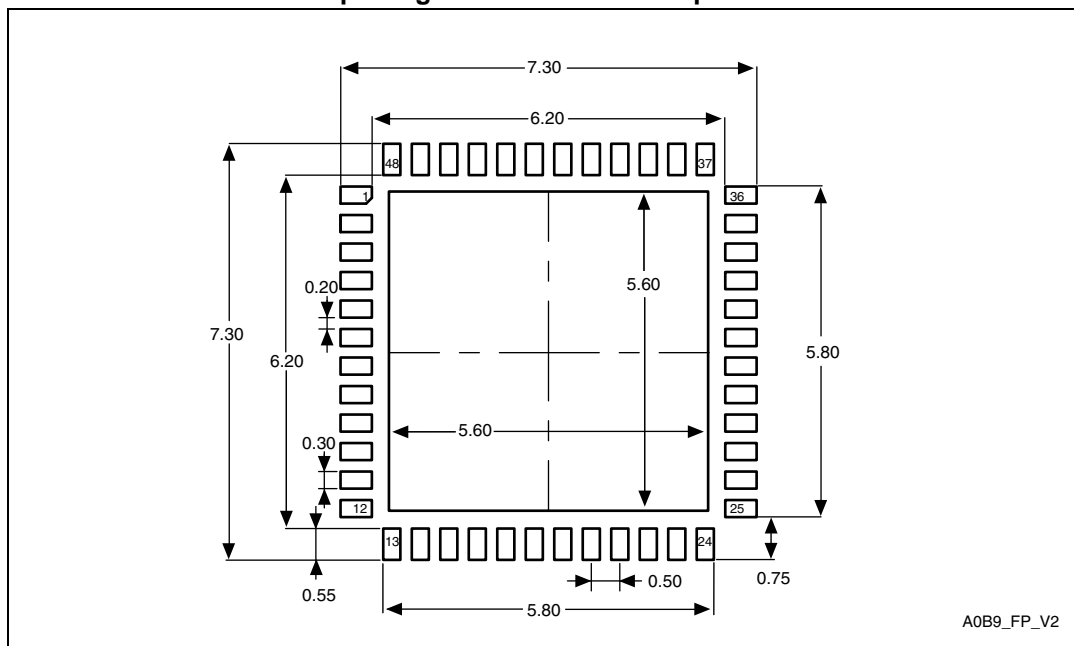


1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 52. UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

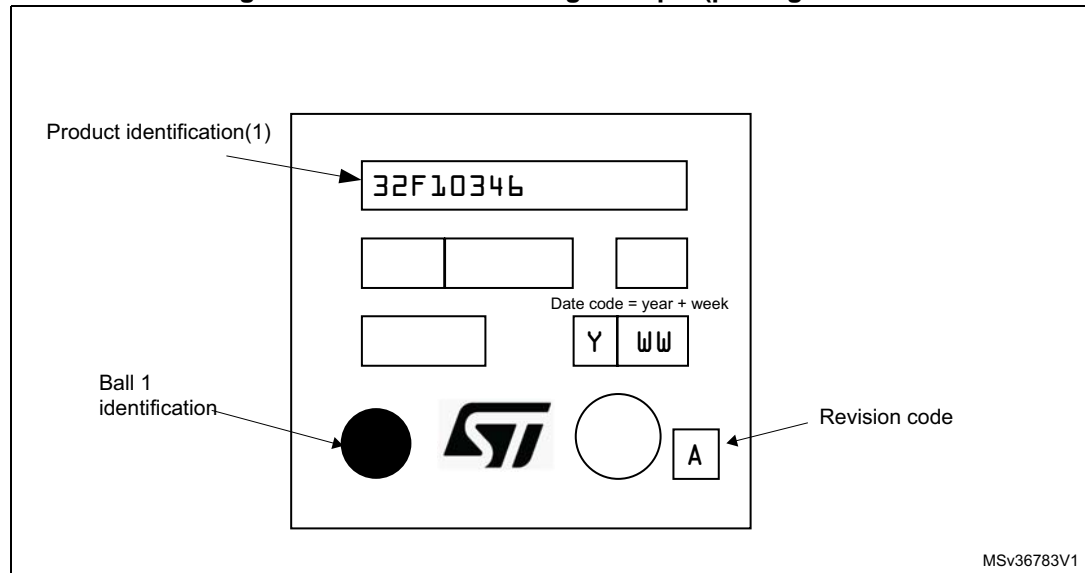
Figure 42. UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package recommended footprint

1. Dimensions are expressed in millimeters.

Device Marking for TFBGA64

The following figure gives an example of topside marking orientation versus ball 1 identifier location.

Figure 49. TFBGA64 marking example (package view)



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