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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, Motor Control PWM, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	51
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f103r6t7a

2 Description

The STM32F103x4 and STM32F103x6 performance line family incorporates the high-performance ARM® Cortex™-M3 32-bit RISC core operating at a 72 MHz frequency, high-speed embedded memories (Flash memory up to 32 Kbytes and SRAM up to 6 Kbytes), and an extensive range of enhanced I/Os and peripherals connected to two APB buses. All devices offer two 12-bit ADCs, three general purpose 16-bit timers plus one PWM timer, as well as standard and advanced communication interfaces: up to two I^2Cs and SPIs, three USARTs, an USB and a CAN.

The STM32F103xx low-density performance line family operates from a 2.0 to 3.6 V power supply. It is available in both the –40 to +85 °C temperature range and the –40 to +105 °C extended temperature range. A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F103xx low-density performance line family includes devices in four different package types: from 36 pins to 64 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

These features make the STM32F103xx low-density performance line microcontroller family suitable for a wide range of applications such as motor drives, application control, medical and handheld equipment, PC and gaming peripherals, GPS platforms, industrial applications, PLCs, inverters, printers, scanners, alarm systems, video intercoms, and HVACs.

2.1 Device overview

Table 2. STM32F103xx low-density device features and peripheral counts

Peripheral		STM32F103Tx		STM32F103Cx		STM32F103Rx	
Flash - Kbytes		16	32	16	32	16	32
SRAM - Kbytes		6	10	6	10	6	10
Timers	General-purpose	2	2	2	2	2	2
	Advanced-control	1		1		1	
Communication	SPI	1	1	1	1	1	1
	I^2C	1	1	1	1	1	1
	USART	2	2	2	2	2	2
	USB	1	1	1	1	1	1
	CAN	1	1	1	1	1	1
GPIOs		26		37		51	
12-bit synchronized ADC Number of channels		2 10 channels		2 10 channels		2 16 channels(1)	
CPU frequency		72 MHz					
Operating voltage		2.0 to 3.6 V					
Operating temperatures		Ambient temperatures: –40 to +85 °C /–40 to +105 °C (see *Table 9*) Junction temperature: –40 to + 125 °C (see *Table 9*)					
Packages		VFQFPN36		LQFP48, UFQFPN48		LQFP64, TFBGA64	

1. On the TFBGA64 package only 15 channels are available (one analog input pin has been replaced by ‘Vref+’).

3 Pinouts and pin description

Figure 3. STM32F103xx performance line LQFP64 pinout

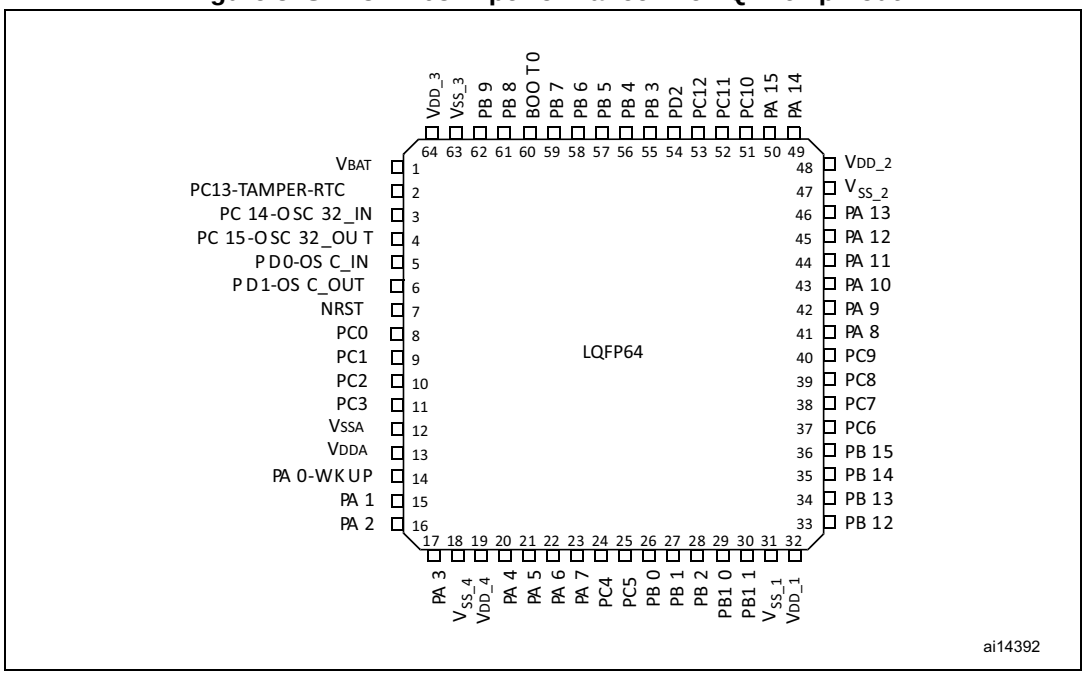


Figure 5. STM32F103xx performance line LQFP48 pinout

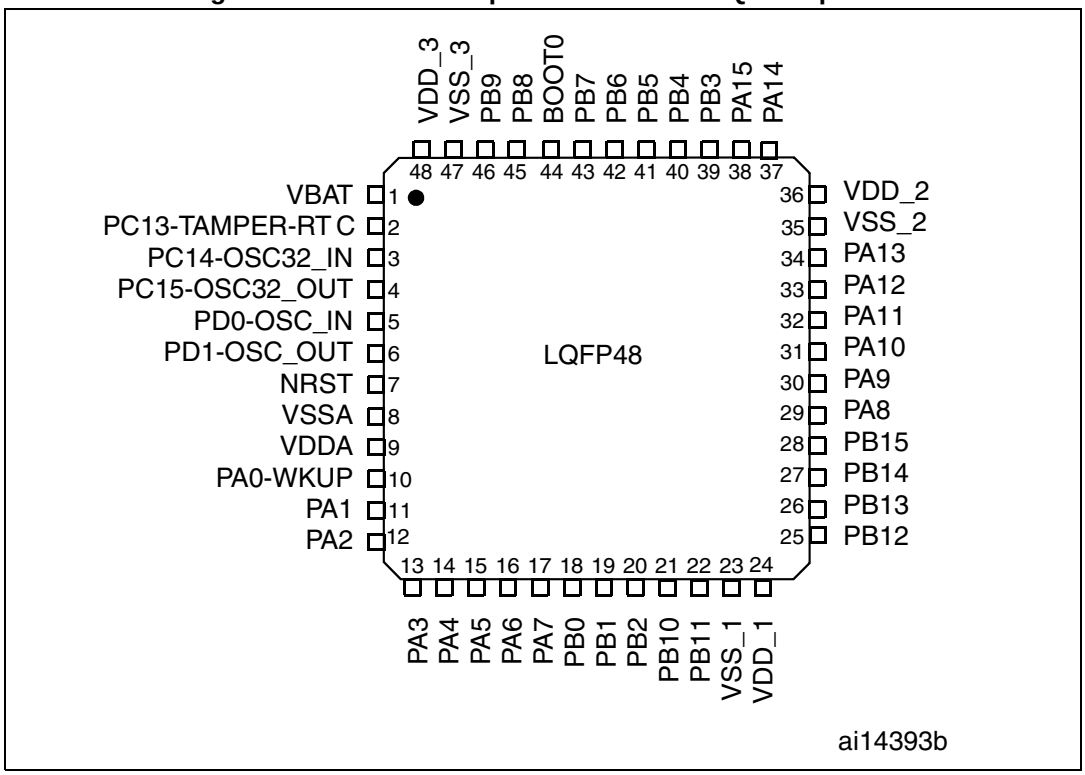


Figure 6. STM32F103xx performance line UFQFPN48 pinout

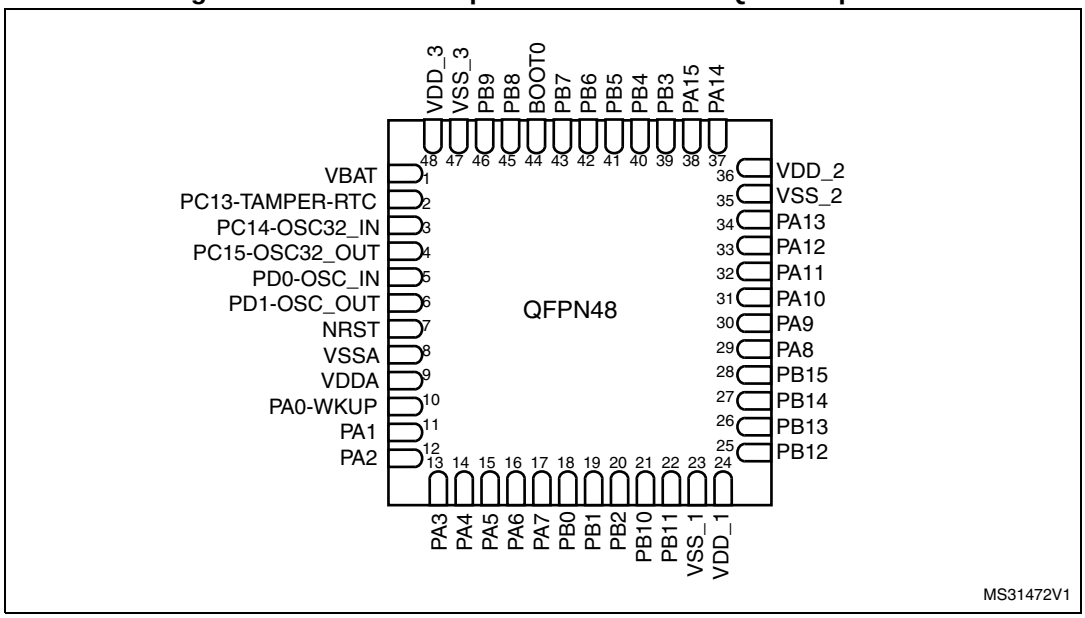


Table 5. Low-density STM32F103xx pin definitions (continued)

Pins				Pin name	Type(1)	I / O Level(2)	Main function(3) (after reset)	Alternate functions(4)	
LQFP48/ UFQFPN48	LQFP64	TFBGA64	VFQFPN36					Default	Remap
-	-	D1	3	PD1	I/O	FT	PD1	-	-
-	54	B5	-	PD2	I/O	FT	PD2	TIM3_ETR	-
39	55	A5	30	PB3	I/O	FT	JTDO	-	TIM2_CH2 / PB3/ TRACESWO
40	56	A4	31	PB4	I/O	FT	NJTRST	-	TIM3_CH1 /PB4 SPI1_MISO
41	57	C4	32	PB5	I/O	-	PB5	I2C1_SMBA	TIM3_CH2 / SPI1_MOSI
42	58	D3	33	PB6	I/O	FT	PB6	I2C1_SCL(9)/	USART1_TX
43	59	C3	34	PB7	I/O	FT	PB7	I2C1_SDA(9)	USART1_RX
44	60	B4	35	BOOT0	I	-	BOOT0	-	-
45	61	B3	-	PB8	I/O	FT	PB8	-	I2C1_SCL /CAN_RX
46	62	A3	-	PB9	I/O	FT	PB9	-	I2C1_SDA / CAN_TX
47	63	D4	36	V_{SS_3}	S	-	V_{SS_3}	-	-
48	64	E4	1	V_{DD_3}	S	-	V_{DD_3}	-	-

1. I = input, O = output, S = supply.
2. FT = 5 V tolerant.
3. Function availability depends on the chosen device. For devices having reduced peripheral counts, it is always the lower number of peripheral that is included. For example, if a device has only one SPI and two USARTs, they will be called SPI1 and USART1 & USART2, respectively. Refer to *Table 2 on page 11*.
4. If several peripherals share the same I/O pin, to avoid conflict between these alternate functions only one peripheral should be enabled at a time through the peripheral clock enable bit (in the corresponding RCC peripheral clock enable register).
5. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited: the speed should not exceed 2 MHz with a maximum load of 30 pF and these IOs must not be used as a current source (e.g. to drive an LED).
6. Main function after the first backup domain power-up. Later on, it depends on the contents of the Backup registers even after reset (because these registers are not reset by the main reset). For details on how to manage these IOs, refer to the Battery backup domain and BKP register description sections in the STM32F10xxx reference manual, available from the STMicroelectronics website: www.st.com.
7. The pins number 2 and 3 in the VFQFPN36 package, 5 and 6 in the LQFP48, UFQFPN48 and LQFP64 packages and C1 and C2 in the TFBGA64 package are configured as OSC_IN/OSC_OUT after reset, however the functionality of PD0 and PD1 can be remapped by software on these pins. For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual.
8. Unlike in the LQFP64 package, there is no PC3 in the TFBGA64 package. The V_{REF+} functionality is provided instead.
9. This alternate function can be remapped by software to some other port pins (if available on the used package). For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual, available from the STMicroelectronics website: www.st.com.

Figure 9. Pin loading conditions

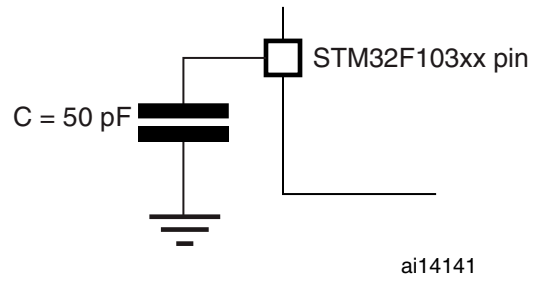
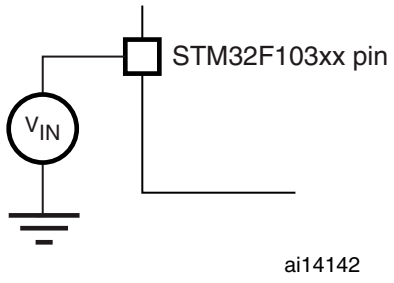
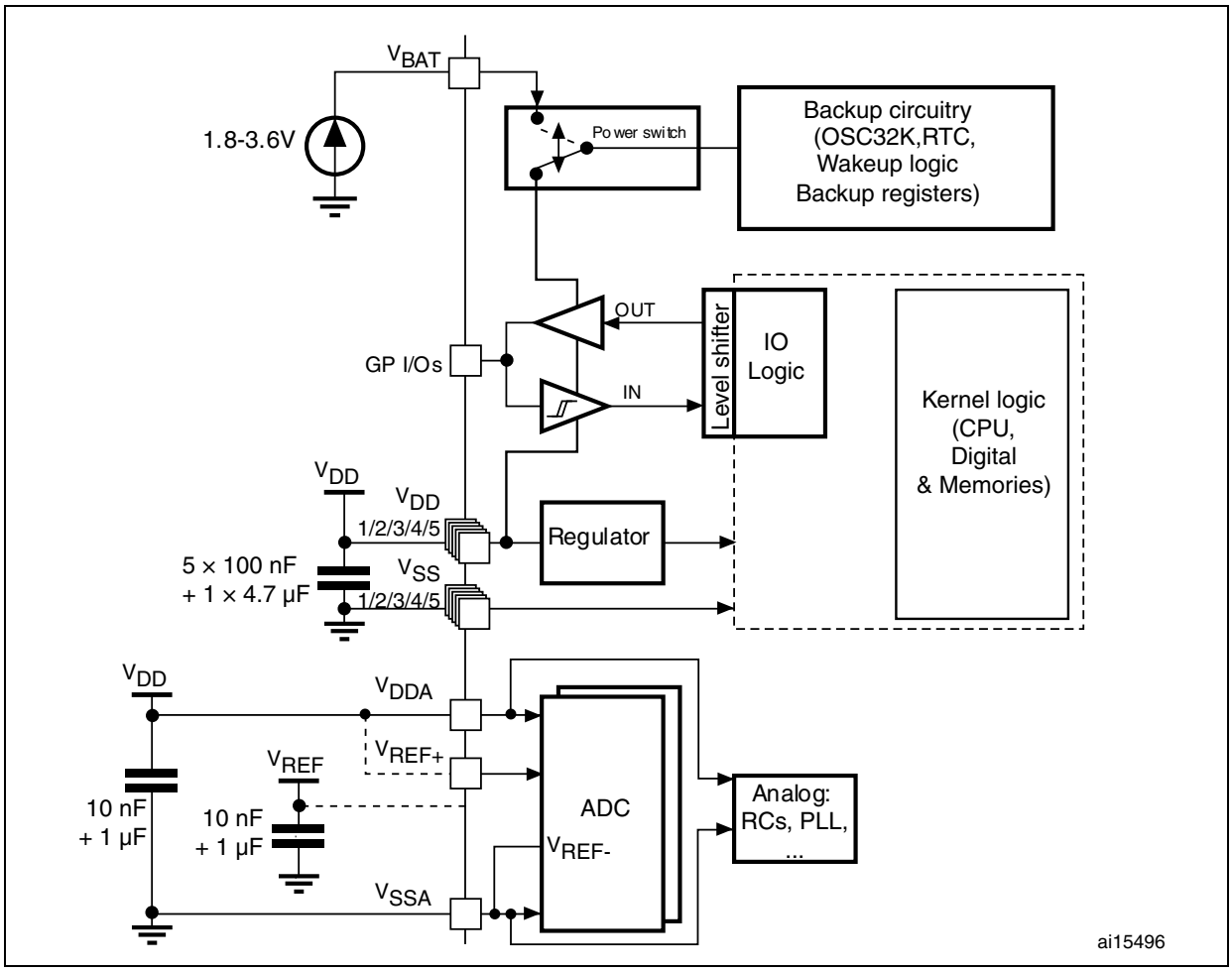


Figure 10. Pin input voltage



5.1.6 Power supply scheme

Figure 11. Power supply scheme



Caution: In *Figure 11*, the 4.7 µF capacitor must be connected to V_{DD3}.

Table 9. General operating conditions (continued)

Symbol	Parameter	Conditions		Min	Max	Unit
V_{IN}	I/O input voltage	Standard IO		–0.3	V_{DD}+ 0.3	V
		FT IO(3)	2 V < V_{DD} ≤ 3.6 V	–0.3	5.5	
			V_{DD} = 2 V	–0.3	5.2	
		BOOT0		0	5.5	
P_D	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7(4)	TFBGA64		-	308	mW
		LQFP64		-	444	
		LQFP48		-	363	
		UFQFPN48		-	624	
		VFQFPN36		-	1000	
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation		–40	85	°C
		Low power dissipation(5)		–40	105	
	Ambient temperature for 7 suffix version	Maximum power dissipation		–40	105	
		Low power dissipation(5)		–40	125	
T_J	Junction temperature range	6 suffix version		–40	105	
		7 suffix version		–40	125	

1. When the ADC is used, refer to *Table 46: ADC characteristics*.
2. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and operation.
3. To sustain a voltage higher than V_{DD}+0.3 V, the internal pull-up/pull-down resistors must be disabled.
4. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed $T_J$max (see *Table 6.6: Thermal characteristics on page 92*).
5. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed $T_J$max (see *Table 6.6: Thermal characteristics on page 92*).

5.3.2 Operating conditions at power-up / power-down

Subject to general operating conditions for T_A.

Table 10. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	¥	µs/V
	V_{DD} fall time rate		20	¥	

5.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 11* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 9*.

Table 11. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.1	2.18	2.26	V
		PLS[2:0]=000 (falling edge)	2	2.08	2.16	V
		PLS[2:0]=001 (rising edge)	2.19	2.28	2.37	V
		PLS[2:0]=001 (falling edge)	2.09	2.18	2.27	V
		PLS[2:0]=010 (rising edge)	2.28	2.38	2.48	V
		PLS[2:0]=010 (falling edge)	2.18	2.28	2.38	V
		PLS[2:0]=011 (rising edge)	2.38	2.48	2.58	V
		PLS[2:0]=011 (falling edge)	2.28	2.38	2.48	V
		PLS[2:0]=100 (rising edge)	2.47	2.58	2.69	V
		PLS[2:0]=100 (falling edge)	2.37	2.48	2.59	V
		PLS[2:0]=101 (rising edge)	2.57	2.68	2.79	V
		PLS[2:0]=101 (falling edge)	2.47	2.58	2.69	V
		PLS[2:0]=110 (rising edge)	2.66	2.78	2.9	V
		PLS[2:0]=110 (falling edge)	2.56	2.68	2.8	V
		PLS[2:0]=111 (rising edge)	2.76	2.88	3	V
		PLS[2:0]=111 (falling edge)	2.66	2.78	2.9	V
$V_{PVDhyst}$(2)	PVD hysteresis	-	-	100	-	mV
$V_{POR/PDR}$	Power on/power down reset threshold	Falling edge	1.8(1)	1.88	1.96	V
		Rising edge	1.84	1.92	2.0	V
$V_{PDRhyst}$(2)	PDR hysteresis	-	-	40	-	mV
$T_{RSTTEMPO}$(2)	Reset temporization	-	1	2.5	4.5	ms

1. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
2. Guaranteed by design, not tested in production.

Figure 13. Typical current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals enabled

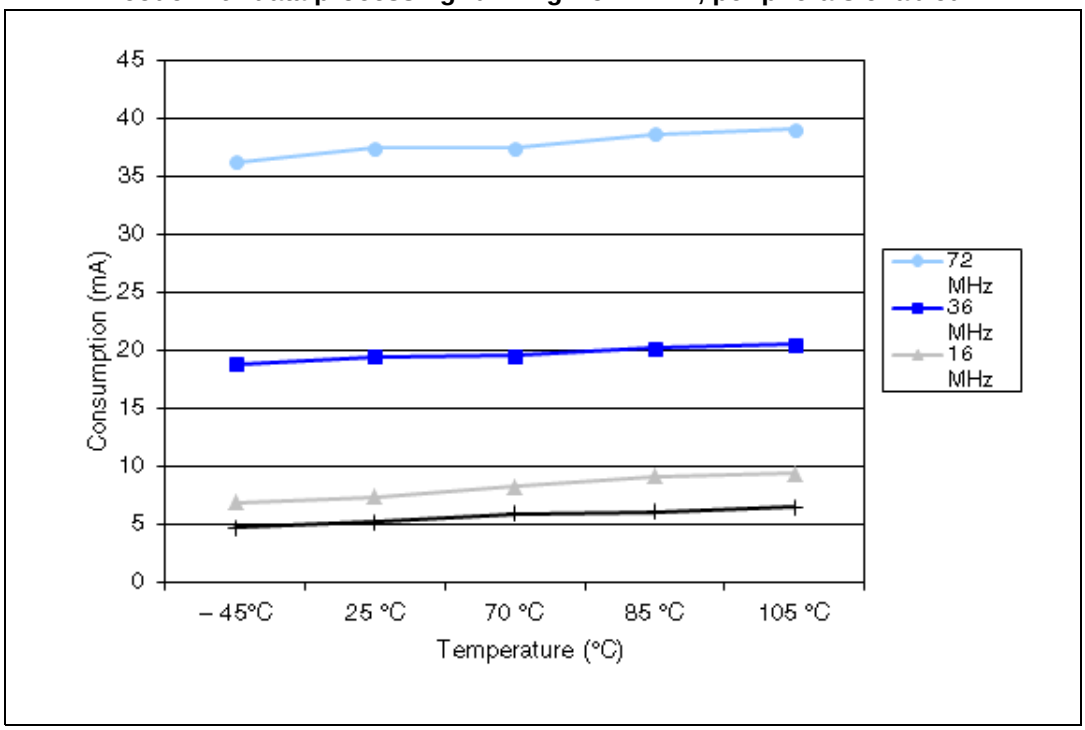


Figure 14. Typical current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals disabled

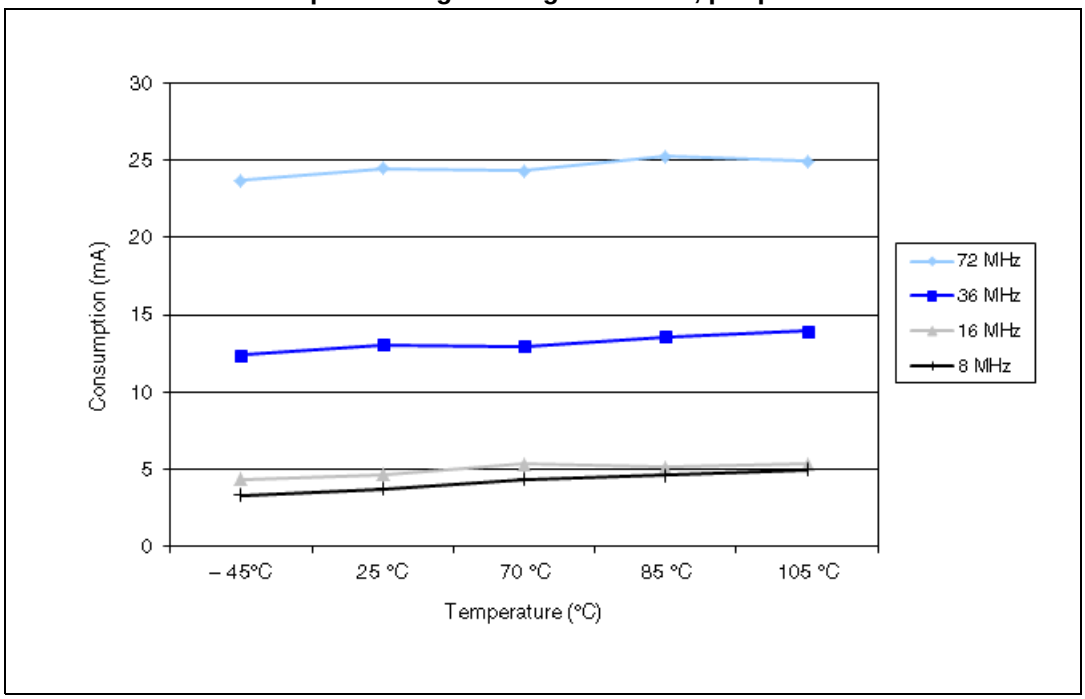
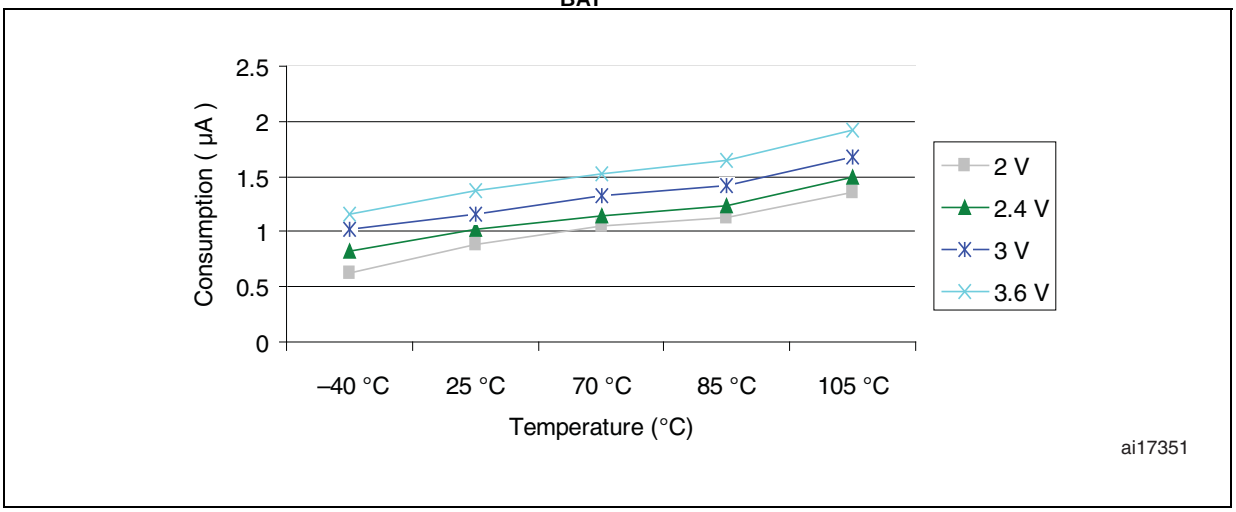


Table 16. Typical and maximum current consumptions in Stop and Standby modes

Symbol	Parameter	Conditions	Typ(1)			Max		Unit
			V_{DD}/V_{BAT} = 2.0 V	V_{DD}/V_{BAT} = 2.4 V	V_{DD}/V_{BAT} = 3.3 V	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Stop mode	Regulator in Run mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	-	21.3	21.7	160	200	µA
		Regulator in Low Power mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	-	11.3	11.7	145	185	
	Supply current in Standby mode	Low-speed internal RC oscillator and independent watchdog ON	-	2.75	3.4	-	-	
		Low-speed internal RC oscillator ON, independent watchdog OFF	-	2.55	3.2	-	-	
		Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF	-	1.55	1.9	3.2	4.5	
I_{DD_VBAT}	Backup domain supply current	Low-speed oscillator and RTC ON	0.9	1.1	1.4	1.9(2)	2.2	

1. Typical values are measured at T_A = 25 °C.
2. Based on characterization, not tested in production.

Figure 15. Typical current consumption on V_{BAT} with RTC on versus temperature at different V_{BAT} values



On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 19*. The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- ambient operating temperature and V_{DD} supply voltage conditions summarized in *Table 6*

Table 19. Peripheral current consumption(1)

Peripheral		Typical consumption at 25 °C	Unit
AHB (up to 72MHz)	DMA1	15.97	µA/MHz
	CRC	1.67	
	BusMatrix(2)	8.33	
APB1(up to 36MHz)	APB1 Bridge	7.22	µA/MHz
	TIM2	33.33	
	TIM3	33.61	
	USART2	12.78	
	I2C1	10.83	
	USB	16.94	
	CAN1	17.50	
	WWDG	3.33	
	PWR	1.94	
	BKP	2.78	
	IWDG	1.39	
APB2 (up to 72MHz)	APB2-Bridge	3.33	µA/MHz
	GPIO A	7.50	
	GPIO B	6.81	
	GPIO C	7.22	
	GPIO D	6.94	
	ADC1(3) (4)	15.54	
	ADC2	14.64	
	TIM1	21.53	
	SPI	4.86	
	USART1	12.78	

1. f_{HCLK} = 72 MHz, $f_{APB1} = f_{HCLK}/2$, $f_{APB2} = f_{HCLK}$, default prescaler value for each peripheral.
2. The BusMatrix is automatically active when at least one master is ON.
3. Specific conditions for ADC: f_{HCLK} = 56 MHz, $f_{APB1} = f_{HCLK}/2$, $f_{APB2} = f_{HCLK}$, $f_{ADCCLK} = f_{APB2/4}$. When ADON bit in the ADC_CR2 register is set to 1,.we have a consumption added equal to 0.68 mA.
4. When we enable the ADC, a current consumption is added equal to 0,06 mA.

5.3.6 External clock source characteristics

High-speed external user clock generated from an external source

The characteristics given in *Table 20* result from tests performed using an high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 9*.

Table 20. High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency(1)	-	1	8	25	MHz
V_{HSEH}	OSC_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(HSE)}$ $t_{w(HSE)}$	OSC_IN high or low time(1)		5	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time(1)		-	-	20	
$C_{in(HSE)}$	OSC_IN input capacitance(1)	-	-	5	-	pF
$DuCy_{(HSE)}$	Duty cycle	-	45	-	55	%
I_L	OSC_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA

1. Guaranteed by design, not tested in production.

Low-speed external user clock generated from an external source

The characteristics given in *Table 21* result from tests performed using an low-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 9*.

Table 21. Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User External clock source frequency(1)	-	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{w(LSE)}$	OSC32_IN high or low time(1)		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time(1)		-	-	50	
$C_{in(LSE)}$	OSC32_IN input capacitance(1)	-	-	5	-	pF
$DuCy_{(LSE)}$	Duty cycle	-	30	-	70	%
I_L	OSC32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	-	-	±1	µA

1. Guaranteed by design, not tested in production.

5.3.11 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 32. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C conforming to JESD22-A114	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C conforming to JESD22-C101	II	500	

1. Based on characterization results, not tested in production.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 33. Electrical sensitivities

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	T_A = +105 °C conforming to JESD78A	II level A

Figure 25. 5 V tolerant I/O input characteristics - CMOS port

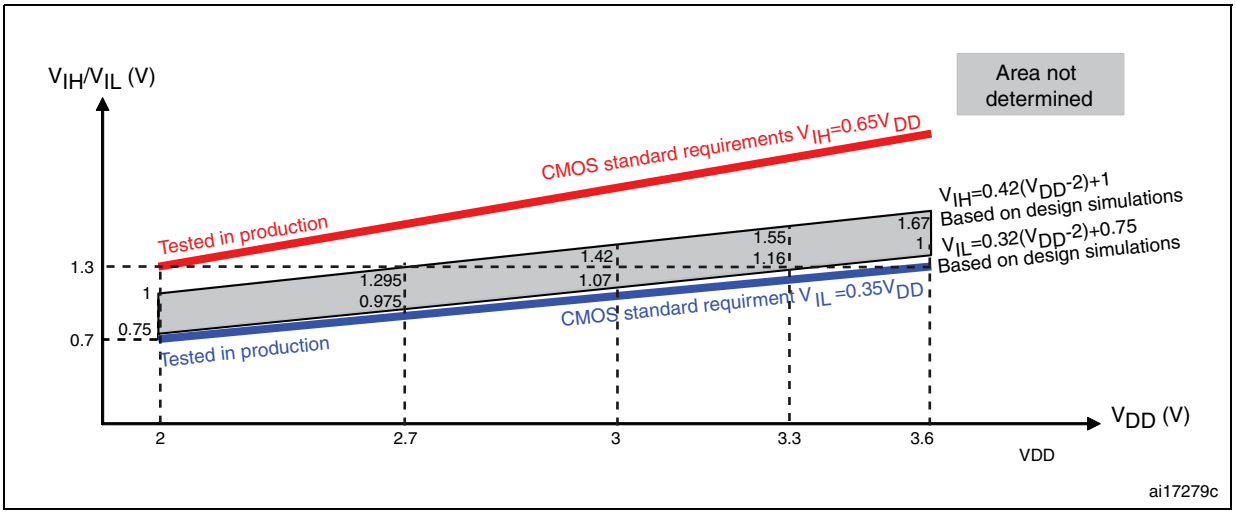


Figure 26. 5 V tolerant I/O input characteristics - TTL port

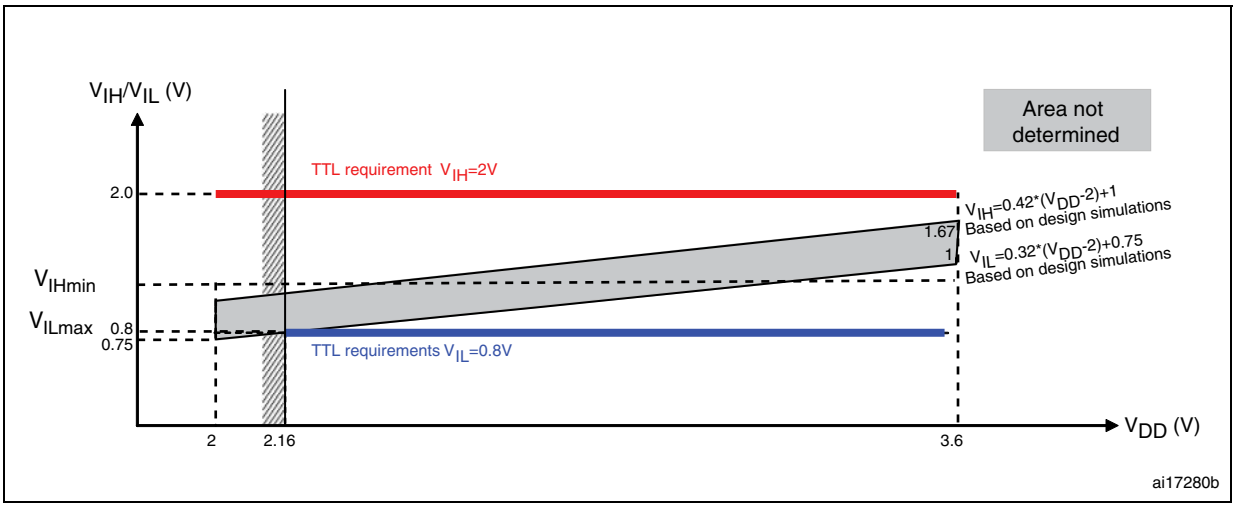
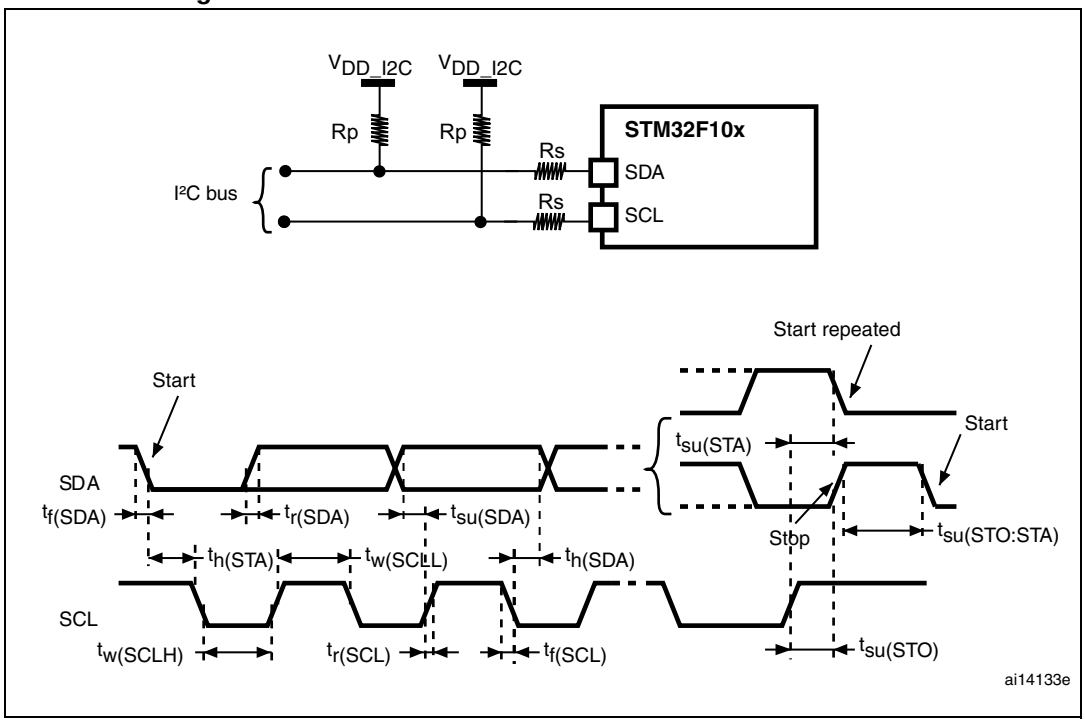


Figure 29. I²C bus AC waveforms and measurement circuit



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.
2. Rs = Series protection resistors, Rp = Pull-up resistors, V_{DD_I2C} = I2C bus supply.

Table 41. SCL frequency (f_{PCLK1}= 36 MHz.,V_{DD_I2C} = 3.3 V)(1)(2)

f_{SCL} (kHz)	I2C_CCR value
	R_P = 4.7 kΩ
400	0x801E
300	0x8028
200	0x803C
100	0x00B4
50	0x0168
20	0x0384

1. R_P = External pull-up resistance, f_{SCL} = I²C speed,
2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed ±2%. These variations depend on the accuracy of the external components used to design the application.

SPI interface characteristics

Unless otherwise specified, the parameters given in *Table 42* are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 9*.

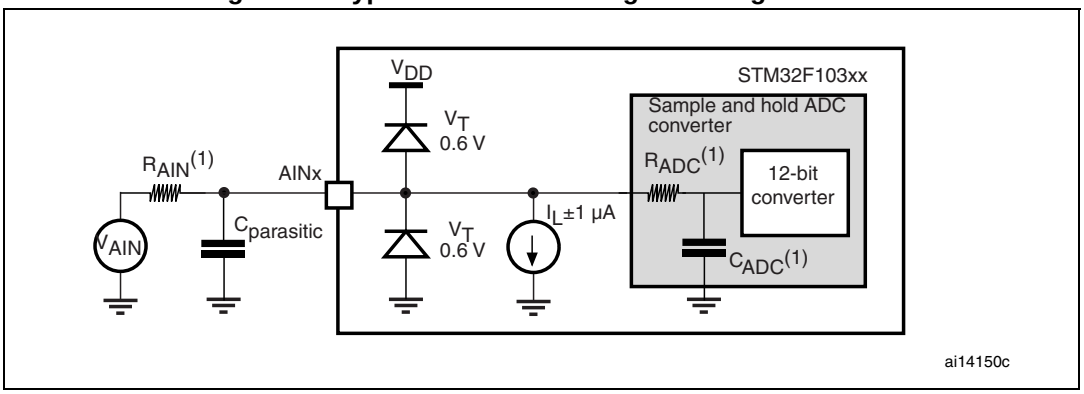
Refer to *Section 5.3.12: I/O current injection characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO).

Table 42. SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	18	MHz
		Slave mode	-	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF		8	ns
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	30	70	%
$t_{su(NSS)}$ (1)	NSS setup time	Slave mode	$4t_{PCLK}$	-	ns
$t_{h(NSS)}$ (1)	NSS hold time	Slave mode	$2t_{PCLK}$	-	
$t_{w(SCKH)}$ (1) $t_{w(SCKL)}$ (1)	SCK high and low time	Master mode, f_{PCLK} = 36 MHz, presc = 4	50	60	
$t_{su(MI)}$ (1) $t_{su(SI)}$ (1)	Data input setup time	Master mode	5	-	
		Slave mode	5	-	
$t_{h(MI)}$ (1)	Data input hold time	Master mode	5	-	
$t_{h(SI)}$ (1)		Slave mode	4	-	
$t_{a(SO)}$ (1)(2)	Data output access time	Slave mode, f_{PCLK} = 20 MHz	0	$3t_{PCLK}$	
$t_{dis(SO)}$ (1)(3)	Data output disable time	Slave mode	2	10	
$t_{v(SO)}$ (1)	Data output valid time	Slave mode (after enable edge)	-	25	
$t_{v(MO)}$ (1)	Data output valid time	Master mode (after enable edge)	-	5	
$t_{h(SO)}$ (1)	Data output hold time	Slave mode (after enable edge)	15	-	
$t_{h(MO)}$ (1)		Master mode (after enable edge)	2	-	

1. Based on characterization, not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

Figure 35. Typical connection diagram using the ADC

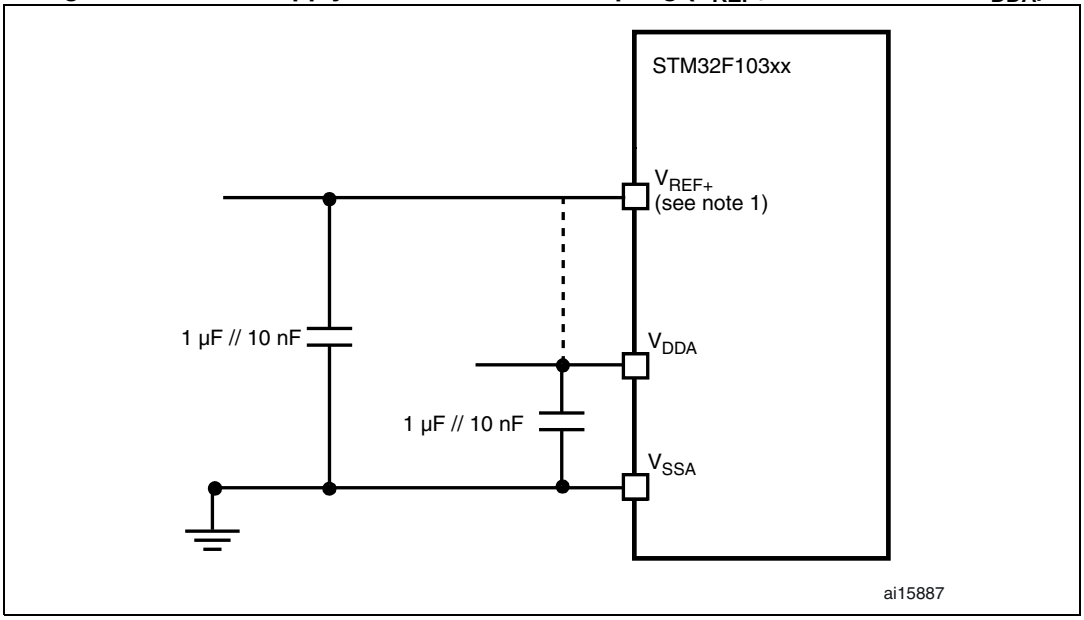


1. Refer to *Table 46* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in*Figure 36* or *Figure 37*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

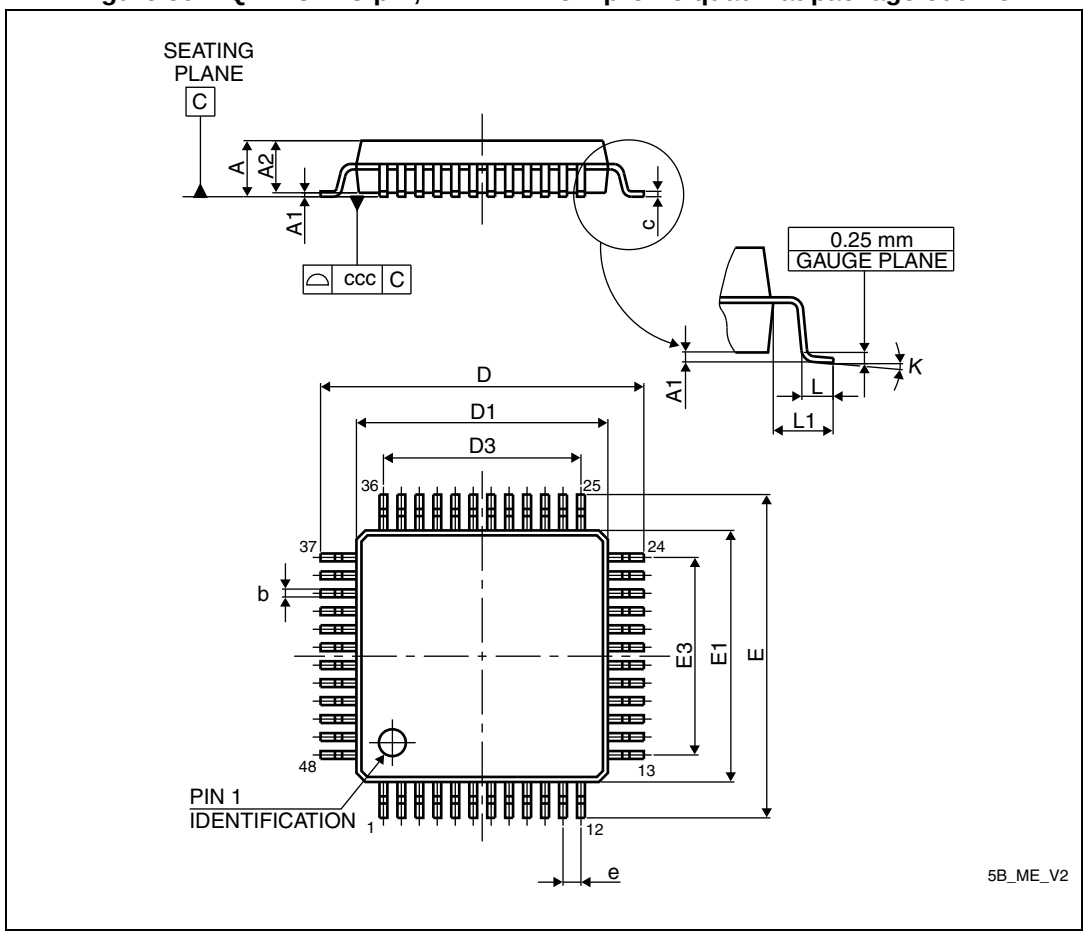
Figure 36. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



1. The V_{REF+} input is available only on the TFBGA64 package.

6.5 LQFP48 package information

Figure 50. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline



1. Drawing is not to scale.

Using the values obtained in *Table 57* T_{Jmax} is calculated as follows:

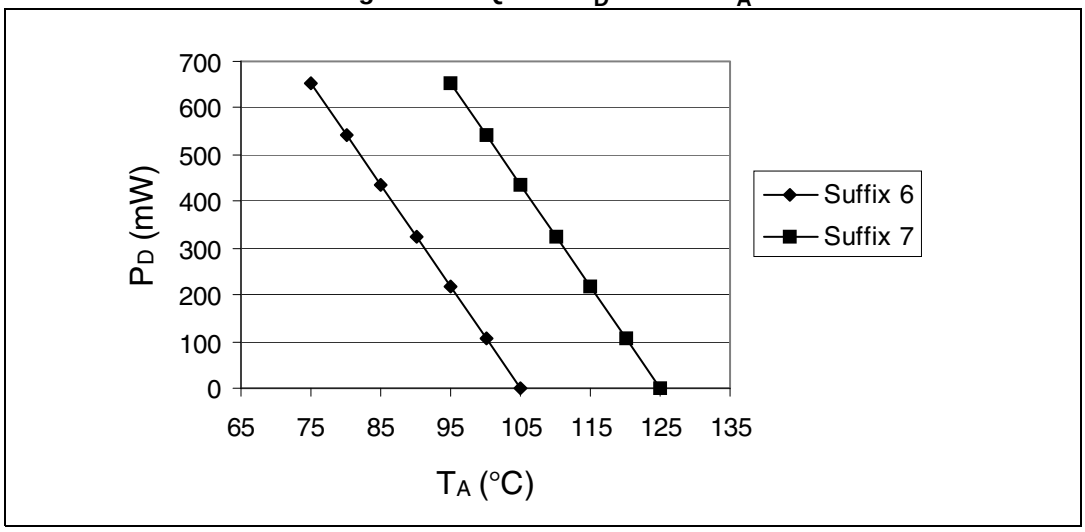
– For LQFP64, 45 °C/W

T_{Jmax} = 115 °C + (45 °C/W × 134 mW) = 115 °C + 6.03 °C = 121.03 °C

This is within the range of the suffix 7 version parts (–40 < T_J < 125 °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Table 58: Ordering information scheme*).

Figure 53. LQFP64 P_D max vs. T_A



8 Revision history

Table 59. Document revision history

Date	Revision	Changes
22-Sep-2008	1	Initial release.
30-Mar-2009	2	"96-bit unique ID" feature added and I/O information clarified *on page 1*. Timers specified *on page 1* (Motor control capability mentioned). *Table 4: Timer feature comparison* added. PB4, PB13, PB14, PB15, PB3/TRACESWO moved from Default column to Remap column, plus small additional changes in *Table 5: Low-density STM32F103xx pin definitions*. *Figure 8: Memory map* modified. References to V_{REF-} removed: – *Figure 1: STM32F103xx performance line block diagram* modified, – *Figure 11: Power supply scheme* modified – *Figure 34: ADC accuracy characteristics* modified – Note modified in *Table 49: ADC accuracy*. *Table 20: High-speed external user clock characteristics* and *Table 21: Low-speed external user clock characteristics* modified. Note modified in *Table 13: Maximum current consumption in Run mode, code with data processing running from Flash* and *Table 15: Maximum current consumption in Sleep mode, code running from Flash or RAM*. *Figure 17* shows a typical curve (title modified). ACC_{HSI} max values modified in *Table 24: HSI oscillator characteristics*. TFBGA64 package added (see *Table 54* and *Table 47*). Small text changes.
24-Sep-2009	3	*Note 5* updated and *Note 4* added in *Table 5: Low-density STM32F103xx pin definitions*. V_{RERINT} and T_{Coeff} added to *Table 12: Embedded internal reference voltage*. Typical I_{DD_VBAT} value added in *Table 16: Typical and maximum current consumptions in Stop and Standby modes*. *Figure 15: Typical current consumption on V_{BAT} with RTC on versus temperature at different V_{BAT} values* added. f_{HSE_ext} min modified in *Table 20: High-speed external user clock characteristics*. C_{L1} and C_{L2} replaced by C in *Table 22: HSE 4-16 MHz oscillator characteristics* and *Table 23: LSE oscillator characteristics (f_{LSE} = 32.768 kHz)*, notes modified and moved below the tables. *Table 24: HSI oscillator characteristics* modified. Conditions removed from *Table 26: Low-power mode wakeup timings*. *Note 1* modified below *Figure 21: Typical application with an 8 MHz crystal*. *Figure 28: Recommended NRST pin protection* modified. Jitter added to *Table 27: PLL characteristics on page 52*. IEC 1000 standard updated to IEC 61000 and SAE J1752/3 updated to IEC 61967-2 in *Section 5.3.10: EMC characteristics on page 53*. C_{ADC} and R_{AIN} parameters modified in *Table 46: ADC characteristics*. R_{AIN} max values modified in *Table 47: R_{AIN} max for f_{ADC} = 14 MHz*. Small text changes.