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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | C166SV2 |
| Core Size | 16/32-Bit |
| Speed | 80MHz |
| Connectivity | CANbus, EBI/EMI, I²C, LINbus, SPI, SSC, UART/USART, USI |
| Peripherals | DMA, I²S, POR, PWM, WDT |
| Number of I/O | 118 |
| Program Memory Size | 768KB (768K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 82K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 5.5V |
| Data Converters | A/D 24x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 144-LQFP Exposed Pad |
| Supplier Device Package | PG-LQFP-144-4 |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/xc228796f80lackxuma1 |

## 2.1 Pin Configuration and Definition

The pins of the XC228x are described in detail in **Table 4**, which includes all alternate functions. For further explanations please refer to the footnotes at the end of the table. **Figure 2** summarizes all pins, showing their locations on the four sides of the package.

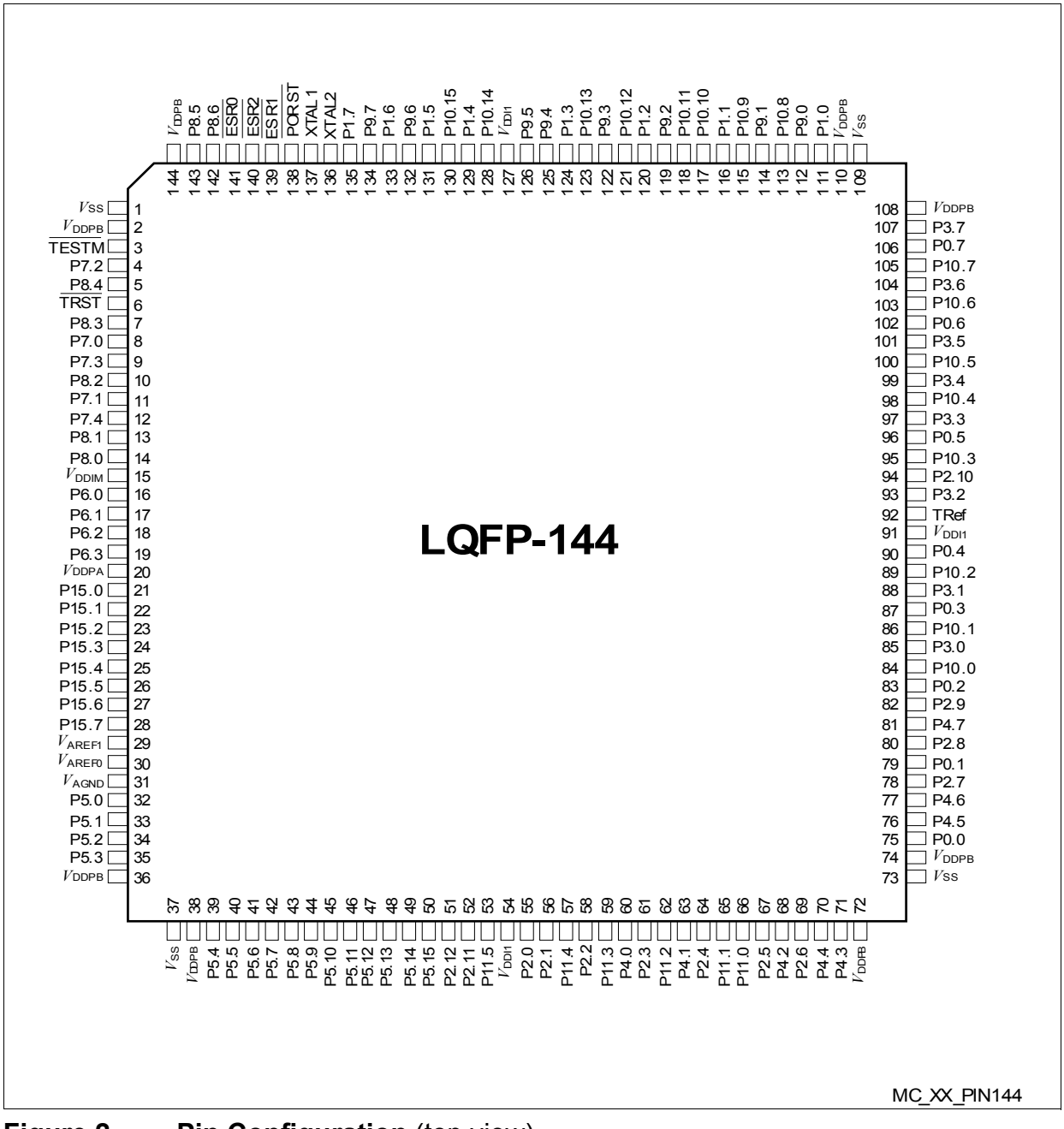


**Figure 2 Pin Configuration** (top view)

**Table 4 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 43 | P5.8 | I | In/A | **Bit 8 of Port 5, General Purpose Input** |
| | ADC0_CH8 | I | In/A | **Analog Input Channel 8 for ADC0** |
| | CCU6x_ T12HRC | I | In/A | **External Run Control Input for T12 of CCU6x** |
| | CCU6x_ T13HRC | I | In/A | **External Run Control Input for T13 of CCU6x** |
| 44 | P5.9 | I | In/A | **Bit 9 of Port 5, General Purpose Input** |
| | ADC0_CH9 | I | In/A | **Analog Input Channel 9 for ADC0** |
| | CC2_T7IN | I | In/A | **CAPCOM2 Timer T7 Count Input** |
| 45 | P5.10 | I | In/A | **Bit 10 of Port 5, General Purpose Input** |
| | ADC0_CH10 | I | In/A | **Analog Input Channel 10 for ADC0** |
| | $\overline{\text{BRKIN\_A}}$ | I | In/A | **OCDS Break Signal Input** |
| 46 | P5.11 | I | In/A | **Bit 11 of Port 5, General Purpose Input** |
| | ADC0_CH11 | I | In/A | **Analog Input Channel 11 for ADC0** |
| 47 | P5.12 | I | In/A | **Bit 12 of Port 5, General Purpose Input** |
| | ADC0_CH12 | I | In/A | **Analog Input Channel 12 for ADC0** |
| 48 | P5.13 | I | In/A | **Bit 13 of Port 5, General Purpose Input** |
| | ADC0_CH13 | I | In/A | **Analog Input Channel 13 for ADC0** |
| | EX0BINB | I | In/A | **External Interrupt Trigger Input** |
| 49 | P5.14 | I | In/A | **Bit 14 of Port 5, General Purpose Input** |
| | ADC0_CH14 | I | In/A | **Analog Input Channel 14 for ADC0** |
| 50 | P5.15 | I | In/A | **Bit 15 of Port 5, General Purpose Input** |
| | ADC0_CH15 | I | In/A | **Analog Input Channel 15 for ADC0** |
| 51 | P2.12 | O0 / I | St/B | **Bit 12 of Port 2, General Purpose Input/Output** |
| | U0C0_ SELO4 | O1 | St/B | **USIC0 Channel 0 Select/Control 4 Output** |
| | U0C1_ SELO3 | O2 | St/B | **USIC0 Channel 1 Select/Control 3 Output** |
| | READY | I | St/B | **External Bus Interface READY Input** |

**Table 4 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 60 | P4.0 | O0 / I | St/B | **Bit 0 of Port 4, General Purpose Input/Output** |
| | CC2_24 | O3 / I | St/B | **CAPCOM2 CC24IO Capture Inp./ Compare Out.** |
| | $\overline{\text{CS0}}$ | OH | St/B | **External Bus Interface Chip Select 0 Output** |
| 61 | P2.3 | O0 / I | St/B | **Bit 3 of Port 2, General Purpose Input/Output** |
| | U0C0_DOUT | O1 | St/B | **USIC0 Channel 0 Shift Data Output** |
| | CCU63_ COUT63 | O2 | St/B | **CCU63 Channel 3 Output** |
| | CC2_16 | O3 / I | St/B | **CAPCOM2 CC16IO Capture Inp./ Compare Out.** |
| | A16 | OH | St/B | **External Bus Interface Address Line 16** |
| | ESR2_0 | I | St/B | **ESR2 Trigger Input 0** |
| | U0C0_DX0E | I | St/B | **USIC0 Channel 0 Shift Data Input** |
| | U0C1_DX0D | I | St/B | **USIC0 Channel 1 Shift Data Input** |
| | RxDC0A | I | St/B | **CAN Node 0 Receive Data Input** |
| 62 | P11.2 | O0 / I | St/B | **Bit 2 of Port 11, General Purpose Input/Output** |
| | CCU63_ CCPOS2A | I | St/B | **CCU63 Position Input 2** |
| 63 | P4.1 | O0 / I | St/B | **Bit 1 of Port 4, General Purpose Input/Output** |
| | TxDC2 | O2 | St/B | **CAN Node 2 Transmit Data Output** |
| | CC2_25 | O3 / I | St/B | **CAPCOM2 CC25IO Capture Inp./ Compare Out.** |
| | $\overline{\text{CS1}}$ | OH | St/B | **External Bus Interface Chip Select 1 Output** |
| 64 | P2.4 | O0 / I | St/B | **Bit 4 of Port 2, General Purpose Input/Output** |
| | U0C1_DOUT | O1 | St/B | **USIC0 Channel 1 Shift Data Output** |
| | TxDC0 | O2 | St/B | **CAN Node 0 Transmit Data Output** |
| | CC2_17 | O3 / I | St/B | **CAPCOM2 CC17IO Capture Inp./ Compare Out.** |
| | A17 | OH | St/B | **External Bus Interface Address Line 17** |
| | ESR1_0 | I | St/B | **ESR1 Trigger Input 0** |
| | U0C0_DX0F | I | St/B | **USIC0 Channel 0 Shift Data Input** |
| | RxDC1A | I | St/B | **CAN Node 1 Receive Data Input** |
| 65 | P11.1 | O0 / I | St/B | **Bit 1 of Port 11, General Purpose Input/Output** |
| | CCU63_ CCPOS1A | I | St/B | **CCU63 Position Input 1** |

**Table 4 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 83 | P0.2 | O0 / I | St/B | **Bit 2 of Port 0, General Purpose Input/Output** |
| | U1C0_ SCLKOUT | O1 | St/B | **USIC1 Channel 0 Shift Clock Output** |
| | TxDC0 | O2 | St/B | **CAN Node 0 Transmit Data Output** |
| | CCU61_ CC62 | O3 / I | St/B | **CCU61 Channel 2 Input/Output** |
| | A2 | OH | St/B | **External Bus Interface Address Line 2** |
| | U1C0_DX1B | I | St/B | **USIC1 Channel 0 Shift Clock Input** |
| 84 | P10.0 | O0 / I | St/B | **Bit 0 of Port 10, General Purpose Input/Output** |
| | U0C1_DOUT | O1 | St/B | **USIC0 Channel 1 Shift Data Output** |
| | CCU60_ CC60 | O2 / I | St/B | **CCU60 Channel 0 Input/Output** |
| | AD0 | OH / I | St/B | **External Bus Interface Address/Data Line 0** |
| | ESR1_2 | I | St/B | **ESR1 Trigger Input 2** |
| | U0C0_DX0A | I | St/B | **USIC0 Channel 0 Shift Data Input** |
| | U0C1_DX0A | I | St/B | **USIC0 Channel 1 Shift Data Input** |
| 85 | P3.0 | O0 / I | St/B | **Bit 0 of Port 3, General Purpose Input/Output** |
| | U2C0_DOUT | O1 | St/B | **USIC2 Channel 0 Shift Data Output** |
| | BREQ | OH | St/B | **External Bus Request Output** |
| | ESR1_1 | I | St/B | **ESR1 Trigger Input 1** |
| | U2C0_DX0A | I | St/B | **USIC2 Channel 0 Shift Data Input** |
| | RxDC3B | I | St/B | **CAN Node 3 Receive Data Input** |
| | U2C0_DX1A | I | St/B | **USIC2 Channel 0 Shift Clock Input** |
| 86 | P10.1 | O0 / I | St/B | **Bit 1 of Port 10, General Purpose Input/Output** |
| | U0C0_DOUT | O1 | St/B | **USIC0 Channel 0 Shift Data Output** |
| | CCU60_ CC61 | O2 / I | St/B | **CCU60 Channel 1 Input/Output** |
| | AD1 | OH / I | St/B | **External Bus Interface Address/Data Line 1** |
| | U0C0_DX0B | I | St/B | **USIC0 Channel 0 Shift Data Input** |
| | U0C0_DX1A | I | St/B | **USIC0 Channel 0 Shift Clock Input** |

**Table 4 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 101 | P3.5 | O0 / I | St/B | **Bit 5 of Port 3, General Purpose Input/Output** |
| | U2C1_ SCLKOUT | O1 | St/B | **USIC2 Channel 1 Shift Clock Output** |
| | U2C0_ SELO2 | O2 | St/B | **USIC2 Channel 0 Select/Control 2 Output** |
| | U0C0_ SELO5 | O3 | St/B | **USIC0 Channel 0 Select/Control 5 Output** |
| | U2C1_DX1A | I | St/B | **USIC2 Channel 1 Shift Clock Input** |
| 102 | P0.6 | O0 / I | St/B | **Bit 6 of Port 0, General Purpose Input/Output** |
| | U1C1_DOUT | O1 | St/B | **USIC1 Channel 1 Shift Data Output** |
| | TxDC1 | O2 | St/B | **CAN Node 1 Transmit Data Output** |
| | CCU61_ COUT63 | O3 | St/B | **CCU61 Channel 3 Output** |
| | A6 | OH | St/B | **External Bus Interface Address Line 6** |
| | U1C1_DX0A | I | St/B | **USIC1 Channel 1 Shift Data Input** |
| | CCU61_ CTRAPA | I | St/B | **CCU61 Emergency Trap Input** |
| | U1C1_DX1B | I | St/B | **USIC1 Channel 1 Shift Clock Input** |
| 103 | P10.6 | O0 / I | St/B | **Bit 6 of Port 10, General Purpose Input/Output** |
| | U0C0_DOUT | O1 | St/B | **USIC0 Channel 0 Shift Data Output** |
| | TxDC4 | O2 | St/B | **CAN Node 4 Transmit Data Output** |
| | U1C0_ SELO0 | O3 | St/B | **USIC1 Channel 0 Select/Control 0 Output** |
| | AD6 | OH / I | St/B | **External Bus Interface Address/Data Line 6** |
| | U0C0_DX0C | I | St/B | **USIC0 Channel 0 Shift Data Input** |
| | U1C0_DX2D | I | St/B | **USIC1 Channel 0 Shift Control Input** |
| | CCU60_ CTRAPA | I | St/B | **CCU60 Emergency Trap Input** |

**Table 4 Pin Definitions and Functions** (cont'd)

| Pin | Symbol | Ctrl. | Type | Function |
|---|---|---|---|---|
| 131 | P1.5 | O0 / I | St/B | **Bit 5 of Port 1, General Purpose Input/Output** |
| | CCU62_ COUT60 | O1 | St/B | **CCU62 Channel 0 Output** |
| | U1C1_ SELO3 | O2 | St/B | **USIC1 Channel 1 Select/Control 3 Output** |
| | $\overline{\text{BRKOUT}}$ | O3 | St/B | **OCDS Break Signal Output** |
| | A13 | OH | St/B | **External Bus Interface Address Line 13** |
| | U2C0_DX0C | I | St/B | **USIC2 Channel 0 Shift Data Input** |
| 132 | P9.6 | O0 / I | St/B | **Bit 6 of Port 9, General Purpose Input/Output** |
| | CCU63_ COUT63 | O1 | St/B | **CCU63 Channel 3 Output** |
| | CCU63_ COUT62 | O2 | St/B | **CCU63 Channel 2 Output** |
| | CCU63 _ CTRAPA | I | St/B | **CCU63 Emergency Trap Input** |
| | CCU60_ CCPOS1B | I | St/B | **CCU60 Position Input 1** |
| 133 | P1.6 | O0 / I | St/B | **Bit 6 of Port 1, General Purpose Input/Output** |
| | CCU62_ CC61 | O1 / I | St/B | **CCU62 Channel 1 Input/Output** |
| | U1C1_ SELO2 | O2 | St/B | **USIC1 Channel 1 Select/Control 2 Output** |
| | U2C0_DOUT | O3 | St/B | **USIC2 Channel 0 Shift Data Output** |
| | A14 | OH | St/B | **External Bus Interface Address Line 14** |
| | U2C0_DX0D | I | St/B | **USIC2 Channel 0 Shift Data Input** |
| 134 | P9.7 | O0 / I | St/B | **Bit 7 of Port 9, General Purpose Input/Output** |
| | CCU63_ CTRAPB | I | St/B | **CCU63 Emergency Trap Input** |
| | U2C0_DX1D | I | St/B | **USIC2 Channel 0 Shift Clock Input** |
| | CCU60_ CCPOS0B | I | St/B | **CCU60 Position Input 0** |

# 3 Functional Description

The architecture of the XC228x combines advantages of RISC, CISC, and DSP processors with an advanced peripheral subsystem in a well-balanced design. On-chip memory blocks allow the design of compact systems-on-silicon with maximum performance suited for computing, control, and communication.

The on-chip memory blocks (program code memory and SRAM, dual-port RAM, data SRAM) and the generic peripherals are connected to the CPU by separate high-speed buses. Another bus, the LXBus, connects additional on-chip resources and external resources (see **Figure 3**). This bus structure enhances overall system performance by enabling the concurrent operation of several subsystems of the XC228x.

The block diagram gives an overview of the on-chip components and the advanced internal bus structure of the XC228x.

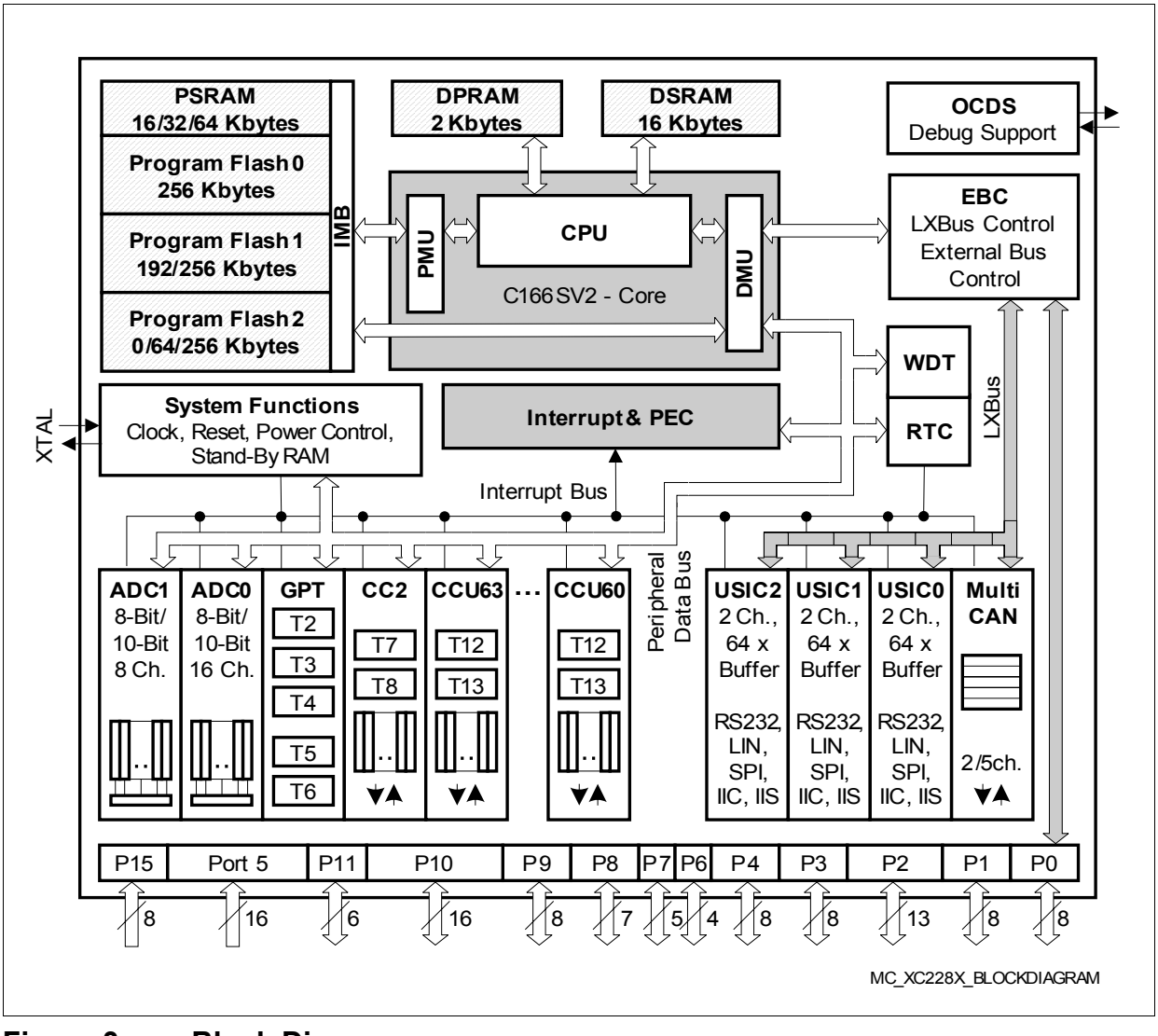


**Figure 3 Block Diagram**

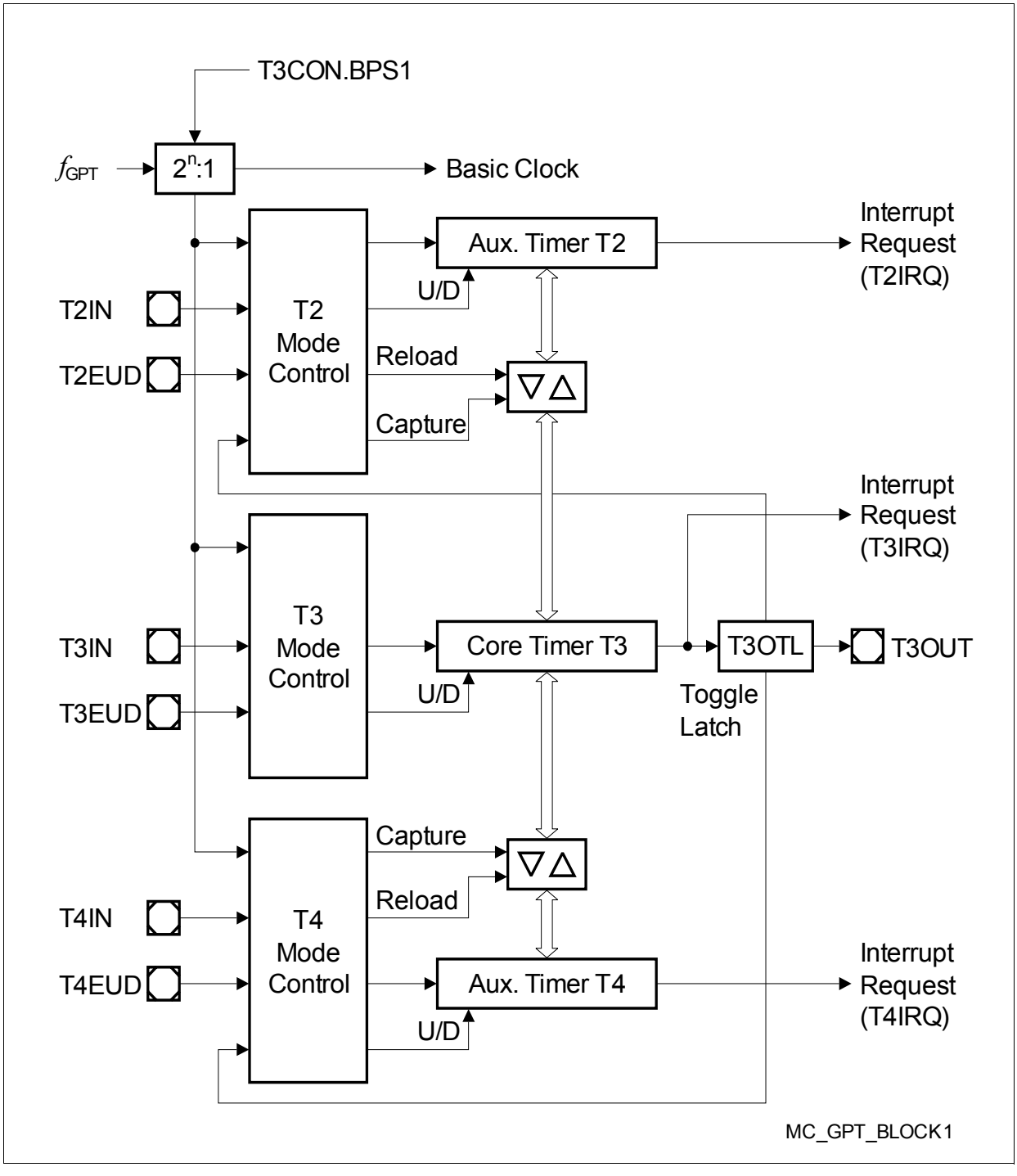


**Figure 7 Block Diagram of GPT1**

## 3.9 Real Time Clock

The Real Time Clock (RTC) module of the XC228x can be clocked with a clock signal selected from internal sources or external sources (pins).

The RTC basically consists of a chain of divider blocks:

- Selectable 32:1 and 8:1 dividers (on - off)
- The reloadable 16-bit timer T14
- The 32-bit RTC timer block (accessible via registers RTCH and RTCL) consisting of:
  - a reloadable 10-bit timer
  - a reloadable 6-bit timer
  - a reloadable 6-bit timer
  - a reloadable 10-bit timer

All timers count up. Each timer can generate an interrupt request. All requests are combined to a common node request.

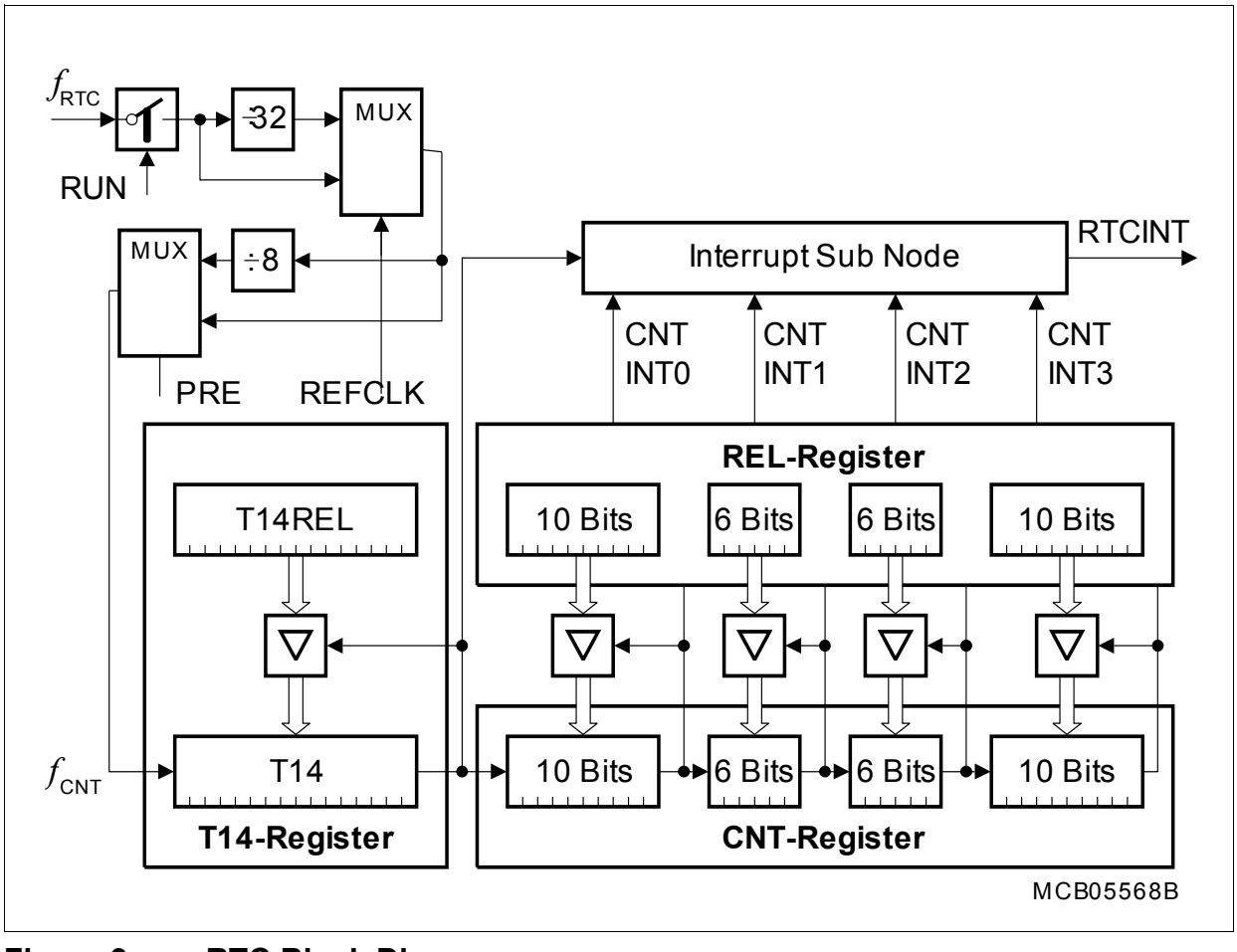


**Figure 9 RTC Block Diagram**

*Note: The registers associated with the RTC are only affected by a power reset.*

## 3.12 MultiCAN Module

The MultiCAN module contains up to five independently operating CAN nodes with Full-CAN functionality which are able to exchange Data and Remote Frames using a gateway function. Transmission and reception of CAN frames is handled in accordance with CAN specification V2.0 B (active). Each CAN node can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

All CAN nodes share a common set of up to 128 message objects. Each message object can be individually allocated to one of the CAN nodes. Besides serving as a storage container for incoming and outgoing frames, message objects can be combined to build gateways between the CAN nodes or to set up a FIFO buffer.

The message objects are organized in double-chained linked lists, where each CAN node has its own list of message objects. A CAN node stores frames only into message objects that are allocated to its own message object list and it transmits only messages belonging to this message object list. A powerful, command-driven list controller performs all message object list operations.

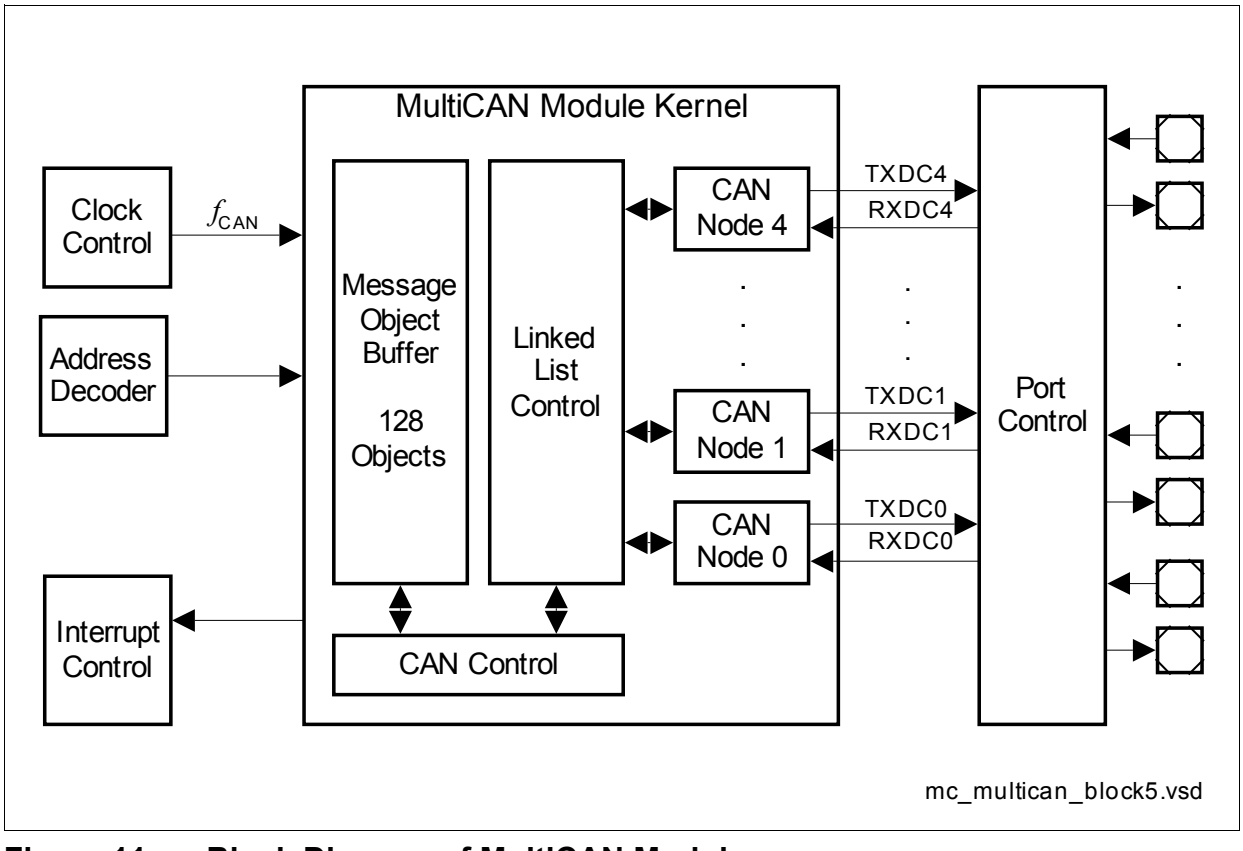


**Figure 11 Block Diagram of MultiCAN Module**

### MultiCAN Features

- CAN functionality conforming to CAN specification V2.0 B active for each CAN node (compliant to ISO 11898)
- Up to five independent CAN nodes
- Up to 128 independent message objects (shared by the CAN nodes)
- Dedicated control registers for each CAN node
- Data transfer rate up to 1 Mbit/s, individually programmable for each node
- Flexible and powerful message transfer control and error handling capabilities
- Full-CAN functionality for message objects:
  - Can be assigned to one of the CAN nodes
  - Configurable as transmit or receive objects, or as message buffer FIFO
  - Handle 11-bit or 29-bit identifiers with programmable acceptance mask for filtering
  - Remote Monitoring Mode, and frame counter for monitoring
- Automatic Gateway Mode support
- 16 individually programmable interrupt nodes
- Analyzer mode for CAN bus monitoring

## 3.16 Power Management

The XC228x provides the means to control the power it consumes either at a given time or averaged over a certain duration.
Three mechanisms can be used (and partly in parallel):

- **Supply Voltage Management** permits the temporary reduction of the supply voltage of major parts of the logic or even its complete disconnection. This drastically reduces the power consumed because it eliminates leakage current, particularly at high temperature.
  Several power reduction modes provide the best balance of power reduction and wake-up time.
- **Clock Generation Management** controls the frequency of internal and external clock signals. Clock signals for currently inactive parts of logic are disabled automatically. The user can drastically reduce the consumed power by reducing the XC228x system clock frequency.
  External circuits can be controlled using the programmable frequency output EXTCLK.
- **Peripheral Management** permits temporary disabling of peripheral modules. Each peripheral can be disabled and enabled separately. The CPU can be switched off while the peripherals can continue to operate.

Wake-up from power reduction modes can be triggered either externally with signals generated by the external system, or internally by the on-chip wake-up timer. This supports intermittent operation of the XC228x by generating cyclic wake-up signals. Full performance is available to quickly react to action requests while the intermittent sleep phases greatly reduce the average system power consumption.

*Note: When selecting the supply voltage and the clock source and generation method, the required parameters must be carefully written to the respective bitfields, to avoid unintended intermediate states. Recommended sequences are provided which ensure the intended operation of power supply system and clock system. Please refer to the Programmer's Guide.*

**Table 10 Instruction Set Summary** (cont'd)

| Mnemonic | Description | Bytes |
|---|---|---|
| ROL/ROR | Rotate left/right direct word GPR | 2 |
| ASHR | Arithmetic (sign bit) shift right direct word GPR | 2 |
| MOV(B) | Move word (byte) data | 2 / 4 |
| MOVBS/Z | Move byte operand to word op. with sign/zero extension | 2 / 4 |
| JMPA/I/R | Jump absolute/indirect/relative if condition is met | 4 |
| JMPS | Jump absolute to a code segment | 4 |
| JB(C) | Jump relative if direct bit is set (and clear bit) | 4 |
| JNB(S) | Jump relative if direct bit is not set (and set bit) | 4 |
| CALLA/I/R | Call absolute/indirect/relative subroutine if condition is met | 4 |
| CALLS | Call absolute subroutine in any code segment | 4 |
| PCALL | Push direct word register onto system stack and call absolute subroutine | 4 |
| TRAP | Call interrupt service routine via immediate trap number | 2 |
| PUSH/POP | Push/pop direct word register onto/from system stack | 2 |
| SCXT | Push direct word register onto system stack and update register with word operand | 4 |
| RET(P) | Return from intra-segment subroutine (and pop direct word register from system stack) | 2 |
| RETS | Return from inter-segment subroutine | 2 |
| RETI | Return from interrupt service subroutine | 2 |
| SBRK | Software Break | 2 |
| SRST | Software Reset | 4 |
| IDLE | Enter Idle Mode | 4 |
| PWRDN | Unused instruction[1)] | 4 |
| SRVWDT | Service Watchdog Timer | 4 |
| DISWDT/ENWDT | Disable/Enable Watchdog Timer | 4 |
| EINIT | End-of-Initialization Register Lock | 4 |
| ATOMIC | Begin ATOMIC sequence | 2 |
| EXTR | Begin EXTended Register sequence | 2 |
| EXTP(R) | Begin EXTended Page (and Register) sequence | 2 / 4 |
| EXTS(R) | Begin EXTended Segment (and Register) sequence | 2 / 4 |

**Table 10 Instruction Set Summary** (cont'd)

| Mnemonic | Description | Bytes |
|---|---|---|
| NOP | Null operation | 2 |
| CoMUL/CoMAC | Multiply (and accumulate) | 4 |
| CoADD/CoSUB | Add/Subtract | 4 |
| Co(A)SHR | (Arithmetic) Shift right | 4 |
| CoSHL | Shift left | 4 |
| CoLOAD/STORE | Load accumulator/Store MAC register | 4 |
| CoCMP | Compare | 4 |
| CoMAX/MIN | Maximum/Minimum | 4 |
| CoABS/CoRND | Absolute value/Round accumulator | 4 |
| CoMOV | Data move | 4 |
| CoNEG/NOP | Negate accumulator/Null operation | 4 |

1) The Enter Power Down Mode instruction is not used in the XC228x, due to the enhanced power control scheme. PWRDN will be correctly decoded, but will trigger no action.

## Operating Conditions

The following operating conditions must not be exceeded to ensure correct operation of the XC228x. All parameters specified in the following sections refer to these operating conditions, unless otherwise noticed.

**Table 12 Operating Condition Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Digital core supply voltage | $V_{DDI}$ | 1.4 | – | 1.6 | V | |
| Core Supply Voltage Difference | ΔVDDI | -10 | – | +10 | mV | $V_{DDIM}$ - $V_{DDI1}$ [1] |
| Digital supply voltage for IO pads and voltage regulators, upper voltage range | $V_{DDPA}$, $V_{DDPB}$ | 4.5 | – | 5.5 | V | [2] |
| Digital supply voltage for IO pads and voltage regulators, lower voltage range | $V_{DDPA}$, $V_{DDPB}$ | 3.0 | – | 4.5 | V | [2] |
| Digital ground voltage | $V_{SS}$ | 0 | – | 0 | V | Reference voltage |
| Overload current | $I_{OV}$ | -5 | – | 5 | mA | Per IO pin [3][4] |
| | | -2 | – | 5 | mA | Per analog input pin [3][4] |
| Overload positive current coupling factor for analog inputs [5] | $K_{OVA}$ | – | $1.0 \times 10^{-6}$ | $1.0 \times 10^{-4}$ | – | $I_{OV} > 0$ |
| Overload negative current coupling factor for analog inputs [5] | $K_{OVA}$ | – | $2.5 \times 10^{-4}$ | $1.5 \times 10^{-3}$ | – | $I_{OV} < 0$ |
| Overload positive current coupling factor for digital I/O pins [5] | $K_{OVD}$ | – | $1.0 \times 10^{-4}$ | $5.0 \times 10^{-3}$ | – | $I_{OV} > 0$ |
| Overload negative current coupling factor for digital I/O pins [5] | $K_{OVD}$ | – | $1.0 \times 10^{-2}$ | $3.0 \times 10^{-2}$ | – | $I_{OV} < 0$ |
| Absolute sum of overload currents | Σ\|IOV\| | – | – | 50 | mA | [4] |

### Parameter Interpretation

The parameters listed in the following include both the characteristics of the XC228x and its demands on the system. To aid in correctly interpreting the parameters when evaluating them for a design, they are marked accordingly in the column “Symbol”:

**CC** (**C**ontroller **C**haracteristics):
The logic of the XC228x provides signals with the specified characteristics.

**SR** (**S**ystem **R**equirement):
The external system must provide signals with the specified characteristics to the XC228x.

## 4.4 System Parameters

The following parameters specify several aspects which are important when integrating the XC228x into an application system.

*Note: These parameters are not subject to production test but verified by design and/or characterization.*

**Table 20 Various System Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Supply watchdog (SWD) supervision level (see Table 21) | $V_{SWD}$ CC | $V_{LV}$ - 0.150 | $V_{LV}$ | $V_{LV}$ + 0.100 | V | $V_{LV}$ = selected voltage in upper voltage area |
| | | $V_{LV}$ - 0.125 | $V_{LV}$ | $V_{LV}$ + 0.050 | V | $V_{LV}$ = selected voltage in lower voltage area |
| Core voltage (PVC) supervision level (see Table 22) | $V_{PVC}$ CC | $V_{LV}$ - 0.070 | $V_{LV}$ | $V_{LV}$ + 0.030 | V | $V_{LV}$ = selected voltage |
| Current control limit | $I_{CC}$ CC | 13 | – | 30 | mA | Power domain DMP_M |
| | | 90 | – | 150 | mA | Power domain DMP_1 |
| Wakeup clock source frequency | $f_{WU}$ CC | 400 | 500 | 600 | kHz | FREQSEL = $00_B$ |
| Internal clock source frequency | $f_{INT}$ CC | 4.8 | 5.0 | 5.2 | MHz | |
| Startup time from stopover mode | $t_{SSO}$ CC | 200 | 260 | 320 | µs | User instruction from PSRAM |
| Startup time from standby mode | $t_{SSB}$ CC | 2.5 | 2.8 | 3.5 | ms | User instruction from Flash |

## 4.5 Flash Memory Parameters

The XC228x is delivered with all Flash sectors erased and with no protection installed.

The data retention time of the XC228x's Flash memory (i.e. the time after which stored data can still be retrieved) depends on the number of times the Flash memory has been erased and programmed.

*Note: These parameters are not subject to production test but verified by design and/or characterization.*

**Table 23 Flash Characteristics (Operating Conditions apply)**

| Parameter | Symbol | Limit Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Programming time per 128-byte page | $t_{PR}$ | – | 3[1)] | 3.5 | ms | ms |
| Erase time per sector/page | $t_{ER}$ | – | 4[1)] | 5 | ms | ms |
| Data retention time | $t_{RET}$ | 20 | – | – | years | 1,000 erase / program cycles |
| Flash erase endurance for user sectors[2)] | $N_{ER}$ | 15,000 | – | – | cycles | Data retention time 5 years |
| Flash erase endurance for security pages | $N_{SEC}$ | 10 | – | – | cycles | Data retention time 20 years |
| Drain disturb limit | $N_{DD}$ | 64 | – | – | cycles | 3) |

1) Programming and erase times depend on the internal Flash clock source. The control state machine needs a few system clock cycles. This requirement is only relevant for extremely low system frequencies.
In the XC228x erased areas must be programmed completely (with actual code/data or dummy values) before that area is read.

2) A maximum of 64 Flash sectors can be cycled 15,000 times. For all other sectors the limit is 1,000 cycles.

3) This parameter limits the number of subsequent programming operations within a physical sector. The drain disturb limit is applicable if wordline erase is used repeatedly. For normal sector erase/program cycles this limit will not be violated.

Access to the XC228x Flash modules is controlled by the IMB. Built-in prefetch mechanisms optimize the performance for sequential access.

Flash access waitstates only affect non-sequential access. Due to prefetch mechanisms, the performance for sequential access (depending on the software structure) is only partially influenced by waitstates.

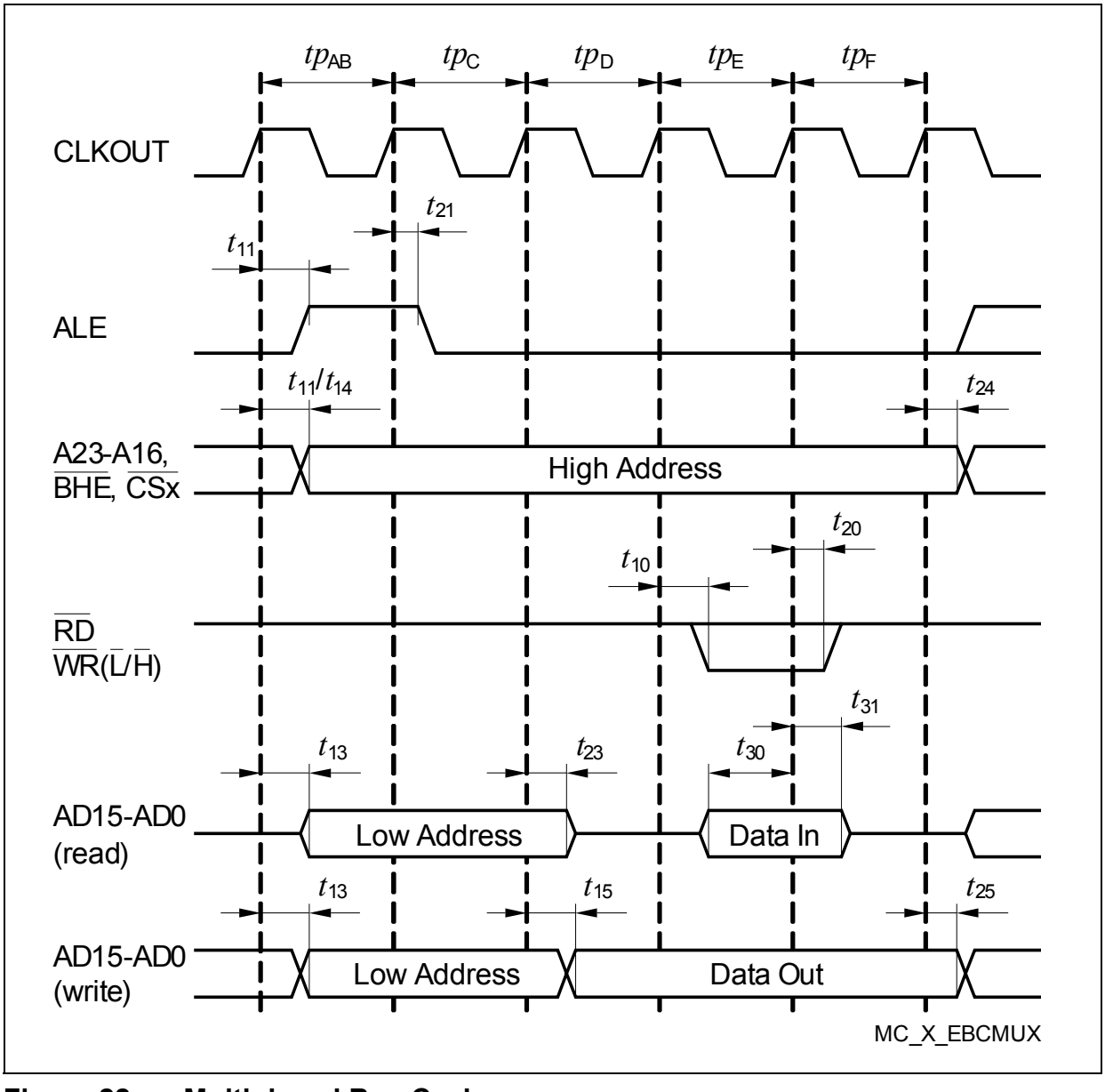


**Figure 22 Multiplexed Bus Cycle**

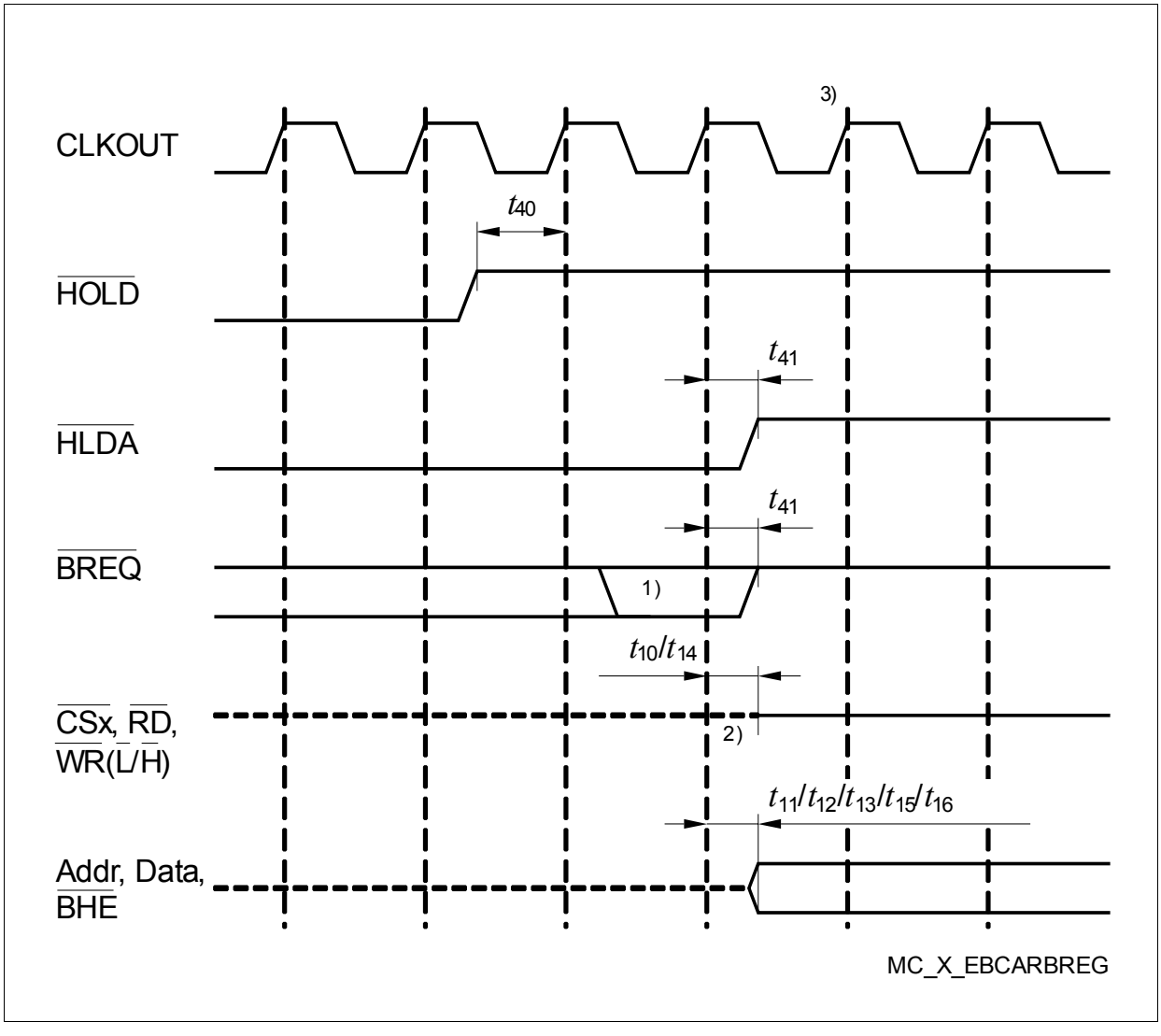


**Figure 26 External Bus Arbitration, Regaining the Bus**

**Notes**

1. *This is the last chance for $\overline{BREQ}$ to trigger the indicated regain sequence. Even if $\overline{BREQ}$ is activated earlier, the regain sequence is initiated by $\overline{HOLD}$ going high. Please note that $\overline{HOLD}$ may also be deactivated without the XC228x requesting the bus.*
2. *The control outputs will be resistive high (pull-up) before being driven inactive (ALE will be low).*
3. *The next XC228x-driven bus cycle may start here.*