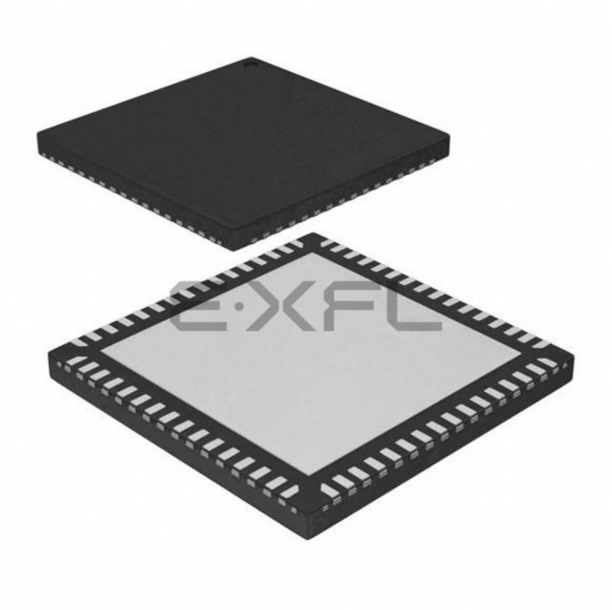
# Silicon Labs - EFM32WG940F64-QFN64T Datasheet



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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| **Details** | |
|---|---|
| Product Status | Discontinued at Digi-Key |
| Core Processor | ARM® Cortex®-M4F |
| Core Size | 32-Bit Single-Core |
| Speed | 48MHz |
| Connectivity | I²C, IrDA, SmartCard, SPI, UART/USART, USB |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, LCD, POR, PWM, WDT |
| Number of I/O | 52 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 32K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.98V ~ 3.8V |
| Data Converters | A/D 8x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-VFQFN Exposed Pad |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/silicon-labs/efm32wg940f64-qfn64t |

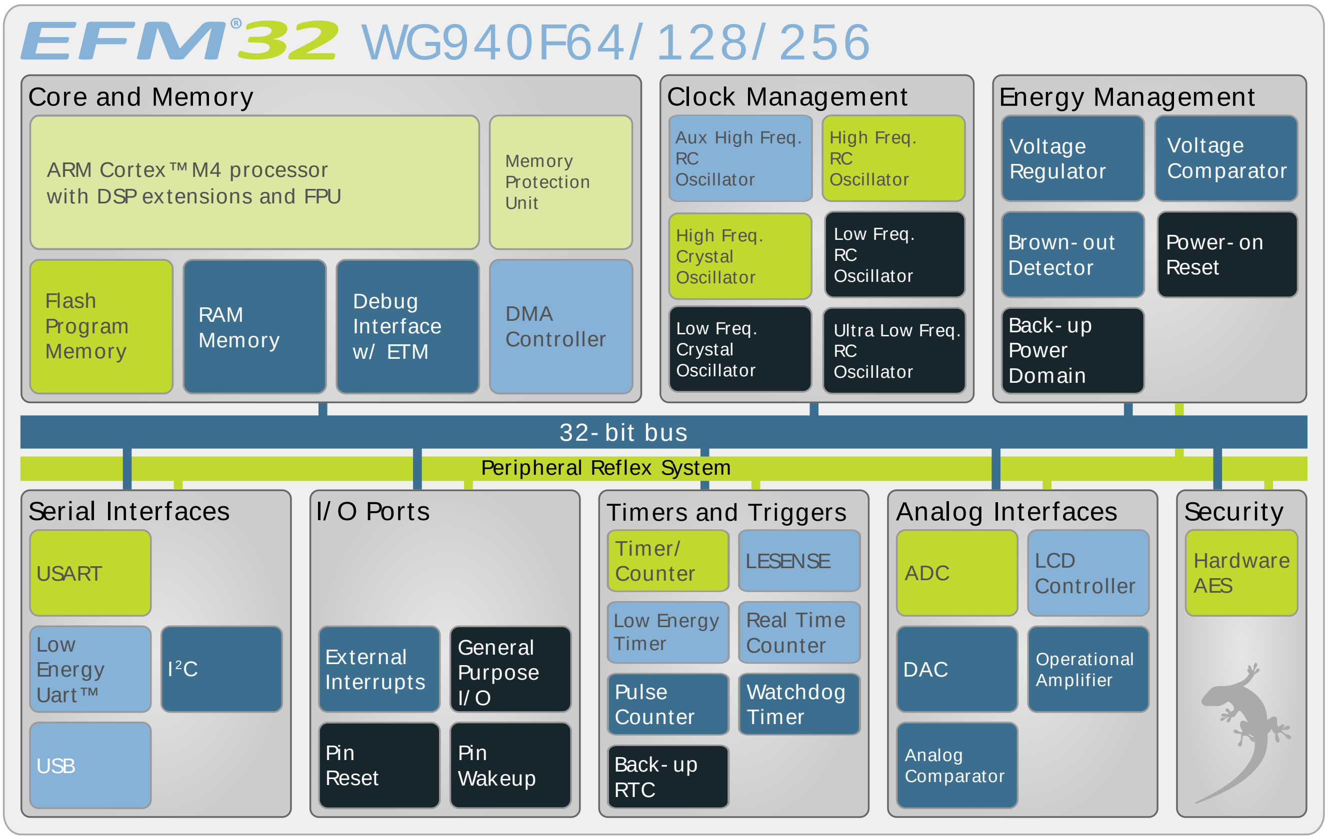
# 2 System Summary

## 2.1 System Introduction

The EFM32 MCUs are the world's most energy friendly microcontrollers. With a unique combination of the powerful 32-bit ARM Cortex-M4, with DSP instruction support and floating-point unit, innovative low energy techniques, short wake-up time from energy saving modes, and a wide selection of peripherals, the EFM32WG microcontroller is well suited for any battery operated application as well as other systems requiring high performance and low-energy consumption. This section gives a short introduction to each of the modules in general terms and also shows a summary of the configuration for the EFM32WG940 devices. For a complete feature set and in-depth information on the modules, the reader is referred to the *EFM32WG Reference Manual*.

A block diagram of the EFM32WG940 is shown in Figure 2.1 (p. 3) .

***Figure 2.1. Block Diagram***



### 2.1.1 ARM Cortex-M4 Core

The ARM Cortex-M4 includes a 32-bit RISC processor, with DSP instruction support and floating-point unit, which can achieve as much as 1.25 Dhrystone MIPS/MHz. A Memory Protection Unit with support for up to 8 memory segments is included, as well as a  Wake-up Interrupt Controller handling interrupts triggered while the CPU is asleep. The EFM32 implementation of the Cortex-M4 is described in detail in *ARM Cortex-M4 Devices Generic User Guide*.

### 2.1.2 Debug Interface (DBG)

This device includes hardware debug support through a 2-pin serial-wire debug interface and an Embedded Trace Module (ETM) for data/instruction tracing.  In addition there is also a 1-wire Serial Wire Viewer pin which can be used to output profiling information, data trace and software-generated messages.

## 2.1.3 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the EFM32WG microcontroller. The flash memory is readable and writable from both the Cortex-M4 and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block. Additionally, the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in the energy modes EM0 and EM1.

## 2.1.4 Direct Memory Access Controller (DMA)

The Direct Memory Access (DMA) controller performs memory operations independently of the CPU. This has the benefit of reducing the energy consumption and the workload of the CPU, and enables the system to stay in low energy modes when moving for instance data from the USART to RAM or from the External Bus Interface to a PWM-generating timer. The DMA controller uses the PL230 µDMA controller licensed from ARM.

## 2.1.5 Reset Management Unit (RMU)

The RMU is responsible for handling the reset functionality of the EFM32WG.

## 2.1.6 Energy Management Unit (EMU)

The Energy Management Unit (EMU) manage all the low energy modes (EM) in EFM32WG microcontrollers. Each energy mode manages if the CPU and the various peripherals are available. The EMU can also be used to turn off the power to unused SRAM blocks.

## 2.1.7 Clock Management Unit (CMU)

The Clock Management Unit (CMU) is responsible for controlling the oscillators and clocks on-board the EFM32WG. The CMU provides the capability to turn on and off the clock on an individual basis to all peripheral modules in addition to enable/disable and configure the available oscillators. The high degree of flexibility enables software to minimize energy consumption in any specific application by not wasting power on peripherals and oscillators that are inactive.

## 2.1.8 Watchdog (WDOG)

The purpose of the watchdog timer is to generate a reset in case of a system failure, to increase application reliability. The failure may e.g. be caused by an external event, such as an ESD pulse, or by a software failure.

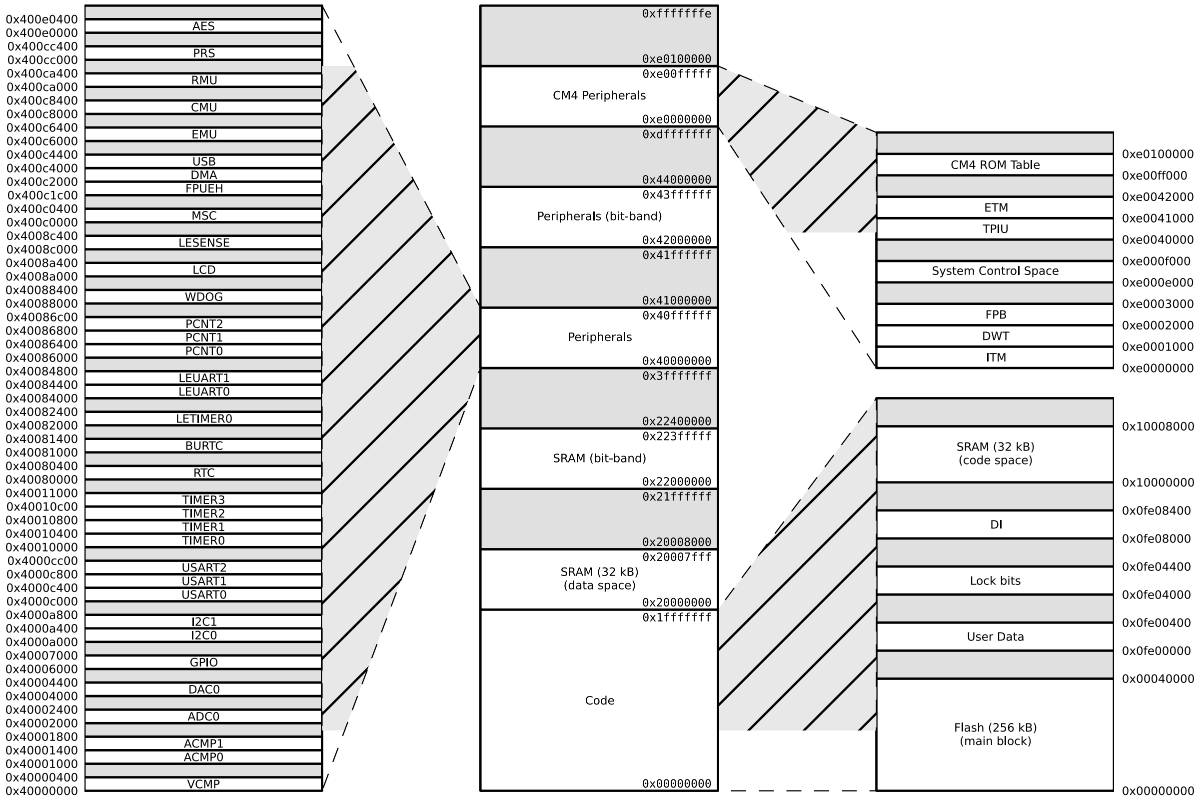
## 2.1.9 Peripheral Reflex System (PRS)

The Peripheral Reflex System (PRS) system is a network which lets the different peripheral module communicate directly with each other without involving the CPU. Peripheral modules which send out Reflex signals are called producers. The PRS routes these reflex signals to consumer peripherals which apply actions depending on the data received. The format for the Reflex signals is not given, but edge triggers and other functionality can be applied by the PRS.

## 2.1.10 Universal Serial Bus Controller (USB)

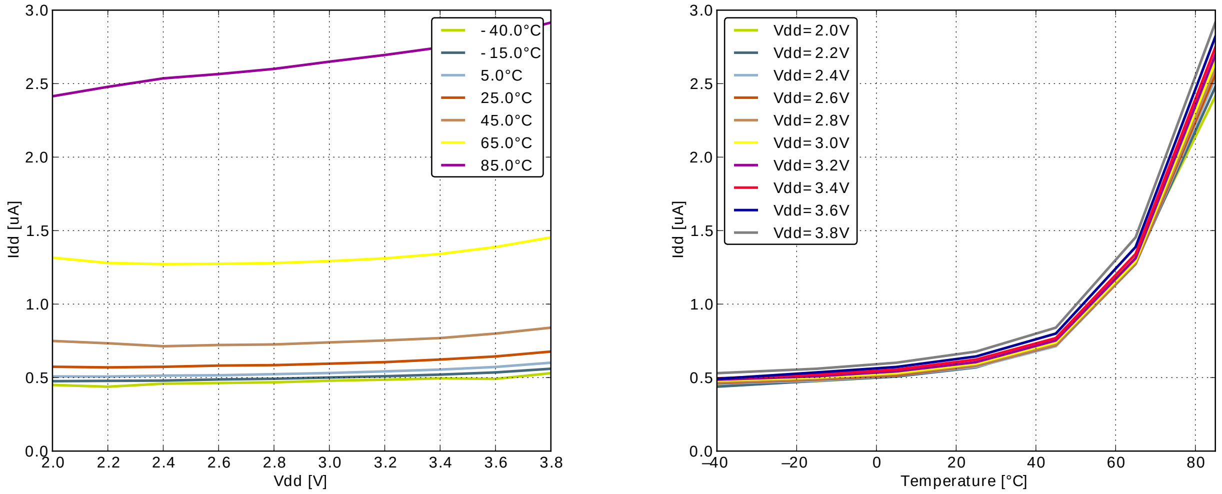
The USB is a full-speed USB 2.0 compliant OTG host/device controller. The USB can be used in Device, On-the-go (OTG) Dual Role Device or Host-only configuration. In OTG mode the USB supports both Host Negotiation Protocol (HNP) and Session Request Protocol (SRP). The device supports both full-speed (12MBit/s) and low speed (1.5MBit/s) operation. The USB device includes an internal dedicated

***Figure 2.2. EFM32WG940 Memory Map with largest RAM and Flash sizes***



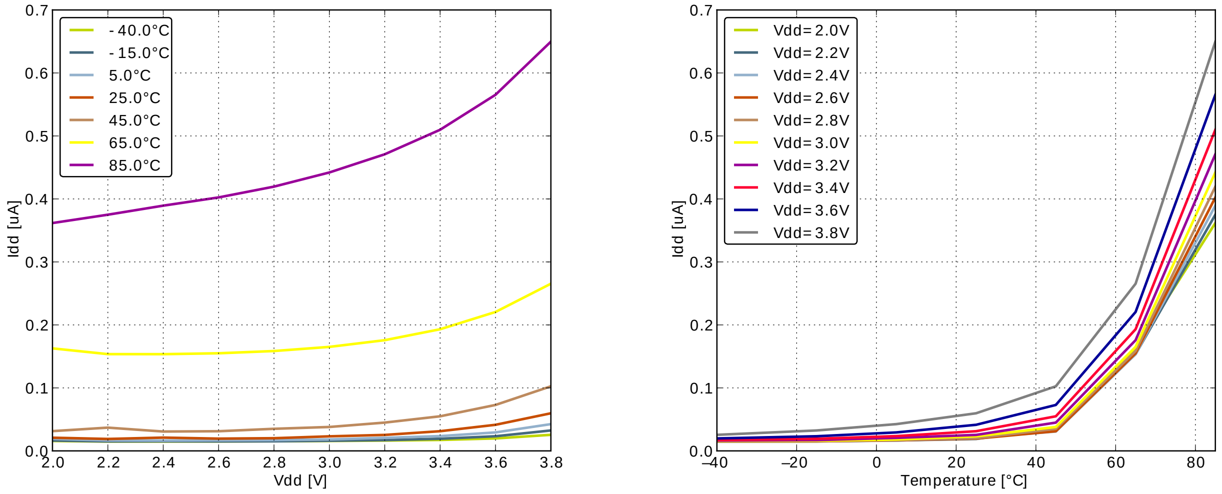
### 3.4.3 EM3 Current Consumption

*Figure 3.9. EM3 current consumption.*



### 3.4.4 EM4 Current Consumption

*Figure 3.10. EM4 current consumption.*



## 3.5 Transition between Energy Modes

The transition times are measured from the trigger to the first clock edge in the CPU.

*Table 3.5. Energy Modes Transitions*

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{EM10}$ | Transition time from EM1 to EM0 | | 0 | | HF-CORE-CLK cycles |
| $t_{EM20}$ | Transition time from EM2 to EM0 | | 2 | | µs |
| $t_{EM30}$ | Transition time from EM3 to EM0 | | 2 | | µs |
| $t_{EM40}$ | Transition time from EM4 to EM0 | | 163 | | µs |

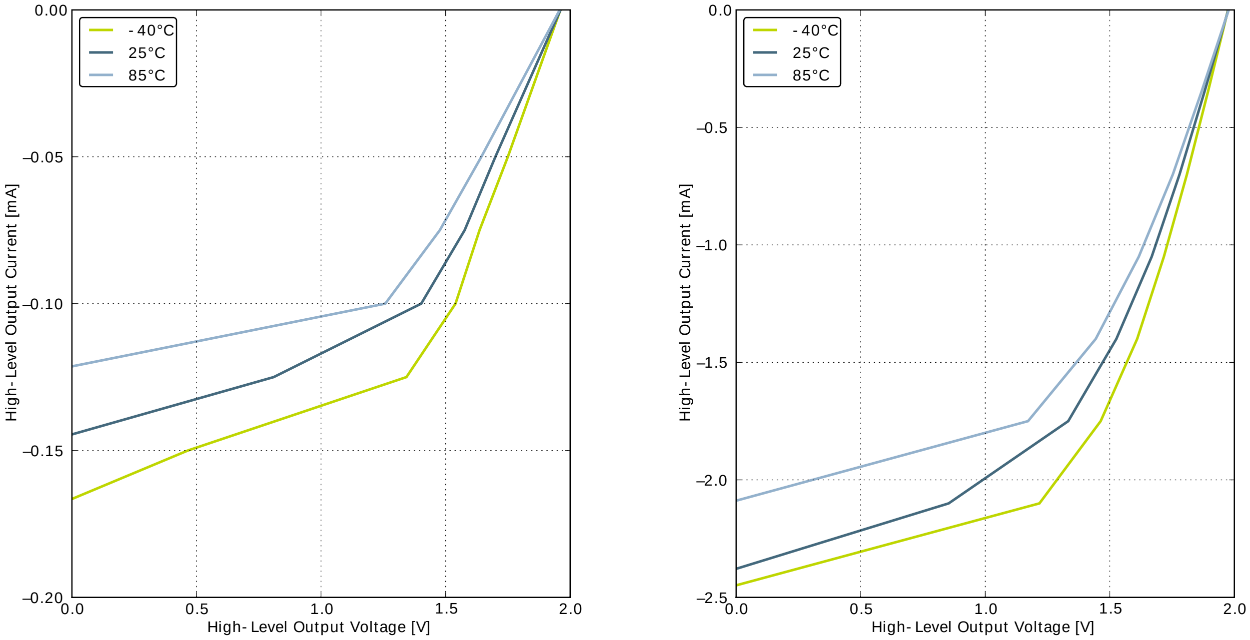
## 3.6 Power Management

The EFM32WG requires the AVDD_x, VDD_DREG and IOVDD_x pins to be connected together (with optional filter) at the PCB level. For practical schematic recommendations, please see the application note, "AN0002 EFM32 Hardware Design Considerations".

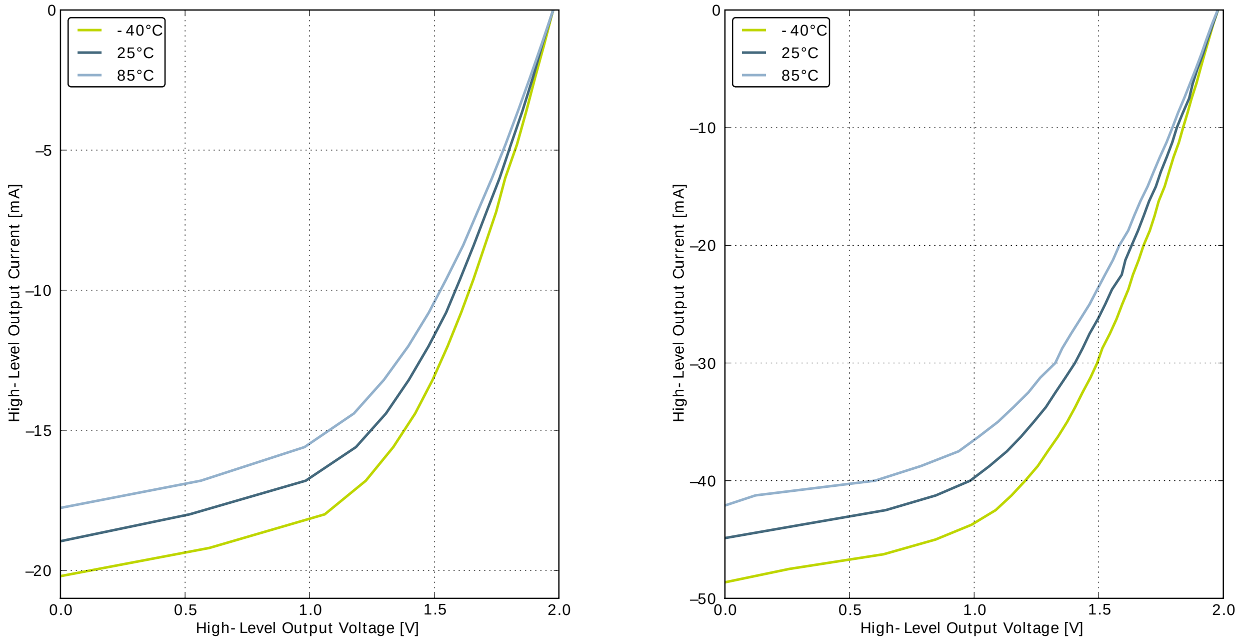
***Table 3.6. Power Management***

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{BODextthr-}$ | BOD threshold on falling external supply voltage | | 1.74 | | 1.96 | V |
| $V_{BODextthr+}$ | BOD threshold on rising external supply voltage | | | 1.85 | 1.98 | V |
| $V_{PORthr+}$ | Power-on Reset (POR) threshold on rising external supply voltage | | | | 1.98 | V |
| $t_{RESET}$ | Delay from reset is released until program execution starts | Applies to Power-on Reset, Brown-out Reset and pin reset. | | 163 | | µs |
| $C_{DECOUPLE}$ | Voltage regulator decoupling capacitor. | X5R capacitor recommended. Apply between DECOUPLE pin and GROUND | | 1 | | µF |
| $C_{USB\_VREGO}$ | USB voltage regulator out decoupling capacitor. | X5R capacitor recommended. Apply between USB_VREGO pin and GROUND | | 1 | | µF |
| $C_{USB\_VREGI}$ | USB voltage regulator in decoupling capacitor. | X5R capacitor recommended. Apply between USB_VREGI pin and GROUND | | 4.7 | | µF |

## Figure 3.12. Typical High-Level Output Current, 2V Supply Voltage

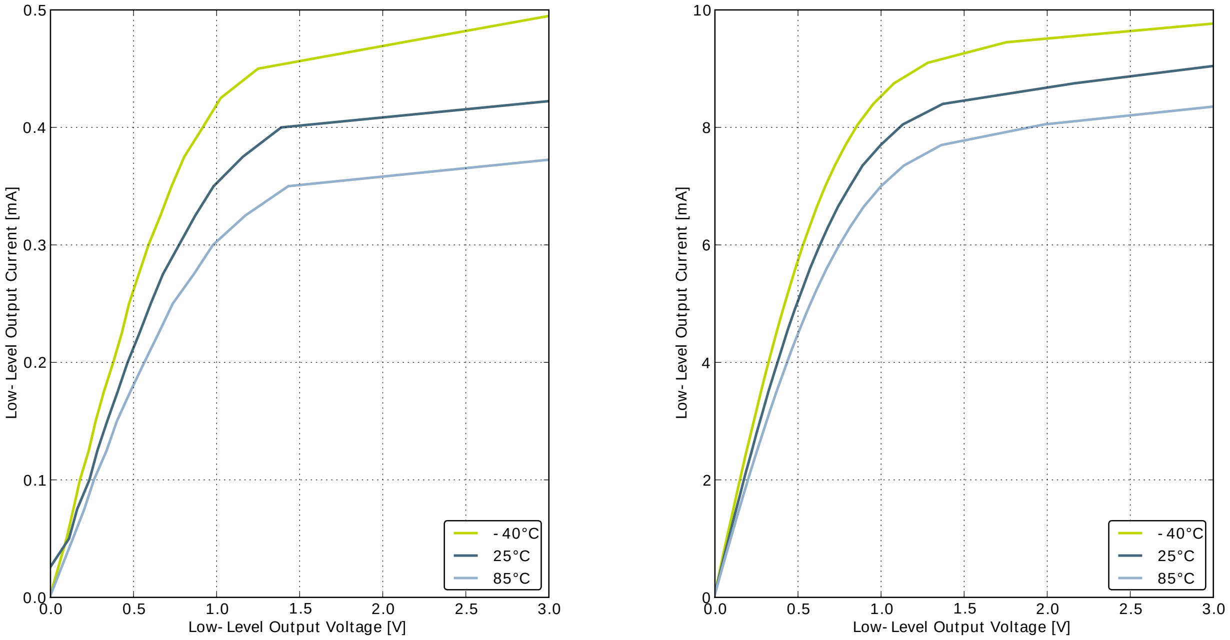


GPIO_Px_CTRL DRIVEMODE = LOWEST GPIO_Px_CTRL DRIVEMODE = LOW



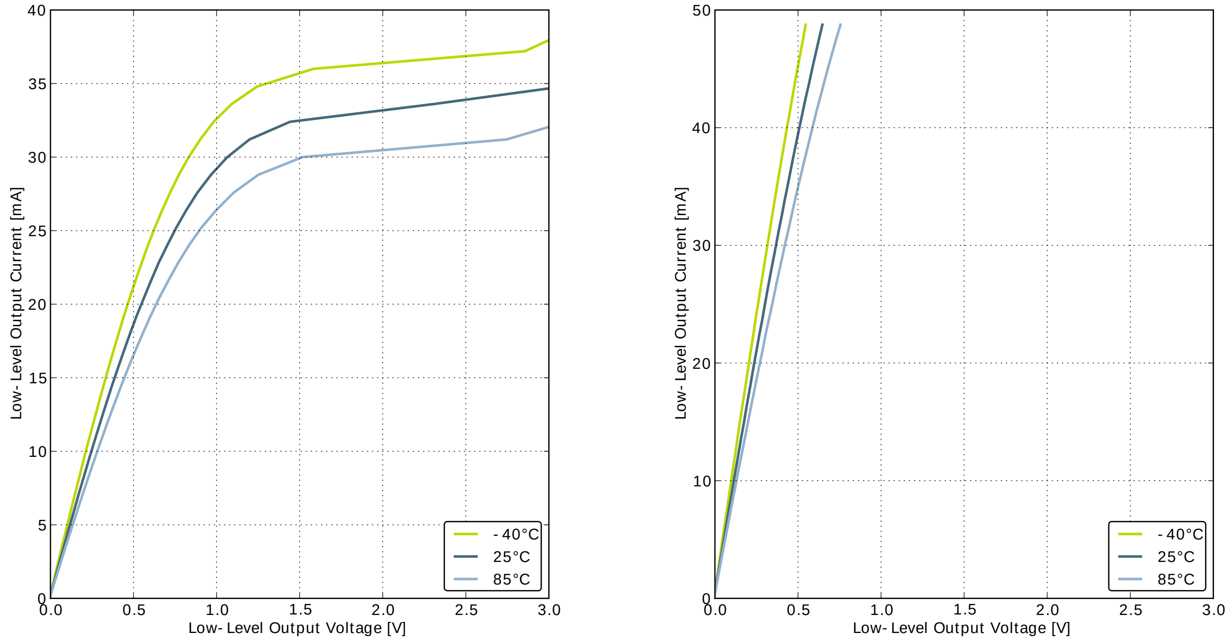
GPIO_Px_CTRL DRIVEMODE = STANDARD GPIO_Px_CTRL DRIVEMODE = HIGH

## *Figure 3.13. Typical Low-Level Output Current, 3V Supply Voltage*



GPIO_Px_CTRL DRIVEMODE = LOWEST

GPIO_Px_CTRL DRIVEMODE = LOW



GPIO_Px_CTRL DRIVEMODE = STANDARD

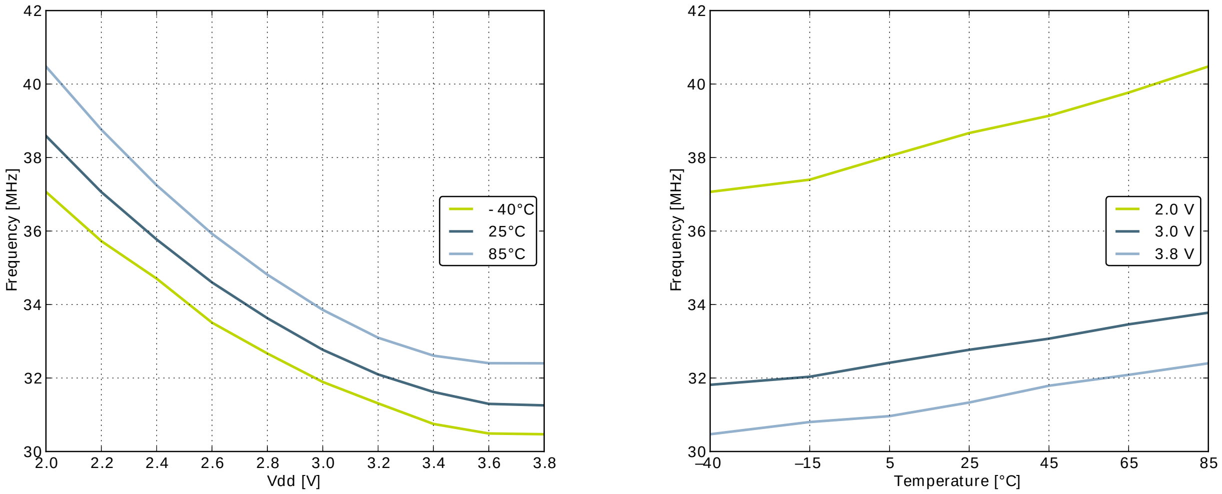
GPIO_Px_CTRL DRIVEMODE = HIGH

### 3.9.3 LFRCO

*Table 3.11. LFRCO*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{LFRCO}$ | Oscillation frequency , $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | | 31.29 | 32.768 | 34.28 | kHz |
| $t_{LFRCO}$ | Startup time not including software calibration | | | 150 | | µs |
| $I_{LFRCO}$ | Current consumption | | | 300 | | nA |
| $TUNESTEP_{LFRCO}$ | Frequency step for LSB change in TUNING value | | | 1.5 | | % |

*Figure 3.17. Calibrated LFRCO Frequency vs Temperature and Supply Voltage*



### 3.9.5 AUXHFRCO

*Table 3.13. AUXHFRCO*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{AUXHFRCO}$ | Oscillation frequency, $V_{DD}$= 3.0 V, $T_{AMB}$=25°C | 28 MHz frequency band | 27.5 | 28.0 | 28.5 | MHz |
| | | 21 MHz frequency band | 20.6 | 21.0 | 21.4 | MHz |
| | | 14 MHz frequency band | 13.7 | 14.0 | 14.3 | MHz |
| | | 11 MHz frequency band | 10.8 | 11.0 | 11.2 | MHz |
| | | 7 MHz frequency band | 6.48 | 6.60 | 6.72 | MHz |
| | | 1 MHz frequency band | 1.15 | 1.20 | 1.25 | MHz |
| $t_{AUXHFRCO\_settling}$ | Settling time after start-up | $f_{AUXHFRCO}$ = 14 MHz | | 0.6 | | Cycles |
| $DC_{AUXHFRCO}$ | Duty cycle | $f_{AUXHFRCO}$ = 14 MHz | 48.5 | 50 | 51 | % |
| $TUNESTEP_{AUXHFRCO}$ | Frequency step for LSB change in TUNING value | | | 0.3[1] | | % |

[1] The TUNING field in the CMU_AUXHFRCOCTRL register may be used to adjust the AUXHFRCO frequency. There is enough adjustment range to ensure that the frequency bands above 7 MHz will always have some overlap across supply voltage and temperature. By using a stable frequency reference such as the LFXO or HFXO, a firmware calibration routine can vary the TUNING bits and the frequency band to maintain the AUXHFRCO frequency at any arbitrary value between 7 MHz and 28 MHz across operating conditions.

### 3.9.6 ULFRCO

*Table 3.14. ULFRCO*

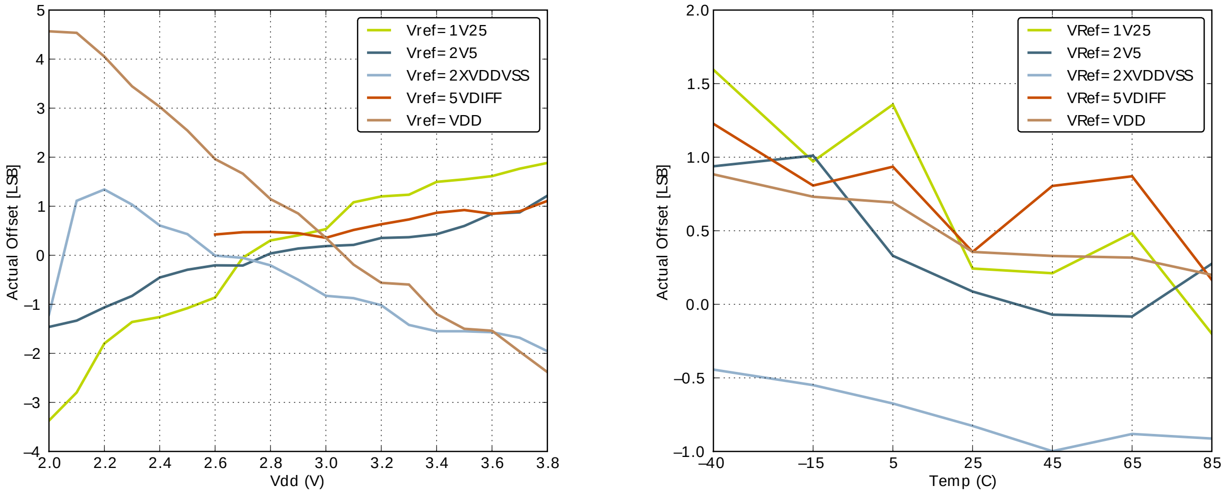
| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $f_{ULFRCO}$ | Oscillation frequency | 25°C, 3V | 0.7 | | 1.75 | kHz |
| $TC_{ULFRCO}$ | Temperature coefficient | | | 0.05 | | %/°C |
| $VC_{ULFRCO}$ | Supply voltage coefficient | | | -18.2 | | %/V |

## 3.10 Analog Digital Converter (ADC)

*Table 3.15. ADC*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{ADCIN}$ | Input voltage range | Single ended | 0 | | $V_{REF}$ | V |
| | | Differential | $-V_{REF}/2$ | | $V_{REF}/2$ | V |
| $V_{ADCREFIN}$ | Input range of external reference voltage, single ended and differential | | 1.25 | | $V_{DD}$ | V |
| $V_{ADCREFIN\_CH7}$ | Input range of external negative reference voltage on channel 7 | See $V_{ADCREFIN}$ | 0 | | $V_{DD}$ - 1.1 | V |
| $V_{ADCREFIN\_CH6}$ | Input range of external positive ref- | See $V_{ADCREFIN}$ | 0.625 | | $V_{DD}$ | V |

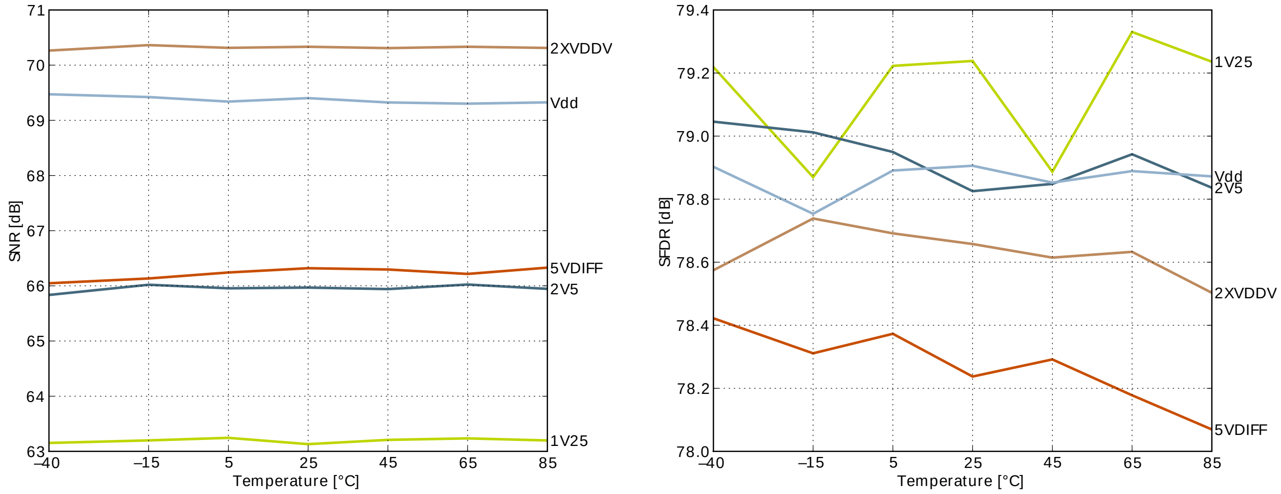
### Figure 3.29. ADC Absolute Offset, Common Mode = Vdd /2



Offset vs Supply Voltage, Temp = 25°C

Offset vs Temperature, Vdd = 3V

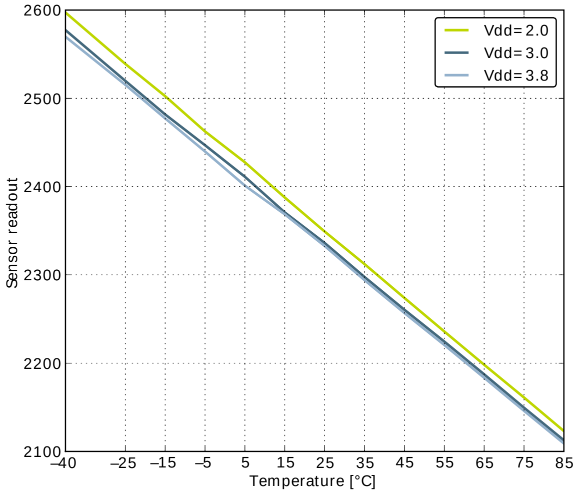
### Figure 3.30. ADC Dynamic Performance vs Temperature for all ADC References, Vdd = 3V



Signal to Noise Ratio (SNR)

Spurious-Free Dynamic Range (SFDR)

*Figure 3.31. ADC Temperature sensor readout*



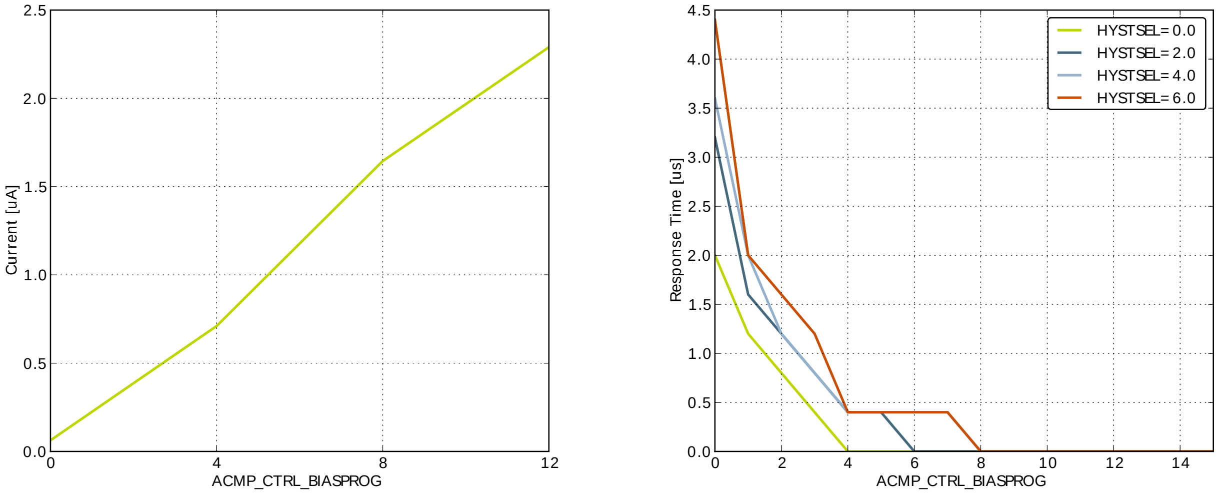
## 3.11 Digital Analog Converter (DAC)

*Table 3.16. DAC*

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DACOUT}$ | Output voltage range | VDD voltage reference, single ended | 0 | | $V_{DD}$ | V |
| | | VDD voltage reference, differential | $-V_{DD}$ | | $V_{DD}$ | V |
| $V_{DACCM}$ | Output common mode voltage range | | 0 | | $V_{DD}$ | V |
| $I_{DAC}$ | Active current including references for 2 channels | 500 kSamples/s, 12 bit | | 400[1] | | µA |
| | | 100 kSamples/s, 12 bit | | 200[1] | | µA |
| | | 1 kSamples/s 12 bit NORMAL | | 17[1] | | µA |
| $SR_{DAC}$ | Sample rate | | | | 500 | ksamples/s |
| $f_{DAC}$ | DAC clock frequency | Continuous Mode | | | 1000 | kHz |
| | | Sample/Hold Mode | | | 250 | kHz |
| | | Sample/Off Mode | | | 250 | kHz |
| $CYC_{DACCONV}$ | Clock cyckles per conversion | | | 2 | | |
| $t_{DACCONV}$ | Conversion time | | 2 | | | µs |
| $t_{DACSETTLE}$ | Settling time | | | 5 | | µs |
| $SNR_{DAC}$ | Signal to Noise Ratio (SNR) | 500 kSamples/s, 12 bit, single ended, internal 1.25V reference | | 58 | | dB |
| | | 500 kSamples/s, 12 bit, single ended, internal 2.5V reference | | 59 | | dB |
| | | 500 kSamples/s, 12 bit, differential, internal 1.25V reference | | 58 | | dB |

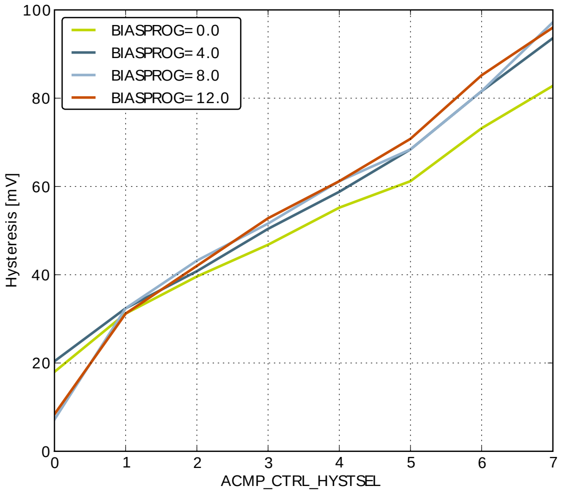
| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | | (OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1, Unity Gain | | 13 | 25 | µA |
| $G_{OL}$ | Open Loop Gain | (OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0 | | 101 | | dB |
| | | (OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1 | | 98 | | dB |
| | | (OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1 | | 91 | | dB |
| $GBW_{OPAMP}$ | Gain Bandwidth Product | (OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0 | | 6.1 | | MHz |
| | | (OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1 | | 1.8 | | MHz |
| | | (OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1 | | 0.25 | | MHz |
| $PM_{OPAMP}$ | Phase Margin | (OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0, $C_L$=75 pF | | 64 | | ° |
| | | (OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1, $C_L$=75 pF | | 58 | | ° |
| | | (OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1, $C_L$=75 pF | | 58 | | ° |
| $R_{INPUT}$ | Input Resistance | | | 100 | | Mohm |
| $R_{LOAD}$ | Load Resistance | | 200 | | | Ohm |
| $I_{LOAD\_DC}$ | DC Load Current | | | | 11 | mA |
| $V_{INPUT}$ | Input Voltage | OPAxHCMDIS=0 | $V_{SS}$ | | $V_{DD}$ | V |
| | | OPAxHCMDIS=1 | $V_{SS}$ | | $V_{DD}$-1.2 | V |
| $V_{OUTPUT}$ | Output Voltage | | $V_{SS}$ | | $V_{DD}$ | V |
| $V_{OFFSET}$ | Input Offset Voltage | Unity Gain, $V_{SS}$<$V_{in}$<$V_{DD}$, OPAxHCMDIS=0 | -13 | 0 | 11 | mV |
| | | Unity Gain, $V_{SS}$<$V_{in}$<$_{DD}$-1.2, OPAxHCMDIS=1 | | 1 | | mV |
| $V_{OFFSET\_DRIFT}$ | Input Offset Voltage Drift | | | | 0.02 | mV/°C |
| $SR_{OPAMP}$ | Slew Rate | (OPA2)BIASPROG=0xF, (OPA2)HALFBIAS=0x0 | | 3.2 | | V/µs |
| | | (OPA2)BIASPROG=0x7, (OPA2)HALFBIAS=0x1 | | 0.8 | | V/µs |
| | | (OPA2)BIASPROG=0x0, (OPA2)HALFBIAS=0x1 | | 0.1 | | V/µs |
| $N_{OPAMP}$ | Voltage Noise | $V_{out}$=1V, RESSEL=0, 0.1 Hz<f<10 kHz, OPAxHCMDIS=0 | | 101 | | $\mu V_{RMS}$ |
| | | $V_{out}$=1V, RESSEL=0, 0.1 Hz<f<10 kHz, OPAxHCMDIS=1 | | 141 | | $\mu V_{RMS}$ |

**Figure 3.37. ACMP Characteristics, Vdd = 3V, Temp = 25°C, FULLBIAS = 0, HALFBIAS = 1**



Current consumption, HYSTSEL = 4

Response time



Hysteresis

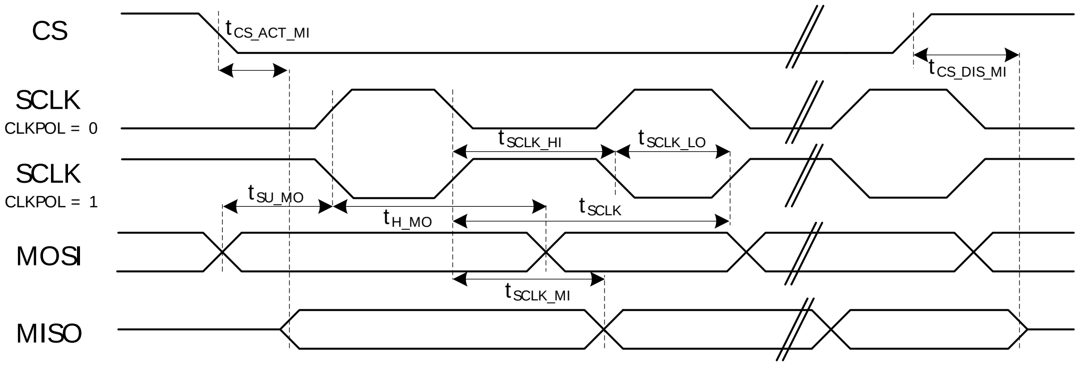
### Table 3.25. SPI Master Timing with SSSEARLY and SMSDELAY

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{SCLK}$ [1,2] | SCLK period | | 2 * $t_{HFPERCLK}$ | | | ns |
| $t_{CS\_MO}$ [1,2] | CS to MOSI | | -2.00 | | 2.00 | ns |
| $t_{SCLK\_MO}$ [1,2] | SCLK to MOSI | | -1.00 | | 3.00 | ns |
| $t_{SU\_MI}$ [1,2] | MISO setup time | IOVDD = 3.0 V | -32.00 | | | ns |
| $t_{H\_MI}$ [1,2] | MISO hold time | | 63.00 | | | ns |

[1] Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)

[2] Measurement done at 10% and 90% of $V_{DD}$ (figure shows 50% of $_{VDD}$)

### Figure 3.39. SPI Slave Timing



### Table 3.26. SPI Slave Timing

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{SCLK\_sl}$ [1,2] | SCKL period | 6 * $t_{HFPERCLK}$ | | | ns |
| $t_{SCLK\_hi}$ [1,2] | SCLK high period | 3 * $t_{HFPERCLK}$ | | | ns |
| $t_{SCLK\_lo}$ [1,2] | SCLK low period | 3 * $t_{HFPERCLK}$ | | | ns |
| $t_{CS\_ACT\_MI}$ [1,2] | CS active to MISO | 5.00 | | 35.00 | ns |
| $t_{CS\_DIS\_MI}$ [1,2] | CS disable to MISO | 5.00 | | 35.00 | ns |
| $t_{SU\_MO}$ [1,2] | MOSI setup time | 5.00 | | | ns |
| $t_{H\_MO}$ [1,2] | MOSI hold time | 2 + 2 * $t_{HFPERCLK}$ | | | ns |
| $t_{SCLK\_MI}$ [1,2] | SCLK to MISO | 7 + $t_{HFPERCLK}$ | | 42 + 2 * $t_{HFPERCLK}$ | ns |

[1] Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)

[2] Measurement done at 10% and 90% of $V_{DD}$ (figure shows 50% of $V_{DD}$)

### Table 3.27. SPI Slave Timing with SSSEARLY and SMSDELAY

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{SCLK\_sl}$ [1,2] | SCKL period | 6 * $t_{HFPERCLK}$ | | | ns |

# 4 Pinout and Package

**Note**

Please refer to the application note "AN0002 EFM32 Hardware Design Considerations" for guidelines on designing Printed Circuit Boards (PCB's) for the EFM32WG940.

## 4.1 Pinout

The *EFM32WG940* pinout is shown in Figure 4.1 (p. 55) and Table 4.1 (p. 55). Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

***Figure 4.1. EFM32WG940 Pinout (top view, not to scale)***

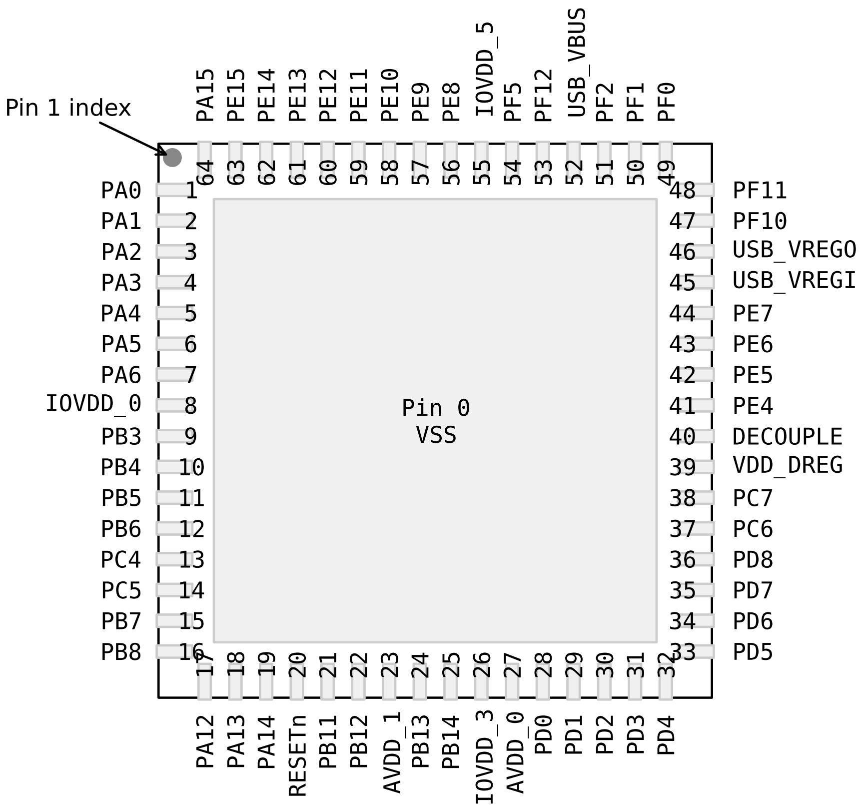


***Table 4.1. Device Pinout***

| QFN64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 0 | VSS | Ground | | | |
| 1 | PA0 | LCD_SEG13 | TIM0_CC0 #0/1/4 | LEU0_RX #4<br>I2C0_SDA #0 | PRS_CH0 #0<br>GPIO_EM4WU0 |
| 2 | PA1 | LCD_SEG14 | TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0<br>PRS_CH1 #0 |

| QFN64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 3 | PA2 | LCD_SEG15 | TIM0_CC2 #0/1 | | CMU_CLK0 #0<br>ETM_TD0 #3 |
| 4 | PA3 | LCD_SEG16 | TIM0_CDTI0 #0 | | LES_ALTEX2 #0<br>ETM_TD1 #3 |
| 5 | PA4 | LCD_SEG17 | TIM0_CDTI1 #0 | | LES_ALTEX3 #0<br>ETM_TD2 #3 |
| 6 | PA5 | LCD_SEG18 | TIM0_CDTI2 #0 | LEU1_TX #1 | LES_ALTEX4 #0<br>ETM_TD3 #3 |
| 7 | PA6 | LCD_SEG19 | | LEU1_RX #1 | ETM_TCLK #3<br>GPIO_EM4WU1 |
| 8 | IOVDD_0 | Digital IO power supply 0. | | | |
| 9 | PB3 | LCD_SEG20/ LCD_COM4 | PCNT1_S0IN #1 | US2_TX #1 | |
| 10 | PB4 | LCD_SEG21/ LCD_COM5 | PCNT1_S1IN #1 | US2_RX #1 | |
| 11 | PB5 | LCD_SEG22/ LCD_COM6 | | US2_CLK #1 | |
| 12 | PB6 | LCD_SEG23/ LCD_COM7 | | US2_CS #1 | |
| 13 | PC4 | ACMP0_CH4<br>DAC0_P0 / OPAMP_P0 | TIM0_CDTI2 #4<br>LETIM0_OUT0 #3<br>PCNT1_S0IN #0 | US2_CLK #0<br>I2C1_SDA #0 | LES_CH4 #0 |
| 14 | PC5 | ACMP0_CH5<br>DAC0_N0 / OPAMP_N0 | LETIM0_OUT1 #3<br>PCNT1_S1IN #0 | US2_CS #0<br>I2C1_SCL #0 | LES_CH5 #0 |
| 15 | PB7 | LFXTAL_P | TIM1_CC0 #3 | US0_TX #4<br>US1_CLK #0 | |
| 16 | PB8 | LFXTAL_N | TIM1_CC1 #3 | US0_RX #4<br>US1_CS #0 | |
| 17 | PA12 | LCD_BCAP_P | TIM2_CC0 #1 | | |
| 18 | PA13 | LCD_BCAP_N | TIM2_CC1 #1 | | |
| 19 | PA14 | LCD_BEXT | TIM2_CC2 #1 | | |
| 20 | RESETn | Reset input, active low.<br>To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | |
| 21 | PB11 | DAC0_OUT0 / OPAMP_OUT0 | TIM1_CC2 #3<br>LETIM0_OUT0 #1 | I2C1_SDA #1 | |
| 22 | PB12 | DAC0_OUT1 / OPAMP_OUT1 | LETIM0_OUT1 #1 | I2C1_SCL #1 | |
| 23 | AVDD_1 | Analog power supply 1. | | | |
| 24 | PB13 | HFXTAL_P | | US0_CLK #4/5<br>LEU0_TX #1 | |
| 25 | PB14 | HFXTAL_N | | US0_CS #4/5<br>LEU0_RX #1 | |
| 26 | IOVDD_3 | Digital IO power supply 3. | | | |
| 27 | AVDD_0 | Analog power supply 0. | | | |
| 28 | PD0 | ADC0_CH0<br>DAC0_OUT0ALT #4/ OPAMP_OUT0ALT<br>OPAMP_OUT2 #1 | PCNT2_S0IN #0 | US1_TX #1 | |
| 29 | PD1 | ADC0_CH1<br>DAC0_OUT1ALT #4/ | TIM0_CC0 #3<br>PCNT2_S1IN #0 | US1_RX #1 | DBG_SWO #2 |

| QFN64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| | | OPAMP_OUT1ALT | | | |
| 30 | PD2 | ADC0_CH2 | TIM0_CC1 #3 | USB_DMPU #0<br>US1_CLK #1 | DBG_SWO #3 |
| 31 | PD3 | ADC0_CH3<br>OPAMP_N2 | TIM0_CC2 #3 | US1_CS #1 | ETM_TD1 #0/2 |
| 32 | PD4 | ADC0_CH4<br>OPAMP_P2 | | LEU0_TX #0 | ETM_TD2 #0/2 |
| 33 | PD5 | ADC0_CH5<br>OPAMP_OUT2 #0 | | LEU0_RX #0 | ETM_TD3 #0/2 |
| 34 | PD6 | ADC0_CH6<br>DAC0_P1 /<br>OPAMP_P1 | TIM1_CC0 #4<br>LETIM0_OUT0 #0<br>PCNT0_S0IN #3 | US1_RX #2<br>I2C0_SDA #1 | LES_ALTEX0 #0<br>ACMP0_O #2<br>ETM_TD0 #0 |
| 35 | PD7 | ADC0_CH7<br>DAC0_N1 /<br>OPAMP_N1 | TIM1_CC1 #4<br>LETIM0_OUT1 #0<br>PCNT0_S1IN #3 | US1_TX #2<br>I2C0_SCL #1 | CMU_CLK0 #2<br>LES_ALTEX1 #0<br>ACMP1_O #2<br>ETM_TCLK #0 |
| 36 | PD8 | BU_VIN | | | CMU_CLK1 #1 |
| 37 | PC6 | ACMP0_CH6 | | LEU1_TX #0<br>I2C0_SDA #2 | LES_CH6 #0<br>ETM_TCLK #2 |
| 38 | PC7 | ACMP0_CH7 | | LEU1_RX #0<br>I2C0_SCL #2 | LES_CH7 #0<br>ETM_TD0 #2 |
| 39 | VDD_DREG | Power supply for on-chip voltage regulator. | | | |
| 40 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin. | | | |
| 41 | PE4 | LCD_COM0 | | US0_CS #1 | |
| 42 | PE5 | LCD_COM1 | | US0_CLK #1 | |
| 43 | PE6 | LCD_COM2 | | US0_RX #1 | |
| 44 | PE7 | LCD_COM3 | | US0_TX #1 | |
| 45 | USB_VREGI | USB Input to internal 3.3 V regulator. | | | |
| 46 | USB_VREGO | USB Decoupling for internal 3.3 V USB regulator and regulator output. | | | |
| 47 | PF10 | | | USB_DM | |
| 48 | PF11 | | | USB_DP | |
| 49 | PF0 | | TIM0_CC0 #5<br>LETIM0_OUT0 #2 | US1_CLK #2<br>LEU0_TX #3<br>I2C0_SDA #5 | DBG_SWCLK #0/1/2/3 |
| 50 | PF1 | | TIM0_CC1 #5<br>LETIM0_OUT1 #2 | US1_CS #2<br>LEU0_RX #3<br>I2C0_SCL #5 | DBG_SWDIO #0/1/2/3<br>GPIO_EM4WU3 |
| 51 | PF2 | LCD_SEG0 | TIM0_CC2 #5 | LEU0_TX #4 | ACMP1_O #0<br>DBG_SWO #0<br>GPIO_EM4WU4 |
| 52 | USB_VBUS | USB 5.0 V VBUS input. | | | |
| 53 | PF12 | | | USB_ID | |
| 54 | PF5 | LCD_SEG3 | TIM0_CDTI2 #2/5 | USB_VBUSEN #0 | PRS_CH2 #1 |
| 55 | IOVDD_5 | Digital IO power supply 5. | | | |
| 56 | PE8 | LCD_SEG4 | PCNT2_S0IN #1 | | PRS_CH3 #1 |
| 57 | PE9 | LCD_SEG5 | PCNT2_S1IN #1 | | |
| 58 | PE10 | LCD_SEG6 | TIM1_CC0 #1 | US0_TX #0 | BOOT_TX |
| 59 | PE11 | LCD_SEG7 | TIM1_CC1 #1 | US0_RX #0 | LES_ALTEX5 #0<br>BOOT_RX |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Functionality** | **0** | **1** | **2** | **3** | **4** | **5** | **6** | **Description** |
| OPAMP_N0 | | | | | | | | |
| DAC0_N1 / OPAMP_N1 | PD7 | | | | | | | Operational Amplifier 1 external negative input. |
| OPAMP_N2 | PD3 | | | | | | | Operational Amplifier 2 external negative input. |
| DAC0_OUT0 / OPAMP_OUT0 | PB11 | | | | | | | Digital to Analog Converter DAC0_OUT0 / OPAMP output channel number 0. |
| DAC0_OUT0ALT / OPAMP_OUT0ALT | | | | | PD0 | | | Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0. |
| DAC0_OUT1 / OPAMP_OUT1 | PB12 | | | | | | | Digital to Analog Converter DAC0_OUT1 / OPAMP output channel number 1. |
| DAC0_OUT1ALT / OPAMP_OUT1ALT | | | | | PD1 | | | Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1. |
| OPAMP_OUT2 | PD5 | PD0 | | | | | | Operational Amplifier 2 output. |
| DAC0_P0 / OPAMP_P0 | PC4 | | | | | | | Operational Amplifier 0 external positive input. |
| DAC0_P1 / OPAMP_P1 | PD6 | | | | | | | Operational Amplifier 1 external positive input. |
| OPAMP_P2 | PD4 | | | | | | | Operational Amplifier 2 external positive input. |
| DBG_SWCLK | PF0 | PF0 | PF0 | PF0 | | | | Debug-interface Serial Wire clock input.<br>Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | PF1 | PF1 | PF1 | | | | Debug-interface Serial Wire data input / output.<br>Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| DBG_SWO | PF2 | | PD1 | PD2 | | | | Debug-interface Serial Wire viewer Output.<br>Note that this function is not enabled after reset, and must be enabled by software to be used. |
| ETM_TCLK | PD7 | | PC6 | PA6 | | | | Embedded Trace Module ETM clock . |
| ETM_TD0 | PD6 | | PC7 | PA2 | | | | Embedded Trace Module ETM data 0. |
| ETM_TD1 | PD3 | | PD3 | PA3 | | | | Embedded Trace Module ETM data 1. |
| ETM_TD2 | PD4 | | PD4 | PA4 | | | | Embedded Trace Module ETM data 2. |
| ETM_TD3 | PD5 | | PD5 | PA5 | | | | Embedded Trace Module ETM data 3. |
| GPIO_EM4WU0 | PA0 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU1 | PA6 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU3 | PF1 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU4 | PF2 | | | | | | | Pin can be used to wake the system up from EM4 |
| GPIO_EM4WU5 | PE13 | | | | | | | Pin can be used to wake the system up from EM4 |
| HFXTAL_N | PB14 | | | | | | | High Frequency Crystal negative pin. Also used as external optional clock input pin. |
| HFXTAL_P | PB13 | | | | | | | High Frequency Crystal positive pin. |
| I2C0_SCL | PA1 | PD7 | PC7 | | | PF1 | PE13 | I2C0 Serial Clock Line input / output. |
| I2C0_SDA | PA0 | PD6 | PC6 | | | PF0 | PE12 | I2C0 Serial Data input / output. |
| I2C1_SCL | PC5 | PB12 | | | | | | I2C1 Serial Clock Line input / output. |
| I2C1_SDA | PC4 | PB11 | | | | | | I2C1 Serial Data input / output. |
| LCD_BCAP_N | PA13 | | | | | | | LCD voltage booster (optional), boost capacitor, negative pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P. |

# 5 PCB Layout and Soldering

## 5.1 Recommended PCB Layout

*Figure 5.1. QFN64 PCB Land Pattern*

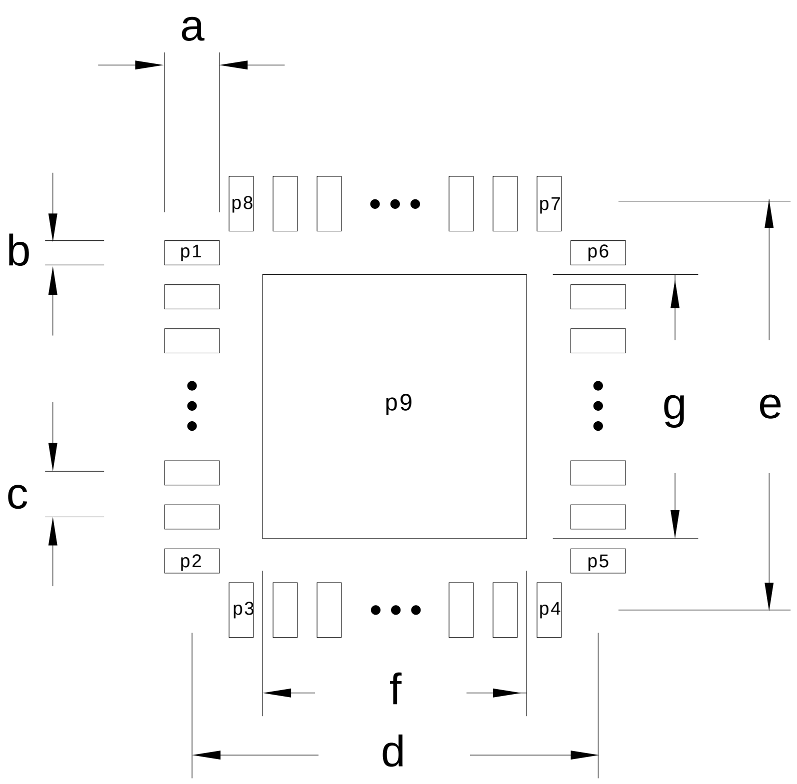


*Table 5.1. QFN64 PCB Land Pattern Dimensions (Dimensions in mm)*

| Symbol | Dim. (mm) | Symbol | Pin number | Symbol | Pin number |
|---|---|---|---|---|---|
| a | 0.85 | P1 | 1 | P8 | 64 |
| b | 0.30 | P2 | 16 | P9 | 65 |
| c | 0.50 | P3 | 17 | - | - |
| d | 8.90 | P4 | 32 | - | - |
| e | 8.90 | P5 | 33 | - | - |
| f | 7.20 | P6 | 48 | - | - |
| g | 7.20 | P7 | 49 | - | - |

# List of Tables