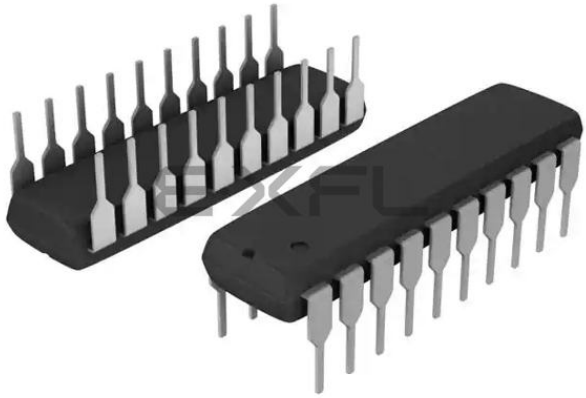

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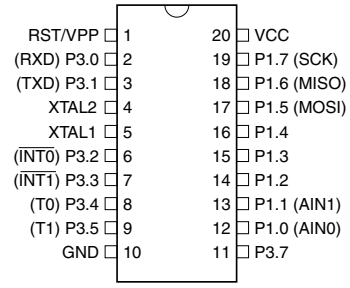
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	24MHz
Connectivity	UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM
Number of I/O	15
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	20-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at89s2051-24pu

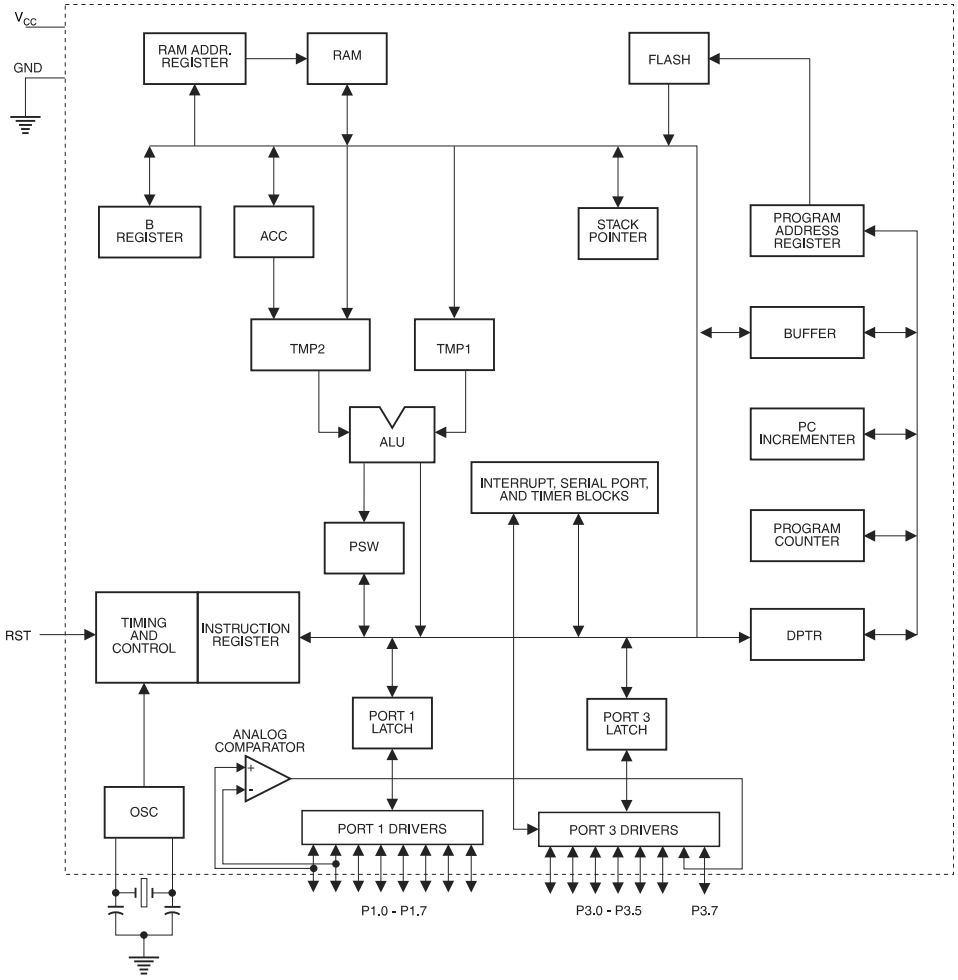
The on-board Flash program memory is accessible through the ISP serial interface. Holding RST active forces the device into a serial programming interface and allows the program memory to be written to or read from, unless one or more lock bits have been activated.

2. Pin Configuration

2.1 20-lead PDIP/SOIC



3. Block Diagram



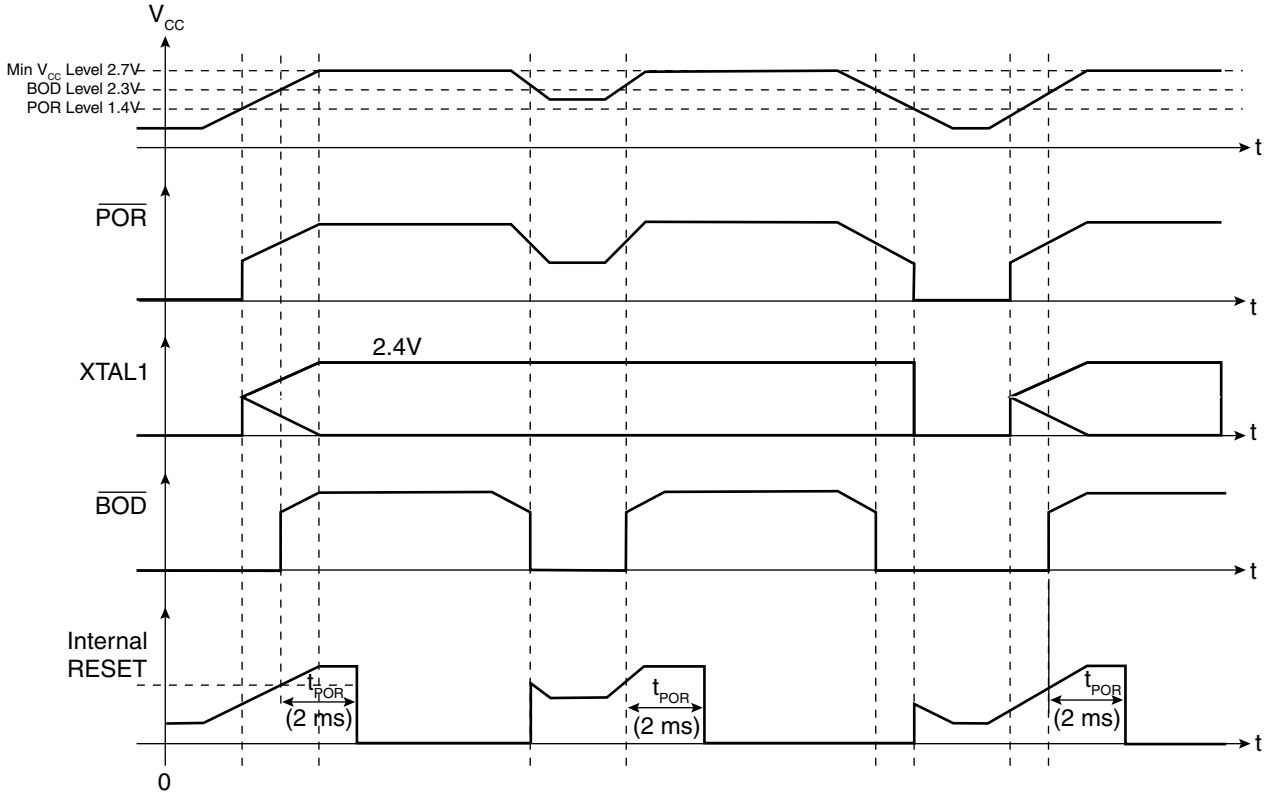
10. Reset

During reset, all I/O Registers are set to their initial values, the port pins are weakly pulled to V_{CC}, and the program starts execution from the Reset Vector, 0000H. The AT89S2051/S4051 has three sources of reset: power-on reset, brown-out reset, and external reset.

10.1 Power-On Reset

A Power-On Reset (POR) is generated by an on-chip detection circuit. The detection level is nominally 1.4V. The POR is activated whenever V_{CC} is below the detection level. The POR circuit can be used to trigger the start-up reset or to detect a supply voltage failure in devices without a brown-out detector. The POR circuit ensures that the device is reset from power-on. When V_{CC} reaches the Power-on Reset threshold voltage, the Pierce Oscillator is enabled (if the XTAL Oscillator Bypass fuse is OFF). Only after V_{CC} has also reached the BOD (brown-out detection) level (see Section 10.2 ”Brown-out Reset”), the BOD delay counter starts measuring a 2-ms delay after which the Internal Reset is deasserted and the microcontroller starts executing. The built-in 2-ms delay allows the V_{CC} voltage to reach the minimum 2.7V level before executing, thus guaranteeing the maximum operating clock frequency. The POR signal is activated again, without any delay, when V_{CC} falls below the POR threshold level. A Power-On Reset (i.e. a cold reset) will set the POF flag in PCON. Refer to Figure 10-1 for details on the POR/BOD behavior.

Figure 10-1. Power-up and Brown-out Detection Sequence



12. Power Saving Modes

The AT89S2051/S4051 supports two power-reducing modes: Idle and Power-down. These modes are accessed through the PCON register.

12.1 Idle Mode

Setting the IDL bit in PCON enters idle mode. Idle mode halts the internal CPU clock. The CPU state is preserved in its entirety, including the RAM, stack pointer, program counter, program status word, and accumulator. The Port pins hold the logical states they had at the time that Idle was activated. Idle mode leaves the peripherals running in order to allow them to wake up the CPU when an interrupt is generated. Timer 0, Timer 1, and the UART will continue to function during Idle mode. The analog comparator is disabled during Idle. Any enabled interrupt source or reset may terminate Idle mode. When exiting Idle mode with an interrupt, the interrupt will immediately be serviced, and following RETI, the next instruction to be executed will be the one following the instruction that put the device into Idle.

P1.0 and P1.1 should be set to “0” if no external pull-ups are used, or set to “1” if external pull-ups are used.

12.2 Power-down Mode

Setting the PD bit in PCON enters Power-down mode. Power-down mode stops the and powers down the Flash memory in order to minimize power consumption. Only the power-on circuitry will continue to draw power during Power-down. During Power-down the power supply voltage may be reduced to the RAM keep-alive voltage. The RAM contents will be retained; however, the SFR contents are not guaranteed once V_{CC} has been reduced. Power-down may be exited by external reset, power-on reset, or certain interrupts.

The user should not attempt to enter (or re-enter) the power-down mode for a minimum of 4 µs until after one of the following conditions has occurred: Start of code execution (after any type of reset), or Exit from power-down mode.

12.3 Interrupt Recovery from Power-down

Two external interrupts may be configured to terminate Power-down mode. External interrupts $\overline{\text{INT0}}$ (P3.2) and $\overline{\text{INT1}}$ (P3.3) may be used to exit Power-down. To wake up by external interrupt $\overline{\text{INT0}}$ or $\overline{\text{INT1}}$, the interrupt must be enabled and configured for level-sensitive operation.

When terminating Power-down by an interrupt, two different wake up modes are available. When PWDEX in CLKREG.2 is zero, the wake up period is internally timed. At the falling edge on the interrupt pin, Power-down is exited, the is restarted, and an internal timer begins counting. The internal clock will not be allowed to propagate and the CPU will not resume execution until after the timer has counted for nominally 2 ms. After the timeout period the interrupt service routine will begin. To prevent the interrupt from re-triggering, the ISR should disable the interrupt before returning. The interrupt pin should be held low until the device has timed out and begun executing.

When PWDEX = 1 the wakeup period is controlled externally by the interrupt. Again, at the falling edge on the interrupt pin, Power-down is exited and the is restarted. However, the internal clock will not propagate and CPU will not resume execution until the **rising edge** of the interrupt pin. After the rising edge on the pin, the interrupt service routine will begin. The interrupt should be held low long enough for the to stabilize.

14. Interrupt Registers

Table 14-1. IE – Interrupt Enable Register

IE = A8H — Reset Value = 00X0 0000B

Bit Addressable

	EA	EC	–	ES	ET1	EX1	ET0	EX0
Bit	7	6	5	4	3	2	1	0

Symbol	Function
EA	Global enable/disable. All interrupts are disabled when EA = 0. When EA = 1, each interrupt source is enabled/disabled by setting/clearing its own enable bit.
EC	Comparator Interrupt Enable
ES	Serial Port Interrupt Enable
ET1	Timer 1 Interrupt Enable
EX1	External Interrupt 1 Enable
ET0	Timer 0 Interrupt Enable
EX0	External Interrupt 0 Enable

Table 14-2. IP – Interrupt Priority Register

IP = B8H — Reset Value = X0X0 0000B

Bit Addressable

	–	PC	–	PS	PT1	PX1	PT0	PX0
Bit	7	6	5	4	3	2	1	0

Symbol	Function
PC	Comparator Interrupt Priority Low
PS	Serial Port Interrupt Priority Low
PT1	Timer 1 Interrupt Priority Low
PX1	External Interrupt 1 Priority Low
PT0	Timer 0 Interrupt Priority Low
PX0	External Interrupt 0 Priority Low

Table 14-3. IPH – Interrupt Priority High Register

IPH = B7H — Reset Value = X0X0 0000B

Not Bit Addressable

	–	PCH	–	PSH	PT1H	PX1H	PT0H	PX0H
Bit	7	6	5	4	3	2	1	0

Symbol	Function
PCH	Comparator Interrupt Priority High
PSH	Serial Port Interrupt Priority High
PT1H	Timer 1 Interrupt Priority High
PX1H	External Interrupt 1 Priority High
PT0H	Timer 0 Interrupt Priority High
PX0H	External Interrupt 0 Priority High

15. Timer/Counters

The AT89S2051/S4051 have two 16-bit Timer/Counters: Timer 0 and Timer 1. The Timer/Counters are identical to those in the AT89C2051/C4051. For more detailed information on the Timer/Counter operation, please click on the document link below:

http://www.atmel.com/dyn/resources/prod_documents/DOC4316.PDF

16. Pulse Width Modulation

Timer 0 and Timer 1 may be configured as an 8-bit pulse width modulator by setting the PWMEN bit in PCON. The generated waveform is output on the Timer 1 input pin, T1. In PWM mode Timer 0 acts as an 8-bit prescaler to select the PWM timebase. Timer 0 is forced into Mode 2 (8-bit auto-reload) by PWMEN and the value in TH0 will determine the clock division from 0 (FFh) to 256 (00h). Timer 1 acts as the 8-bit PWM counter. TL1 counts once on every overflow from TL0. TH1 stores the 8-bit pulse width value. On the FFh-->00h overflow of TL1, the PWM output is set high. When the count in TL1 matches the value in TH1, the PWM output is set low. Therefore, the output pulse width is proportional to the value in TH1. To prevent glitches, writes to TH1 only take effect on the FFh-->00h overflow of TL1. However, a read from TH1 will read the new value at any time after a write to TH1. See Figure 16-1 for PWM waveform example.

Figure 16-1. Pulse Width Modulation (PWM) Output Waveform

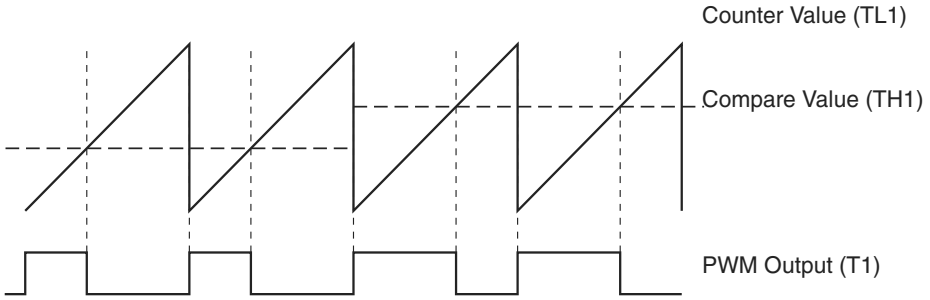
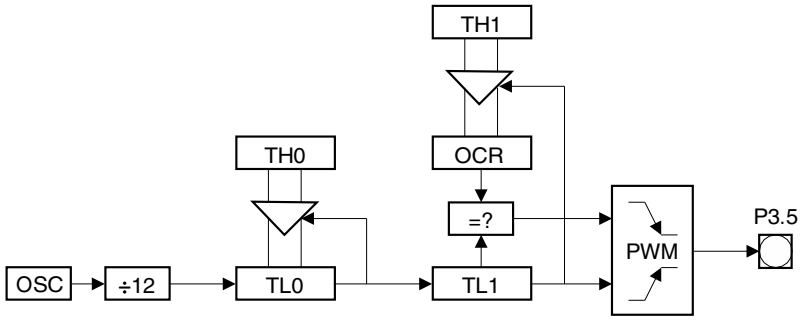


Figure 16-2. Timer 0/1 Pulse Width Modulation Mode



TL0 counts once every machine cycle (1 machine cycle = 12 clocks in X1 mode) and TH0 is the reload value for when TL0 overflows. Every time TL0 overflows TL1 increments by one, with TL0 overflowing after counting 256 minus TH0 machine cycles.

To calculate the pulse width for the PWM output on pin T1, users should use the following formula:

TH1 * (256 - TH0) * (1/clock_freq) * 12 = Pulse Width

be logically ANDed with the SADDR to create the “Given” address which the master will use for addressing each of the slaves. Use of the Given address allows multiple slaves to be recognized while excluding others. The following examples will help to show the versatility of this scheme:

Slave 0 SADDR = 1100 0000

SADEN = 1111 1101

Given = 1100 00X0

Slave 1 SADDR = 1100 0000

SADEN = 1111 1110

Given = 1100 000X

In the previous example SADDR is the same and the SADEN data is used to differentiate between the two slaves. Slave 0 requires a 0 in bit 0 and it ignores bit 1. Slave 1 requires a 0 in bit 1 and bit 0 is ignored. A unique address for slave 0 would be 1100 0010 since slave 1 requires a 0 in bit 1. A unique address for slave 1 would be 1100 0001 since a 1 in bit 0 will exclude slave 0. Both slaves can be selected at the same time by an address which has bit 0 = 0 (for slave 0) and bit 1 = 0 (for slave 1). Thus, both could be addressed with 1100 0000.

In a more complex system the following could be used to select slaves 1 and 2 while excluding slave 0:

Slave 0 SADDR = 1100 0000

SADEN = 1111 1001

Given = 1100 0XX0

Slave 1 SADDR = 1110 0000

SADEN = 1111 1010

Given = 1110 0X0X

Slave 2 SADDR = 1110 0000

SADEN = 1111 1100

Given = 1110 00XX

In the above example the differentiation among the 3 slaves is in the lower 3 address bits. Slave 0 requires that bit 0 = 0 and it can be uniquely addressed by 1110 0110. Slave 1 requires that bit 1 = 0 and it can be uniquely addressed by 1110 and 0101. Slave 2 requires that bit 2 = 0 and its unique address is 1110 0011. To select Slaves 0 and 1 and exclude Slave 2, use address 1110 0100, since it is necessary to make bit 2 = 1 to exclude slave 2.

The Broadcast Address for each slave is created by taking the logical OR of SADDR and SADEN. Zeros in this result are trended as don’t cares. In most cases, interpreting the don’t cares as ones, the broadcast address will be FF hexadecimal.

Upon reset SADDR (SFR address 0A9H) and SADEN (SFR address 0B9H) are loaded with 0s. This produces a given address of all “don’t cares” as well as a Broadcast address of all “don’t cares”. This effectively disables the Automatic Addressing mode and allows the microcontroller to use standard 80C51-type UART drivers which do not make use of this feature.

Table 17-1. SCON – Serial Port Control Register

SCON Address = 98H — Reset Value = 0000 0000B

Bit Addressable

Bit	7	6	5	4	3	2	1	0
	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI

(SMOD = 0/1)[1]

Symbol	Function
FE	Framing error bit. This bit is set by the receiver when an invalid stop bit is detected. The FE bit is not cleared by valid frames but should be cleared by software. The SMOD0 bit must be set to enable access to the FE bit. FE will be set regardless of the state of SMOD.
SM0	Serial Port Mode Bit 0, (SMOD must = 0 to access bit SM0)
SM1	Serial Port Mode Bit 1 SM0 SM1 Mode Description Baud Rate[2] 0 0 0 shift register $f_{osc}/12$ 0 1 1 8-bit UART variable 1 0 2 9-bit UART $f_{osc}/64$ or $f_{osc}/32$ 1 1 3 9-bit UART variable
SM2	Enables the Automatic Address Recognition feature in modes 2 or 3. If SM2 = 1 then RI will not be set unless the received 9th data bit (RB8) is 1, indicating an address, and the received byte is a Given or Broadcast Address. In mode 1, if SM2 = 1 then RI will not be activated unless a valid stop bit was received, and the received byte is a Given or Broadcast Address. In Mode 0, SM2 should be 0.
REN	Enables serial reception. Set by software to enable reception. Clear by software to disable reception.
TB8	The 9th data bit that will be transmitted in modes 2 and 3. Set or clear by software as desired.
RB8	In modes 2 and 3, the 9th data bit that was received. In mode 1, if SM2 = 0, RB8 is the stop bit that was received. In mode 0, RB8 is not used.
TI	Transmit interrupt flag. Set by hardware at the end of the 8th bit time in mode 0, or at the beginning of the stop bit in the other modes, in any serial transmission. Must be cleared by software.
RI	Receive interrupt flag. Set by hardware at the end of the 8th bit time in mode 0, or halfway through the stop bit time in the other modes, in any serial reception (except see SM2). Must be cleared by software.

Notes: 1. SMOD is located at PCON.7.
2. f_{osc} = frequency.

24. Chip Erase

Function:

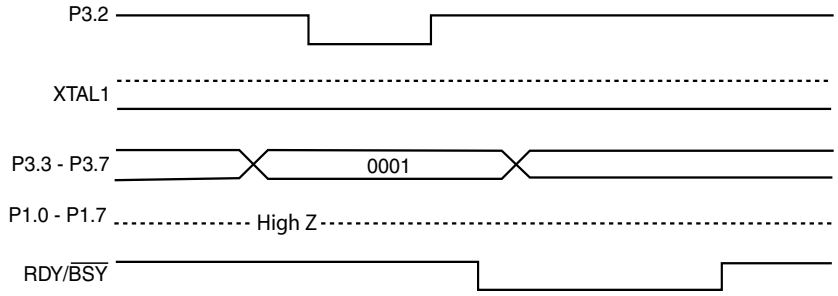
1. FFH programmed to every address location.
2. FFH programmed to User Signature Row if User Row Fuse bit is enabled.
3. Lockbit1 and Lockbit2 programmed to “unlock” state.

Usage:

1. Apply “0001” TestCode to P3.7, P3.5, P3.4, P3.3.
2. Pulse P3.2 low for 1 µs.
3. Wait 4 ms, monitor P3.1, or poll data.

Note: This and the following waveforms are not to scale.

Figure 24-1. Chip Erase Sequence



25. Load X-Address

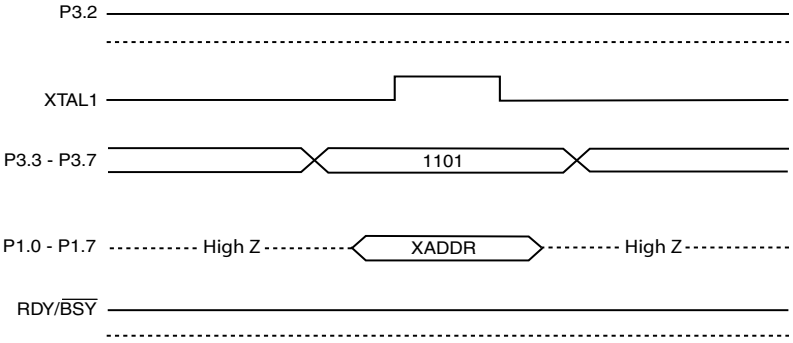
Function:

1. Loads the X-Address register with data on Port P1. The loaded address will select the page for subsequent write/read commands. The X-Address is equivalent to bits [11:5] of the full byte address.
2. Resets the Y-Address counter to 00H. The Y-Address is equivalent to bits [4:0] of the full byte address and selects a byte within a page.

Usage:

1. Apply “1101” TestCode to P3.7, P3.5, P3.4, P3.3.
2. Drive Port P1 with 8-bit X-address data.
3. Pulse XTAL1 high for at least 100 ns. The address is latched on the falling edge of XTAL1.

Figure 25-1. Load X-Address Sequence



26. Page Write 4K Code

Function:

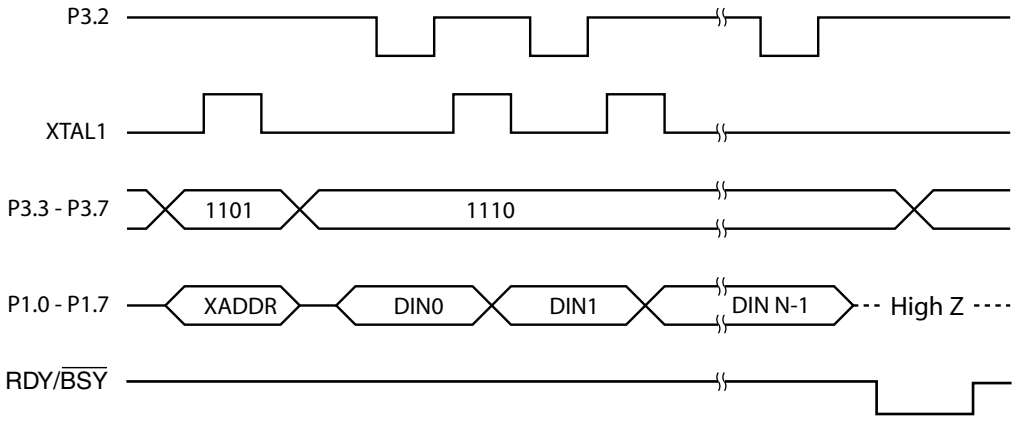
1. Programs 1 page (1 to 32 bytes) of data into the Code Memory array.
2. X-address (page) determined by previous Load-X command.
3. Y-address (offset) incremented by positive pulse on XTAL1.
4. 1 byte of data is loaded from Port P1 for the current X- and Y-address by a low pulse on P3.2.

Usage:

1. Execute the Load-X command to set the page address and reset the offset.
2. Apply “1110” TestCode to P3.7, P3.5, P3.4, P3.3.
3. Drive Port P1 with 8-bit data.
4. Pulse P3.2 low for 1 µs to load the data from Port P1.
5. For additional bytes (up to 32), pulse XTAL1 high for at least 100 ns to increment the Y-address and repeat steps 3 and 4 within 150 µs.
6. Wait 2 ms, monitor P3.1, or poll data.

Note: It is possible to skip bytes by pulsing XTAL1 high multiple times before pulsing P3.2 low.

Figure 26-1. Page Write 4K Code Programming Sequence



27. Read 4K Code

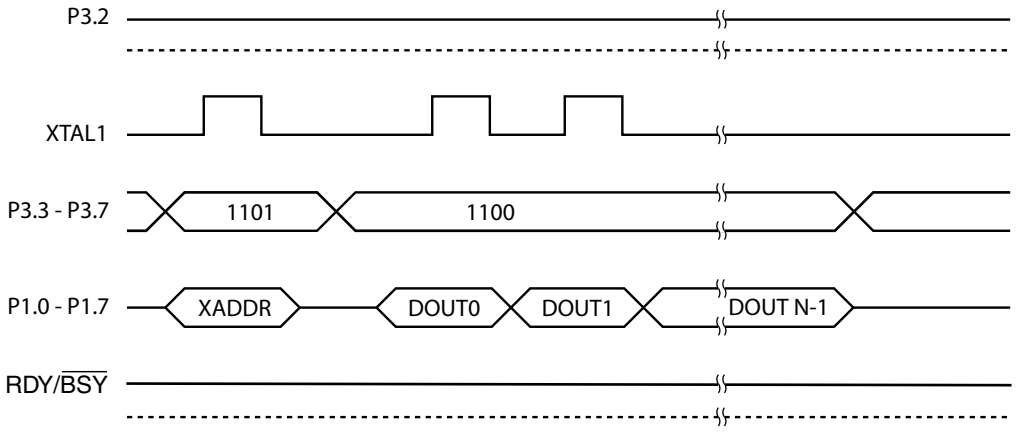
Function:

1. Read 1 page (1 to 32 bytes) of data from the Code Memory array.
2. X-address (page) determined by previous Load-X command.
3. Y-address (offset) incremented by positive pulse on XTAL1.

Usage:

1. Execute the Load-X command to set the page address and reset the offset.
2. Apply “1100” TestCode to P3.7, P3.5, P3.4, P3.3.
3. Read 8-bit data on Port P1.
4. For additional bytes (up to 32), pulse XTAL1 high for at least 100 ns to increment the Y-address and repeat step 3. The address will change on the falling edge of XTAL1.

Figure 27-1. Read 4K Code Programming Sequence



29. Read User Signature Row

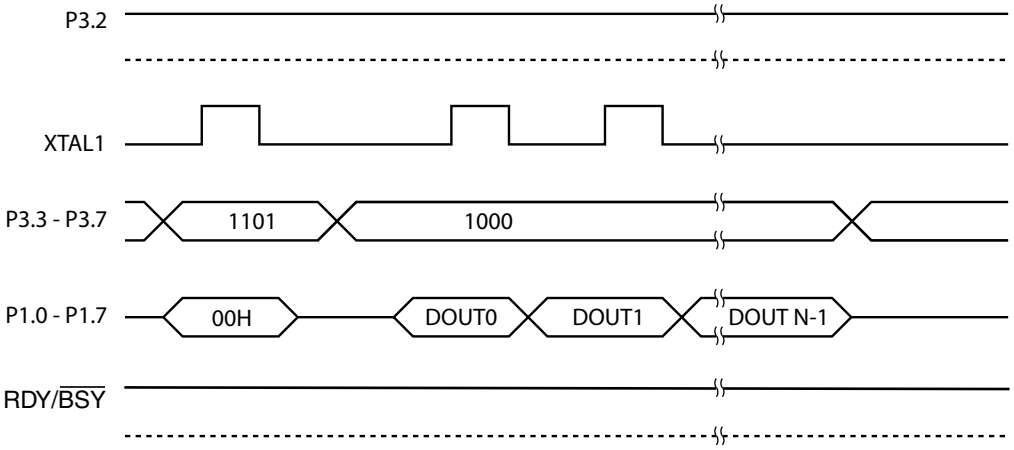
Function:

1. Reads 1 to 32 bytes of data from the User Signature Row.
2. X-address (page) should be 00H from a previous Load-X command.
3. Y-address (offset) incremented by positive pulse on XTAL1.

Usage:

1. Execute the Load-X command to set the page to 00H and reset the offset.
2. Apply “1000” TestCode to P3.7, P3.5, P3.4, P3.3.
3. Read 8-bit data on Port P1.
4. For additional bytes (up to 32), pulse XTAL1 high for at least 100 ns to increment the Y-address and repeat step 3. The address will change on the falling edge of XTAL1.

Figure 29-1. Read User Signature Row Sequence



30. Read Atmel Signature Row

Function:

1. Reads 1 to 32 bytes of data from the Atmel Signature Row.
2. X-address (page) should be 01H from a previous Load-X command.
3. Y-address (offset) incremented by positive pulse on XTAL1.

Usage:

1. Execute the Load-X command to set the page to 01H and reset the offset.
2. Apply “1000” TestCode to P3.7, P3.5, P3.4, P3.3.
3. Read 8-bit data on Port P1.
4. For additional bytes (up to 32), pulse XTAL1 high for at least 100 ns to increment the Y-address and repeat step 3. The address will change on the falling edge of XTAL1.

Figure 30-1. Read Atmel Signature Row Sequence

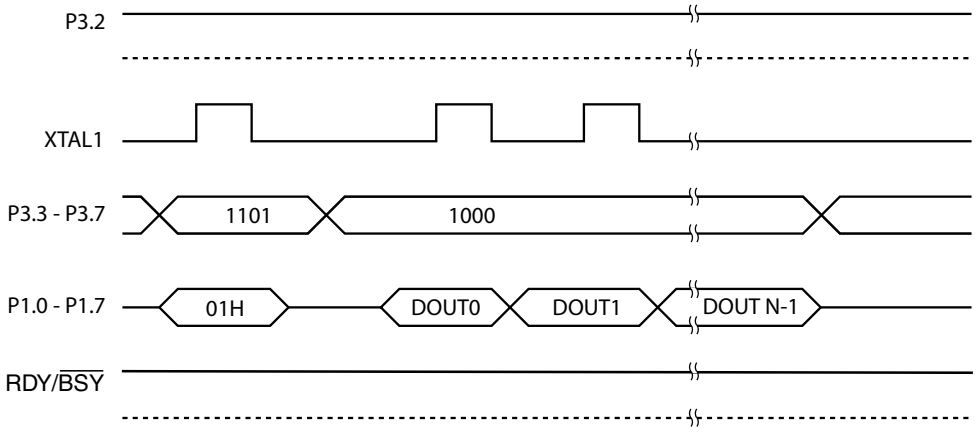
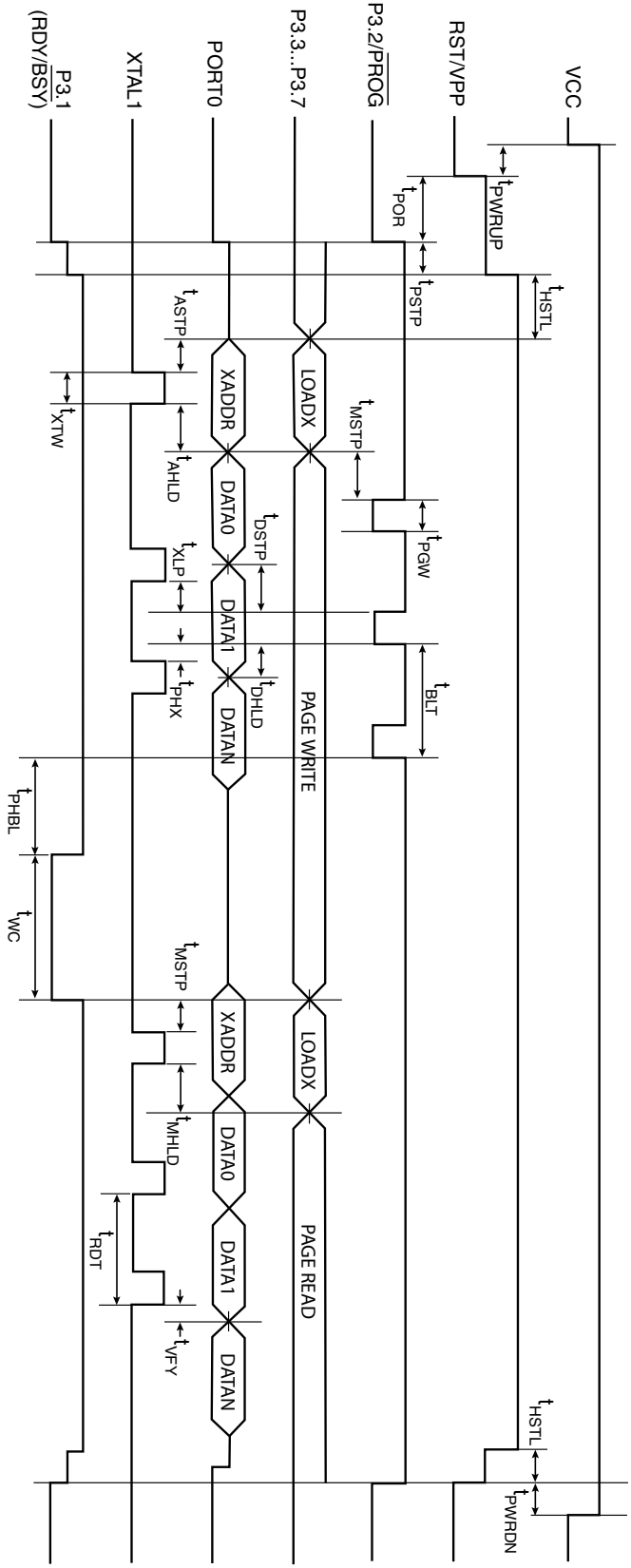


Figure 32-2. Flash Programming and Verification Waveforms in **Parallel Mode**



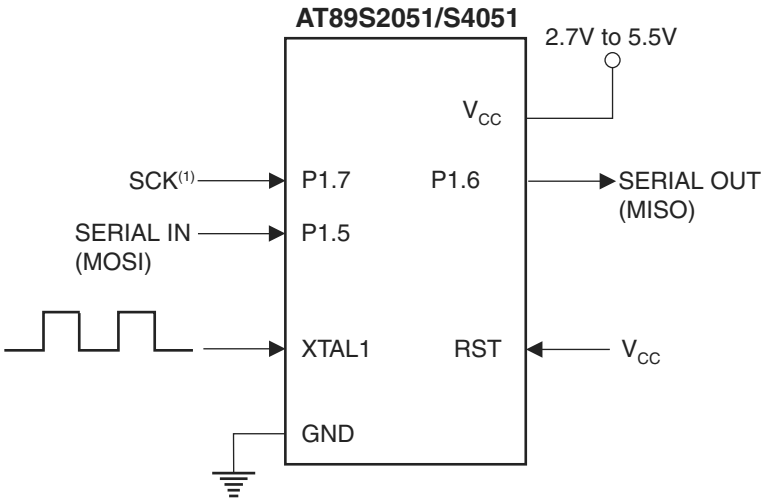
33. In-System Programming (ISP) Specification

Atmel's AT89S2051/S4051 offers 2K/4K bytes of In-System Programmable Flash code memory. In addition, the device contains a 32-byte User Signature Row and a 32-byte read-only Atmel Signature Row.

Table 33-1. Memory Organization

Device #	Page Size	# Pages	Address Range	Page Range
AT89S2051	32 bytes	64	0000H - 07FFH	00H - 3FH
AT89S4051	32 bytes	128	0000H - 0FFFH	00H - 7FH

Figure 33-1. ISP Programming Device Connections



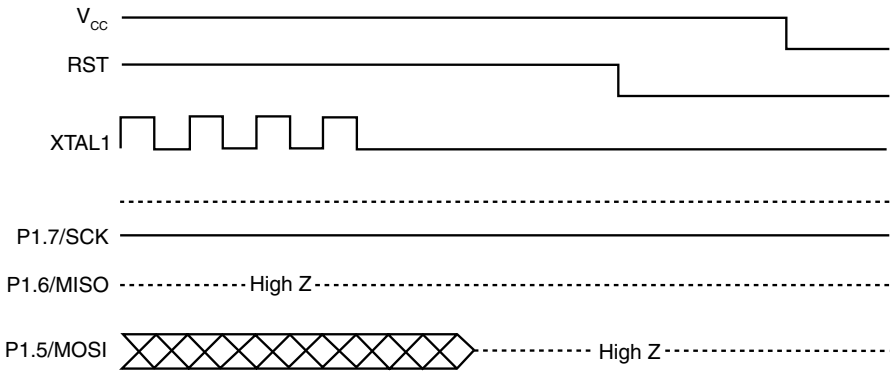
Note: 1. SCK frequency should be less than (XTAL frequency)/8.

37. Power-down Sequence

Execute this sequence to power-down the device **after** programming.

1. Set XTAL1 to “L” if a crystal is not used.
2. Bring RST to “L”.
3. Tri-state MOSI (P1.5).

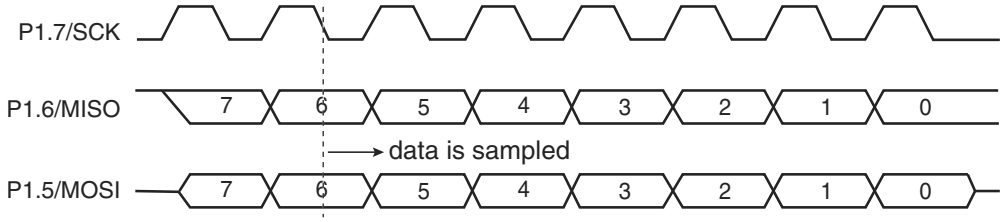
Figure 37-1. ISP Power-down Sequence



38. ISP Byte Sequence

1. Data shifts in/out MSB first.
2. MISO changes at **rising** of SCK.
3. MOSI is sampled at **falling** edge of SCK.

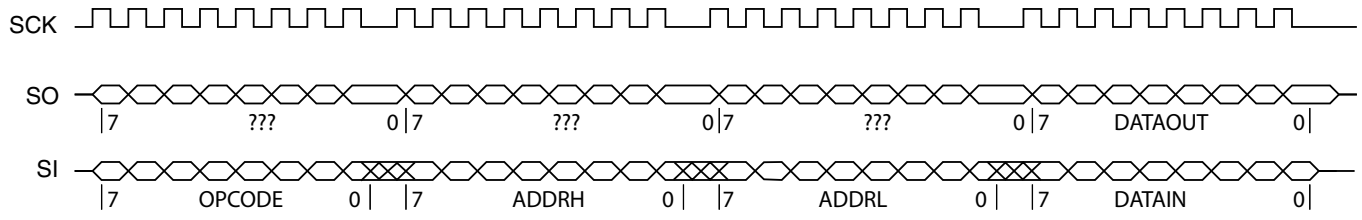
Figure 38-1. ISP Byte Sequence



39. ISP Command Sequence

1. **Byte** Format: 4 byte packet (3 header bytes + 1 data byte)
2. **Page** Format: 35 byte packet (3 header bytes + 32 data bytes)
3. All bytes are required, even if they are don’t care.

Figure 39-1. ISP Command Sequence



40. Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-0.7V to +6.2V
Maximum Operating Voltage	5.5V
DC Output Current	25.0 mA (15.0 mA for AT89S4051)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

41. DC Characteristics

T_A = -40°C to 85°C, V_{CC} = 2.7V to 5.5V (unless otherwise noted)

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low-voltage		-0.5	0.2 V_{CC} - 0.1	V
V_{IH}	Input High-voltage	(Except XTAL1, RST)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V
V_{IH1}	Input High-voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low-voltage(1) (Ports 1, 3)	I_{OL} = 10 mA, V_{CC} = 2.7V, T_A = 85°C		0.5	V
V_{OH}	Output High-voltage (Ports 1, 3)	I_{OH} = -80 µA, V_{CC} = 5V ±10%	2.4		V
		I_{OH} = -30 µA	0.75 V_{CC}		V
		I_{OH} = -12 µA	0.9 V_{CC}		V
I_{IL}	Logical 0 Input Current (Ports 1, 3)	V_{IN} = 0.45V		-50	µA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1, 3)	V_{IN} = 2V, V_{CC} = 5V ±10%		-350	µA
I_{LI}	Input Leakage Current (Port P1.0, P1.1)	0 < V_{IN} < V_{CC}		±10	µA
V_{OS}	Comparator Input Offset Voltage	V_{CC} = 5V		20	mV
V_{CM}	Comparator Input Common Mode Voltage		0	V_{CC}	V
RRST	Reset Pull-down Resistor		50	150	KΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current (without the)	Active Mode, 24/12 MHz, V_{CC} = 5V/3V		10.5/3.5	mA
		Idle Mode, 24/12 MHz, V_{CC} = 5V/3V P1.0 & P1.1 = 0V or V_{CC}		4.5/2.5	mA
	Power-down Mode(2)	V_{CC} = 5V, P1.0 & P1.1 = 0V or V_{CC}(3)		10	µA
		V_{CC} = 3V, P1.0 & P1.1 = 0V or V_{CC}(3)		5	µA

Notes:
1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum total I_{OL} for all output pins: 25 mA (15 mA for AT89S4051)
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V.
3. P1.0 and P1.1 are comparator inputs and have no internal pullups. They should not be left floating.

55. Ordering Information

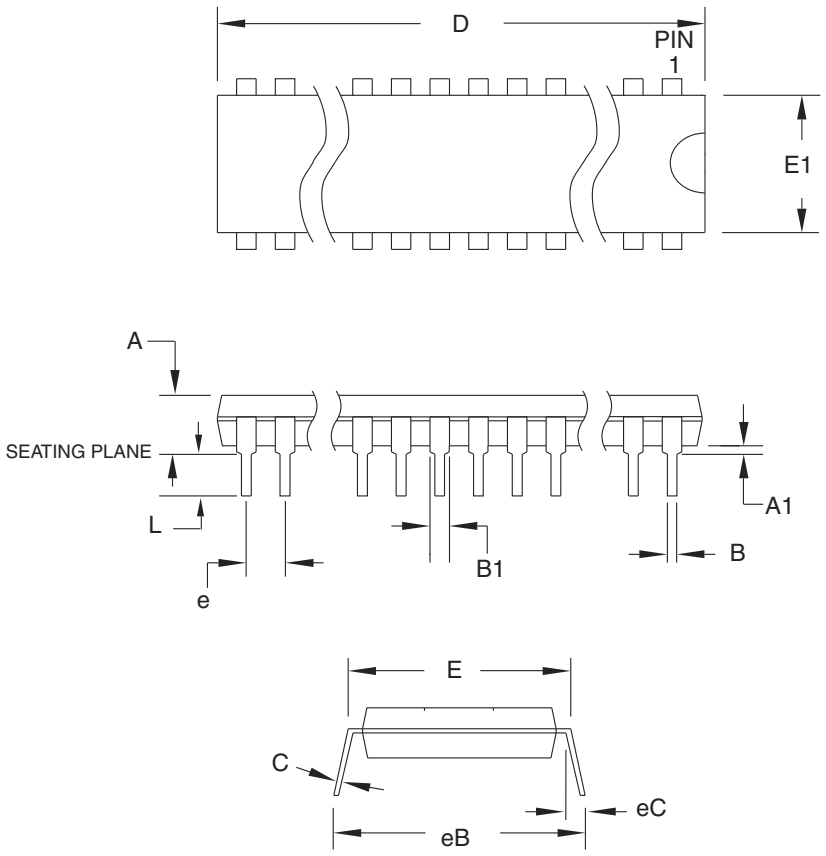
55.1 Green Package Option (Pb/Halide-free)

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
24	2.7V to 5.5V	AT89S2051/S4051-24PU AT89S2051/S4051-24SU	20P3 20S2	Industrial (-40° C to 85° C)

Package Type	
20P3	20-lead, 0.300” Wide, Plastic Dual In-line Package (PDIP)
20S2	20-lead, 0.300” Wide, Plastic Gull Wing Small Outline (SOIC)

56. Package Information

56.1 20P3 – PDIP



COMMON DIMENSIONS
(Unit of Measure = mm)

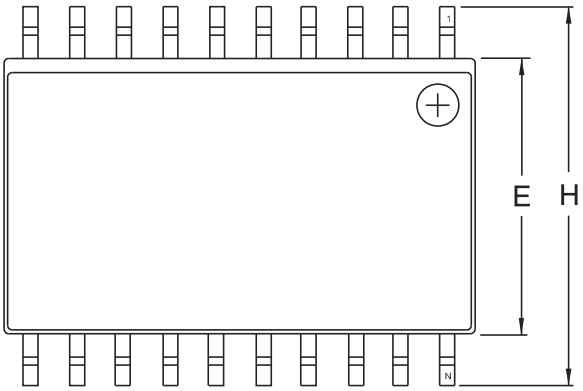
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	5.334	
A1	0.381	–	–	
D	24.892	–	26.924	Note 2
E	7.620	–	8.255	
E1	6.096	–	7.112	Note 2
B	0.356	–	0.559	
B1	1.270	–	1.551	
L	2.921	–	3.810	
C	0.203	–	0.356	
eB	–	–	10.922	
eC	0.000	–	1.524	
e	2.540 TYP			

Notes: 1. This package conforms to JEDEC reference MS-001, Variation AD.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

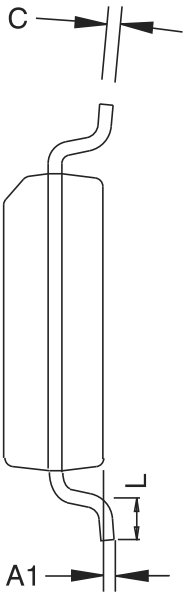
1/23/04

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**20P3**, 20-lead (0.300"/7.62 mm Wide) Plastic Dual Inline Package (PDIP)	20P3	D

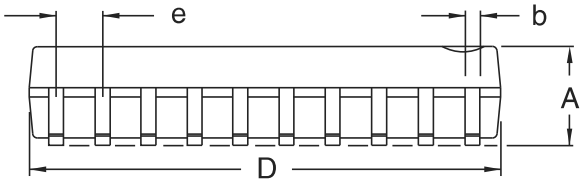
56.2 20S2 – SOIC



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure – mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	2.35		2.65	
A1	0.10		0.30	
b	0.33		0.51	4
C	0.23		0.32	
D	12.60		13.00	1
E	7.40		7.60	2
H	10.00		10.65	
L	0.40		1.27	3
e	1.27 BSC			

Notes.
1. This drawing is for general information only; refer to JEDEC Drawing MS-013, Variation AC for additional information.
2. Dimension 'D' does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006') per side.
3. Dimension 'E' does not include inter-lead Flash or protrusion. Inter-lead Flash and protrusions shall not exceed 0.25 mm (0.010') per side.
4. 'L' is the length of the terminal for soldering to a substrate.
5. The lead width 'b', as measured 0.36 mm (0.014') or greater above the seating plane, shall not exceed a maximum value of 0.61 mm (0.024') per side.

11/6/06

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**20S2**, 20-lead, 0.300' Wide Body, Plastic Gull Wing Small Outline Package (SOIC)	20S2	B

57. Revision History

Revision No.	History
Revision D – Feb. 2007	• Removed Preliminary Status. • Added the qualifier “x1 and x2 Modes” to the Static Operation range. • Changed the value ranges for Capacitors C1 and C2 in Figure 5-1 on page 4. • Changed the trigger level for the BOD from 2.2V to 2.0V.
Revision E – June 2008	• Removed Standard Packaging Offering.