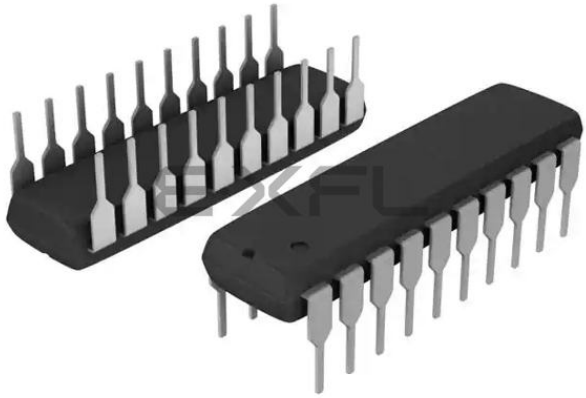

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	24MHz
Connectivity	UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM
Number of I/O	15
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	20-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at89s4051-24pu

4.5 RST

Reset input. Holding the RST pin high for two machine cycles while the is running resets the device.

Each machine cycle takes 6 or clock cycles.

4.6 XTAL1

Input to the inverting amplifier and input to the internal clock operating circuit.

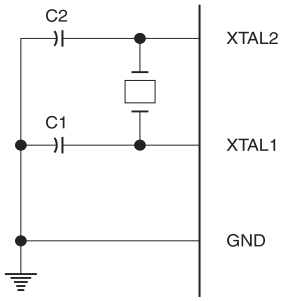
4.7 XTAL2

Output from the inverting amplifier.

5. Characteristics

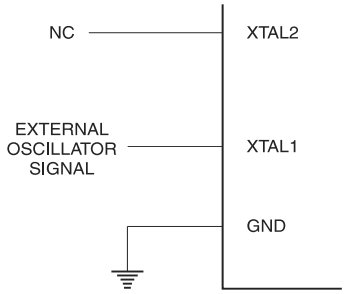
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip , as shown in Figure 5-1. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven as shown in Figure 5-2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Figure 5-1. Connections



Note: C1, C2 = 5 pF ±5 pF for Crystals
= 5 pF ±5 pF for Ceramic Resonators

Figure 5-2. External Clock Drive Configuration



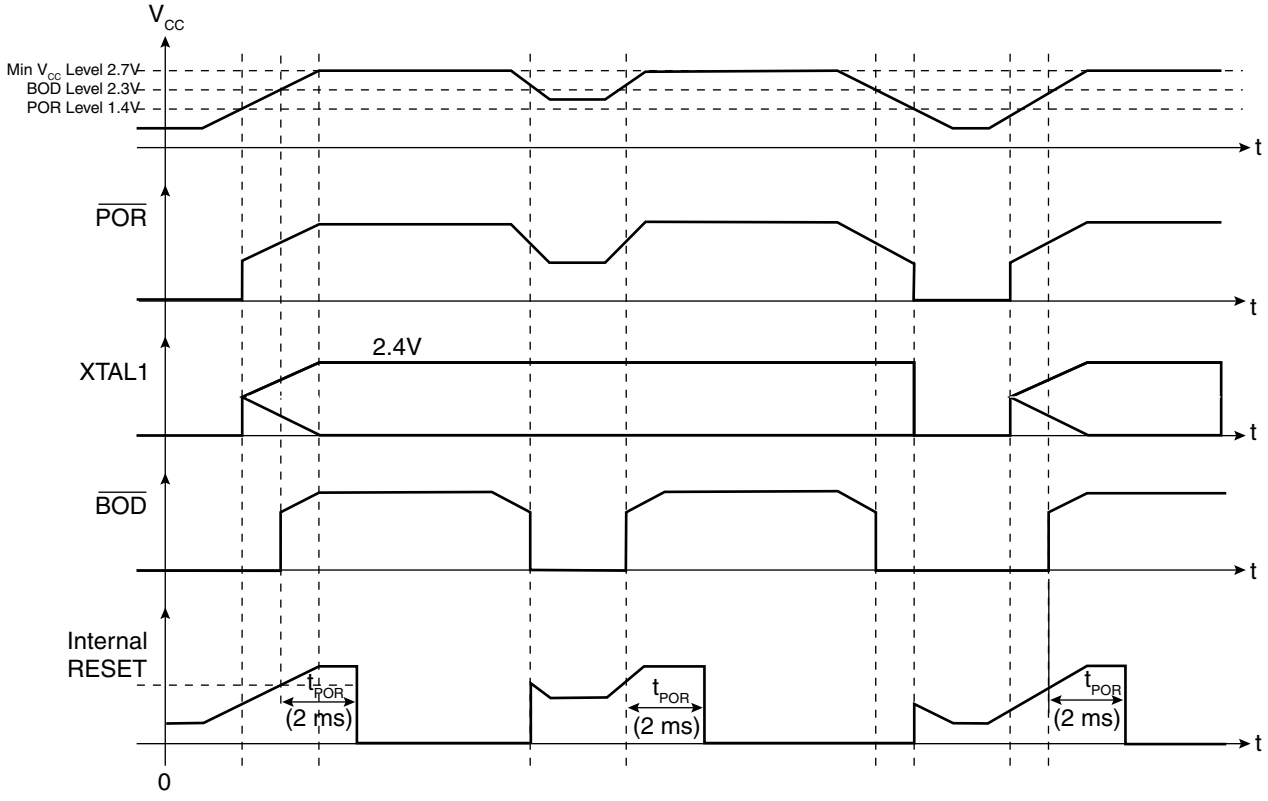
10. Reset

During reset, all I/O Registers are set to their initial values, the port pins are weakly pulled to V_{CC}, and the program starts execution from the Reset Vector, 0000H. The AT89S2051/S4051 has three sources of reset: power-on reset, brown-out reset, and external reset.

10.1 Power-On Reset

A Power-On Reset (POR) is generated by an on-chip detection circuit. The detection level is nominally 1.4V. The POR is activated whenever V_{CC} is below the detection level. The POR circuit can be used to trigger the start-up reset or to detect a supply voltage failure in devices without a brown-out detector. The POR circuit ensures that the device is reset from power-on. When V_{CC} reaches the Power-on Reset threshold voltage, the Pierce Oscillator is enabled (if the XTAL Oscillator Bypass fuse is OFF). Only after V_{CC} has also reached the BOD (brown-out detection) level (see Section 10.2 ”Brown-out Reset”), the BOD delay counter starts measuring a 2-ms delay after which the Internal Reset is deasserted and the microcontroller starts executing. The built-in 2-ms delay allows the V_{CC} voltage to reach the minimum 2.7V level before executing, thus guaranteeing the maximum operating clock frequency. The POR signal is activated again, without any delay, when V_{CC} falls below the POR threshold level. A Power-On Reset (i.e. a cold reset) will set the POF flag in PCON. Refer to Figure 10-1 for details on the POR/BOD behavior.

Figure 10-1. Power-up and Brown-out Detection Sequence



12.4 Reset Recovery from Power-down

Wakeup from Power-down through an external reset is similar to the interrupt with PWDEX = 0. At the rising edge of RST, Power-down is exited, the is restarted, and an internal timer begins counting. The internal clock will not be allowed to propagate to the CPU until after the timer has counted for nominally 2 ms. The RST pin must be held high for longer than the timeout period to ensure that the device is reset properly. The device will begin executing once RST is brought low.

It should be noted that when idle is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

P1.0 and P1.1 should be set to “0” if no external pull-ups are used, or set to “1” if external pull-ups are used.

Table 12-1. PCON – Power Control Register

PCON = 87H — Reset Value = 000X 0000B

Not Bit Addressable

	SMOD1	SMOD0	PWMEN	POF	GF1	GF0	PD	IDL
Bit	7	6	5	4	3	2	1	0

Symbol	Function
SMOD1	Double Baud Rate bit. Doubles the baud rate of the UART in modes 1, 2, or 3.
SMOD0	Frame Error Select. When SMOD0 = 0, SCON.7 is SM0. When SMOD0 = 1, SCON.7 is FE. Note that FE will be set after a frame error regardless of the state of SMOD0.
PWMEN	Pulse Width Modulation Enable. When PWMEN = 1, Timer 0 and Timer 1 are configured as an 8-bit PWM counter with 8-bit auto-reload prescaler. The PWM outputs on T1 (P3.5).
POF	Power Off Flag. POF is set to “1” during power up (i.e. cold reset). It can be set or reset under software control and is not affected by RST or BOD (i.e. warm resets).
GF1, GF0	General-purpose Flags
PD	Power Down bit. Setting this bit activates power down operation.
IDL	Idle Mode bit. Setting this bit activates idle mode operation

13. Interrupts

The AT89S2051/S4051 provides 6 interrupt sources: two external interrupts, two timer interrupts, a serial port interrupt, and an analog comparator interrupt. These interrupts and the system reset each have a separate program vector at the start of the program memory space. Each interrupt source can be individually enabled or disabled by setting or clearing a bit in the interrupt enable register IE. The IE register also contains a global disable bit, EA, which disables all interrupts.

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing bits in the interrupt priority registers IP and IPH. An interrupt service routine in progress can be interrupted by a higher priority interrupt, but not by another interrupt of the same or lower priority. The highest priority interrupt cannot be interrupted by any other interrupt source. If two requests of different priority levels are pending at the end of an instruction, the request of higher priority level is serviced. If requests of the same priority level are pending at the end of an instruction, an internal polling sequence determines which request is serviced. The polling sequence is based on the vector address; an interrupt with a lower vector address has higher priority than an interrupt with a higher vector address. Note that the polling sequence is only used to resolve pending requests of the same priority level.

The External Interrupts $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ can each be either level-activated or transition-activated, depending on bits IT0 and IT1 in Register TCON. The flags that actually generate these interrupts are the IE0 and IE1 bits in TCON. When the service routine is vectored to, hardware clears the flag that generated an external interrupt only if the interrupt was transition-activated. If the interrupt was level activated, then the external requesting source (rather than the on-chip hardware) controls the request flag.

The Timer 0 and Timer 1 Interrupts are generated by TF0 and TF1, which are set by a rollover in their respective Timer/Counter registers (except for Timer 0 in Mode 3). When a timer interrupt is generated, the on-chip hardware clears the flag that generated it when the service routine is vectored to.

The Serial Port Interrupt is generated by the logical OR of RI and TI in SCON. Neither of these flags is cleared by hardware when the service routine is vectored to. In fact, the service routine normally must determine whether RI or TI generated the interrupt, and the bit must be cleared in software.

The CF bit in ACSR generates the Comparator Interrupt. The flag is not cleared by hardware when the service routine is vectored to and must be cleared by software.

Most of the bits that generate interrupts can be set or cleared by software, with the same result as though they had been set or cleared by hardware. That is, interrupts can be generated and pending interrupts can be canceled in software.

Interrupt	Source	Vector Address
System Reset	RST or POR or BOD	0000H
External Interrupt 0	IE0	0003H
Timer 0 Overflow	TF0	000BH
External Interrupt 1	IE1	0013H
Timer 1 Overflow	TF1	001BH
Serial Port	RI or TI	0023H
Analog Comparator	CF	0033H

14. Interrupt Registers

Table 14-1. IE – Interrupt Enable Register

IE = A8H — Reset Value = 00X0 0000B

Bit Addressable

	EA	EC	–	ES	ET1	EX1	ET0	EX0
Bit	7	6	5	4	3	2	1	0

Symbol	Function
EA	Global enable/disable. All interrupts are disabled when EA = 0. When EA = 1, each interrupt source is enabled/disabled by setting/clearing its own enable bit.
EC	Comparator Interrupt Enable
ES	Serial Port Interrupt Enable
ET1	Timer 1 Interrupt Enable
EX1	External Interrupt 1 Enable
ET0	Timer 0 Interrupt Enable
EX0	External Interrupt 0 Enable

Table 14-2. IP – Interrupt Priority Register

IP = B8H — Reset Value = X0X0 0000B

Bit Addressable

	–	PC	–	PS	PT1	PX1	PT0	PX0
Bit	7	6	5	4	3	2	1	0

Symbol	Function
PC	Comparator Interrupt Priority Low
PS	Serial Port Interrupt Priority Low
PT1	Timer 1 Interrupt Priority Low
PX1	External Interrupt 1 Priority Low
PT0	Timer 0 Interrupt Priority Low
PX0	External Interrupt 0 Priority Low

Table 14-3. IPH – Interrupt Priority High Register

IPH = B7H — Reset Value = X0X0 0000B

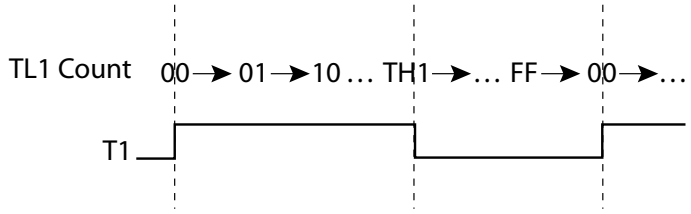
Not Bit Addressable

	–	PCH	–	PSH	PT1H	PX1H	PT0H	PX0H
Bit	7	6	5	4	3	2	1	0

Symbol	Function
PCH	Comparator Interrupt Priority High
PSH	Serial Port Interrupt Priority High
PT1H	Timer 1 Interrupt Priority High
PX1H	External Interrupt 1 Priority High
PT0H	Timer 0 Interrupt Priority High
PX0H	External Interrupt 0 Priority High

TL1 will always count from 00h to FFh. The output on the Timer 1 (T1) pin will be high from when TL1 equals 00h until TL1 equals TH1 (see Figure 16-3). TH1 does not act as the reload value for TL1 on overflow. Instead, TH1 is used strictly as a compare value (see Figure 16-2).

Figure 16-3. Example of a PWM Output



17. UART

The UART in the AT89S2051/S4051 operates the same way as the UART in the AT89C2051/C4051. For more detailed information on the UART operation, please click on the document link below:

http://www.atmel.com/dyn/resources/prod_documents/DOC4316.PDF

17.1 Enhanced UART

In addition to all of its usual modes, the UART can perform framing error detection by looking for missing stop bits, and automatic address recognition. The UART also fully supports multiprocessor communication as does the standard 80C51 UART.

When used for framing error detect, the UART looks for missing stop bits in the communication. A missing bit will set the FE bit in the SCON register. The FE bit shares the SCON.7 bit with SM0 and the function of SCON.7 is determined by PCON.6 (SMOD0). If SMOD0 is set then SCON.7 functions as FE. SCON.7 functions as SM0 when SMOD0 is cleared. When used as FE, SCON.7 can only be cleared by software.

17.2 Automatic Address Recognition

Automatic Address Recognition is a feature which allows the UART to recognize certain addresses in the serial bit stream by using hardware to make the comparisons. This feature saves a great deal of software overhead by eliminating the need for the software to examine every serial address which passes by the serial port. This feature is enabled by setting the SM2 bit in SCON. In the 9-bit UART modes, mode 2 and mode 3, the Receive Interrupt flag (RI) will be automatically set when the received byte contains either the “Given” address or the “Broadcast” address. The 9-bit mode requires that the 9th information bit is a 1 to indicate that the received information is an address and not data.

The 8-bit mode is called mode 1. In this mode the RI flag will be set if SM2 is enabled and the information received has a valid stop bit following the 8 address bits and the information is either a Given or Broadcast address.

Mode 0 is the Shift Register mode and SM2 is ignored.

Using the Automatic Address Recognition feature allows a master to selectively communicate with one or more slaves by invoking the given slave address or addresses. All of the slaves may be contacted by using the Broadcast address. Two special Function Registers are used to define the slave’s address, SADDR, and the address mask, SADEN. SADEN is used to define which bits in the SADDR are to be used and which bits are “don’t care”. The SADEN mask can

be logically ANDed with the SADDR to create the “Given” address which the master will use for addressing each of the slaves. Use of the Given address allows multiple slaves to be recognized while excluding others. The following examples will help to show the versatility of this scheme:

Slave 0 SADDR = 1100 0000

SADEN = 1111 1101

Given = 1100 00X0

Slave 1 SADDR = 1100 0000

SADEN = 1111 1110

Given = 1100 000X

In the previous example SADDR is the same and the SADEN data is used to differentiate between the two slaves. Slave 0 requires a 0 in bit 0 and it ignores bit 1. Slave 1 requires a 0 in bit 1 and bit 0 is ignored. A unique address for slave 0 would be 1100 0010 since slave 1 requires a 0 in bit 1. A unique address for slave 1 would be 1100 0001 since a 1 in bit 0 will exclude slave 0. Both slaves can be selected at the same time by an address which has bit 0 = 0 (for slave 0) and bit 1 = 0 (for slave 1). Thus, both could be addressed with 1100 0000.

In a more complex system the following could be used to select slaves 1 and 2 while excluding slave 0:

Slave 0 SADDR = 1100 0000

SADEN = 1111 1001

Given = 1100 0XX0

Slave 1 SADDR = 1110 0000

SADEN = 1111 1010

Given = 1110 0X0X

Slave 2 SADDR = 1110 0000

SADEN = 1111 1100

Given = 1110 00XX

In the above example the differentiation among the 3 slaves is in the lower 3 address bits. Slave 0 requires that bit 0 = 0 and it can be uniquely addressed by 1110 0110. Slave 1 requires that bit 1 = 0 and it can be uniquely addressed by 1110 and 0101. Slave 2 requires that bit 2 = 0 and its unique address is 1110 0011. To select Slaves 0 and 1 and exclude Slave 2, use address 1110 0100, since it is necessary to make bit 2 = 1 to exclude slave 2.

The Broadcast Address for each slave is created by taking the logical OR of SADDR and SADEN. Zeros in this result are trended as don’t cares. In most cases, interpreting the don’t cares as ones, the broadcast address will be FF hexadecimal.

Upon reset SADDR (SFR address 0A9H) and SADEN (SFR address 0B9H) are loaded with 0s. This produces a given address of all “don’t cares” as well as a Broadcast address of all “don’t cares”. This effectively disables the Automatic Addressing mode and allows the microcontroller to use standard 80C51-type UART drivers which do not make use of this feature.

Table 17-1. SCON – Serial Port Control Register

SCON Address = 98H — Reset Value = 0000 0000B

Bit Addressable

Bit	7	6	5	4	3	2	1	0
	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI

(SMOD = 0/1)[1]

Symbol	Function
FE	Framing error bit. This bit is set by the receiver when an invalid stop bit is detected. The FE bit is not cleared by valid frames but should be cleared by software. The SMOD0 bit must be set to enable access to the FE bit. FE will be set regardless of the state of SMOD.
SM0	Serial Port Mode Bit 0, (SMOD must = 0 to access bit SM0)
SM1	Serial Port Mode Bit 1 SM0 SM1 Mode Description Baud Rate[2] 0 0 0 shift register $f_{osc}/12$ 0 1 1 8-bit UART variable 1 0 2 9-bit UART $f_{osc}/64$ or $f_{osc}/32$ 1 1 3 9-bit UART variable
SM2	Enables the Automatic Address Recognition feature in modes 2 or 3. If SM2 = 1 then RI will not be set unless the received 9th data bit (RB8) is 1, indicating an address, and the received byte is a Given or Broadcast Address. In mode 1, if SM2 = 1 then RI will not be activated unless a valid stop bit was received, and the received byte is a Given or Broadcast Address. In Mode 0, SM2 should be 0.
REN	Enables serial reception. Set by software to enable reception. Clear by software to disable reception.
TB8	The 9th data bit that will be transmitted in modes 2 and 3. Set or clear by software as desired.
RB8	In modes 2 and 3, the 9th data bit that was received. In mode 1, if SM2 = 0, RB8 is the stop bit that was received. In mode 0, RB8 is not used.
TI	Transmit interrupt flag. Set by hardware at the end of the 8th bit time in mode 0, or at the beginning of the stop bit in the other modes, in any serial transmission. Must be cleared by software.
RI	Receive interrupt flag. Set by hardware at the end of the 8th bit time in mode 0, or halfway through the stop bit time in the other modes, in any serial reception (except see SM2). Must be cleared by software.

Notes: 1. SMOD is located at PCON.7.
2. f_{osc} = frequency.

18. Analog Comparator

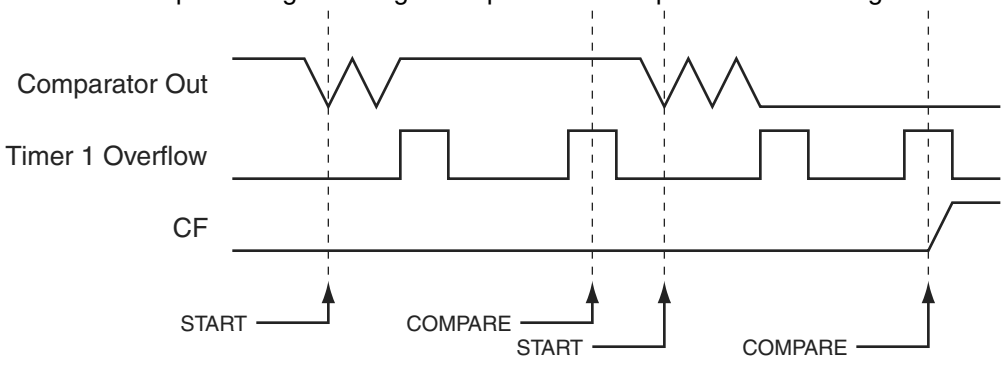
A single analog comparator is provided in the AT89S2051/S4051. The comparator operation is such that the output is a logical “1” when the positive input AIN0 (P1.0]) is greater than the negative input AIN1 (P1.1). Otherwise the output is a zero. Setting the CEN bit in ACSR enables the comparator. When the comparator is first enabled, the comparator output and interrupt flag are not guaranteed to be stable for 10 microseconds. The corresponding comparator interrupt should not be enabled during that time, and the comparator interrupt flag must be cleared before the interrupt is enabled in order to prevent an immediate interrupt service.

The comparator may be configured to cause an interrupt under a variety of output value conditions by setting the CM bits in ACSR. The comparator interrupt flag CF in ACSR is set whenever the comparator output matches the condition specified by CM. The flag may be polled by software or may be used to generate an interrupt and must be cleared by software. The analog comparator is always disabled during Idle or Power-down modes.

19. Comparator Interrupt with Debouncing

The comparator output is sampled at every State 4 (S4) of every machine cycle. The conditions on the analog inputs may be such that the comparator output will toggle excessively. This is especially true if applying slow moving analog inputs. Three debouncing modes are provided to filter out this noise. In debouncing mode, the comparator uses Timer 1 to modulate its sampling time. When a relevant transition occurs, the comparator waits until two Timer 1 overflows have occurred before resampling the output. If the new sample agrees with the expected value, CF is set. Otherwise, the event is ignored. The filter may be tuned by adjusting the timeout period of Timer 1. Because Timer 1 is free running, the debouncer must wait for two overflows to guarantee that the sampling delay is at least 1 timeout period. Therefore after the initial edge event, the interrupt may occur between 1 and 2 timeout periods later. See Figure 19-1.

Figure 19-1. Example of Negative Edge Comparator Interrupt with Debouncing



20. Analog Comparator Register

Table 20-1. ACSR – Analog Comparator Control & Status Register

ACSR = 97H — Reset Value = XXX0 0000B

Not Bit Addressable

	–	–	–	CF	CEN	CM2	CM1	CM0
Bit	7	6	5	4	3	2	1	0

Symbol	Function
CF	Comparator Interrupt Flag. Set when the comparator output meets the conditions specified by the CM [2:0] bits and CEN is set. The flag must be cleared by software. The interrupt may be enabled/disabled by setting/clearing bit 6 of IE.
CEN	Comparator Enable. Set this bit to enable the comparator. Clearing this bit will force the comparator output low and prevent further events from setting CF.
CM [2:0]	Comparator Interrupt Mode **2 1 0 Interrupt Mode** 0 0 0 Negative (Low) level 0 0 1 Positive edge 0 1 0 Toggle with debounce 0 1 1 Positive edge with debounce 1 0 0 Negative edge 1 0 1 Toggle 1 1 0 Negative edge with debounce 1 1 1 Positive (High) level

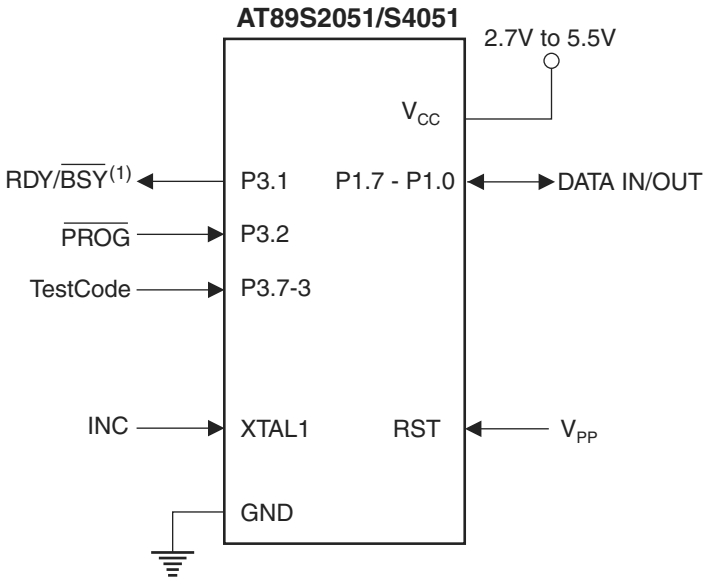
21. Parallel Programming Specification

Atmel's AT89S2051/S4051 offers 2K/4K bytes of In-System Programmable Flash code memory. In addition, the device contains a 32-byte User Signature Row and a 32-byte read-only Atmel Signature Row.

Table 21-1. Memory Organization

Device #	Page Size	# Pages	Address Range	Page Range
AT89S2051	32 bytes	64	0000H - 07FFH	00H - 3FH
AT89S4051	32 bytes	128	0000H - 0FFFH	00H - 7FH

Figure 21-1. Flash Parallel Programming Device Connections



Note: 1. Sampling of pin P3.1 (RDY/$\overline{BSY}$) is optional. In Parallel Mode, P3.1 will be pulled low while the device is busy. However, it requires an external passive pull-up to V_{CC}. Also, note that P3.6 does not exist, so TestCode connects to P3.7, P3.5, P3.4, and P3.3.

24. Chip Erase

Function:

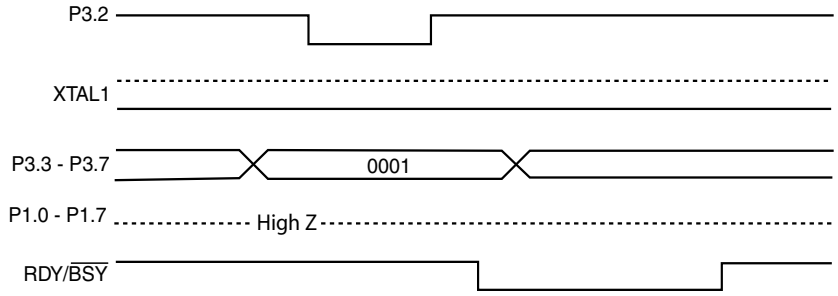
1. FFH programmed to every address location.
2. FFH programmed to User Signature Row if User Row Fuse bit is enabled.
3. Lockbit1 and Lockbit2 programmed to “unlock” state.

Usage:

1. Apply “0001” TestCode to P3.7, P3.5, P3.4, P3.3.
2. Pulse P3.2 low for 1 µs.
3. Wait 4 ms, monitor P3.1, or poll data.

Note: This and the following waveforms are not to scale.

Figure 24-1. Chip Erase Sequence



25. Load X-Address

Function:

1. Loads the X-Address register with data on Port P1. The loaded address will select the page for subsequent write/read commands. The X-Address is equivalent to bits [11:5] of the full byte address.
2. Resets the Y-Address counter to 00H. The Y-Address is equivalent to bits [4:0] of the full byte address and selects a byte within a page.

Usage:

1. Apply “1101” TestCode to P3.7, P3.5, P3.4, P3.3.
2. Drive Port P1 with 8-bit X-address data.
3. Pulse XTAL1 high for at least 100 ns. The address is latched on the falling edge of XTAL1.

Figure 25-1. Load X-Address Sequence

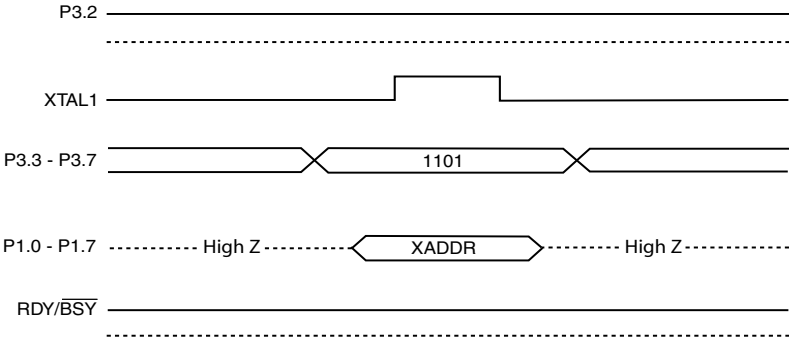
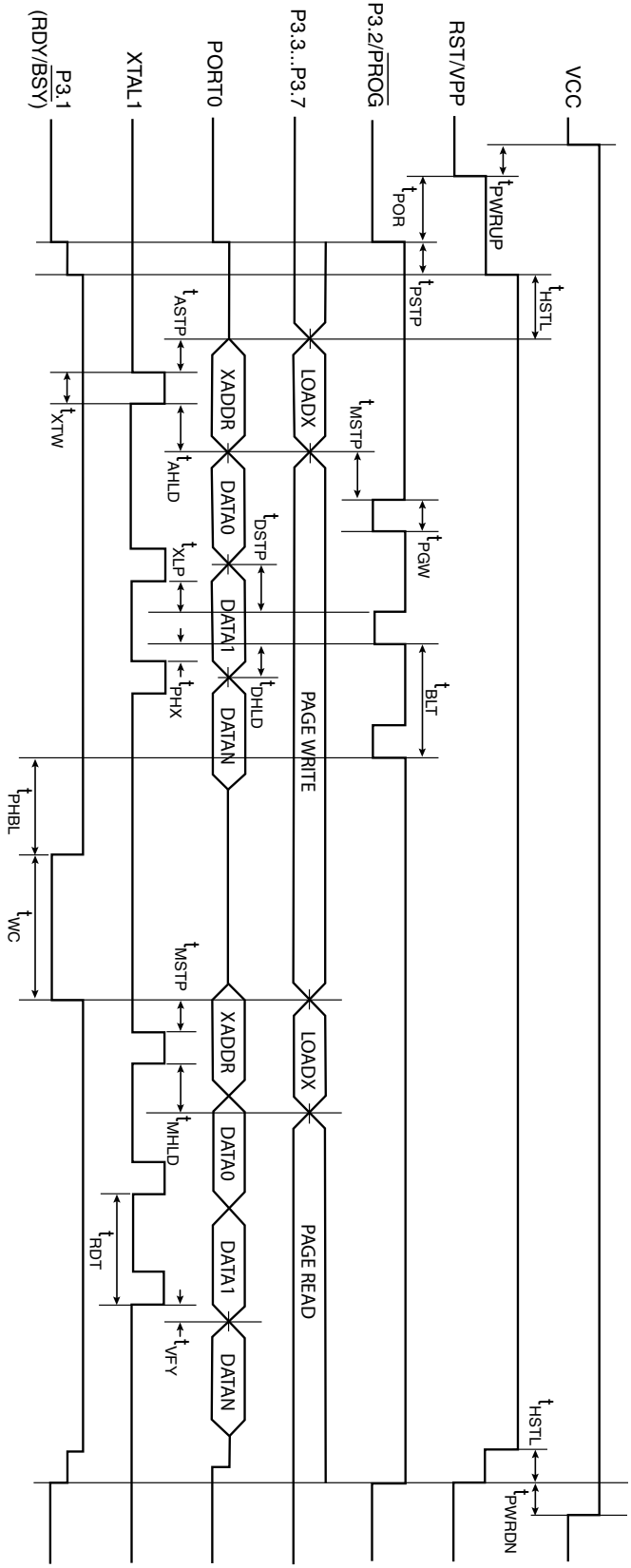


Figure 32-2. Flash Programming and Verification Waveforms in **Parallel Mode**



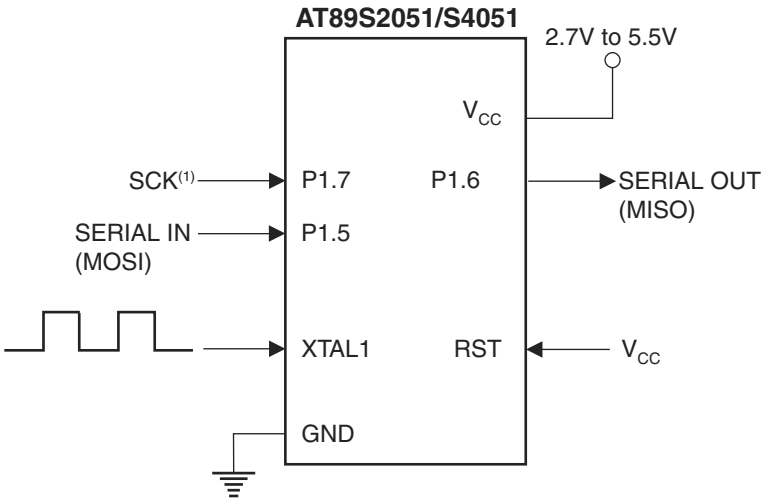
33. In-System Programming (ISP) Specification

Atmel's AT89S2051/S4051 offers 2K/4K bytes of In-System Programmable Flash code memory. In addition, the device contains a 32-byte User Signature Row and a 32-byte read-only Atmel Signature Row.

Table 33-1. Memory Organization

Device #	Page Size	# Pages	Address Range	Page Range
AT89S2051	32 bytes	64	0000H - 07FFH	00H - 3FH
AT89S4051	32 bytes	128	0000H - 0FFFH	00H - 7FH

Figure 33-1. ISP Programming Device Connections



Note: 1. SCK frequency should be less than (XTAL frequency)/8.

40. Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-0.7V to +6.2V
Maximum Operating Voltage	5.5V
DC Output Current	25.0 mA (15.0 mA for AT89S4051)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

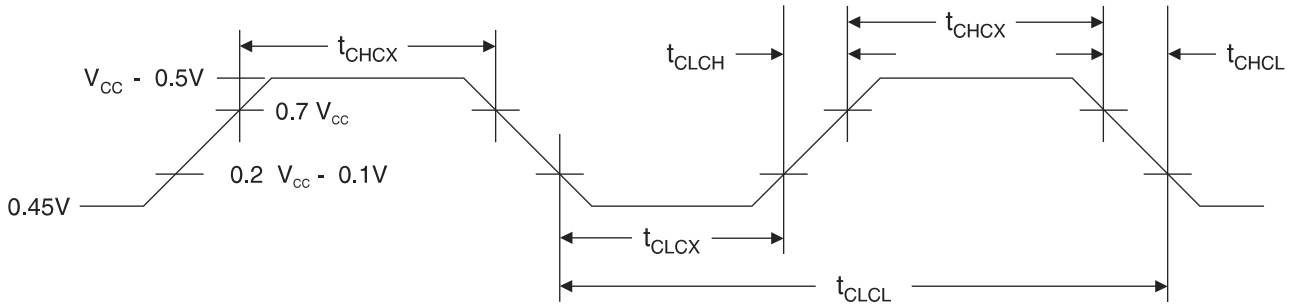
41. DC Characteristics

T_A = -40°C to 85°C, V_{CC} = 2.7V to 5.5V (unless otherwise noted)

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low-voltage		-0.5	0.2 V_{CC} - 0.1	V
V_{IH}	Input High-voltage	(Except XTAL1, RST)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V
V_{IH1}	Input High-voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low-voltage(1) (Ports 1, 3)	I_{OL} = 10 mA, V_{CC} = 2.7V, T_A = 85°C		0.5	V
V_{OH}	Output High-voltage (Ports 1, 3)	I_{OH} = -80 µA, V_{CC} = 5V ±10%	2.4		V
		I_{OH} = -30 µA	0.75 V_{CC}		V
		I_{OH} = -12 µA	0.9 V_{CC}		V
I_{IL}	Logical 0 Input Current (Ports 1, 3)	V_{IN} = 0.45V		-50	µA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1, 3)	V_{IN} = 2V, V_{CC} = 5V ±10%		-350	µA
I_{LI}	Input Leakage Current (Port P1.0, P1.1)	0 < V_{IN} < V_{CC}		±10	µA
V_{OS}	Comparator Input Offset Voltage	V_{CC} = 5V		20	mV
V_{CM}	Comparator Input Common Mode Voltage		0	V_{CC}	V
RRST	Reset Pull-down Resistor		50	150	KΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current (without the)	Active Mode, 24/12 MHz, V_{CC} = 5V/3V		10.5/3.5	mA
		Idle Mode, 24/12 MHz, V_{CC} = 5V/3V P1.0 & P1.1 = 0V or V_{CC}		4.5/2.5	mA
	Power-down Mode(2)	V_{CC} = 5V, P1.0 & P1.1 = 0V or V_{CC}(3)		10	µA
		V_{CC} = 3V, P1.0 & P1.1 = 0V or V_{CC}(3)		5	µA

Notes:
1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum total I_{OL} for all output pins: 25 mA (15 mA for AT89S4051)
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V.
3. P1.0 and P1.1 are comparator inputs and have no internal pullups. They should not be left floating.

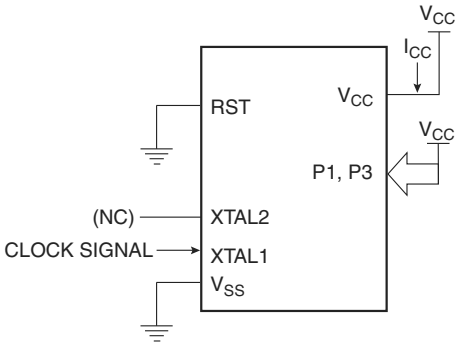
42. External Clock Drive Waveforms



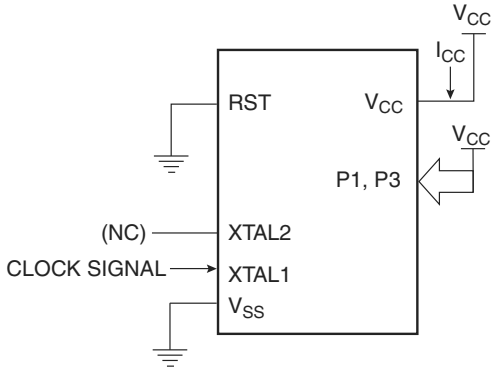
43. External Clock Drive

Symbol	Parameter	V_{CC} = 2.7V to 5.5V		Units
		Min	Max	
$1/t_{CLCL}$	Frequency	0	24	MHz
t_{CLCL}	Clock Period	41.6		ns
t_{CHCX}	High Time	12		ns
t_{CLCX}	Low Time	12		ns
t_{CLCH}	Rise Time		5	ns
t_{CHCL}	Fall Time		5	ns

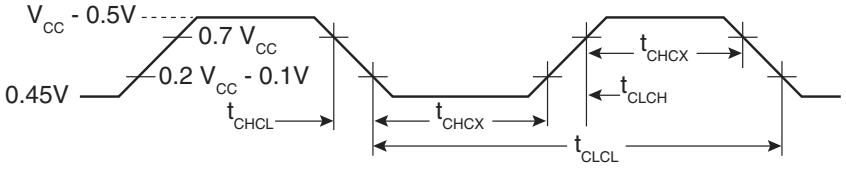
48. I_{CC} Test Condition, Active Mode, All Other Pins are Disconnected



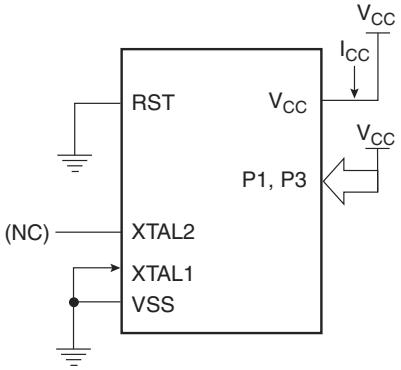
49. I_{CC} Test Condition, Idle Mode, All Other Pins are Disconnected



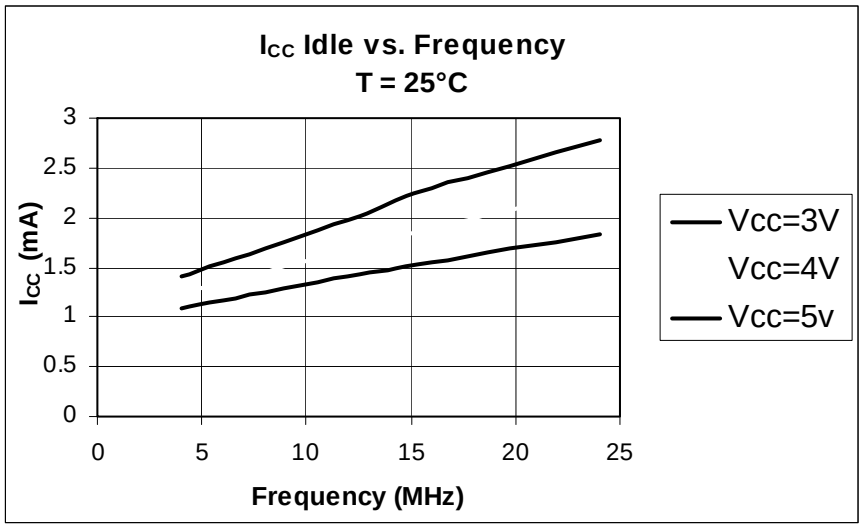
50. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes, $t_{CLCH} = t_{CHCL} = 5$ ns



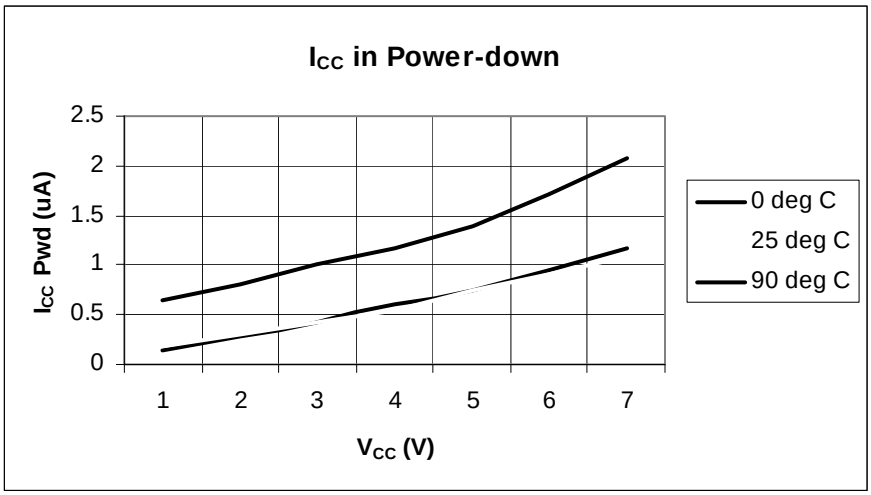
51. I_{CC} Test Condition, Power-down Mode, All Other Pins are Disconnected, V_{CC} = 2V to 5.5V



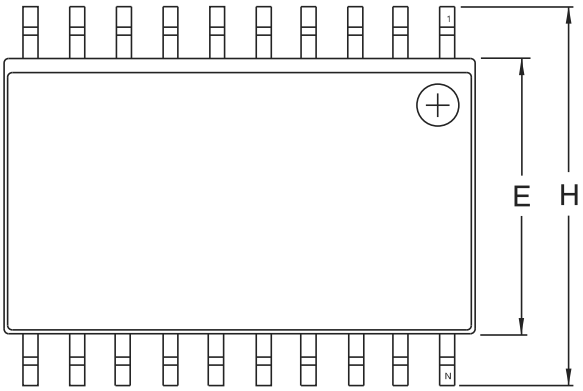
53. I_{CC} (Idle Mode) Measurements



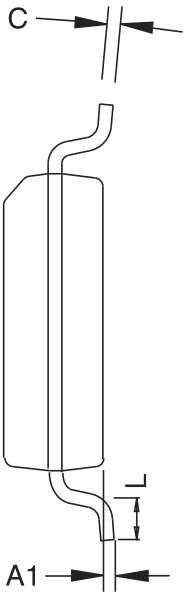
54. I_{CC} (Power Down Mode) Measurements



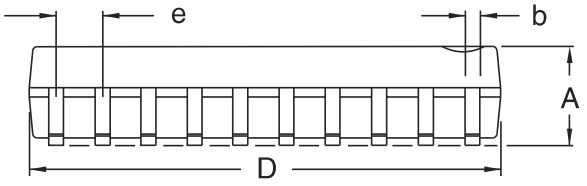
56.2 20S2 – SOIC



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure – mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	2.35		2.65	
A1	0.10		0.30	
b	0.33		0.51	4
C	0.23		0.32	
D	12.60		13.00	1
E	7.40		7.60	2
H	10.00		10.65	
L	0.40		1.27	3
e	1.27 BSC			

Notes.
1. This drawing is for general information only; refer to JEDEC Drawing MS-013, Variation AC for additional information.
2. Dimension 'D' does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006') per side.
3. Dimension 'E' does not include inter-lead Flash or protrusion. Inter-lead Flash and protrusions shall not exceed 0.25 mm (0.010') per side.
4. 'L' is the length of the terminal for soldering to a substrate.
5. The lead width 'b', as measured 0.36 mm (0.014') or greater above the seating plane, shall not exceed a maximum value of 0.61 mm (0.024') per side.

11/6/06

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**20S2**, 20-lead, 0.300' Wide Body, Plastic Gull Wing Small Outline Package (SOIC)	20S2	B

57. Revision History

Revision No.	History
Revision D – Feb. 2007	• Removed Preliminary Status. • Added the qualifier “x1 and x2 Modes” to the Static Operation range. • Changed the value ranges for Capacitors C1 and C2 in Figure 5-1 on page 4. • Changed the trigger level for the BOD from 2.2V to 2.0V.
Revision E – June 2008	• Removed Standard Packaging Offering.