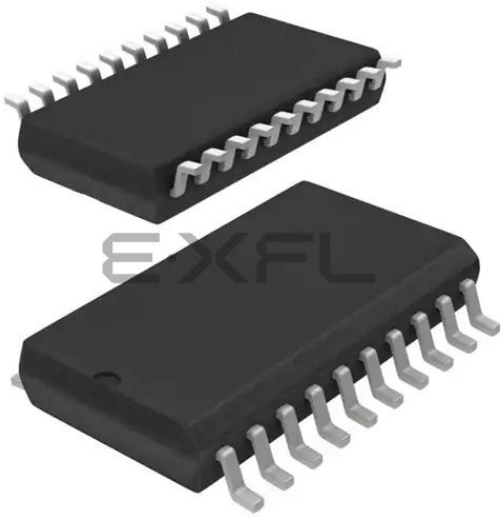

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	24MHz
Connectivity	UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM
Number of I/O	15
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at89s4051-24su

4. Pin Description

4.1 VCC

Supply voltage.

4.2 GND

Ground.

4.3 Port 1

Port 1 is an 8-bit bi-directional I/O port. Port pins P1.2 to P1.7 provide internal pull-ups. P1.0 and P1.1 require external pull-ups. P1.0 and P1.1 also serve as the positive input (AIN0) and the negative input (AIN1), respectively, of the on-chip precision analog comparator. The Port 1 output buffers can sink 20 mA and can drive LED displays directly. When 1s are written to Port 1 pins, they can be used as inputs. When pins P1.2 to P1.7 are used as inputs and are externally pulled low, they will source current (I_{IL}) because of the internal pull-ups.

Port 1 also receives code data during Flash programming and verification.

Port Pin	Alternate Functions
P1.5	MOSI (Master data output, slave data input pin for ISP channel)
P1.6	MISO (Master data input, slave data output pin for ISP channel)
P1.7	SCK (Master clock output, slave clock input pin for ISP channel)

4.4 Port 3

Port 3 pins P3.0 to P3.5, P3.7 are seven bi-directional I/O pins with internal pull-ups. P3.6 is hard-wired as an input to the output of the on-chip comparator and is not accessible as a general-purpose I/O pin. The Port 3 output buffers can sink 20 mA. When 1s are written to Port 3 pins they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pull-ups.

Port 3 also serves the functions of various special features of the AT89S2051/S4051 as listed below:

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)/ PWM output

Port 3 also receives some control signals for Flash programming and verification.

4.5 RST

Reset input. Holding the RST pin high for two machine cycles while the is running resets the device.

Each machine cycle takes 6 or clock cycles.

4.6 XTAL1

Input to the inverting amplifier and input to the internal clock operating circuit.

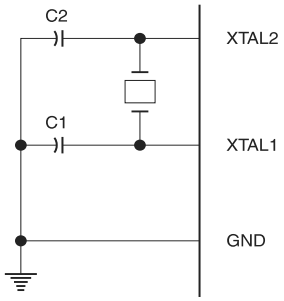
4.7 XTAL2

Output from the inverting amplifier.

5. Characteristics

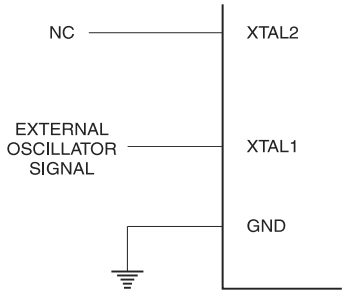
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip , as shown in Figure 5-1. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven as shown in Figure 5-2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Figure 5-1. Connections



Note: C1, C2 = 5 pF ±5 pF for Crystals
= 5 pF ±5 pF for Ceramic Resonators

Figure 5-2. External Clock Drive Configuration



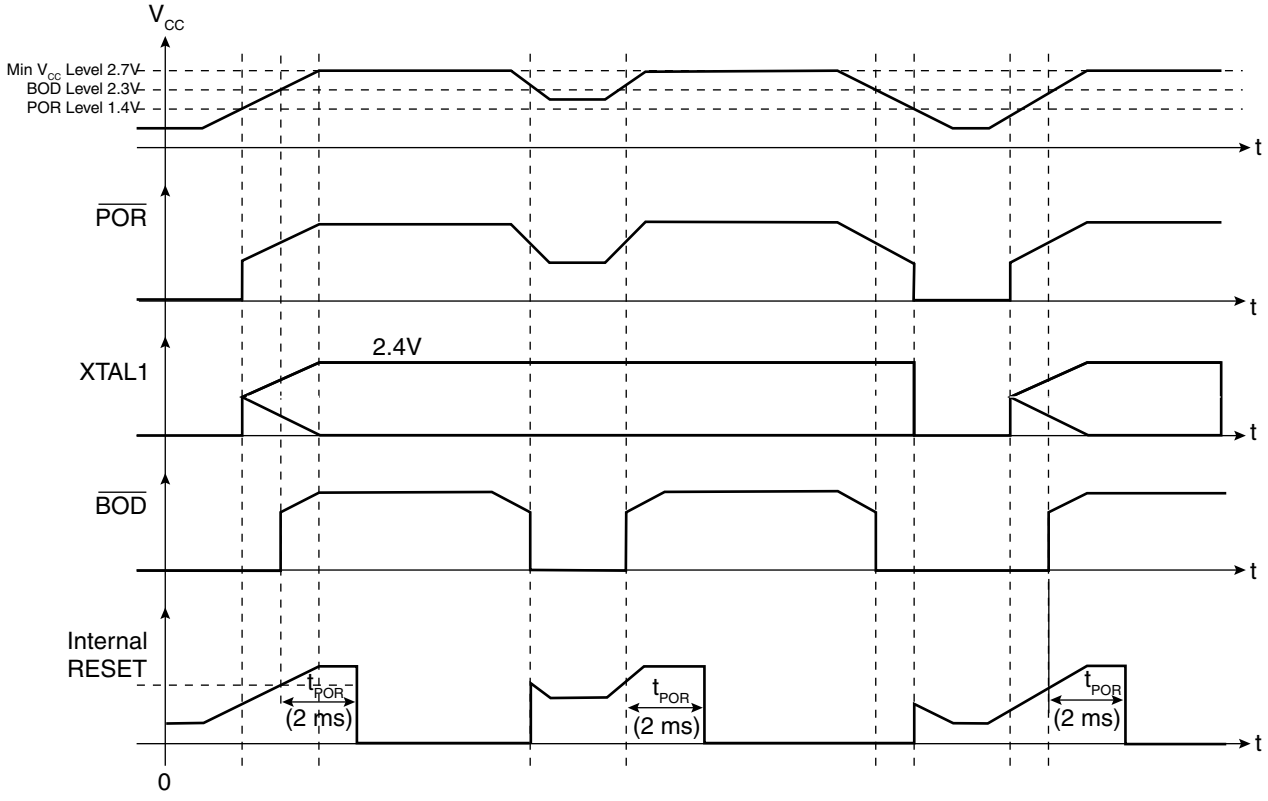
10. Reset

During reset, all I/O Registers are set to their initial values, the port pins are weakly pulled to V_{CC}, and the program starts execution from the Reset Vector, 0000H. The AT89S2051/S4051 has three sources of reset: power-on reset, brown-out reset, and external reset.

10.1 Power-On Reset

A Power-On Reset (POR) is generated by an on-chip detection circuit. The detection level is nominally 1.4V. The POR is activated whenever V_{CC} is below the detection level. The POR circuit can be used to trigger the start-up reset or to detect a supply voltage failure in devices without a brown-out detector. The POR circuit ensures that the device is reset from power-on. When V_{CC} reaches the Power-on Reset threshold voltage, the Pierce Oscillator is enabled (if the XTAL Oscillator Bypass fuse is OFF). Only after V_{CC} has also reached the BOD (brown-out detection) level (see Section 10.2 ”Brown-out Reset”), the BOD delay counter starts measuring a 2-ms delay after which the Internal Reset is deasserted and the microcontroller starts executing. The built-in 2-ms delay allows the V_{CC} voltage to reach the minimum 2.7V level before executing, thus guaranteeing the maximum operating clock frequency. The POR signal is activated again, without any delay, when V_{CC} falls below the POR threshold level. A Power-On Reset (i.e. a cold reset) will set the POF flag in PCON. Refer to Figure 10-1 for details on the POR/BOD behavior.

Figure 10-1. Power-up and Brown-out Detection Sequence



12. Power Saving Modes

The AT89S2051/S4051 supports two power-reducing modes: Idle and Power-down. These modes are accessed through the PCON register.

12.1 Idle Mode

Setting the IDL bit in PCON enters idle mode. Idle mode halts the internal CPU clock. The CPU state is preserved in its entirety, including the RAM, stack pointer, program counter, program status word, and accumulator. The Port pins hold the logical states they had at the time that Idle was activated. Idle mode leaves the peripherals running in order to allow them to wake up the CPU when an interrupt is generated. Timer 0, Timer 1, and the UART will continue to function during Idle mode. The analog comparator is disabled during Idle. Any enabled interrupt source or reset may terminate Idle mode. When exiting Idle mode with an interrupt, the interrupt will immediately be serviced, and following RETI, the next instruction to be executed will be the one following the instruction that put the device into Idle.

P1.0 and P1.1 should be set to “0” if no external pull-ups are used, or set to “1” if external pull-ups are used.

12.2 Power-down Mode

Setting the PD bit in PCON enters Power-down mode. Power-down mode stops the and powers down the Flash memory in order to minimize power consumption. Only the power-on circuitry will continue to draw power during Power-down. During Power-down the power supply voltage may be reduced to the RAM keep-alive voltage. The RAM contents will be retained; however, the SFR contents are not guaranteed once V_{CC} has been reduced. Power-down may be exited by external reset, power-on reset, or certain interrupts.

The user should not attempt to enter (or re-enter) the power-down mode for a minimum of 4 µs until after one of the following conditions has occurred: Start of code execution (after any type of reset), or Exit from power-down mode.

12.3 Interrupt Recovery from Power-down

Two external interrupts may be configured to terminate Power-down mode. External interrupts $\overline{\text{INT0}}$ (P3.2) and $\overline{\text{INT1}}$ (P3.3) may be used to exit Power-down. To wake up by external interrupt $\overline{\text{INT0}}$ or $\overline{\text{INT1}}$, the interrupt must be enabled and configured for level-sensitive operation.

When terminating Power-down by an interrupt, two different wake up modes are available. When PWDEX in CLKREG.2 is zero, the wake up period is internally timed. At the falling edge on the interrupt pin, Power-down is exited, the is restarted, and an internal timer begins counting. The internal clock will not be allowed to propagate and the CPU will not resume execution until after the timer has counted for nominally 2 ms. After the timeout period the interrupt service routine will begin. To prevent the interrupt from re-triggering, the ISR should disable the interrupt before returning. The interrupt pin should be held low until the device has timed out and begun executing.

When PWDEX = 1 the wakeup period is controlled externally by the interrupt. Again, at the falling edge on the interrupt pin, Power-down is exited and the is restarted. However, the internal clock will not propagate and CPU will not resume execution until the **rising edge** of the interrupt pin. After the rising edge on the pin, the interrupt service routine will begin. The interrupt should be held low long enough for the to stabilize.

Table 17-1. SCON – Serial Port Control Register

SCON Address = 98H — Reset Value = 0000 0000B

Bit Addressable

Bit	7	6	5	4	3	2	1	0
	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI

(SMOD = 0/1)[1]

Symbol	Function
FE	Framing error bit. This bit is set by the receiver when an invalid stop bit is detected. The FE bit is not cleared by valid frames but should be cleared by software. The SMOD0 bit must be set to enable access to the FE bit. FE will be set regardless of the state of SMOD.
SM0	Serial Port Mode Bit 0, (SMOD must = 0 to access bit SM0)
SM1	Serial Port Mode Bit 1 SM0 SM1 Mode Description Baud Rate[2] 0 0 0 shift register $f_{osc}/12$ 0 1 1 8-bit UART variable 1 0 2 9-bit UART $f_{osc}/64$ or $f_{osc}/32$ 1 1 3 9-bit UART variable
SM2	Enables the Automatic Address Recognition feature in modes 2 or 3. If SM2 = 1 then RI will not be set unless the received 9th data bit (RB8) is 1, indicating an address, and the received byte is a Given or Broadcast Address. In mode 1, if SM2 = 1 then RI will not be activated unless a valid stop bit was received, and the received byte is a Given or Broadcast Address. In Mode 0, SM2 should be 0.
REN	Enables serial reception. Set by software to enable reception. Clear by software to disable reception.
TB8	The 9th data bit that will be transmitted in modes 2 and 3. Set or clear by software as desired.
RB8	In modes 2 and 3, the 9th data bit that was received. In mode 1, if SM2 = 0, RB8 is the stop bit that was received. In mode 0, RB8 is not used.
TI	Transmit interrupt flag. Set by hardware at the end of the 8th bit time in mode 0, or at the beginning of the stop bit in the other modes, in any serial transmission. Must be cleared by software.
RI	Receive interrupt flag. Set by hardware at the end of the 8th bit time in mode 0, or halfway through the stop bit time in the other modes, in any serial reception (except see SM2). Must be cleared by software.

Notes: 1. SMOD is located at PCON.7.
2. f_{osc} = frequency.

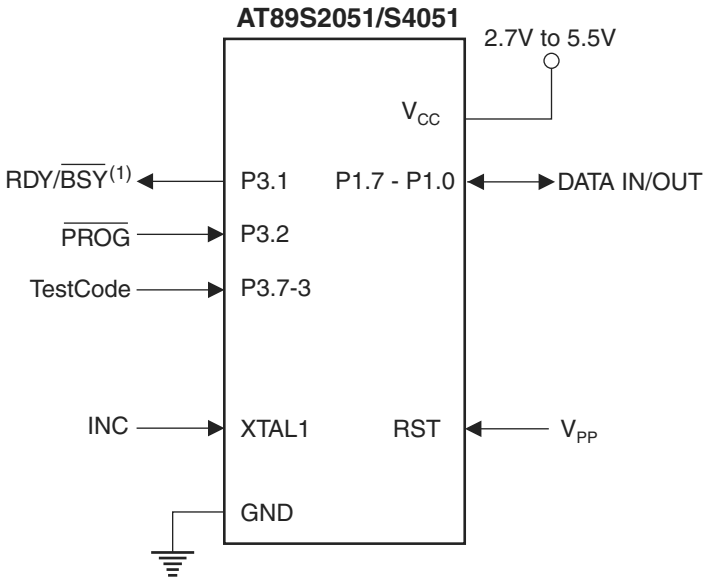
21. Parallel Programming Specification

Atmel's AT89S2051/S4051 offers 2K/4K bytes of In-System Programmable Flash code memory. In addition, the device contains a 32-byte User Signature Row and a 32-byte read-only Atmel Signature Row.

Table 21-1. Memory Organization

Device #	Page Size	# Pages	Address Range	Page Range
AT89S2051	32 bytes	64	0000H - 07FFH	00H - 3FH
AT89S4051	32 bytes	128	0000H - 0FFFH	00H - 7FH

Figure 21-1. Flash Parallel Programming Device Connections



Note: 1. Sampling of pin P3.1 (RDY/$\overline{BSY}$) is optional. In Parallel Mode, P3.1 will be pulled low while the device is busy. However, it requires an external passive pull-up to V_{CC}. Also, note that P3.6 does not exist, so TestCode connects to P3.7, P3.5, P3.4, and P3.3.

Table 21-2. Parallel Programming Mode Command Summary

Mode		Test Control			Test Selects				Data I/O
		P3.2 ⌒	RST(1)	INC ⌒	P3.3	P3.4	P3.5	P3.7	P1.7-0
Chip Erase(5)		1.0 µs	12V	L	H	L	L	L	XX
Load X-Address(2)		H	12V	0.1 µs	H	L	H	H	D_{IN}
Page Write(3)(4)(6)	**Code Memory**	1.0 µs	12V	0.1 µs	L	H	H	H	D_{IN}
Page Read(3)	**Code Memory**	H	12V	0.1 µs	L	L	H	H	D_{OUT}
Page Write(3)(4)(6)(7)	Sig. Row	1.0 µs	12V	0.1 µs	L	L	L	L	D_{IN}
Page Read(3)(8)(10)	Sig. Row	H	12V	0.1 µs	L	L	L	H	D_{OUT}
Write Fuse/Lock Bit(5)(9)		1.0 µs	12V	L	H	H	H	H	D_{IN}
Read Fuse/Lock Bit(9)		H	12V	L	H	H	L	L	D_{OUT}

Notes:
1. The internal Y-address counter is reset to 00H on the rising/falling edge of RST.
2. A positive pulse on XTAL1 loads the address data on Port P1 into the X-address (page) register and resets the Y-address.
3. A positive pulse on XTAL1 advances the Y-address counter.
4. A low pulse on P3.2 loads data from Port P1 for the current address. If another P3.2 low pulse does not arrive within 150 µs, programming starts.
5. Internally timed for 4 ms.
6. Internally timed for 2 ms.
7. 00H must be loaded into the X-address before executing this command.
8. Will read User Signature if X-address is 00H, will read Atmel Signature if X-address is 01H.
9. Fuse/Lock Bit Definitions:

Bit 7	XTAL Osc Bypass	Enable = 0/Disable = 1
Bit 6	User Row Programming	Enable = 0/Disable = 1
Bit 5	x2 Clock	Enable = 0/Disable = 1
Bit 4	Serial Programming	Enable = 0/Disable = 1
Bit 1	Lock Bit 2	Locked = 0/Unlocked = 1
Bit 0	Lock Bit 1	Locked = 0/Unlocked = 1

10. **Atmel Signature Bytes**:

AT89S2051:	Address	00H = 1EH
		01H = 23H
		02H = FFH
AT89S4051:	Address	00H = 1EH
		01H = 43H
		02H = FFH

24. Chip Erase

Function:

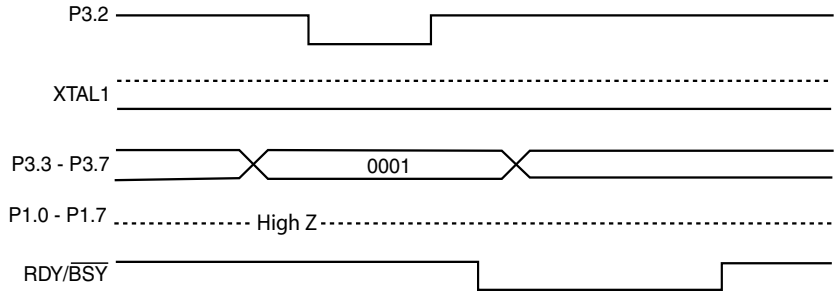
1. FFH programmed to every address location.
2. FFH programmed to User Signature Row if User Row Fuse bit is enabled.
3. Lockbit1 and Lockbit2 programmed to “unlock” state.

Usage:

1. Apply “0001” TestCode to P3.7, P3.5, P3.4, P3.3.
2. Pulse P3.2 low for 1 µs.
3. Wait 4 ms, monitor P3.1, or poll data.

Note: This and the following waveforms are not to scale.

Figure 24-1. Chip Erase Sequence



25. Load X-Address

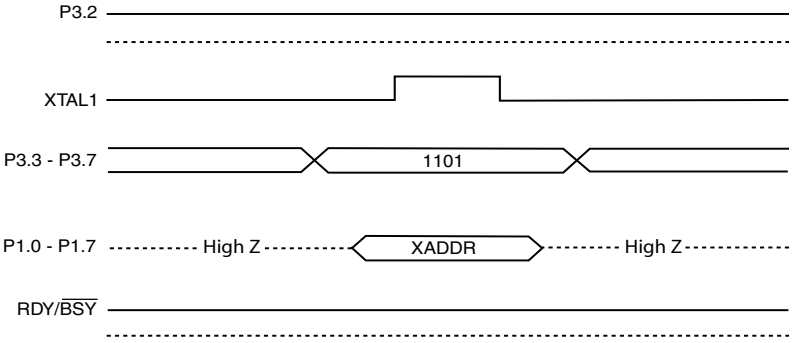
Function:

1. Loads the X-Address register with data on Port P1. The loaded address will select the page for subsequent write/read commands. The X-Address is equivalent to bits [11:5] of the full byte address.
2. Resets the Y-Address counter to 00H. The Y-Address is equivalent to bits [4:0] of the full byte address and selects a byte within a page.

Usage:

1. Apply “1101” TestCode to P3.7, P3.5, P3.4, P3.3.
2. Drive Port P1 with 8-bit X-address data.
3. Pulse XTAL1 high for at least 100 ns. The address is latched on the falling edge of XTAL1.

Figure 25-1. Load X-Address Sequence



29. Read User Signature Row

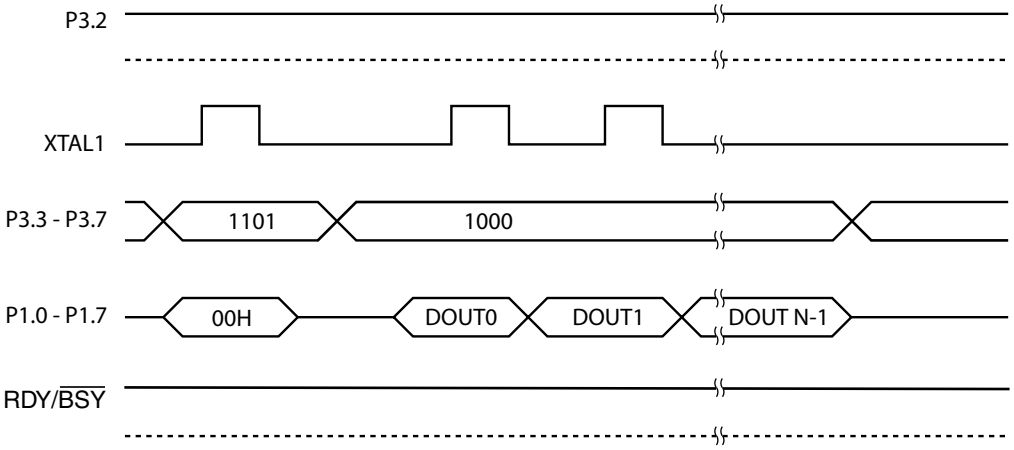
Function:

1. Reads 1 to 32 bytes of data from the User Signature Row.
2. X-address (page) should be 00H from a previous Load-X command.
3. Y-address (offset) incremented by positive pulse on XTAL1.

Usage:

1. Execute the Load-X command to set the page to 00H and reset the offset.
2. Apply “1000” TestCode to P3.7, P3.5, P3.4, P3.3.
3. Read 8-bit data on Port P1.
4. For additional bytes (up to 32), pulse XTAL1 high for at least 100 ns to increment the Y-address and repeat step 3. The address will change on the falling edge of XTAL1.

Figure 29-1. Read User Signature Row Sequence



31. Write Lock Bits/User Fuses

Function:

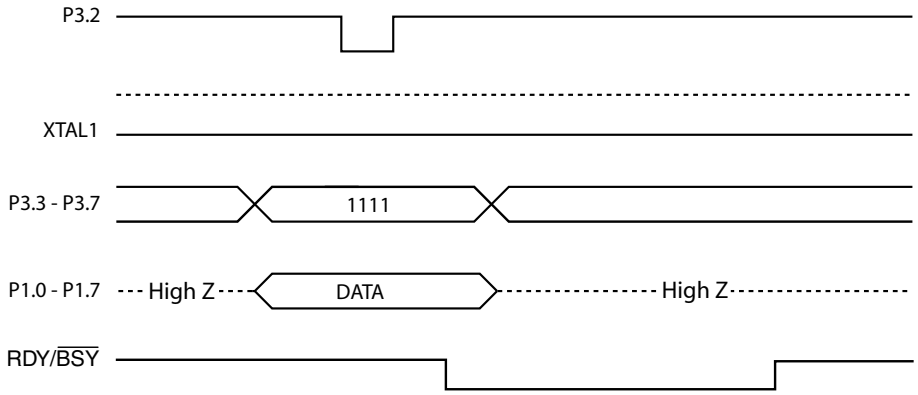
1. Program Lock Bits 1 and 2.
2. Program user fuses.

Usage:

1) Apply “1111” TestCode to P3.7, P3.5, P3.4, P3.3.

3. Drive Port P1 with fuse data, bits [7:4] for fuses and bits [1:0] for lock bits.
4. Pulse P3.2 low for 1 µs.
5. Wait 4 ms, monitor P3.1, or poll data.

Figure 31-1. Write Lock Bits/User Fuses



32. Read Lock Bits/User Fuses

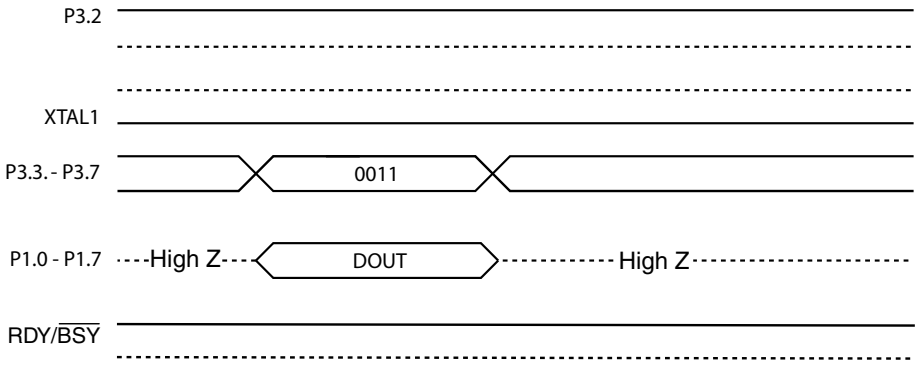
Function:

1. Read status of Lock Bits 1 and 2.
2. Read status of user fuses.

Usage:

1. Apply “0011” TestCode to P3.7, P3.5, P3.4, P3.3.
2. Read fuse data from Port P1, bits [7:4] for fuses and bits [1:0] for lock bits.

Figure 32-1. Read Lock Bits/User Fuses

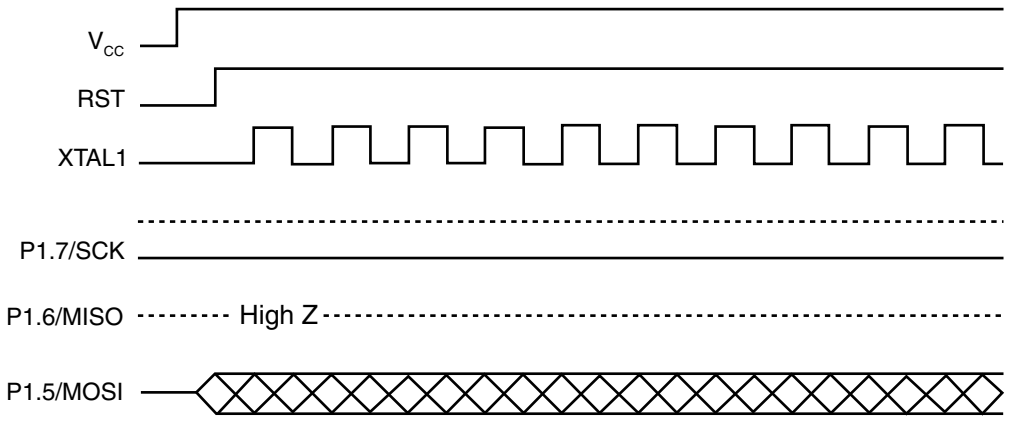


35. Power-up Sequence

Execute this sequence to power-up the device **before** programming.

1. Apply power between VCC and GND pins.
2. Keep SCK (P1.7) at GND.
3. Wait 10 µs and bring RST to “H”.
4. If a crystal is connected between XTAL1 and XTAL2, wait at least 10 ms; otherwise, apply a 3 - 24 MHz clock to XTAL1 and wait 4 ms.

Figure 35-1. ISP Power-up Sequence

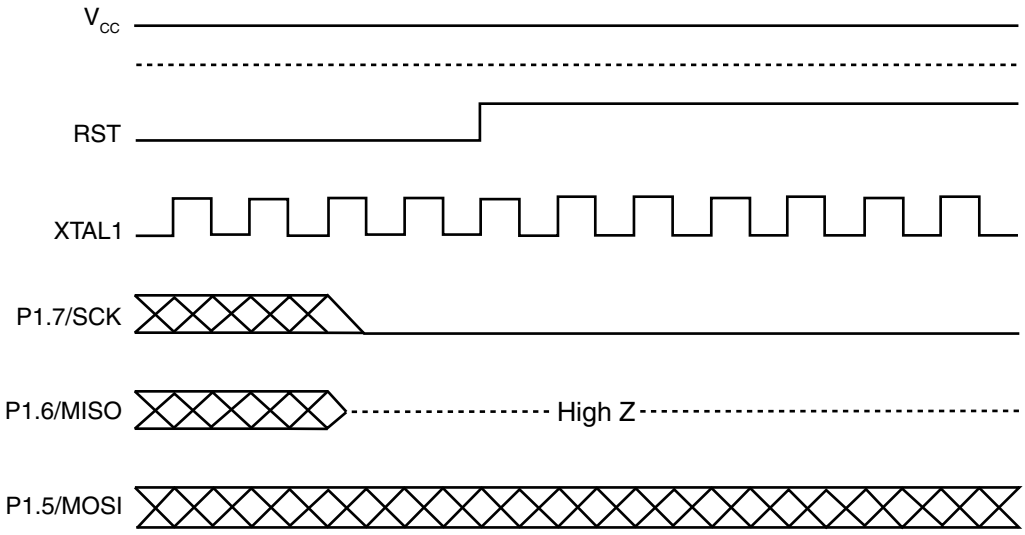


36. ISP Start Sequence

Execute this sequence to enter ISP when the device is **already** operational.

1. Bring SCK (P1.7) to GND.
2. Tri-state MISO (P1.6).
3. Bring RST to “H”.

Figure 36-1. ISP Start Sequence

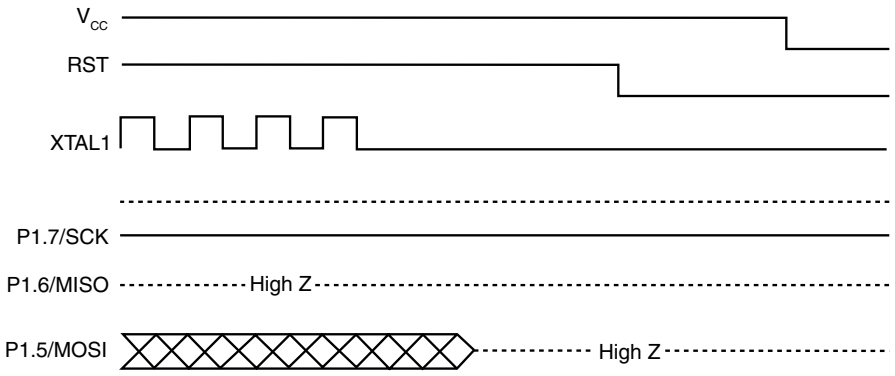


37. Power-down Sequence

Execute this sequence to power-down the device **after** programming.

1. Set XTAL1 to “L” if a crystal is not used.
2. Bring RST to “L”.
3. Tri-state MOSI (P1.5).

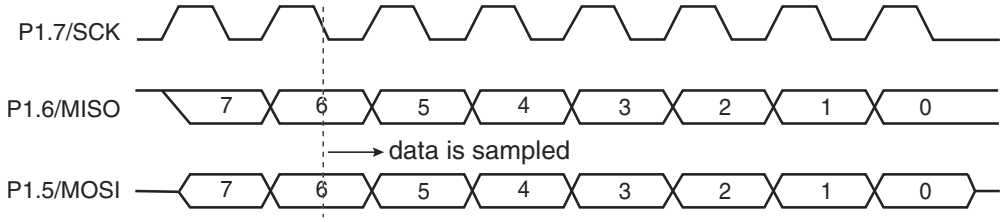
Figure 37-1. ISP Power-down Sequence



38. ISP Byte Sequence

1. Data shifts in/out MSB first.
2. MISO changes at **rising** of SCK.
3. MOSI is sampled at **falling** edge of SCK.

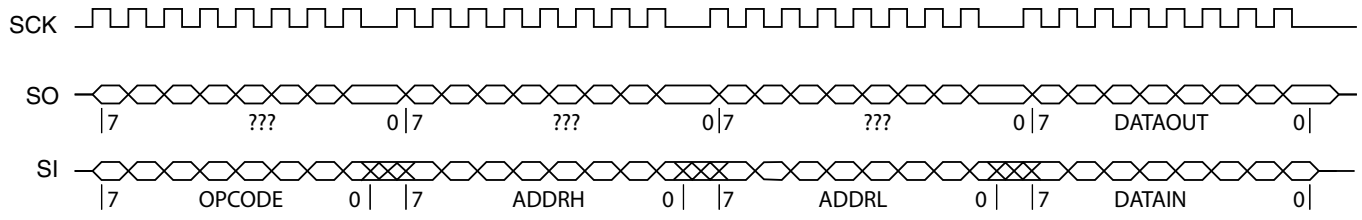
Figure 38-1. ISP Byte Sequence



39. ISP Command Sequence

1. **Byte** Format: 4 byte packet (3 header bytes + 1 data byte)
2. **Page** Format: 35 byte packet (3 header bytes + 32 data bytes)
3. All bytes are required, even if they are don’t care.

Figure 39-1. ISP Command Sequence



40. Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-0.7V to +6.2V
Maximum Operating Voltage	5.5V
DC Output Current	25.0 mA (15.0 mA for AT89S4051)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

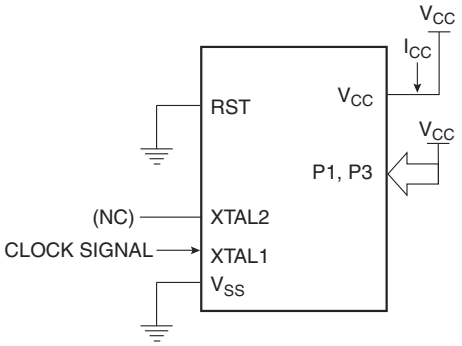
41. DC Characteristics

T_A = -40°C to 85°C, V_{CC} = 2.7V to 5.5V (unless otherwise noted)

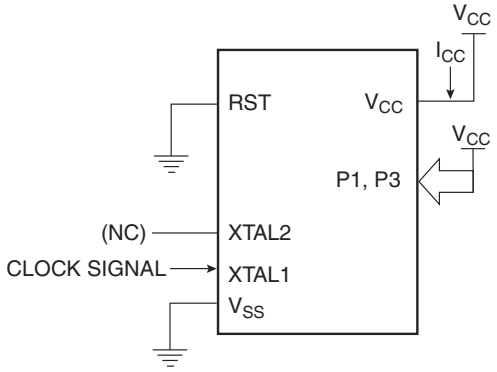
Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low-voltage		-0.5	0.2 V_{CC} - 0.1	V
V_{IH}	Input High-voltage	(Except XTAL1, RST)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V
V_{IH1}	Input High-voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low-voltage(1) (Ports 1, 3)	I_{OL} = 10 mA, V_{CC} = 2.7V, T_A = 85°C		0.5	V
V_{OH}	Output High-voltage (Ports 1, 3)	I_{OH} = -80 µA, V_{CC} = 5V ±10%	2.4		V
		I_{OH} = -30 µA	0.75 V_{CC}		V
		I_{OH} = -12 µA	0.9 V_{CC}		V
I_{IL}	Logical 0 Input Current (Ports 1, 3)	V_{IN} = 0.45V		-50	µA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1, 3)	V_{IN} = 2V, V_{CC} = 5V ±10%		-350	µA
I_{LI}	Input Leakage Current (Port P1.0, P1.1)	0 < V_{IN} < V_{CC}		±10	µA
V_{OS}	Comparator Input Offset Voltage	V_{CC} = 5V		20	mV
V_{CM}	Comparator Input Common Mode Voltage		0	V_{CC}	V
RRST	Reset Pull-down Resistor		50	150	KΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current (without the)	Active Mode, 24/12 MHz, V_{CC} = 5V/3V		10.5/3.5	mA
		Idle Mode, 24/12 MHz, V_{CC} = 5V/3V P1.0 & P1.1 = 0V or V_{CC}		4.5/2.5	mA
	Power-down Mode(2)	V_{CC} = 5V, P1.0 & P1.1 = 0V or V_{CC}(3)		10	µA
		V_{CC} = 3V, P1.0 & P1.1 = 0V or V_{CC}(3)		5	µA

Notes:
1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum total I_{OL} for all output pins: 25 mA (15 mA for AT89S4051)
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V.
3. P1.0 and P1.1 are comparator inputs and have no internal pullups. They should not be left floating.

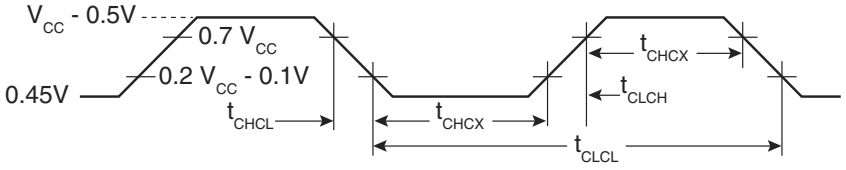
48. I_{CC} Test Condition, Active Mode, All Other Pins are Disconnected



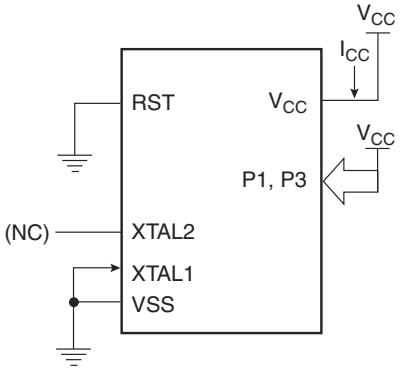
49. I_{CC} Test Condition, Idle Mode, All Other Pins are Disconnected



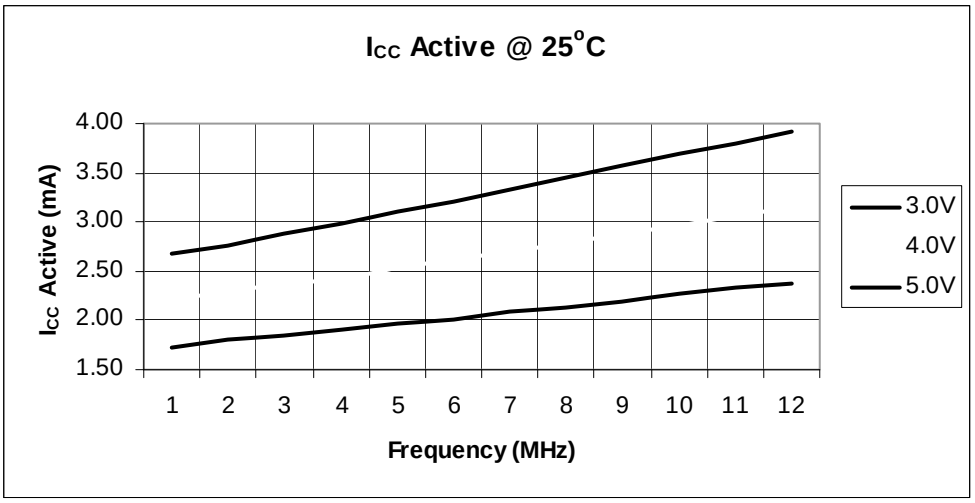
50. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes, $t_{CLCH} = t_{CHCL} = 5$ ns

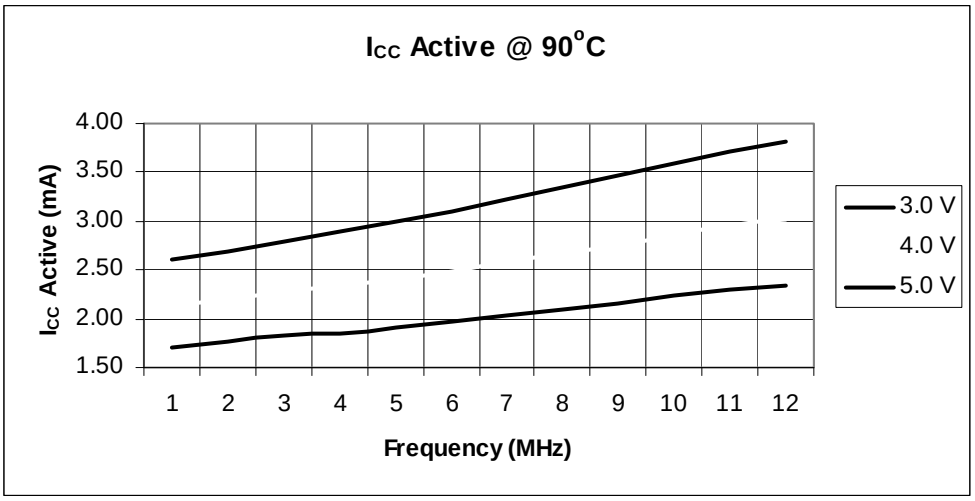


51. I_{CC} Test Condition, Power-down Mode, All Other Pins are Disconnected, V_{CC} = 2V to 5.5V



52. I_{CC} (Active Mode) Measurements





55. Ordering Information

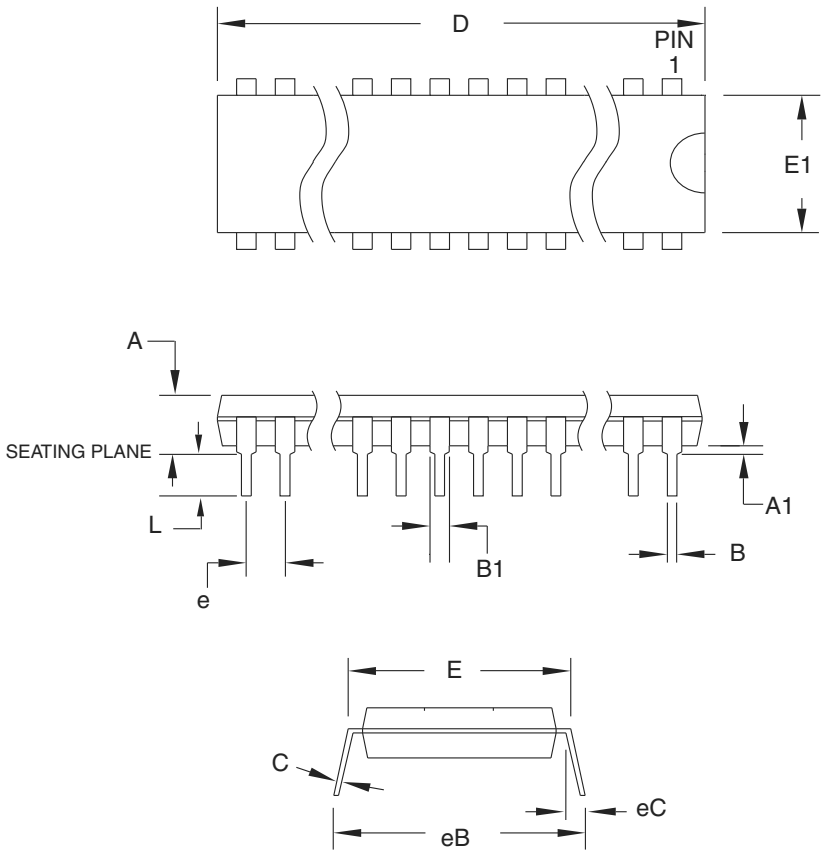
55.1 Green Package Option (Pb/Halide-free)

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
24	2.7V to 5.5V	AT89S2051/S4051-24PU AT89S2051/S4051-24SU	20P3 20S2	Industrial (-40° C to 85° C)

Package Type	
20P3	20-lead, 0.300” Wide, Plastic Dual In-line Package (PDIP)
20S2	20-lead, 0.300” Wide, Plastic Gull Wing Small Outline (SOIC)

56. Package Information

56.1 20P3 – PDIP



COMMON DIMENSIONS
(Unit of Measure = mm)

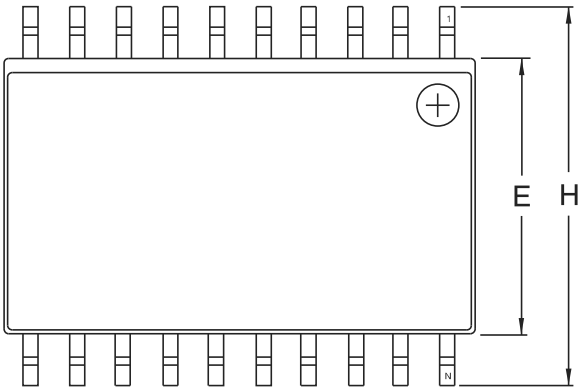
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	5.334	
A1	0.381	–	–	
D	24.892	–	26.924	Note 2
E	7.620	–	8.255	
E1	6.096	–	7.112	Note 2
B	0.356	–	0.559	
B1	1.270	–	1.551	
L	2.921	–	3.810	
C	0.203	–	0.356	
eB	–	–	10.922	
eC	0.000	–	1.524	
e	2.540 TYP			

Notes: 1. This package conforms to JEDEC reference MS-001, Variation AD.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

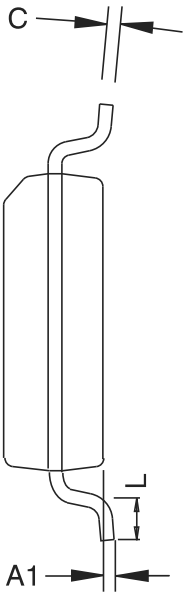
1/23/04

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**20P3**, 20-lead (0.300"/7.62 mm Wide) Plastic Dual Inline Package (PDIP)	20P3	D

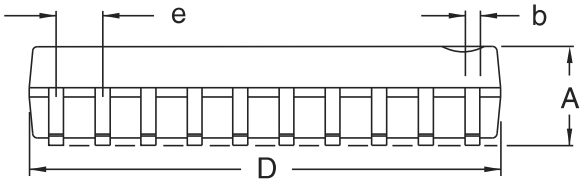
56.2 20S2 – SOIC



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure – mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	2.35		2.65	
A1	0.10		0.30	
b	0.33		0.51	4
C	0.23		0.32	
D	12.60		13.00	1
E	7.40		7.60	2
H	10.00		10.65	
L	0.40		1.27	3
e	1.27 BSC			

Notes.
1. This drawing is for general information only; refer to JEDEC Drawing MS-013, Variation AC for additional information.
2. Dimension 'D' does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006') per side.
3. Dimension 'E' does not include inter-lead Flash or protrusion. Inter-lead Flash and protrusions shall not exceed 0.25 mm (0.010') per side.
4. 'L' is the length of the terminal for soldering to a substrate.
5. The lead width 'b', as measured 0.36 mm (0.014') or greater above the seating plane, shall not exceed a maximum value of 0.61 mm (0.024') per side.

11/6/06

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**20S2**, 20-lead, 0.300' Wide Body, Plastic Gull Wing Small Outline Package (SOIC)	20S2	B

57. Revision History

Revision No.	History
Revision D – Feb. 2007	• Removed Preliminary Status. • Added the qualifier “x1 and x2 Modes” to the Static Operation range. • Changed the value ranges for Capacitors C1 and C2 in Figure 5-1 on page 4. • Changed the trigger level for the BOD from 2.2V to 2.0V.
Revision E – June 2008	• Removed Standard Packaging Offering.

Headquarters

Atmel Corporation
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

International

Atmel Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Atmel Europe
Le Krebs
8, Rue Jean-Pierre Timbaud
BP 309
78054 Saint-Quentin-en-
Yvelines Cedex
France
Tel: (33) 1-30-60-70-00
Fax: (33) 1-30-60-71-11

Atmel Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Product Contact

Web Site
www.atmel.com

Technical Support
mcu@atmel.com

Sales Contact
www.atmel.com/contacts

Literature Requests
www.atmel.com/literature