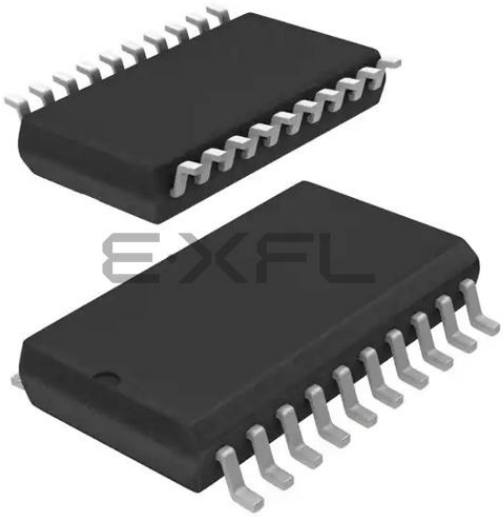

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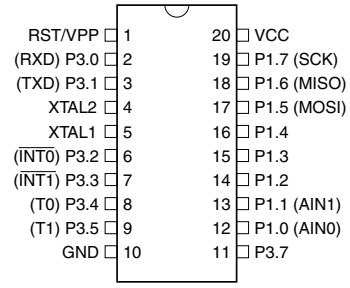
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	24MHz
Connectivity	UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM
Number of I/O	15
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at89s4051-24sur

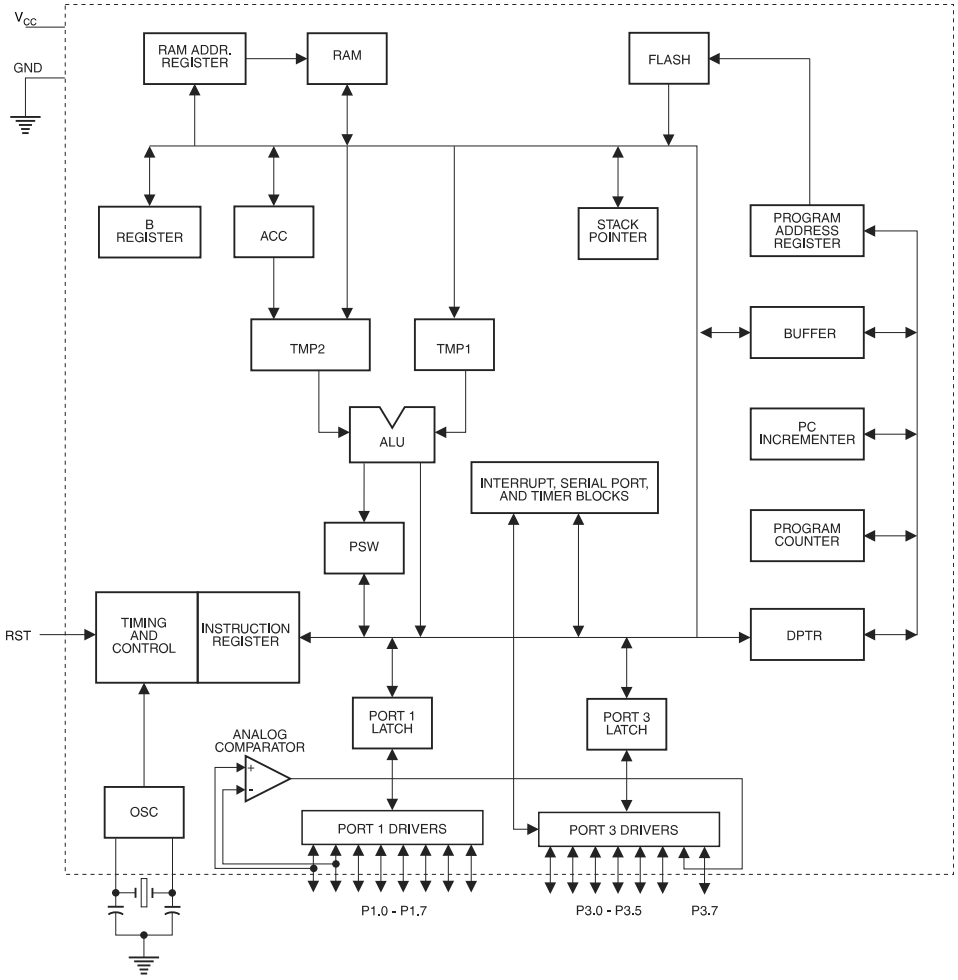
The on-board Flash program memory is accessible through the ISP serial interface. Holding RST active forces the device into a serial programming interface and allows the program memory to be written to or read from, unless one or more lock bits have been activated.

2. Pin Configuration

2.1 20-lead PDIP/SOIC



3. Block Diagram



4. Pin Description

4.1 VCC

Supply voltage.

4.2 GND

Ground.

4.3 Port 1

Port 1 is an 8-bit bi-directional I/O port. Port pins P1.2 to P1.7 provide internal pull-ups. P1.0 and P1.1 require external pull-ups. P1.0 and P1.1 also serve as the positive input (AIN0) and the negative input (AIN1), respectively, of the on-chip precision analog comparator. The Port 1 output buffers can sink 20 mA and can drive LED displays directly. When 1s are written to Port 1 pins, they can be used as inputs. When pins P1.2 to P1.7 are used as inputs and are externally pulled low, they will source current (I_{IL}) because of the internal pull-ups.

Port 1 also receives code data during Flash programming and verification.

Port Pin	Alternate Functions
P1.5	MOSI (Master data output, slave data input pin for ISP channel)
P1.6	MISO (Master data input, slave data output pin for ISP channel)
P1.7	SCK (Master clock output, slave clock input pin for ISP channel)

4.4 Port 3

Port 3 pins P3.0 to P3.5, P3.7 are seven bi-directional I/O pins with internal pull-ups. P3.6 is hard-wired as an input to the output of the on-chip comparator and is not accessible as a general-purpose I/O pin. The Port 3 output buffers can sink 20 mA. When 1s are written to Port 3 pins they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pull-ups.

Port 3 also serves the functions of various special features of the AT89S2051/S4051 as listed below:

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)/ PWM output

Port 3 also receives some control signals for Flash programming and verification.

4.5 RST

Reset input. Holding the RST pin high for two machine cycles while the is running resets the device.

Each machine cycle takes 6 or clock cycles.

4.6 XTAL1

Input to the inverting amplifier and input to the internal clock operating circuit.

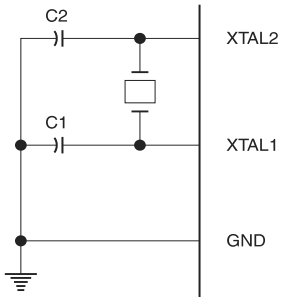
4.7 XTAL2

Output from the inverting amplifier.

5. Characteristics

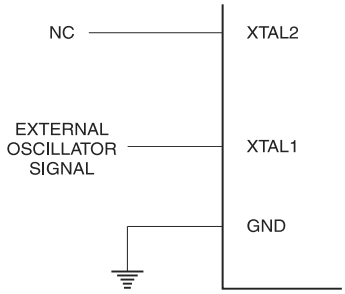
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip , as shown in Figure 5-1. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven as shown in Figure 5-2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Figure 5-1. Connections



Note: C1, C2 = 5 pF ±5 pF for Crystals
= 5 pF ±5 pF for Ceramic Resonators

Figure 5-2. External Clock Drive Configuration



8. Restrictions on Certain Instructions

The AT89S2051/S4051 is an economical and cost-effective member of Atmel's family of microcontrollers. It contains 2K/4K bytes of Flash program memory. It is fully compatible with the MCS-51 architecture, and can be programmed using the MCS-51 instruction set. However, there are a few considerations one must keep in mind when utilizing certain instructions to program this device.

All the instructions related to jumping or branching should be restricted such that the destination address falls within the physical program memory space of the device, which is 2K/4K for the AT89S2051/S4051. This should be the responsibility of the software programmer. For example, LJMP 7E0H would be a valid instruction for the AT89S2051 (with 2K of memory), whereas LJMP 900H would not.

8.1 Branching Instructions

LCALL, LJMP, ACALL, AJMP, SJMP, JMP @A+DPTR. These unconditional branching instructions will execute correctly as long as the programmer keeps in mind that the destination branching address must fall within the physical boundaries of the program memory size (locations 00H to 7FFH/FFFH for the AT89S2051/S4051). Violating the physical space limits may cause unknown program behavior.

CJNE [...], DJNZ [...], JB, JNB, JC, JNC, JBC, JZ, JNZ. With these conditional branching instructions, the same rule above applies. Again, violating the memory boundaries may cause erratic execution.

For applications involving interrupts, the normal interrupt service routine address locations of the 80C51 family architecture have been preserved.

8.2 MOVX-related Instructions, Data Memory

The AT89S2051/S4051 contains 256 bytes of internal data memory. External DATA memory access is not supported in this device, nor is external PROGRAM memory execution. Therefore, no MOVX [...] instructions should be included in the program.

A typical 80C51 assembler will still assemble instructions, even if they are written in violation of the restrictions mentioned above. It is the responsibility of the user to know the physical features and limitations of the device being used and adjust the instructions used accordingly.

9. Program Memory Lock Bits

On the chip are two lock bits which can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in Table 9-1:

Table 9-1. Lock Bit Protection Modes[1]

Program Lock Bits			
	LB1	LB2	Protection Type
1	U	U	No program lock features.
2	P	U	Further programming of the Flash is disabled.
3	P	P	Same as mode 2, also verify is disabled.

Note: 1. The Lock Bits can only be erased with the Chip Erase operation.

12.4 Reset Recovery from Power-down

Wakeup from Power-down through an external reset is similar to the interrupt with PWDEX = 0. At the rising edge of RST, Power-down is exited, the is restarted, and an internal timer begins counting. The internal clock will not be allowed to propagate to the CPU until after the timer has counted for nominally 2 ms. The RST pin must be held high for longer than the timeout period to ensure that the device is reset properly. The device will begin executing once RST is brought low.

It should be noted that when idle is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

P1.0 and P1.1 should be set to “0” if no external pull-ups are used, or set to “1” if external pull-ups are used.

Table 12-1. PCON – Power Control Register

PCON = 87H — Reset Value = 000X 0000B

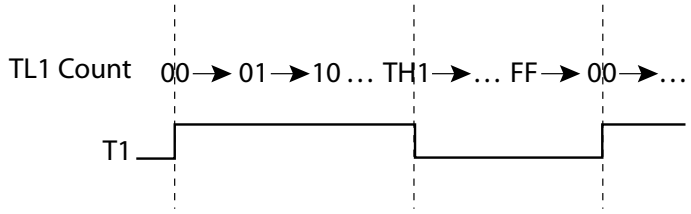
Not Bit Addressable

	SMOD1	SMOD0	PWMEN	POF	GF1	GF0	PD	IDL
Bit	7	6	5	4	3	2	1	0

Symbol	Function
SMOD1	Double Baud Rate bit. Doubles the baud rate of the UART in modes 1, 2, or 3.
SMOD0	Frame Error Select. When SMOD0 = 0, SCON.7 is SM0. When SMOD0 = 1, SCON.7 is FE. Note that FE will be set after a frame error regardless of the state of SMOD0.
PWMEN	Pulse Width Modulation Enable. When PWMEN = 1, Timer 0 and Timer 1 are configured as an 8-bit PWM counter with 8-bit auto-reload prescaler. The PWM outputs on T1 (P3.5).
POF	Power Off Flag. POF is set to “1” during power up (i.e. cold reset). It can be set or reset under software control and is not affected by RST or BOD (i.e. warm resets).
GF1, GF0	General-purpose Flags
PD	Power Down bit. Setting this bit activates power down operation.
IDL	Idle Mode bit. Setting this bit activates idle mode operation

TL1 will always count from 00h to FFh. The output on the Timer 1 (T1) pin will be high from when TL1 equals 00h until TL1 equals TH1 (see Figure 16-3). TH1 does not act as the reload value for TL1 on overflow. Instead, TH1 is used strictly as a compare value (see Figure 16-2).

Figure 16-3. Example of a PWM Output



17. UART

The UART in the AT89S2051/S4051 operates the same way as the UART in the AT89C2051/C4051. For more detailed information on the UART operation, please click on the document link below:

http://www.atmel.com/dyn/resources/prod_documents/DOC4316.PDF

17.1 Enhanced UART

In addition to all of its usual modes, the UART can perform framing error detection by looking for missing stop bits, and automatic address recognition. The UART also fully supports multiprocessor communication as does the standard 80C51 UART.

When used for framing error detect, the UART looks for missing stop bits in the communication. A missing bit will set the FE bit in the SCON register. The FE bit shares the SCON.7 bit with SM0 and the function of SCON.7 is determined by PCON.6 (SMOD0). If SMOD0 is set then SCON.7 functions as FE. SCON.7 functions as SM0 when SMOD0 is cleared. When used as FE, SCON.7 can only be cleared by software.

17.2 Automatic Address Recognition

Automatic Address Recognition is a feature which allows the UART to recognize certain addresses in the serial bit stream by using hardware to make the comparisons. This feature saves a great deal of software overhead by eliminating the need for the software to examine every serial address which passes by the serial port. This feature is enabled by setting the SM2 bit in SCON. In the 9-bit UART modes, mode 2 and mode 3, the Receive Interrupt flag (RI) will be automatically set when the received byte contains either the “Given” address or the “Broadcast” address. The 9-bit mode requires that the 9th information bit is a 1 to indicate that the received information is an address and not data.

The 8-bit mode is called mode 1. In this mode the RI flag will be set if SM2 is enabled and the information received has a valid stop bit following the 8 address bits and the information is either a Given or Broadcast address.

Mode 0 is the Shift Register mode and SM2 is ignored.

Using the Automatic Address Recognition feature allows a master to selectively communicate with one or more slaves by invoking the given slave address or addresses. All of the slaves may be contacted by using the Broadcast address. Two special Function Registers are used to define the slave’s address, SADDR, and the address mask, SADEN. SADEN is used to define which bits in the SADDR are to be used and which bits are “don’t care”. The SADEN mask can

Table 17-1. SCON – Serial Port Control Register

SCON Address = 98H — Reset Value = 0000 0000B

Bit Addressable

Bit	7	6	5	4	3	2	1	0
	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI

(SMOD = 0/1)[1]

Symbol	Function
FE	Framing error bit. This bit is set by the receiver when an invalid stop bit is detected. The FE bit is not cleared by valid frames but should be cleared by software. The SMOD0 bit must be set to enable access to the FE bit. FE will be set regardless of the state of SMOD.
SM0	Serial Port Mode Bit 0, (SMOD must = 0 to access bit SM0)
SM1	Serial Port Mode Bit 1 SM0 SM1 Mode Description Baud Rate[2] 0 0 0 shift register $f_{osc}/12$ 0 1 1 8-bit UART variable 1 0 2 9-bit UART $f_{osc}/64$ or $f_{osc}/32$ 1 1 3 9-bit UART variable
SM2	Enables the Automatic Address Recognition feature in modes 2 or 3. If SM2 = 1 then RI will not be set unless the received 9th data bit (RB8) is 1, indicating an address, and the received byte is a Given or Broadcast Address. In mode 1, if SM2 = 1 then RI will not be activated unless a valid stop bit was received, and the received byte is a Given or Broadcast Address. In Mode 0, SM2 should be 0.
REN	Enables serial reception. Set by software to enable reception. Clear by software to disable reception.
TB8	The 9th data bit that will be transmitted in modes 2 and 3. Set or clear by software as desired.
RB8	In modes 2 and 3, the 9th data bit that was received. In mode 1, if SM2 = 0, RB8 is the stop bit that was received. In mode 0, RB8 is not used.
TI	Transmit interrupt flag. Set by hardware at the end of the 8th bit time in mode 0, or at the beginning of the stop bit in the other modes, in any serial transmission. Must be cleared by software.
RI	Receive interrupt flag. Set by hardware at the end of the 8th bit time in mode 0, or halfway through the stop bit time in the other modes, in any serial reception (except see SM2). Must be cleared by software.

Notes: 1. SMOD is located at PCON.7.
2. f_{osc} = frequency.

18. Analog Comparator

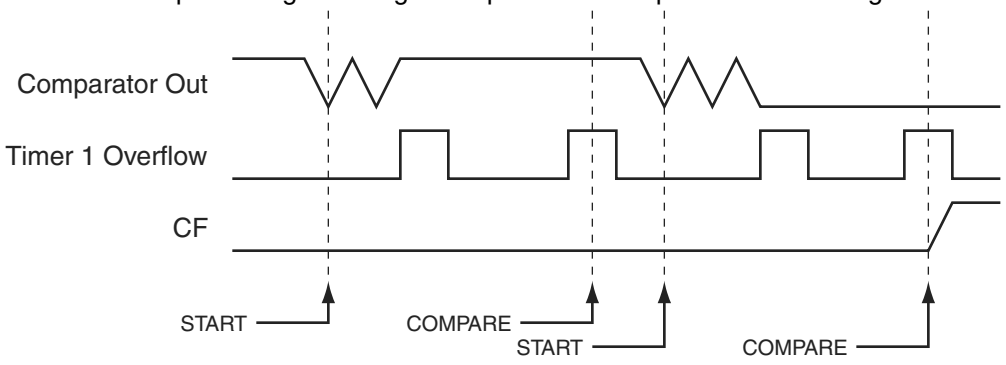
A single analog comparator is provided in the AT89S2051/S4051. The comparator operation is such that the output is a logical “1” when the positive input AIN0 (P1.0]) is greater than the negative input AIN1 (P1.1). Otherwise the output is a zero. Setting the CEN bit in ACSR enables the comparator. When the comparator is first enabled, the comparator output and interrupt flag are not guaranteed to be stable for 10 microseconds. The corresponding comparator interrupt should not be enabled during that time, and the comparator interrupt flag must be cleared before the interrupt is enabled in order to prevent an immediate interrupt service.

The comparator may be configured to cause an interrupt under a variety of output value conditions by setting the CM bits in ACSR. The comparator interrupt flag CF in ACSR is set whenever the comparator output matches the condition specified by CM. The flag may be polled by software or may be used to generate an interrupt and must be cleared by software. The analog comparator is always disabled during Idle or Power-down modes.

19. Comparator Interrupt with Debouncing

The comparator output is sampled at every State 4 (S4) of every machine cycle. The conditions on the analog inputs may be such that the comparator output will toggle excessively. This is especially true if applying slow moving analog inputs. Three debouncing modes are provided to filter out this noise. In debouncing mode, the comparator uses Timer 1 to modulate its sampling time. When a relevant transition occurs, the comparator waits until two Timer 1 overflows have occurred before resampling the output. If the new sample agrees with the expected value, CF is set. Otherwise, the event is ignored. The filter may be tuned by adjusting the timeout period of Timer 1. Because Timer 1 is free running, the debouncer must wait for two overflows to guarantee that the sampling delay is at least 1 timeout period. Therefore after the initial edge event, the interrupt may occur between 1 and 2 timeout periods later. See Figure 19-1.

Figure 19-1. Example of Negative Edge Comparator Interrupt with Debouncing



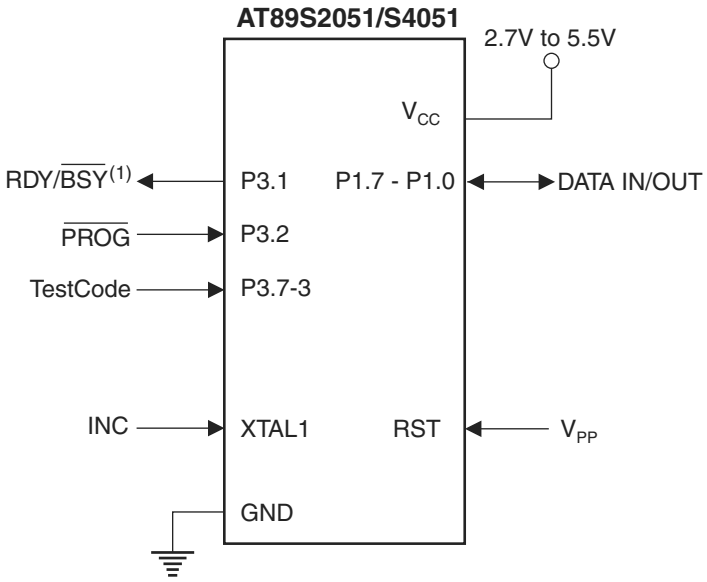
21. Parallel Programming Specification

Atmel's AT89S2051/S4051 offers 2K/4K bytes of In-System Programmable Flash code memory. In addition, the device contains a 32-byte User Signature Row and a 32-byte read-only Atmel Signature Row.

Table 21-1. Memory Organization

Device #	Page Size	# Pages	Address Range	Page Range
AT89S2051	32 bytes	64	0000H - 07FFH	00H - 3FH
AT89S4051	32 bytes	128	0000H - 0FFFH	00H - 7FH

Figure 21-1. Flash Parallel Programming Device Connections



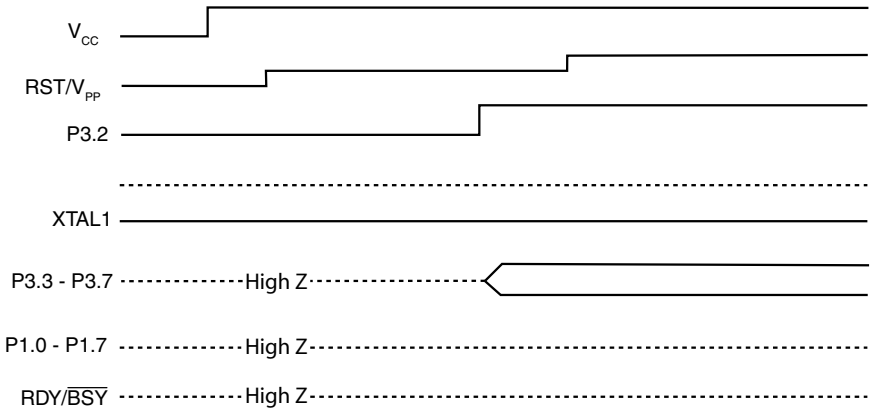
Note: 1. Sampling of pin P3.1 (RDY/$\overline{BSY}$) is optional. In Parallel Mode, P3.1 will be pulled low while the device is busy. However, it requires an external passive pull-up to V_{CC}. Also, note that P3.6 does not exist, so TestCode connects to P3.7, P3.5, P3.4, and P3.3.

22. Power-up Sequence

Execute the following sequence to power-up the device before programming.

1. Apply power between VCC and GND pins.
2. After V_{CC} has settled, wait 10 µs and bring RST to “H”.
3. Wait 4 ms for the internal Power-on Reset to timeout.
4. Bring P3.2 to “H” and drive P3.7, P3.5, P3.4, and P3.3 to known values, then wait 10 µs.
5. Raise RST/V_{PP} to 12V to enable the parallel programming modes.
6. After V_{PP} has settled, wait an additional 10 µs before programming.

Figure 22-1. Power-up Operation

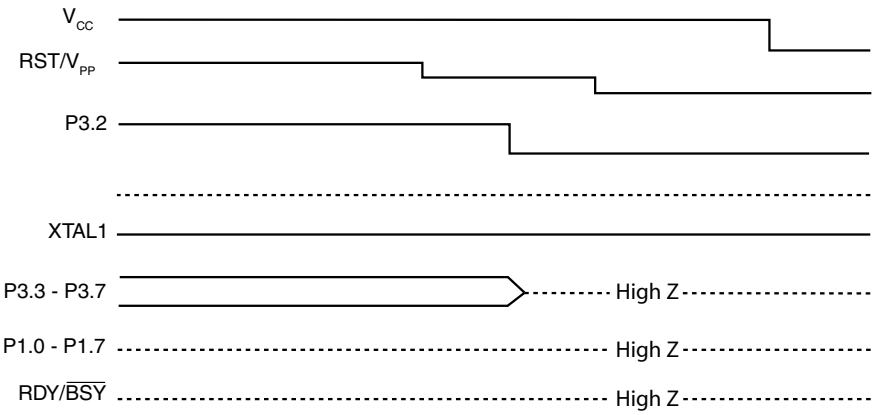


23. Power-down Sequence

Execute the following sequence to power-down the device after programming.

1. Tri-state Port P1.
2. Bring RST/V_{PP} down from 12V to V_{CC} and wait 10 µs.
3. Bring XTAL and P3.2 to “L” and tri-state P3.7, P3.5, P3.4, and P3.3.
4. Bring RST to “L” and wait 10 µs.
5. Power off V_{CC}.

Figure 23-1. Power-down Operation



24. Chip Erase

Function:

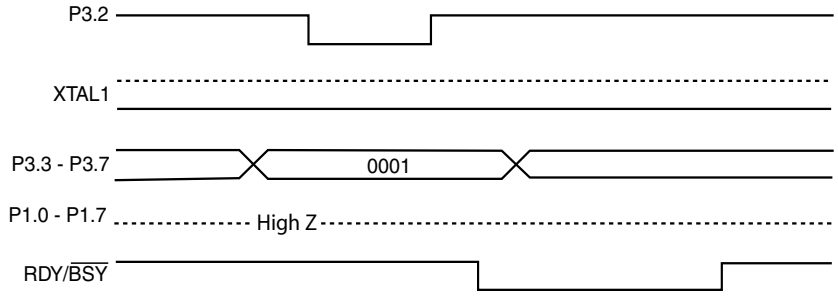
1. FFH programmed to every address location.
2. FFH programmed to User Signature Row if User Row Fuse bit is enabled.
3. Lockbit1 and Lockbit2 programmed to “unlock” state.

Usage:

1. Apply “0001” TestCode to P3.7, P3.5, P3.4, P3.3.
2. Pulse P3.2 low for 1 µs.
3. Wait 4 ms, monitor P3.1, or poll data.

Note: This and the following waveforms are not to scale.

Figure 24-1. Chip Erase Sequence



25. Load X-Address

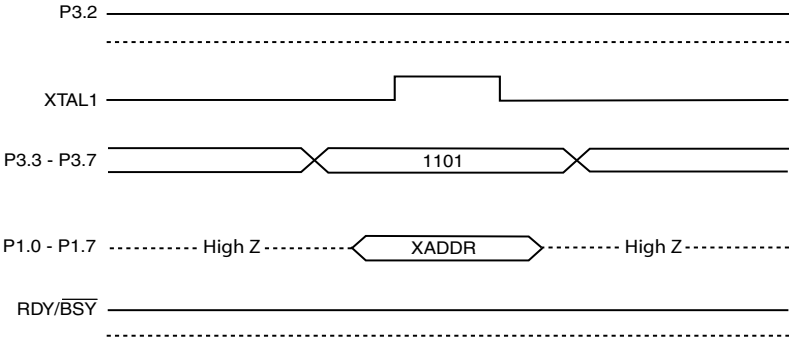
Function:

1. Loads the X-Address register with data on Port P1. The loaded address will select the page for subsequent write/read commands. The X-Address is equivalent to bits [11:5] of the full byte address.
2. Resets the Y-Address counter to 00H. The Y-Address is equivalent to bits [4:0] of the full byte address and selects a byte within a page.

Usage:

1. Apply “1101” TestCode to P3.7, P3.5, P3.4, P3.3.
2. Drive Port P1 with 8-bit X-address data.
3. Pulse XTAL1 high for at least 100 ns. The address is latched on the falling edge of XTAL1.

Figure 25-1. Load X-Address Sequence



27. Read 4K Code

Function:

1. Read 1 page (1 to 32 bytes) of data from the Code Memory array.
2. X-address (page) determined by previous Load-X command.
3. Y-address (offset) incremented by positive pulse on XTAL1.

Usage:

1. Execute the Load-X command to set the page address and reset the offset.
2. Apply “1100” TestCode to P3.7, P3.5, P3.4, P3.3.
3. Read 8-bit data on Port P1.
4. For additional bytes (up to 32), pulse XTAL1 high for at least 100 ns to increment the Y-address and repeat step 3. The address will change on the falling edge of XTAL1.

Figure 27-1. Read 4K Code Programming Sequence

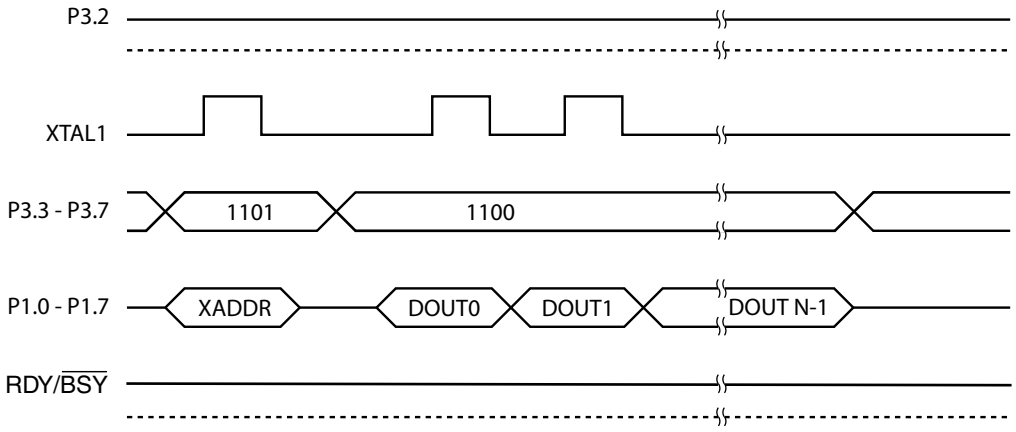


Table 32-1. Parallel Flash Programming and Verification Parameters

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Enable Voltage	11.5	12.5	V
I_{PP}	Programming Enable Current		1.0	mA
t_{PWRUP}	Power-on to RST High	10		µs
t_{POR}	Power-on Reset Time	2		ms
t_{PSTP}	$\overline{PROG}$ Setup to V_{PP} High	10		µs
t_{HSTL}	High Voltage Setting time	10		µs
t_{MSTP}	Mode Setup to $\overline{PROG}$ or XTAL1	1		µs
t_{MHLD}	Mode Hold after $\overline{PROG}$ or XTAL2	1		µs
t_{XTW}	XTAL1 High Width	0.5		µs
t_{ASTP}	Address Setup to XTAL1 High	0.5		µs
t_{AHLD}	Address Hold after XTAL1 Low	0.5		µs
t_{PGW}	$\overline{PROG}$ Low Width	1		µs
t_{DSTP}	Data Setup to $\overline{PROG}$ Low	0.5		µs
t_{DHLD}	Data Hold after $\overline{PROG}$ High	0.5		µs
t_{XLP}	XTAL1 Low to $\overline{PROG}$ Low	0.5		µs
t_{PHX}	$\overline{PROG}$ High to XTAL1 High	0.5		µs
t_{BLT}	Byte Load Period		150	µs
t_{PHBL}	$\overline{PROG}$ High to $\overline{BUSY}$ Low		256	µs
t_{WC}	Wire Cycle Time		4.5	ms
t_{RDT}	Read Byte Time	1		µs
t_{VFY}	XTAL1 Low to Data Verify Valid		0.25	µs
t_{PWRDN}	RST Low to Power Off	1		µs

34. Serial Programming Command Summary

Command	Byte 1	Byte 2	Byte 3	Byte 4	Byte ...
Program Enable(1)	1010 1100	0101 0011	xxxx xxxx	xxxx xxxx	
Chip Erase	1010 1100	100x xxxx	xxxx xxxx	xxxx xxxx	
Write Code **Byte**	0100 0000	xxxx A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	
Read Code **Byte**	0010 0000	xxxx A11 A10 A9 A8	A7 A6 A5 A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	
Write Code **Page**(2)	0101 0000	xxxx A11 A10 A9 A8	A7 A6 A5 0 0000	Data 0 ... Data 31	
Read Code **Page**(2)	0011 0000	xxxx A11 A10 A9 A8	A7 A6 A5 0 0000	Data 0 ... Data 31	
Write User Fuses(3)	1010 1100	0001 F3 F2 F1 F0	xxxx xxxx	xxxx xxxx	
Read User Fuses(3)	0010 0001	xxxx xxxx	xxxx xxxx	xxxx F3 F2 F1 F0	
Write Lock Bits(4)	1010 1100	1110 0x LB2 LB1	xxxx xxxx	xxxx xxxx	
Read Lock Bits(4)	0010 0100	xxxx xxxx	xxxx xxxx	xxxx xx LB2 LB1	
Write User Signature **Byte**	0100 0010	xxxx xxxx	xxx A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	
Read User Signature **Byte**	0010 0010	xxxx xxxx	xxx A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	
Write User Signature **Page**(2)	0101 0010	xxxx xxxx	xxxx xxxx	Data 0 ... Data 31	
Read User Signature **Page**(2)	0011 0010	xxxx xxxx	xxxx xxxx	Data 0 ... Data 31	
Read Atmel Signature Byte(5)	0010 1000	xxxx xxxx	xxx A4 A3 A2 A1 A0	D7 D6 D5 D4 D3 D2 D1 D0	

Notes:
1. Program Enable must be the **first** command issued after entering into the serial programming mode.
2. All 32 Data bytes must be written/read.
3. Fuse Bit Definitions:

Bit 0	ISP Enable*	Enable = 0/Disable = 1
Bit 1	x2 Clock	Enable = 0/Disable = 1
Bit 2	User Row Programming	Enable = 0/Disable = 1
Bit 3	XTAL Osc Bypass**	Enable = 0/Disable = 1

*The ISP Enable Fuse must be enabled before entering ISP mode.
When disabling the ISP fuse during ISP mode, the current fuse state will remain active until RST is brought low.
**Any change will only take effect after the next power-down/power-up cycle event.

4. Lock Bit Definitions:

Bit 0	Lock Bit 1	Locked = 0/Unlocked = 1
Bit 1	Lock Bit 2	Locked = 0/Unlocked = 1

5. **Atmel Signature Bytes**:

AT89S2051: Address 00H = 1EH
01H = 23H
02H = FFH

AT89S4051: Address 00H = 1EH
01H = 43H
02H = FFH

40. Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-0.7V to +6.2V
Maximum Operating Voltage	5.5V
DC Output Current	25.0 mA (15.0 mA for AT89S4051)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

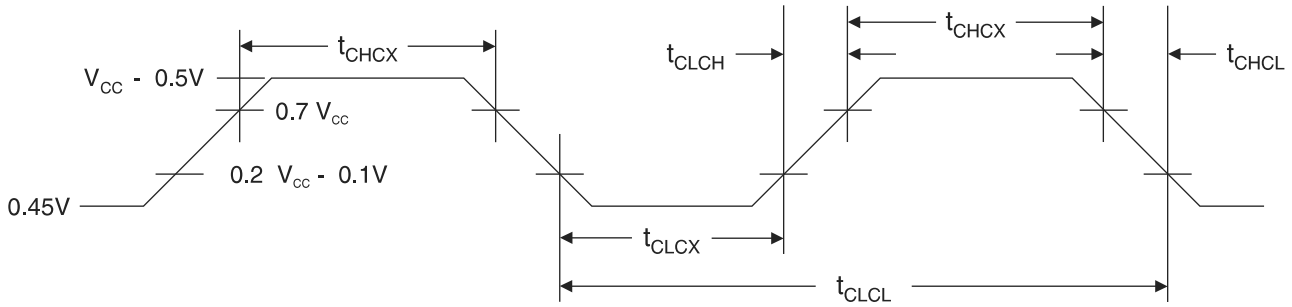
41. DC Characteristics

T_A = -40°C to 85°C, V_{CC} = 2.7V to 5.5V (unless otherwise noted)

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low-voltage		-0.5	0.2 V_{CC} - 0.1	V
V_{IH}	Input High-voltage	(Except XTAL1, RST)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V
V_{IH1}	Input High-voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low-voltage(1) (Ports 1, 3)	I_{OL} = 10 mA, V_{CC} = 2.7V, T_A = 85°C		0.5	V
V_{OH}	Output High-voltage (Ports 1, 3)	I_{OH} = -80 µA, V_{CC} = 5V ±10%	2.4		V
		I_{OH} = -30 µA	0.75 V_{CC}		V
		I_{OH} = -12 µA	0.9 V_{CC}		V
I_{IL}	Logical 0 Input Current (Ports 1, 3)	V_{IN} = 0.45V		-50	µA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1, 3)	V_{IN} = 2V, V_{CC} = 5V ±10%		-350	µA
I_{LI}	Input Leakage Current (Port P1.0, P1.1)	0 < V_{IN} < V_{CC}		±10	µA
V_{OS}	Comparator Input Offset Voltage	V_{CC} = 5V		20	mV
V_{CM}	Comparator Input Common Mode Voltage		0	V_{CC}	V
RRST	Reset Pull-down Resistor		50	150	KΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current (without the)	Active Mode, 24/12 MHz, V_{CC} = 5V/3V		10.5/3.5	mA
		Idle Mode, 24/12 MHz, V_{CC} = 5V/3V P1.0 & P1.1 = 0V or V_{CC}		4.5/2.5	mA
	Power-down Mode(2)	V_{CC} = 5V, P1.0 & P1.1 = 0V or V_{CC}(3)		10	µA
		V_{CC} = 3V, P1.0 & P1.1 = 0V or V_{CC}(3)		5	µA

Notes:
1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum total I_{OL} for all output pins: 25 mA (15 mA for AT89S4051)
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V.
3. P1.0 and P1.1 are comparator inputs and have no internal pullups. They should not be left floating.

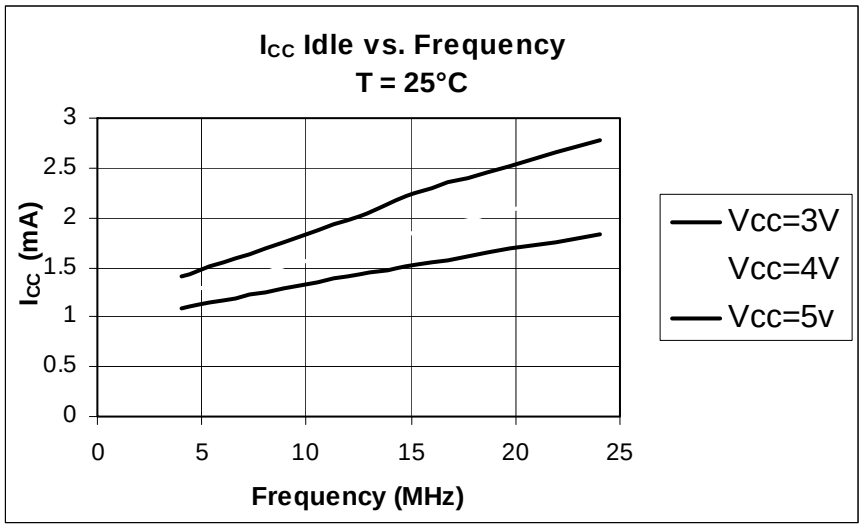
42. External Clock Drive Waveforms



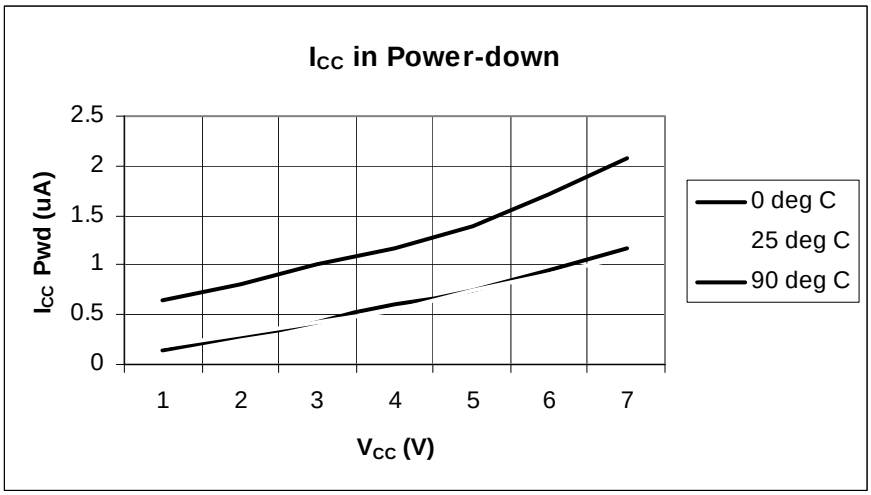
43. External Clock Drive

Symbol	Parameter	V_{CC} = 2.7V to 5.5V		Units
		Min	Max	
$1/t_{CLCL}$	Frequency	0	24	MHz
t_{CLCL}	Clock Period	41.6		ns
t_{CHCX}	High Time	12		ns
t_{CLCX}	Low Time	12		ns
t_{CLCH}	Rise Time		5	ns
t_{CHCL}	Fall Time		5	ns

53. I_{CC} (Idle Mode) Measurements

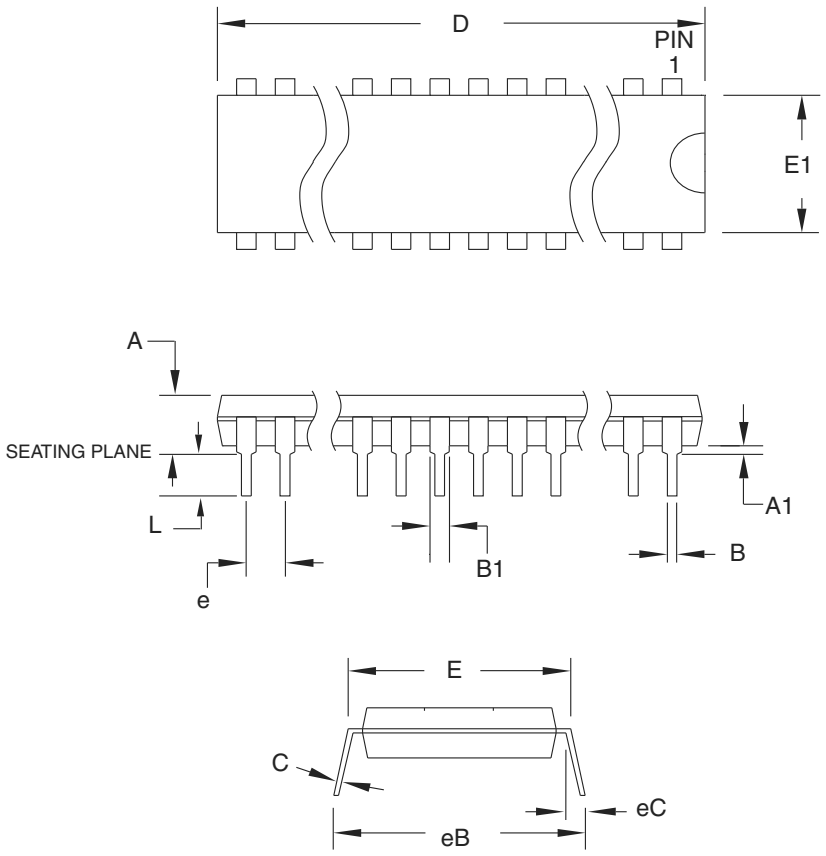


54. I_{CC} (Power Down Mode) Measurements



56. Package Information

56.1 20P3 – PDIP



COMMON DIMENSIONS
(Unit of Measure = mm)

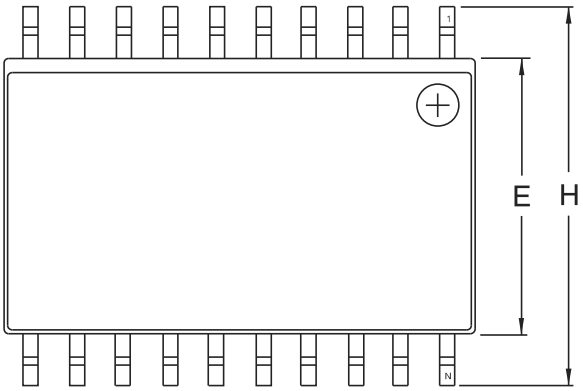
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	5.334	
A1	0.381	–	–	
D	24.892	–	26.924	Note 2
E	7.620	–	8.255	
E1	6.096	–	7.112	Note 2
B	0.356	–	0.559	
B1	1.270	–	1.551	
L	2.921	–	3.810	
C	0.203	–	0.356	
eB	–	–	10.922	
eC	0.000	–	1.524	
e	2.540 TYP			

Notes: 1. This package conforms to JEDEC reference MS-001, Variation AD.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

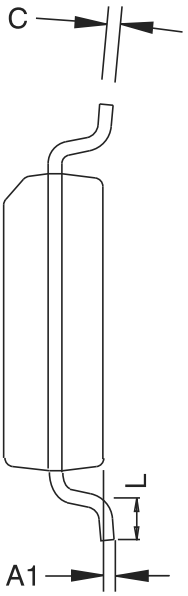
1/23/04

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**20P3**, 20-lead (0.300"/7.62 mm Wide) Plastic Dual Inline Package (PDIP)	20P3	D

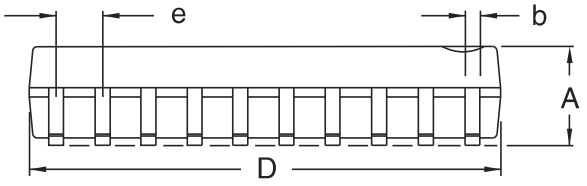
56.2 20S2 – SOIC



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure – mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	2.35		2.65	
A1	0.10		0.30	
b	0.33		0.51	4
C	0.23		0.32	
D	12.60		13.00	1
E	7.40		7.60	2
H	10.00		10.65	
L	0.40		1.27	3
e	1.27 BSC			

Notes.
1. This drawing is for general information only; refer to JEDEC Drawing MS-013, Variation AC for additional information.
2. Dimension 'D' does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006') per side.
3. Dimension 'E' does not include inter-lead Flash or protrusion. Inter-lead Flash and protrusions shall not exceed 0.25 mm (0.010') per side.
4. 'L' is the length of the terminal for soldering to a substrate.
5. The lead width 'b', as measured 0.36 mm (0.014') or greater above the seating plane, shall not exceed a maximum value of 0.61 mm (0.024') per side.

11/6/06

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**20S2**, 20-lead, 0.300' Wide Body, Plastic Gull Wing Small Outline Package (SOIC)	20S2	B

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