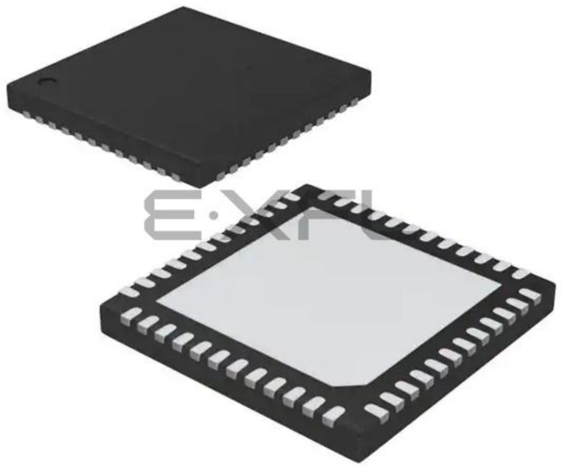

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | 768 |
| Total RAM Bits | - |
| Number of I/O | 34 |
| Number of Gates | 30000 |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Package / Case | 48-VFQFN Exposed Pad |
| Supplier Device Package | 48-QFN (6x6) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/agl030v5-qng48i |

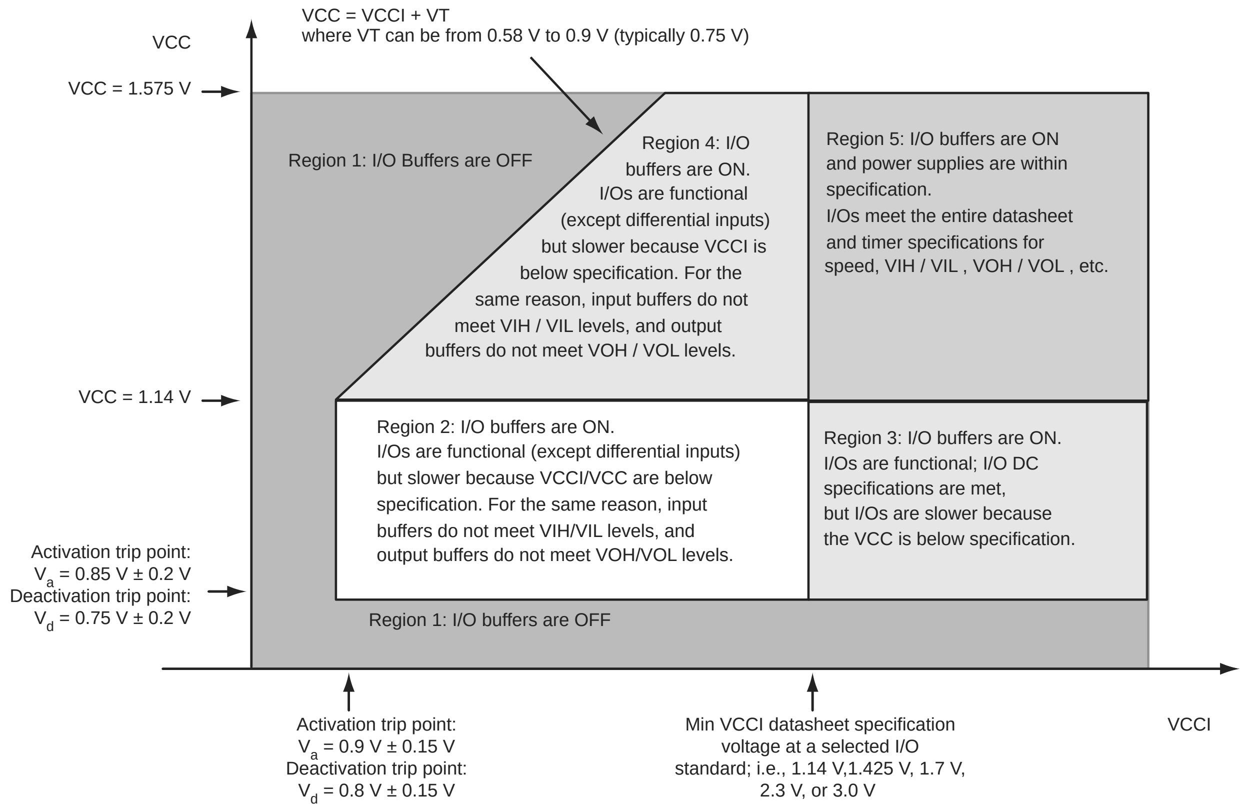



***Figure 2-2 •*** **V2 Devices – I/O State as a Function of VCCI and VCC Voltage Levels**

## Thermal Characteristics

### *Introduction*

The temperature variable in the Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because dynamic and static power consumption cause the chip junction to be higher than the ambient temperature.

EQ 1 can be used to calculate junction temperature.

$$T_J = \text{Junction Temperature} = \Delta T + T_A$$

*EQ 1*

where:

$T_A$ = Ambient Temperature

$\Delta T$ = Temperature gradient between junction (silicon) and ambient $\Delta T = \theta_{ja} * P$

$\theta_{ja}$ = Junction-to-ambient of the package. $\theta_{ja}$ numbers are located in Table 2-5 on page 2-6.

P = Power dissipation

# Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in Microsemi Libero SoC software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in Table 2-23 on page 2-19.
- Enable rates of output buffers—guidelines are provided for typical applications in Table 2-24 on page 2-19.
- Read rate and write rate to the memory—guidelines are provided for typical applications in Table 2-24 on page 2-19. The calculation should be repeated for each clock domain defined in the design.

## Methodology

### Total Power Consumption—$P_{TOTAL}$

$P_{TOTAL} = P_{STAT} + P_{DYN}$

$P_{STAT}$ is the total static power consumption.

$P_{DYN}$ is the total dynamic power consumption.

### Total Static Power Consumption—$P_{STAT}$

$P_{STAT} = (P_{DC1} \text{ or } P_{DC2} \text{ or } P_{DC3}) + N_{BANKS} * P_{DC5} + N_{INPUTS} * P_{DC6} + N_{OUTPUTS} * P_{DC7}$

$N_{INPUTS}$ is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

$N_{BANKS}$ is the number of I/O banks powered in the design.

### Total Dynamic Power Consumption—$P_{DYN}$

$P_{DYN} = P_{CLOCK} + P_{S\text{-}CELL} + P_{C\text{-}CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL}$

### Global Clock Contribution—$P_{CLOCK}$

$P_{CLOCK} = (P_{AC1} + N_{SPINE} * P_{AC2} + N_{ROW} * P_{AC3} + N_{S\text{-}CELL} * P_{AC4}) * F_{CLK}$

$N_{SPINE}$ is the number of global spines used in the user design—guidelines are provided in the "Spine Architecture" section of the *IGLOO FPGA Fabric User Guide.*

$N_{ROW}$ is the number of VersaTile rows used in the design—guidelines are provided in the "Spine Architecture" section of the *IGLOO FPGA Fabric User Guide.*

$F_{CLK}$ is the global clock signal frequency.

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

$P_{AC1}$, $P_{AC2}$, $P_{AC3}$, and $P_{AC4}$ are device-dependent.

### Sequential Cells Contribution—$P_{S\text{-}CELL}$

$P_{S\text{-}CELL} = N_{S\text{-}CELL} * (P_{AC5} + \alpha_1 / 2 * P_{AC6}) * F_{CLK}$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

$\alpha_1$ is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-23 on page 2-19.

$F_{CLK}$ is the global clock signal frequency.

## Summary of I/O Timing Characteristics – Default I/O Software Settings

***Table 2-29 •*** **Summary of AC Measuring Points**

| Standard | Measuring Trip Point (Vtrip) |
|---|---|
| 3.3 V LVTTL / 3.3 V LVCMOS | 1.4 V |
| 3.3 V VCMOS Wide Range | 1.4 V |
| 2.5 V LVCMOS | 1.2 V |
| 1.8 V LVCMOS | 0.90 V |
| 1.5 V LVCMOS | 0.75 V |
| 1.2 V LVCMOS | 0.60 V |
| 1.2 V LVCMOS Wide Range | 0.60 V |
| 3.3 V PCI | 0.285 * VCCI (RR) |
| | 0.615 * VCCI (FF) |
| 3.3 V PCI-X | 0.285 * VCCI (RR) |
| | 0.615 * VCCI (FF) |

***Table 2-30 •*** **I/O AC Parameter Definitions**

| Parameter | Parameter Definition |
|---|---|
| $t_{DP}$ | Data to Pad delay through the Output Buffer |
| $t_{PY}$ | Pad to Data delay through the Input Buffer |
| $t_{DOUT}$ | Data to Output Buffer delay through the I/O interface |
| $t_{EOUT}$ | Enable to Output Buffer Tristate Control delay through the I/O interface |
| $t_{DIN}$ | Input Buffer to Data delay through the I/O interface |
| $t_{HZ}$ | Enable to Pad delay through the Output Buffer—High to Z |
| $t_{ZH}$ | Enable to Pad delay through the Output Buffer—Z to High |
| $t_{LZ}$ | Enable to Pad delay through the Output Buffer—Low to Z |
| $t_{ZL}$ | Enable to Pad delay through the Output Buffer—Z to Low |
| $t_{ZHS}$ | Enable to Pad delay through the Output Buffer with delayed enable—Z to High |
| $t_{ZLS}$ | Enable to Pad delay through the Output Buffer with delayed enable—Z to Low |

**Table 2-31 • Summary of I/O Timing Characteristics—Software Default Settings, Std. Speed Grade, Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI (per standard) Applicable to Advanced I/O Banks**

| I/O Standard | Drive Strength | Equivalent Software Default Drive Strength Option[1] (mA) | Slew Rate | Capacitive Load (pF) | External Resistor (Ω) | $t_{DOUT}$ (ns) | $t_{DP}$ (ns) | $t_{DIN}$ (ns) | $t_{PY}$ (ns) | $t_{EOUT}$ (ns) | $t_{ZL}$ (ns) | $t_{ZH}$ (ns) | $t_{LZ}$ (ns) | $t_{HZ}$ (ns) | $t_{ZLS}$ (ns) | $t_{ZHS}$ (ns) | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 3.3 V LVTTL / 3.3 V LVCMOS | 12 mA | 12 | High | 5 | – | 0.97 | 2.09 | 0.18 | 0.85 | 0.66 | 2.14 | 1.68 | 2.67 | 3.05 | 5.73 | 5.27 | ns |
| 3.3 V LVCMOS Wide Range[2] | 100 µA | 12 | High | 5 | – | 0.97 | 2.93 | 0.18 | 1.19 | 0.66 | 2.95 | 2.27 | 3.81 | 4.30 | 6.54 | 5.87 | ns |
| 2.5 V LVCMOS | 12 mA | 12 | High | 5 | – | 0.97 | 2.09 | 0.18 | 1.08 | 0.66 | 2.14 | 1.83 | 2.73 | 2.93 | 5.73 | 5.43 | ns |
| 1.8 V LVCMOS | 12 mA | 12 | High | 5 | – | 0.97 | 2.24 | 0.18 | 1.01 | 0.66 | 2.29 | 2.00 | 3.02 | 3.40 | 5.88 | 5.60 | ns |
| 1.5 V LVCMOS | 12 mA | 12 | High | 5 | – | 0.97 | 2.50 | 0.18 | 1.17 | 0.66 | 2.56 | 2.27 | 3.21 | 3.48 | 6.15 | 5.86 | ns |
| 3.3 V PCI | Per PCI spec | – | High | 10 | 25 [2] | 0.97 | 2.32 | 0.18 | 0.74 | 0.66 | 2.37 | 1.78 | 2.67 | 3.05 | 5.96 | 5.38 | ns |
| 3.3 V PCI-X | Per PCI-X spec | – | High | 10 | 25 [2] | 0.97 | 2.32 | 0.19 | 0.70 | 0.66 | 2.37 | 1.78 | 2.67 | 3.05 | 5.96 | 5.38 | ns |
| LVDS | 24 mA | – | High | – | – | 0.97 | 1.74 | 0.19 | 1.35 | – | – | – | – | – | – | – | ns |
| LVPECL | 24 mA | – | High | – | – | 0.97 | 1.68 | 0.19 | 1.16 | – | – | – | – | – | – | – | ns |

*Notes:*

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*
3. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-12 on page 2-79 for connectivity. This resistor is not required during normal operation.*
4. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

# Single-Ended I/O Characteristics

## 3.3 V LVTTL / 3.3 V LVCMOS

Low-Voltage Transistor–Transistor Logic (LVTTL) is a general-purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTL input buffer and push-pull output buffer. Furthermore, all LVCMOS 3.3 V software macros comply with LVCMOS 3.3 V wide range as specified in the JESD8a specification.

***Table 2-47 •*** **Minimum and Maximum DC Input and Output Levels Applicable to Advanced I/O Banks**

| 3.3 V LVTTL / 3.3 V LVCMOS | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL[1] | IIH[2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA[3] | Max. mA[3] | µA[4] | µA[4] |
| 2 mA | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 2 | 2 | 25 | 27 | 10 | 10 |
| 4 mA | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 4 | 4 | 25 | 27 | 10 | 10 |
| 6 mA | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 6 | 6 | 51 | 54 | 10 | 10 |
| 8 mA | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 8 | 8 | 51 | 54 | 10 | 10 |
| 12 mA | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 12 | 12 | 103 | 109 | 10 | 10 |
| 16 mA | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 16 | 16 | 132 | 127 | 10 | 10 |
| 24 mA | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 24 | 24 | 268 | 181 | 10 | 10 |

*Notes:*

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at 100°C junction temperature and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

***Table 2-48 •*** **Minimum and Maximum DC Input and Output Levels Applicable to Standard Plus I/O Banks**

| 3.3 V LVTTL / 3.3 V LVCMOS | VIL | | VIH | | $V_{OL}$ | VOH | IOL | IOH | IOSL | IOSH | IIL[1] | IIH[2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA[3] | Max. mA[3] | µA[4] | µA[4] |
| 2 mA | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 2 | 2 | 25 | 27 | 10 | 10 |
| 4 mA | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 4 | 4 | 25 | 27 | 10 | 10 |
| 6 mA | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 6 | 6 | 51 | 54 | 10 | 10 |
| 8 mA | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 8 | 8 | 51 | 54 | 10 | 10 |
| 12 mA | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 12 | 12 | 103 | 109 | 10 | 10 |
| 16 mA | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 16 | 16 | 103 | 109 | 10 | 10 |

*Notes:*

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
3. *Currents are measured at 100°C junction temperature and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

***Table 2-92 •*** **2.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V**
**Applicable to Standard Plus Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 1.55 | 2.91 | 0.26 | 1.19 | 1.10 | 2.95 | 2.66 | 2.50 | 2.72 | 8.74 | 8.45 | ns |
| 4 mA | Std. | 1.55 | 2.91 | 0.26 | 1.19 | 1.10 | 2.95 | 2.66 | 2.50 | 2.72 | 8.74 | 8.45 | ns |
| 6 mA | Std. | 1.55 | 2.51 | 0.26 | 1.19 | 1.10 | 2.54 | 2.18 | 2.75 | 3.21 | 8.33 | 7.97 | ns |
| 8 mA | Std. | 1.55 | 2.51 | 0.26 | 1.19 | 1.10 | 2.54 | 2.18 | 2.75 | 3.21 | 8.33 | 7.97 | ns |
| 12 mA | Std. | 1.55 | 2.29 | 0.26 | 1.19 | 1.10 | 2.32 | 1.94 | 2.94 | 3.52 | 8.10 | 7.73 | ns |

*Notes:*

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

***Table 2-93 •*** **2.5 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V**
**Applicable to Standard Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 1.55 | 4.85 | 0.26 | 1.15 | 1.10 | 4.93 | 4.55 | 2.13 | 2.24 | ns |
| 4 mA | Std. | 1.55 | 4.85 | 0.26 | 1.15 | 1.10 | 4.93 | 4.55 | 2.13 | 2.24 | ns |
| 6 mA | Std. | 1.55 | 4.09 | 0.26 | 1.15 | 1.10 | 4.16 | 3.95 | 2.38 | 2.71 | ns |
| 8 mA | Std. | 1.55 | 4.09 | 0.26 | 1.15 | 1.10 | 4.16 | 3.95 | 2.38 | 2.71 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

***Table 2-94 •*** **2.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V**
**Applicable to Standard Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 1.55 | 2.76 | 0.26 | 1.15 | 1.10 | 2.80 | 2.52 | 2.13 | 2.32 | ns |
| 4 mA | Std. | 1.55 | 2.76 | 0.26 | 1.15 | 1.10 | 2.80 | 2.52 | 2.13 | 2.32 | ns |
| 6 mA | Std. | 1.55 | 2.39 | 0.26 | 1.15 | 1.10 | 2.42 | 2.05 | 2.38 | 2.80 | ns |
| 8 mA | Std. | 1.55 | 2.39 | 0.26 | 1.15 | 1.10 | 2.42 | 2.05 | 2.38 | 2.80 | ns |

*Notes:*

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

## 1.8 V LVCMOS

Low-voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 1.8 V input buffer and a push-pull output buffer.

***Table 2-95 •*** **Minimum and Maximum DC Input and Output Levels Applicable to Advanced I/O Banks**

| 1.8 V LVCMOS | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSH | IOSL | IIL[1] | IIH[2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA[3] | Max. mA[3] | µA[4] | µA[4] |
| 2 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.9 | 0.45 | VCCI – 0.45 | 2 | 2 | 9 | 11 | 10 | 10 |
| 4 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.9 | 0.45 | VCCI – 0.45 | 4 | 4 | 17 | 22 | 10 | 10 |
| 6 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.9 | 0.45 | VCCI – 0.45 | 6 | 6 | 35 | 44 | 10 | 10 |
| 8 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.9 | 0.45 | VCCI – 0.45 | 8 | 8 | 45 | 51 | 10 | 10 |
| 12 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.9 | 0.45 | VCCI – 0.45 | 12 | 12 | 91 | 74 | 10 | 10 |
| 16 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.9 | 0.45 | VCCI – 0.45 | 16 | 16 | 91 | 74 | 10 | 10 |

*Notes:*

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
3. *Currents are measured at 100°C junction temperature and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

***Table 2-96 •*** **Minimum and Maximum DC Input and Output Levels Applicable to Standard Plus I/O Banks**

| 1.8 V LVCMOS | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSH | IOSL | IIL[1] | IIH[2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA[3] | Max. mA[3] | µA[4] | µA[4] |
| 2 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.9 | 0.45 | VCCI – 0.45 | 2 | 2 | 9 | 11 | 10 | 10 |
| 4 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.9 | 0.45 | VCCI – 0.45 | 4 | 4 | 17 | 22 | 10 | 10 |
| 6 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.9 | 0.45 | VCCI – 0.45 | 6 | 6 | 35 | 44 | 10 | 10 |
| 8 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.9 | 0.45 | VCCI – 0.45 | 8 | 8 | 35 | 44 | 10 | 10 |

*Notes:*

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
3. *Currents are measured at 100°C junction temperature and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

**Table 2-104 • 1.8 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V**
**Applicable to Standard Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 2.62 | 0.18 | 0.98 | 0.66 | 2.67 | 2.59 | 1.67 | 1.29 | 2.62 | ns |
| 4 mA | Std. | 2.18 | 0.18 | 0.98 | 0.66 | 2.22 | 1.93 | 1.97 | 2.06 | 2.18 | ns |

*Notes:*

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

### *1.2 V DC Core Voltage*

**Table 2-105 • 1.8 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V**
**Applicable to Advanced I/O Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 1.55 | 6.97 | 0.26 | 1.11 | 1.10 | 7.08 | 6.48 | 2.87 | 2.29 | 12.87 | 12.27 | ns |
| 4 mA | Std. | 1.55 | 5.91 | 0.26 | 1.11 | 1.10 | 6.01 | 5.57 | 3.21 | 3.14 | 11.79 | 11.36 | ns |
| 6 mA | Std. | 1.55 | 5.16 | 0.26 | 1.11 | 1.10 | 5.24 | 4.95 | 3.45 | 3.55 | 11.03 | 10.74 | ns |
| 8 mA | Std. | 1.55 | 4.90 | 0.26 | 1.11 | 1.10 | 4.98 | 4.81 | 3.50 | 3.66 | 10.77 | 10.60 | ns |
| 12 mA | Std. | 1.55 | 4.83 | 0.26 | 1.11 | 1.10 | 4.90 | 4.83 | 3.58 | 4.08 | 10.68 | 10.61 | ns |
| 16 mA | Std. | 1.55 | 4.83 | 0.26 | 1.11 | 1.10 | 4.90 | 4.83 | 3.58 | 4.08 | 10.68 | 10.61 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

**Table 2-106 • 1.8 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V**
**Applicable to Advanced I/O Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 1.55 | 3.73 | 0.26 | 1.11 | 1.10 | 3.71 | 3.73 | 2.86 | 2.34 | 9.49 | 9.51 | ns |
| 4 mA | Std. | 1.55 | 3.12 | 0.26 | 1.11 | 1.10 | 3.16 | 2.97 | 3.21 | 3.22 | 8.95 | 8.75 | ns |
| 6 mA | Std. | 1.55 | 2.79 | 0.26 | 1.11 | 1.10 | 2.83 | 2.59 | 3.45 | 3.65 | 8.62 | 8.38 | ns |
| 8 mA | Std. | 1.55 | 2.73 | 0.26 | 1.11 | 1.10 | 2.77 | 2.52 | 3.50 | 3.75 | 8.56 | 8.30 | ns |
| 12 mA | Std. | 1.55 | 2.72 | 0.26 | 1.11 | 1.10 | 2.76 | 2.43 | 3.58 | 4.19 | 8.55 | 8.22 | ns |
| 16 mA | Std. | 1.55 | 2.72 | 0.26 | 1.11 | 1.10 | 2.76 | 2.43 | 3.58 | 4.19 | 8.55 | 8.22 | ns |

*Notes:*

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

## 1.2 V LVCMOS (JESD8-12A)

Low-Voltage CMOS for 1.2 V complies with the LVCMOS standard JESD8-12A for general purpose 1.2 V applications. It uses a 1.2 V input buffer and a push-pull output buffer. Furthermore, all LVCMOS 1.2 V software macros comply with LVCMOS 1.2 V wide range as specified in the JESD8-12A specification.

***Table 2-127* • Minimum and Maximum DC Input and Output Levels Applicable to Advanced I/O Banks**

| 1.2 V LVCMOS | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSH | IOSL | IIL[1] | IIH[2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA[3] | Max. mA[3] | µA[4] | µA[4] |
| 2 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.26 | 0.25 * VCCI | 0.75 * VCCI | 2 | 2 | 20 | 26 | 10 | 10 |

*Notes:*

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
3. *Currents are measured at 100°C junction temperature and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

***Table 2-128* • Minimum and Maximum DC Input and Output Levels Applicable to Standard Plus I/O Banks**

| 1.2 V LVCMOS | VIL | | VIH | | VOL | VOH | $I_{OL}$ | IOH | IOSH | IOSL | IIL[1] | IIH[2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA[3] | Max. mA[3] | µA[4] | µA[4] |
| 2 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.26 | 0.25 * VCCI | 0.75 * VCCI | 2 | 2 | 20 | 26 | 10 | 10 |

*Notes:*

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
3. *Currents are measured at 100°C junction temperature and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

***Table 2-129* • Minimum and Maximum DC Input and Output Levels Applicable to Standard I/O Banks**

| 1.2 V LVCMOS | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSH | IOSL | IIL[1] | IIH[2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA[3] | Max. mA[3] | µA[4] | µA[4] |
| 1 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.25 * VCCI | 0.75 * VCCI | 1 | 1 | 20 | 26 | 10 | 10 |

*Notes:*

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
3. *Currents are measured at 100°C junction temperature and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

### *1.2 V DC Core Voltage*

***Table 2-165* • Input DDR Propagation Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{DDRICLKQ1}$ | Clock-to-Out Out_QR for Input DDR | 0.76 | ns |
| $t_{DDRICLKQ2}$ | Clock-to-Out Out_QF for Input DDR | 0.94 | ns |
| $t_{DDRISUD1}$ | Data Setup for Input DDR (negedge) | 0.93 | ns |
| $t_{DDRISUD2}$ | Data Setup for Input DDR (posedge) | 0.84 | ns |
| $t_{DDRIHD1}$ | Data Hold for Input DDR (negedge) | 0.00 | ns |
| $t_{DDRIHD2}$ | Data Hold for Input DDR (posedge) | 0.00 | ns |
| $t_{DDRICLR2Q1}$ | Asynchronous Clear-to-Out Out_QR for Input DDR | 1.23 | ns |
| $t_{DDRICLR2Q2}$ | Asynchronous Clear-to-Out Out_QF for Input DDR | 1.42 | ns |
| $t_{DDRIREMCLR}$ | Asynchronous Clear Removal Time for Input DDR | 0.00 | ns |
| $t_{DDRIRECCLR}$ | Asynchronous Clear Recovery Time for Input DDR | 0.24 | ns |
| $t_{DDRIWCLR}$ | Asynchronous Clear Minimum Pulse Width for Input DDR | 0.19 | ns |
| $t_{DDRICKMPWH}$ | Clock Minimum Pulse Width High for Input DDR | 0.31 | ns |
| $t_{DDRICKMPWL}$ | Clock Minimum Pulse Width Low for Input DDR | 0.28 | ns |
| $F_{DDRIMAX}$ | Maximum Frequency for Input DDR | 160.00 | MHz |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

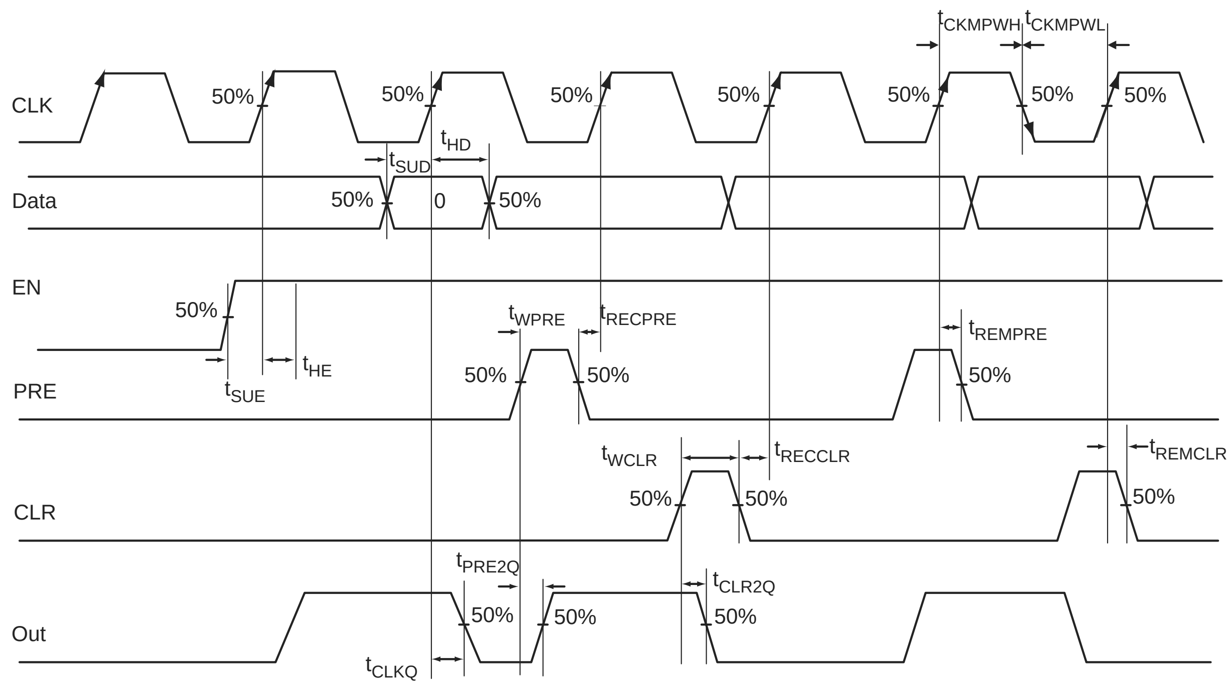



***Figure 2-28 •*** **Timing Model and Waveforms**

## *Timing Characteristics*

### *1.5 V DC Core Voltage*

***Table 2-171 •*** **Register Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{CLKQ}$ | Clock-to-Q of the Core Register | 0.89 | ns |
| $t_{SUD}$ | Data Setup Time for the Core Register | 0.81 | ns |
| $t_{HD}$ | Data Hold Time for the Core Register | 0.00 | ns |
| $t_{SUE}$ | Enable Setup Time for the Core Register | 0.73 | ns |
| $t_{HE}$ | Enable Hold Time for the Core Register | 0.00 | ns |
| $t_{CLR2Q}$ | Asynchronous Clear-to-Q of the Core Register | 0.60 | ns |
| $t_{PRE2Q}$ | Asynchronous Preset-to-Q of the Core Register | 0.62 | ns |
| $t_{REMCLR}$ | Asynchronous Clear Removal Time for the Core Register | 0.00 | ns |
| $t_{RECCLR}$ | Asynchronous Clear Recovery Time for the Core Register | 0.24 | ns |
| $t_{REMPRE}$ | Asynchronous Preset Removal Time for the Core Register | 0.00 | ns |
| $t_{RECPRE}$ | Asynchronous Preset Recovery Time for the Core Register | 0.23 | ns |
| $t_{WCLR}$ | Asynchronous Clear Minimum Pulse Width for the Core Register | 0.30 | ns |
| $t_{WPRE}$ | Asynchronous Preset Minimum Pulse Width for the Core Register | 0.30 | ns |
| $t_{CKMPWH}$ | Clock Minimum Pulse Width High for the Core Register | 0.56 | ns |
| $t_{CKMPWL}$ | Clock Minimum Pulse Width Low for the Core Register | 0.56 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

***Table 2-187* • AGL600 Global Resource**
**Commercial-Case Conditions: $T_J$ = 70°C, VCC = 1.14 V**

| Parameter | Description | Std. | | Units |
|---|---|---|---|---|
| | | Min.[1] | Max.[2] | |
| $t_{RCKL}$ | Input Low Delay for Global Clock | 2.22 | 2.67 | ns |
| $t_{RCKH}$ | Input High Delay for Global Clock | 2.32 | 2.93 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | 1.40 | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock | 1.65 | | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | | 0.61 | ns |

*Notes:*

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

***Table 2-188* • AGL1000 Global Resource**
**Commercial-Case Conditions: $T_J$ = 70°C, VCC = 1.14 V**

| Parameter | Description | Std. | | Units |
|---|---|---|---|---|
| | | Min.[1] | Max.[2] | |
| $t_{RCKL}$ | Input Low Delay for Global Clock | 2.31 | 2.76 | ns |
| $t_{RCKH}$ | Input High Delay for Global Clock | 2.42 | 3.03 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | 1.40 | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock | 1.65 | | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | | 0.61 | ns |

*Notes:*

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

# JTAG Pins

IGLOO devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). VCC must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; VJTAG alone is insufficient. Both VJTAG and VCC to the part must be supplied to allow JTAG signals to transition the device. Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND.

### TCK Test Clock

Test clock input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/-down resistor. If JTAG is not used, Microsemi recommends tying off TCK to GND through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state.

Note that to operate at all VJTAG voltages, 500 Ω to 1 kΩ will satisfy the requirements. Refer to Table 3-2 for more information.

***Table 3-2*** **• Recommended Tie-Off Values for the TCK and TRST Pins**

| VJTAG | Tie-Off Resistance [1,2] |
|---|---|
| VJTAG at 3.3 V | 200 Ω to 1 kΩ |
| VJTAG at 2.5 V | 200 Ω to 1 kΩ |
| VJTAG at 1.8 V | 500 Ω to 1 kΩ |
| VJTAG at 1.5 V | 500 Ω to 1 kΩ |

*Notes:*

1. *The TCK pin can be pulled-up or pulled-down.*
2. *The TRST pin is pulled-down.*
3. *Equivalent parallel resistance if more than one device is on the JTAG chain*

***Table 3-3*** **• TRST and TCK Pull-Down Recommendations**

| VJTAG | Tie-Off Resistance* |
|---|---|
| VJTAG at 3.3 V | 200 Ω to 1 kΩ |
| VJTAG at 2.5 V | 200 Ω to 1 kΩ |
| VJTAG at 1.8 V | 500 Ω to 1 kΩ |
| VJTAG at 1.5 V | 500 Ω to 1 kΩ |

*Note: Equivalent parallel resistance if more than one device is on the JTAG chain*

### TDI Test Data Input

Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.

### TDO Test Data Output

Serial output for JTAG boundary scan, ISP, and UJTAG usage.

### TMS Test Mode Select

The TMS pin controls the use of the IEEE 1532 boundary scan pins (TCK, TDI, TDO, TRST). There is an internal weak pull-up resistor on the TMS pin.

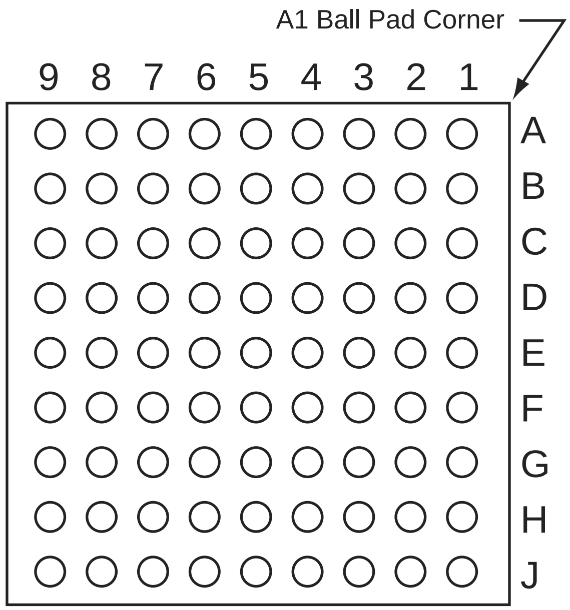
### TRST Boundary Scan Reset Pin

The TRST pin functions as an active-low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. If JTAG is not used, an external pull-down resistor could be included to ensure the test access port (TAP) is held in reset mode. The resistor values must be chosen from Table 3-2 and must satisfy the parallel resistance value requirement. The values in Table 3-2 correspond to the resistor recommended when a single device is used, and the equivalent parallel resistor when multiple devices are connected via a JTAG chain.

In critical applications, an upset in the JTAG circuit could allow entrance to an undesired JTAG state. In such cases, Microsemi recommends tying off TRST to GND through a resistor placed close to the FPGA pin.

# 4 – Package Pin Assignments

## UC81

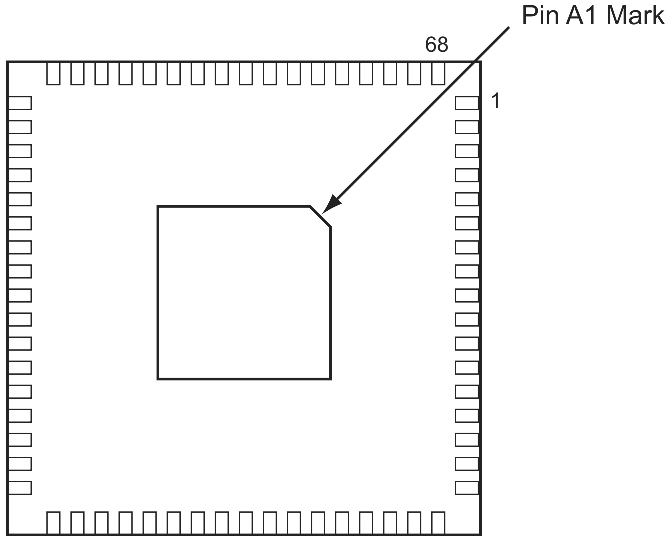



*Note: This is the bottom view of the package.*

### *Note*

For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

# QN68




*Notes:*

1. *This is the bottom view of the package.*
2. *The die attach paddle center of the package is tied to ground (GND).*

## *Note*

For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

| QN132 | |
|---|---|
| Pin Number | AGL030 Function |
| A1 | IO80RSB1 |
| A2 | IO77RSB1 |
| A3 | NC |
| A4 | IO76RSB1 |
| A5 | GEC0/IO73RSB1 |
| A6 | NC |
| A7 | GEB0/IO71RSB1 |
| A8 | IO69RSB1 |
| A9 | NC |
| A10 | VCC |
| A11 | IO67RSB1 |
| A12 | IO64RSB1 |
| A13 | IO59RSB1 |
| A14 | IO56RSB1 |
| A15 | NC |
| A16 | IO55RSB1 |
| A17 | IO53RSB1 |
| A18 | VCC |
| A19 | IO50RSB1 |
| A20 | IO48RSB1 |
| A21 | IO45RSB1 |
| A22 | IO44RSB1 |
| A23 | IO43RSB1 |
| A24 | TDI |
| A25 | TRST |
| A26 | IO40RSB0 |
| A27 | NC |
| A28 | IO39RSB0 |
| A29 | IO38RSB0 |
| A30 | IO36RSB0 |
| A31 | IO35RSB0 |
| A32 | GDC0/IO32RSB0 |
| A33 | NC |
| A34 | VCC |
| A35 | IO30RSB0 |
| A36 | IO27RSB0 |

| QN132 | |
|---|---|
| Pin Number | AGL030 Function |
| A37 | IO22RSB0 |
| A38 | IO19RSB0 |
| A39 | NC |
| A40 | IO18RSB0 |
| A41 | IO16RSB0 |
| A42 | IO14RSB0 |
| A43 | VCC |
| A44 | IO11RSB0 |
| A45 | IO08RSB0 |
| A46 | IO06RSB0 |
| A47 | IO05RSB0 |
| A48 | IO02RSB0 |
| B1 | IO81RSB1 |
| B2 | IO78RSB1 |
| B3 | GND |
| B4 | IO75RSB1 |
| B5 | NC |
| B6 | GND |
| B7 | IO70RSB1 |
| B8 | NC |
| B9 | GND |
| B10 | IO66RSB1 |
| B11 | IO63RSB1 |
| B12 | FF/IO60RSB1 |
| B13 | IO57RSB1 |
| B14 | GND |
| B15 | IO54RSB1 |
| B16 | IO52RSB1 |
| B17 | GND |
| B18 | IO49RSB1 |
| B19 | IO46RSB1 |
| B20 | GND |
| B21 | IO42RSB1 |
| B22 | TMS |
| B23 | TDO |
| B24 | IO41RSB0 |

| QN132 | |
|---|---|
| Pin Number | AGL030 Function |
| B25 | GND |
| B26 | NC |
| B27 | IO37RSB0 |
| B28 | GND |
| B29 | GDA0/IO33RSB0 |
| B30 | NC |
| B31 | GND |
| B32 | IO29RSB0 |
| B33 | IO26RSB0 |
| B34 | IO23RSB0 |
| B35 | IO20RSB0 |
| B36 | GND |
| B37 | IO17RSB0 |
| B38 | IO15RSB0 |
| B39 | GND |
| B40 | IO12RSB0 |
| B41 | IO09RSB0 |
| B42 | GND |
| B43 | IO04RSB0 |
| B44 | IO01RSB0 |
| C1 | IO82RSB1 |
| C2 | IO79RSB1 |
| C3 | NC |
| C4 | IO74RSB1 |
| C5 | GEA0/IO72RSB1 |
| C6 | NC |
| C7 | NC |
| C8 | VCCIB1 |
| C9 | IO65RSB1 |
| C10 | IO62RSB1 |
| C11 | IO61RSB1 |
| C12 | IO58RSB1 |
| C13 | NC |
| C14 | NC |
| C15 | IO51RSB1 |
| C16 | VCCIB1 |

| QN132 | |
|---|---|
| **Pin Number** | **AGL125 Function** |
| C17 | IO83RSB1 |
| C18 | VCCIB1 |
| C19 | TCK |
| C20 | VMV1 |
| C21 | VPUMP |
| C22 | VJTAG |
| C23 | VCCIB0 |
| C24 | NC |
| C25 | NC |
| C26 | GCA1/IO55RSB0 |
| C27 | GCC0/IO52RSB0 |
| C28 | VCCIB0 |
| C29 | IO42RSB0 |
| C30 | GNDQ |
| C31 | GBA1/IO40RSB0 |
| C32 | GBB0/IO37RSB0 |
| C33 | VCC |
| C34 | IO24RSB0 |
| C35 | IO19RSB0 |
| C36 | IO16RSB0 |
| C37 | IO10RSB0 |
| C38 | VCCIB0 |
| C39 | GAB1/IO03RSB0 |
| C40 | VMV0 |
| D1 | GND |
| D2 | GND |
| D3 | GND |
| D4 | GND |

| FG484 | |
|---|---|
| **Pin Number** | **AGL600 Function** |
| H19 | IO66PDB1 |
| H20 | VCC |
| H21 | NC |
| H22 | NC |
| J1 | NC |
| J2 | NC |
| J3 | NC |
| J4 | IO166NDB3 |
| J5 | IO168NPB3 |
| J6 | IO167PPB3 |
| J7 | IO169PDB3 |
| J8 | VCCIB3 |
| J9 | GND |
| J10 | VCC |
| J11 | VCC |
| J12 | VCC |
| J13 | VCC |
| J14 | GND |
| J15 | VCCIB1 |
| J16 | IO62NDB1 |
| J17 | IO64NPB1 |
| J18 | IO65PPB1 |
| J19 | IO66NDB1 |
| J20 | NC |
| J21 | IO68PDB1 |
| J22 | IO68NDB1 |
| K1 | IO157PDB3 |
| K2 | IO157NDB3 |
| K3 | NC |
| K4 | IO165NDB3 |
| K5 | IO165PDB3 |
| K6 | IO168PPB3 |
| K7 | GFC1/IO164PPB3 |
| K8 | VCCIB3 |
| K9 | VCC |
| K10 | GND |

| Revision | Changes | Page |
|---|---|---|
| Revision 19 (continued) | The following sentence was removed from the "Advanced Architecture" section:<br>"In addition, extensive on-chip programming circuitry allows for rapid, single-voltage (3.3 V) programming of IGLOO devices via an IEEE 1532 JTAG interface" (SAR 28756). | 1-3 |
| | The "Specifying I/O States During Programming" section is new (SAR 21281). | 1-8 |
| | Values for VCCPLL at 1.2 V –1.5 V DC core supply voltage were revised in Table 2-2 • Recommended Operating Conditions 1 (SAR 22356).<br>The value for VPUMP operation was changed from "0 to 3.45 V" to "0 to 3.6 V" (SAR 25220).<br>The value for VCCPLL 1.5 V DC core supply voltage was changed from "1.4 to 1.6 V" to "1.425 to 1.575 V" (SAR 26551).<br>The notes in the table were renumbered in order of their appearance in the table (SAR 21869). | 2-2 |
| | The temperature used in EQ 2 was revised from 110°C to 100°C for consistency with the limits given in Table 2-2 • Recommended Operating Conditions 1. The resulting maximum power allowed is thus 1.28 W. Formerly it was 1.71 W (SAR 26259). | 2-6 |
| | Values for CS196, CS281, and QN132 packages were added to Table 2-5 • Package Thermal Resistivities (SARs 26228, 32301). | 2-6 |
| | Table 2-6 • Temperature and Voltage Derating Factors for Timing Delays (normalized to TJ = 70°C, VCC = 1.425 V) and Table 2-7 • Temperature and Voltage Derating Factors for Timing Delays (normalized to TJ = 70°C, VCC = 1.14 V) were updated to remove the column for –20°C and shift the data over to correct columns (SAR 23041). | 2-7 |
| | The tables in the "Quiescent Supply Current" section were updated with revised notes on IDD (SAR 24112). Table 2-8 • Power Supply State per Mode is new. | 2-7 |
| | The formulas in the table notes for Table 2-41 • I/O Weak Pull-Up/Pull-Down Resistances were corrected (SAR 21348). | 2-37 |
| | The row for 110°C was removed from Table 2-45 • Duration of Short Circuit Event before Failure. The example in the associated paragraph was changed from 110°C to 100°C. Table 2-46 • I/O Input Rise Time, Fall Time, and Related I/O Reliability1 was revised to change 110° to 100°C. (SAR 26259). | 2-40 |
| | The notes regarding drive strength in the "Summary of I/O Timing Characteristics – Default I/O Software Settings" section, "3.3 V LVCMOS Wide Range" section and "1.2 V LVCMOS Wide Range" section tables were revised for clarification. They now state that the minimum drive strength for the default software configuration when run in wide range is ±100 µA. The drive strength displayed in software is supported in normal range only. For a detailed I/V curve, refer to the IBIS models (SAR 25700). | 2-28, 2-47, 2-77 |
| | The following sentence was deleted from the "2.5 V LVCMOS" section (SAR 24916): "It uses a 5 V–tolerant input buffer and push-pull output buffer." | 2-56 |
| | The values for $F_{DDRIMAX}$ and $F_{DDOMAX}$ were updated in the tables in the "Input DDR Module" section and "Output DDR Module" section (SAR 23919). | 2-94, 2-97 |
| | The following notes were removed from Table 2-147 • Minimum and Maximum DC Input and Output Levels (SAR 29428):<br>±5%<br>Differential input voltage = ±350 mV | 2-81 |
| | Table 2-189 • IGLOO CCC/PLL Specification and Table 2-190 • IGLOO CCC/PLL Specification were updated. A note was added to both tables indicating that when the CCC/PLL core is generated by Mircosemi core generator software, not all delay values of the specified delay increments are available (SAR 25705). | 2-115 |

| Revision / Version | Changes | Page |
|---|---|---|
| **Revision 3 (Feb 2008)**<br>Product Brief rev. 2 | This document was updated to include AGL015 device information. QN68 is a new package offered in the AGL015. The following sections were updated:<br>"Features and Benefits"<br>"IGLOO Ordering Information"<br>"Temperature Grade Offerings"<br>"IGLOO Devices" Product Family Table<br>Table 1 • IGLOO FPGAs Package Sizes Dimensions<br>"AGL015 and AGL030" note | N/A |
| | The "Temperature Grade Offerings" table was updated to include M1AGL600. | IV |
| | In the "IGLOO Ordering Information" table, the QN package measurements were updated to include both 0.4 mm and 0.5 mm. | III |
| | In the "General Description" section, the number of I/Os was updated from 288 to 300. | 1-1 |
| Packaging v1.2 | The "QN68" section is new. | 4-25 |
| **Revision 2 (Jan 2008)**<br>Packaging v1.1 | The "CS196" package and pin table was added for AGL125. | 4-10 |
| **Revision 1 (Jan 2008)**<br>Product Brief rev. 1 | The "Low Power" section was updated to change the description of low power active FPGA operation to "from 12 µW" from "from 25 µW." The same update was made in the "General Description" section and the "Flash*Freeze Technology" section. | I, 1-1 |
| **Revision 0 (Jan 2008)** | This document was previously in datasheet Advance v0.7. As a result of moving to the handbook format, Actel has restarted the numbering. | N/A |
| Advance v0.7<br>(December 2007) | Table 1 • IGLOO Product Family, the "I/Os Per Package1" table, and the Temperature Grade Offerings table were updated to reflect the following: CS196 is now supported for AGL250; device/package support for QN132 is to be determined for AGL250; the CS281 package was added for AGL600 and AGL1000. | i, ii, iv |
| | Table 2 • IGLOO FPGAs Package Sizes Dimensions is new, and package sizes were removed from the "I/Os Per Package1" table. | ii |
| | The "I/Os Per Package1"table was updated to reflect 77 instead of 79 single-ended I/Os for the VG100 package for AGL030. | ii |
| | The "Timing Model" was updated to be consistent with the revised timing numbers. | 2-20 |
| | In Table 2-27 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings, $T_J$ was changed to $T_A$ in notes 1 and 2. | 2-26 |
| | All AC Loading figures for single-ended I/O standards were changed from Datapaths at 35 pF to 5 pF. | N/A |
| | The "1.2 V LVCMOS (JESD8-12A)" section is new. | 2-74 |
| | This document was previously in datasheet Advance v0.7. As a result of moving to the handbook format, Actel has restarted the version numbers. The new version number is Advance v0.1. | N/A |
| | Table 2-4 • IGLOO CCC/PLL Specification and Table 2-5 • IGLOO CCC/PLL Specification were updated. | 2-19, 2-20 |