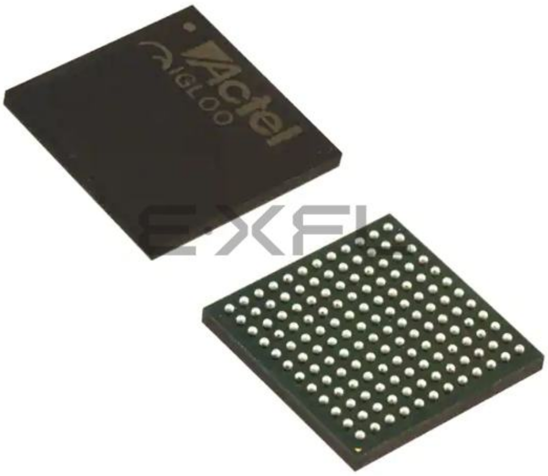
Microchip Technology - AGL1000V2-FG144I Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	24576
Total RAM Bits	147456
Number of I/O	97
Number of Gates	1000000
Voltage - Supply	1.14V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	144-LBGA
Supplier Device Package	144-FPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/agl1000v2-fg144i

I/Os Per Package[1]

IGLOO Devices	AGL015[2]	AGL030	AGL060	AGL125	AGL250		AGL400		AGL600		AGL1000	
ARM-Enabled IGLOO Devices					M1AGL250				M1AGL600		M1AGL1000	
	I/O Type[3]											
Package	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O[4]	Differential I/O Pairs	Single-Ended I/O[4]	Differential I/O Pairs	Single-Ended I/O[4]	Differential I/O Pairs	Single-Ended I/O[4]	Differential I/O Pairs
QN48	–	34	–	–	–	–	–	–	–	–	–	–
QN68	49	49	–	–	–	–	–	–	–	–	–	–
UC81	–	66	–	–	–	–	–	–	–	–	–	–
CS81	–	66	–	–	–	–	–	–	–	–	–	–
CS121	–	–	96	96	–	–	–	–	–	–	–	–
VQ100	–	77	71	71	68	13	–	–	–	–	–	–
QN132[6]	–	81	80	84	–	–	–	–	–	–	–	–
CS196	–	–	–	133	143[5]	35[5]	143	35	–	–	–	–
FG144	–	–	–	97	97	24	97	25	97	25	97	25
FG256[7]	–	–	–	–	–	–	178	38	177	43	177	44
CS281	–	–	–	–	–	–	–	–	215	53	215	53
FG484[7]	–	–	–	–	–	–	194	38	235	60	300	74

Notes:

1. *When considering migrating your design to a lower- or higher-density device, refer to the* IGLOO FPGA Fabric User Guide *to ensure compliance with design and board migration requirements.*
2. *AGL015 is not recommended for new designs.*
3. *When the Flash*Freeze pin is used to directly enable Flash*Freeze mode and not used as a regular I/O, the number of single-ended user I/Os available is reduced by one.*
4. *Each used differential I/O pair reduces the number of single-ended I/Os available by two.*
5. *The M1AGL250 device does not support QN132 or CS196 packages.*
6. *Package not available.*
7. *FG256 and FG484 are footprint-compatible packages.*

Table 1 • IGLOO FPGAs Package Sizes Dimensions

Package	UC81	CS81	CS121	QN48	QN68	QN132*	CS196	CS281	FG144	VQ100	FG256	FG484
Length × Width (mm\mm)	4 × 4	5 × 5	6 × 6	6 × 6	8 × 8	8 × 8	8 × 8	10 × 10	13 × 13	14 × 14	17 × 17	23 × 23
Nominal Area (mm^2)	16	25	36	36	64	64	64	100	169	196	289	529
Pitch (mm)	0.4	0.5	0.5	0.4	0.4	0.5	0.5	0.5	1.0	0.5	1.0	1.0
Height (mm)	0.80	0.80	0.99	0.90	0.90	0.75	1.20	1.05	1.45	1.00	1.60	2.23

Note: * *Package not available.*

Flash*Freeze Technology

The IGLOO device has an ultra-low power static mode, called Flash*Freeze mode, which retains all SRAM and register information and can still quickly return to normal operation. Flash*Freeze technology enables the user to quickly (within 1 µs) enter and exit Flash*Freeze mode by activating the Flash*Freeze pin while all power supplies are kept at their original values. In addition, I/Os and global I/Os can still be driven and can be toggling without impact on power consumption, clocks can still be driven or can be toggling without impact on power consumption, and the device retains all core registers, SRAM information, and states. I/O states are tristated during Flash*Freeze mode or can be set to a certain state using weak pull-up or pull-down I/O attribute configuration. No power is consumed by the I/O banks, clocks, JTAG pins, or PLL, and the device consumes as little as 5 µW in this mode.

Flash*Freeze technology allows the user to switch to active mode on demand, thus simplifying the power management of the device.

The Flash*Freeze pin (active low) can be routed internally to the core to allow the user's logic to decide when it is safe to transition to this mode. It is also possible to use the Flash*Freeze pin as a regular I/O if Flash*Freeze mode usage is not planned, which is advantageous because of the inherent low power static (as low as 12 µW) and dynamic capabilities of the IGLOO device. Refer to Figure 1-3 for an illustration of entering/exiting Flash*Freeze mode.

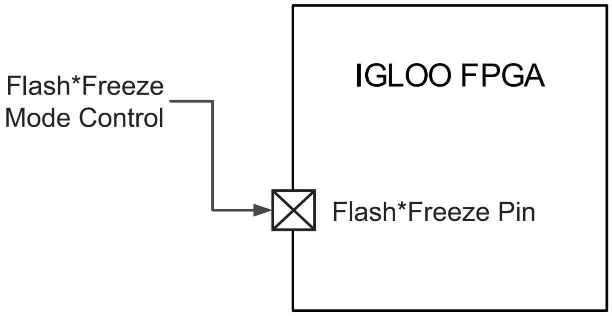

Figure 1-3 • **IGLOO Flash*Freeze Mode**

VersaTiles

The IGLOO core consists of VersaTiles, which have been enhanced beyond the ProASIC$^{\text{PLUS}®}$ core tiles. The IGLOO VersaTile supports the following:

- All 3-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set

Refer to Figure 1-4 for VersaTile configurations.

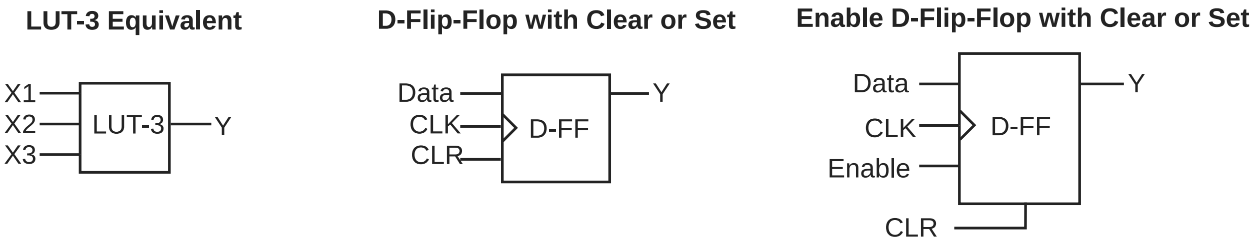

Figure 1-4 • **VersaTile Configurations**

Power per I/O Pin

Table 2-13 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings Applicable to Advanced I/O Banks

	VCCI (V)	Static Power PDC6 (mW)[1]	Dynamic Power PAC9 (µW/MHz)[2]
Single-Ended			
3.3 V LVTTL / 3.3 V LVCMOS	3.3	–	16.27
3.3 V LVCMOS Wide Range[3]	3.3	–	16.27
2.5 V LVCMOS	2.5	–	4.65
1.8 V LVCMOS	1.8	–	1.61
1.5 V LVCMOS (JESD8-11)	1.5	–	0.96
1.2 V LVCMOS[4]	1.2	–	0.58
1.2 V LVCMOS Wide Range[4]	1.2	–	0.58
3.3 V PCI	3.3	–	17.67
3.3 V PCI-X	3.3	–	17.67
Differential			
LVDS	2.5	2.26	23.39
LVPECL	3.3	5.72	59.05

Notes:

1. *P_{DC6} is the static power (where applicable) measured on VCCI.*
2. *P_{AC9} is the total dynamic power measured on VCCI.*
3. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*
4. *Applicable for IGLOO V2 devices only*

Table 2-14 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings Applicable to Standard Plus I/O Banks

	VCCI (V)	Static Power PDC6 (mW)[1]	Dynamic Power PAC9 (µW/MHz)[2]
Single-Ended			
3.3 V LVTTL / 3.3 V LVCMOS	3.3	–	16.41
3.3 V LVCMOS Wide Range[3]	3.3	–	16.41
2.5 V LVCMOS	2.5	–	4.75
1.8 V LVCMOS	1.8	–	1.66
1.5 V LVCMOS (JESD8-11)	1.5	–	1.00
1.2 V LVCMOS[4]	1.2	–	0.61
1.2 V LVCMOS Wide Range[4]	1.2	–	0.61
3.3 V PCI	3.3	–	17.78
3.3 V PCI-X	3.3	–	17.78

Notes:

1. *PDC6 is the static power (where applicable) measured on VCCI.*
2. *PAC9 is the total dynamic power measured on VCCI.*
3. *Applicable for IGLOO V2 devices only.*
4. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*

Table 2-15 • **Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings Applicable to Standard I/O Banks**

	VCCI (V)	Static Power PDC6 (mW)[1]	Dynamic Power PAC9 (µW/MHz)[2]
Single-Ended			
3.3 V LVTTL / 3.3 V LVCMOS	3.3	–	17.24
3.3 V LVCMOS Wide Range[3]	3.3	–	17.24
2.5 V LVCMOS	2.5	–	5.64
1.8 V LVCMOS	1.8	–	2.63
1.5 V LVCMOS (JESD8-11)	1.5	–	1.97
1.2 V LVCMOS[4]	1.2	–	0.57
1.2 V LVCMOS Wide Range[4]	1.2	–	0.57

Notes:

1. *PDC6 is the static power (where applicable) measured on VCCI.*
2. *PAC9 is the total dynamic power measured on VCCI.*
3. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*
4. *Applicable for IGLOO V2 devices only.*

Table 2-16 • **Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings[1] Applicable to Advanced I/O Banks**

	C_{LOAD} (pF)	VCCI (V)	Static Power PDC7 (mW)[2]	Dynamic Power PAC10 (µW/MHz)[3]
Single-Ended				
3.3 V LVTTL / 3.3 V LVCMOS	5	3.3	–	136.95
3.3 V LVCMOS Wide Range[4]	5	3.3	–	136.95
2.5 V LVCMOS	5	2.5	–	76.84
1.8 V LVCMOS	5	1.8	–	49.31
1.5 V LVCMOS (JESD8-11)	5	1.5	–	33.36
1.2 V LVCMOS[5]	5	1.2	–	16.24
1.2 V LVCMOS Wide Range[5]	5	1.2	–	16.24
3.3 V PCI	10	3.3	–	194.05
3.3 V PCI-X	10	3.3	–	194.05
Differential				
LVDS	–	2.5	7.74	156.22
LVPECL	–	3.3	19.54	339.35

Notes:

1. *Dynamic power consumption is given for standard load and software default drive strength and output slew.*
2. *PDC7 is the static power (where applicable) measured on VCCI.*
3. *PAC10 is the total dynamic power measured on VCCI.*
4. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*
5. *Applicable for IGLOO V2 devices only.*

Table 2-42 • **I/O Short Currents IOSH/IOSL Applicable to Advanced I/O Banks**

	Drive Strength	IOSL (mA)*	IOSH (mA)*
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	25	27
	4 mA	25	27
	6 mA	51	54
	8 mA	51	54
	12 mA	103	109
	16 mA	132	127
	24 mA	268	181
3.3 V LVCMOS Wide Range	100 µA	Same as regular 3.3 V LVCMOS	Same as regular 3.3 V LVCMOS
2.5 V LVCMOS	2 mA	16	18
	4 mA	16	18
	6 mA	32	37
	8 mA	32	37
	12 mA	65	74
	16 mA	83	87
	24 mA	169	124
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
	6 mA	35	44
	8 mA	45	51
	12 mA	91	74
	16 mA	91	74
1.5 V LVCMOS	2 mA	13	16
	4 mA	25	33
	6 mA	32	39
	8 mA	66	55
	12 mA	66	55
1.2 V LVCMOS	2 mA	20	26
1.2 V LVCMOS Wide Range	100 µA	20	26
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	103	109

Note: *$T_J = 100°C$

Timing Characteristics

Applies to 1.5 V DC Core Voltage

Table 2-51 • **3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	4.47	0.18	0.85	0.66	4.56	3.89	2.24	2.19	8.15	7.48	ns
4 mA	Std.	0.97	4.47	0.18	0.85	0.66	4.56	3.89	2.24	2.19	8.15	7.48	ns
6 mA	Std.	0.97	3.74	0.18	0.85	0.66	3.82	3.37	2.49	2.63	7.42	6.96	ns
8 mA	Std.	0.97	3.74	0.18	0.85	0.66	3.82	3.37	2.49	2.63	7.42	6.96	ns
12 mA	Std.	0.97	3.23	0.18	0.85	0.66	3.30	2.98	2.66	2.91	6.89	6.57	ns
16 mA	Std.	0.97	3.08	0.18	0.85	0.66	3.14	2.89	2.70	2.99	6.74	6.48	ns
24 mA	Std.	0.97	3.00	0.18	0.85	0.66	3.06	2.91	2.74	3.27	6.66	6.50	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-52 • **3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	2.73	0.18	0.85	0.66	2.79	2.22	2.25	2.32	6.38	5.82	ns
4 mA	Std.	0.97	2.73	0.18	0.85	0.66	2.79	2.22	2.25	2.32	6.38	5.82	ns
6 mA	Std.	0.97	2.32	0.18	0.85	0.66	2.37	1.85	2.50	2.76	5.96	5.45	ns
8 mA	Std.	0.97	2.32	0.18	0.85	0.66	2.37	1.85	2.50	2.76	5.96	5.45	ns
12 mA	Std.	0.97	2.09	0.18	0.85	0.66	2.14	1.68	2.67	3.05	5.73	5.27	ns
16 mA	Std.	0.97	2.05	0.18	0.85	0.66	2.10	1.64	2.70	3.12	5.69	5.24	ns
24 mA	Std.	0.97	2.07	0.18	0.85	0.66	2.12	1.60	2.75	3.41	5.71	5.20	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-53 • **3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	3.94	0.18	0.85	0.66	4.02	3.46	1.98	2.03	7.62	7.05	ns
4 mA	Std.	0.97	3.94	0.18	0.85	0.66	4.02	3.46	1.98	2.03	7.62	7.05	ns
6 mA	Std.	0.97	3.24	0.18	0.85	0.66	3.31	2.99	2.21	2.42	6.90	6.59	ns
8 mA	Std.	0.97	3.24	0.18	0.85	0.66	3.31	2.99	2.21	2.42	6.90	6.59	ns
12 mA	Std.	0.97	2.76	0.18	0.85	0.66	2.82	2.63	2.36	2.68	6.42	6.22	ns
16 mA	Std.	0.97	2.76	0.18	0.85	0.66	2.82	2.63	2.36	2.68	6.42	6.22	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Timing Characteristics

Applies to 1.5 V DC Core Voltage

Table 2-67 • **3.3 V LVCMOS Wide Range Low Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.7 V
Applicable to Advanced Banks

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 µA	2 mA	Std.	0.97	6.61	0.18	1.19	0.66	6.63	5.63	3.15	2.98	10.22	9.23	ns
100 µA	4 mA	Std.	0.97	6.61	0.18	1.19	0.66	6.63	5.63	3.15	2.98	10.22	9.23	ns
100 µA	6 mA	Std.	0.97	5.49	0.18	1.19	0.66	5.51	4.84	3.54	3.66	9.10	8.44	ns
100 µA	8 mA	Std.	0.97	5.49	0.18	1.19	0.66	5.51	4.84	3.54	3.66	9.10	8.44	ns
100 µA	12 mA	Std.	0.97	4.69	0.18	1.19	0.66	4.71	4.25	3.80	4.10	8.31	7.85	ns
100 µA	16 mA	Std.	0.97	4.46	0.18	1.19	0.66	4.48	4.11	3.86	4.21	8.07	7.71	ns
100 µA	24 mA	Std.	0.97	4.34	0.18	1.19	0.66	4.36	4.14	3.93	4.64	7.95	7.74	ns

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ± 100 µA. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-68 • **3.3 V LVCMOS Wide Range High Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.7 V
Applicable to Advanced Banks

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 µA	2 mA	Std.	0.97	3.92	0.18	1.19	0.66	3.94	3.10	3.16	3.17	7.54	6.70	ns
100 µA	4 mA	Std.	0.97	3.92	0.18	1.19	0.66	3.94	3.10	3.16	3.17	7.54	6.70	ns
100 µA	6 mA	Std.	0.97	3.28	0.18	1.19	0.66	3.30	2.54	3.54	3.86	6.90	6.14	ns
100 µA	8 mA	Std.	0.97	3.28	0.18	1.19	0.66	3.30	2.54	3.54	3.86	6.90	6.14	ns
100 µA	12 mA	Std.	0.97	2.93	0.18	1.19	0.66	2.95	2.27	3.81	4.30	6.54	5.87	ns
100 µA	16 mA	Std.	0.97	2.87	0.18	1.19	0.66	2.89	2.22	3.86	4.41	6.49	5.82	ns
100 µA	24 mA	Std.	0.97	2.90	0.18	1.19	0.66	2.92	2.16	3.94	4.86	6.51	5.75	ns

Notes:

1. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*
2. *Software default selection highlighted in gray.*
3. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ± 100 µA. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*

Table 2-69 • 3.3 V LVCMOS Wide Range Low Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.7 V
Applicable to Standard Plus Banks

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 µA	2 mA	Std.	0.97	5.84	0.18	1.20	0.66	5.86	5.04	2.74	2.71	9.46	8.64	ns
100 µA	4 mA	Std.	0.97	5.84	0.18	1.20	0.66	5.86	5.04	2.74	2.71	9.46	8.64	ns
100 µA	6 mA	Std.	0.97	4.76	0.18	1.20	0.66	4.78	4.33	3.09	3.33	8.37	7.93	ns
100 µA	8 mA	Std.	0.97	4.76	0.18	1.20	0.66	4.78	4.33	3.09	3.33	8.37	7.93	ns
100 µA	12 mA	Std.	0.97	4.02	0.18	1.20	0.66	4.04	3.78	3.33	3.73	7.64	7.37	ns
100 µA	16 mA	Std.	0.97	4.02	0.18	1.20	0.66	4.04	3.78	3.33	3.73	7.64	7.37	ns

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ± 100 µA. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-70 • 3.3 V LVCMOS Wide Range High Slew – Applies to 1.5 V DC Core Voltage
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.7 V
Applicable to Standard Plus Banks

Drive Strength	Equivalent Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 µA	2 mA	Std.	0.97	3.33	0.18	1.20	0.66	3.35	2.68	2.73	2.88	6.94	6.27	ns
100 µA	4 mA	Std.	0.97	3.33	0.18	1.20	0.66	3.35	2.68	2.73	2.88	6.94	6.27	ns
100 µA	6 mA	Std.	0.97	2.75	0.18	1.20	0.66	2.77	2.17	3.08	3.50	6.36	5.77	ns
100 µA	8 mA	Std.	0.97	2.75	0.18	1.20	0.66	2.77	2.17	3.08	3.50	6.36	5.77	ns
100 µA	12 mA	Std.	0.97	2.45	0.18	1.20	0.66	2.47	1.92	3.33	3.90	6.06	5.51	ns
100 µA	16 mA	Std.	0.97	2.45	0.18	1.20	0.66	2.47	1.92	3.33	3.90	6.06	5.51	ns

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ± 100 µA. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*
3. *Software default selection highlighted in gray.*

Table 2-100 • **1.8 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	3.25	0.18	1.01	0.66	3.21	3.25	2.33	1.61	6.80	6.85	ns
4 mA	Std.	0.97	2.62	0.18	1.01	0.66	2.68	2.51	2.66	2.46	6.27	6.11	ns
6 mA	Std.	0.97	2.31	0.18	1.01	0.66	2.36	2.15	2.90	2.87	5.95	5.75	ns
8 mA	Std.	0.97	2.25	0.18	1.01	0.66	2.30	2.08	2.95	2.98	5.89	5.68	ns
12 mA	Std.	0.97	2.24	0.18	1.01	0.66	2.29	2.00	3.02	3.40	5.88	5.60	ns
16 mA	Std.	0.97	2.24	0.18	1.01	0.66	2.29	2.00	3.02	3.40	5.88	5.60	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-101 • **1.8 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	5.78	0.18	1.01	0.66	5.90	5.32	1.95	1.47	9.49	8.91	ns
4 mA	Std.	0.97	4.75	0.18	1.01	0.66	4.85	4.54	2.25	2.21	8.44	8.13	ns
6 mA	Std.	0.97	4.07	0.18	1.01	0.66	4.15	3.98	2.46	2.58	7.75	7.57	ns
8 mA	Std.	0.97	4.07	0.18	1.01	0.66	4.15	3.98	2.46	2.58	7.75	7.57	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-102 • **1.8 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	2.76	0.18	1.01	0.66	2.79	2.76	1.94	1.51	6.39	6.35	ns
4 mA	Std.	0.97	2.25	0.18	1.01	0.66	2.30	2.09	2.24	2.29	5.89	5.69	ns
6 mA	Std.	0.97	1.97	0.18	1.01	0.66	2.02	1.76	2.46	2.66	5.61	5.36	ns
8 mA	Std.	0.97	1.97	0.18	1.01	0.66	2.02	1.76	2.46	2.66	5.61	5.36	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-103 • **1.8 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.97	5.63	0.18	0.98	0.66	5.74	5.30	1.68	1.24	ns
4 mA	Std.	0.97	4.69	0.18	0.98	0.66	4.79	4.52	1.97	1.98	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

***Table 2-104* • 1.8 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	2.62	0.18	0.98	0.66	2.67	2.59	1.67	1.29	2.62	ns
4 mA	Std.	2.18	0.18	0.98	0.66	2.22	1.93	1.97	2.06	2.18	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

1.2 V DC Core Voltage

***Table 2-105* • 1.8 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	6.97	0.26	1.11	1.10	7.08	6.48	2.87	2.29	12.87	12.27	ns
4 mA	Std.	1.55	5.91	0.26	1.11	1.10	6.01	5.57	3.21	3.14	11.79	11.36	ns
6 mA	Std.	1.55	5.16	0.26	1.11	1.10	5.24	4.95	3.45	3.55	11.03	10.74	ns
8 mA	Std.	1.55	4.90	0.26	1.11	1.10	4.98	4.81	3.50	3.66	10.77	10.60	ns
12 mA	Std.	1.55	4.83	0.26	1.11	1.10	4.90	4.83	3.58	4.08	10.68	10.61	ns
16 mA	Std.	1.55	4.83	0.26	1.11	1.10	4.90	4.83	3.58	4.08	10.68	10.61	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

***Table 2-106* • 1.8 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	3.73	0.26	1.11	1.10	3.71	3.73	2.86	2.34	9.49	9.51	ns
4 mA	Std.	1.55	3.12	0.26	1.11	1.10	3.16	2.97	3.21	3.22	8.95	8.75	ns
6 mA	Std.	1.55	2.79	0.26	1.11	1.10	2.83	2.59	3.45	3.65	8.62	8.38	ns
8 mA	Std.	1.55	2.73	0.26	1.11	1.10	2.77	2.52	3.50	3.75	8.56	8.30	ns
12 mA	Std.	1.55	2.72	0.26	1.11	1.10	2.76	2.43	3.58	4.19	8.55	8.22	ns
16 mA	Std.	1.55	2.72	0.26	1.11	1.10	2.76	2.43	3.58	4.19	8.55	8.22	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

***Table 2-113* • Minimum and Maximum DC Input and Output Levels Applicable to Standard I/O Banks**

1.5 V LVCMOS	**VIL**		**VIH**		**VOL**	**VOH**	**IOL**	**IOH**	**IOSH**	**IOSL**	**IIL**[1]	**IIH**[2]
Drive Strength	**Min. V**	**Max. V**	**Min. V**	**Max. V**	**Max. V**	**Min. V**	**mA**	**mA**	**Max. mA**[3]	**Max. mA**[3]	**μA**[4]	**μA**[4]
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2	13	16	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN <V CCI. Input current is larger when operating outside recommended ranges*
3. *Currents are measured at 100°C junction temperature and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

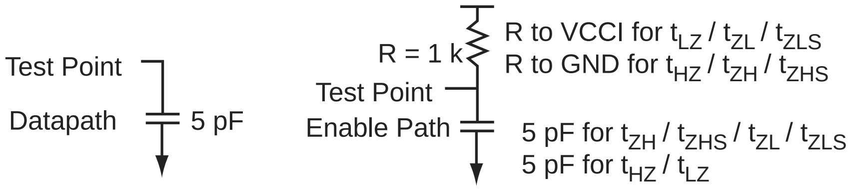

***Figure 2-10* • AC Loading**

***Table 2-114* • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	**Input High (V)**	**Measuring Point* (V)**	**C_{LOAD} (pF)**
0	1.5	0.75	5

Note: *Measuring point = Vtrip. See Table 2-29 on page 2-28 for a complete table of trip points.

Table 2-138 • Minimum and Maximum DC Input and Output Levels for LVCMOS 1.2 V Wide Range Applicable to Standard Plus I/O Banks

1.2 V LVCMOS Wide Range		VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[2]	IIH[3]
Drive Strength	Equivalent Software Default Drive Strength Option[1]	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[4]	Max. mA[4]	µA[5]	µA[5]
100 µA	2mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.26	0.25 * VCCI	0.75 * VCCI	100	100	20	26	10	10

Notes:

1. *The minimum drive strength for the default LVCMOS 1.2 V software configuration when run in wide range is ± 100 µA. The drive strength displayed in software is supported in normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
3. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
4. *Currents are measured at 100°C junction temperature and maximum voltage.*
5. *Currents are measured at 85°C junction temperature.*
6. *Software default selection highlighted in gray.*

Table 2-139 • Minimum and Maximum DC Input and Output Levels for LVCMOS 1.2 V Wide Range Applicable to Standard I/O Banks

1.2 V LVCMOS Wide Range		VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[2]	IIH[3]
Drive Strength	Equivalent Software Default Drive Strength Option[1]	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[4]	Max. mA[4]	µA[5]	µA[5]
100 µA	1 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	100	100	20	26	10	10

Notes:

1. *The minimum drive strength for the default LVCMOS 1.2 V software configuration when run in wide range is ± 100 µA. The drive strength displayed in software is supported in normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
3. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
4. *Currents are measured at 100°C junction temperature and maximum voltage.*
5. *Currents are measured at 85°C junction temperature.*
6. *Software default selection highlighted in gray.*

Table 2-140 • 1.2 V LVCMOS Wide Range AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	1.2	0.6	5

*Note: *Measuring point = Vtrip. See Table 2-29 on page 2-28 for a complete table of trip points.*

Timing Characteristics

Refer to LVCMOS 1.2 V (normal range) "Timing Characteristics" on page 2-75 for worst-case timing.

Input Register

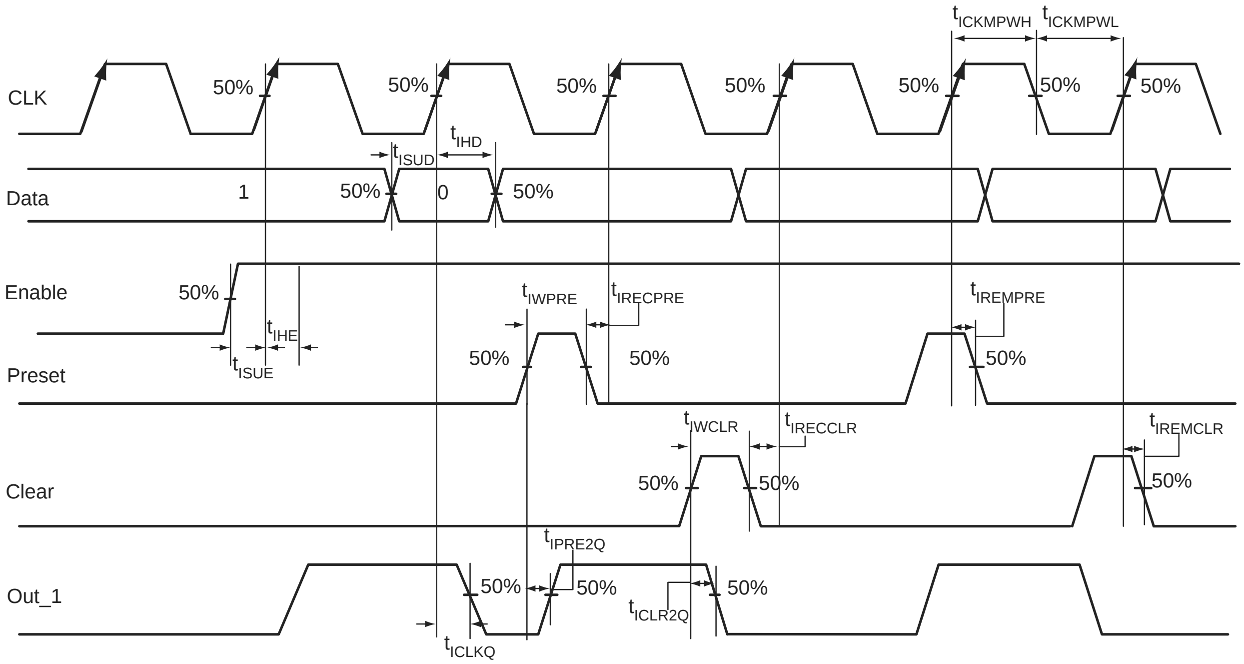

Figure 2-18 • **Input Register Timing Diagram**

Timing Characteristics

1.5 V DC Core Voltage

Table 2-157 • **Input Data Register Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	Std.	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.42	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.47	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	ns
t_{ISUE}	Enable Setup Time for the Input Data Register	0.67	ns
t_{IHE}	Enable Hold Time for the Input Data Register	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.79	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.79	ns
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.24	ns
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.24	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.19	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.19	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width High for the Input Data Register	0.31	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width Low for the Input Data Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-179 • **AGL600 Global Resource**
Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.48	1.82	ns
t_{RCKH}	Input High Delay for Global Clock	1.52	1.94	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.18		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.42	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

Table 2-180 • **AGL1000 Global Resource**
Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	Std.		Units
		Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.55	1.89	ns
t_{RCKH}	Input High Delay for Global Clock	1.60	2.02	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.18		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.42	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

1.2 V DC Core Voltage

Table 2-193 **• RAM4K9**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V

Parameter	Description	Std.	Units
t_{AS}	Address setup time	1.53	ns
t_{AH}	Address hold time	0.29	ns
t_{ENS}	REN WEN setup time	1.50	ns
t_{ENH}	REN, WEN hold time	0.29	ns
t_{BKS}	BLK setup time	3.05	ns
t_{BKH}	BLK hold time	0.29	ns
t_{DS}	Input data (DIN) setup time	1.33	ns
t_{DH}	Input data (DIN) hold time	0.66	ns
t_{CKQ1}	Clock High to new data valid on DOUT (output retained, WMODE = 0)	6.61	ns
	Clock High to new data valid on DOUT (flow-through, WMODE = 1)	5.72	ns
t_{CKQ2}	Clock High to new data valid on DOUT (pipelined)	3.38	ns
t_{C2CWWL}[1]	Address collision clk-to-clk delay for reliable write after write on same address – Applicable to Closing Edge	0.30	ns
t_{C2CRWH}[1]	Address collision clk-to-clk delay for reliable read access after write on same address – Applicable to Opening Edge	0.89	ns
t_{C2CWRH}[1]	Address collision clk-to-clk delay for reliable write access after read on same address – Applicable to Opening Edge	1.01	ns
t_{RSTBQ}	RESET Low to data out Low on DOUT (flow-through)	3.86	ns
	RESET Low to data out Low on DOUT (pipelined)	3.86	ns
$t_{REMRSTB}$	RESET removal	1.12	ns
$t_{RECRSTB}$	RESET recovery	5.93	ns
$t_{MPWRSTB}$	RESET minimum pulse width	1.18	ns
t_{CYC}	Clock cycle time	10.90	ns
F_{MAX}	Maximum frequency	92	MHz

Notes:

1. *For more information, refer to the application note* Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs*.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

CS196	
Pin Number	**AGL125 Function**
H11	GCB0/IO54RSB0
H12	GCA1/IO55RSB0
H13	IO49RSB0
H14	GCA2/IO57RSB0
J1	GFC2/IO115RSB1
J2	IO110RSB1
J3	IO94RSB1
J4	IO93RSB1
J5	IO89RSB1
J6	NC
J7	VCC
J8	VCC
J9	NC
J10	IO60RSB0
J11	GCB2/IO58RSB0
J12	IO50RSB0
J13	GDC1/IO61RSB0
J14	GDC0/IO62RSB0
K1	IO99RSB1
K2	GND
K3	IO95RSB1
K4	VCCIB1
K5	NC
K6	IO86RSB1
K7	IO80RSB1
K8	IO74RSB1
K9	IO72RSB1
K10	NC
K11	VCCIB0
K12	GDA1/IO65RSB0
K13	GND
K14	GDB1/IO63RSB0
L1	GEB1/IO107RSB1
L2	GEC1/IO109RSB1
L3	GEC0/IO108RSB1
L4	IO96RSB1
L5	IO91RSB1
L6	IO90RSB1
L7	IO83RSB1
L8	IO81RSB1
L9	IO71RSB1
L10	IO70RSB1
L11	VPUMP
L12	VJTAG
L13	GDA0/IO66RSB0
L14	GDB0/IO64RSB0
M1	GEB0/IO106RSB1
M2	GEA1/IO105RSB1
M3	GNDQ
M4	VCCIB1
M5	IO92RSB1
M6	IO88RSB1
M7	NC
M8	VCCIB1
M9	IO76RSB1
M10	GDB2/IO68RSB1
M11	VCCIB1
M12	VMV1
M13	TRST
M14	VCCIB0
N1	GEA0/IO104RSB1
N2	VMV1
N3	GEC2/IO101RSB1
N4	IO100RSB1
N5	GND
N6	IO87RSB1
N7	IO82RSB1
N8	IO78RSB1
N9	IO73RSB1
N10	GND
N11	TCK
N12	TDI
N13	GNDQ
N14	TDO
P1	GND
P2	GEA2/IO103RSB1
P3	FF/GEB2/IO102RSB1
P4	IO98RSB1
P5	IO97RSB1
P6	IO85RSB1
P7	IO84RSB1
P8	IO79RSB1
P9	IO77RSB1
P10	IO75RSB1
P11	GDC2/IO69RSB1
P12	GDA2/IO67RSB1
P13	TMS
P14	GND

FG256	
Pin Number	**AGL600 Function**
H3	GFB1/IO163PPB3
H4	VCOMPLF
H5	GFC0/IO164NPB3
H6	VCC
H7	GND
H8	GND
H9	GND
H10	GND
H11	VCC
H12	GCC0/IO69NPB1
H13	GCB1/IO70PPB1
H14	GCA0/IO71NPB1
H15	IO67NPB1
H16	GCB0/IO70NPB1
J1	GFA2/IO161PPB3
J2	GFA1/IO162PDB3
J3	VCCPLF
J4	IO160NDB3
J5	GFB2/IO160PDB3
J6	VCC
J7	GND
J8	GND
J9	GND
J10	GND
J11	VCC
J12	GCB2/IO73PPB1
J13	GCA1/IO71PPB1
J14	GCC2/IO74PPB1
J15	IO80PPB1
J16	GCA2/IO72PDB1
K1	GFC2/IO159PDB3
K2	IO161NPB3
K3	IO156PPB3
K4	IO129RSB2
K5	VCCIB3
K6	VCC
K7	GND
K8	GND
K9	GND
K10	GND
K11	VCC
K12	VCCIB1
K13	IO73NPB1
K14	IO80NPB1
K15	IO74NPB1
K16	IO72NDB1
L1	IO159NDB3
L2	IO156NPB3
L3	IO151PPB3
L4	IO158PSB3
L5	VCCIB3
L6	GND
L7	VCC
L8	VCC
L9	VCC
L10	VCC
L11	GND
L12	VCCIB1
L13	GDB0/IO87NPB1
L14	IO85NDB1
L15	IO85PDB1
L16	IO84PDB1
M1	IO150PDB3
M2	IO151NPB3
M3	IO147NPB3
M4	GEC0/IO146NPB3
M5	VMV3
M6	VCCIB2
M7	VCCIB2
M8	IO117RSB2
M9	IO110RSB2
M10	VCCIB2
M11	VCCIB2
M12	VMV2
M13	IO94RSB2
M14	GDB1/IO87PPB1
M15	GDC1/IO86PDB1
M16	IO84NDB1
N1	IO150NDB3
N2	IO147PPB3
N3	GEC1/IO146PPB3
N4	IO140RSB2
N5	GNDQ
N6	GEA2/IO143RSB2
N7	IO126RSB2
N8	IO120RSB2
N9	IO108RSB2
N10	IO103RSB2
N11	IO99RSB2
N12	GNDQ
N13	IO92RSB2
N14	VJTAG
N15	GDC0/IO86NDB1
N16	GDA1/IO88PDB1
P1	GEB1/IO145PDB3
P2	GEB0/IO145NDB3
P3	VMV2
P4	IO138RSB2
P5	IO136RSB2
P6	IO131RSB2
P7	IO124RSB2
P8	IO119RSB2
P9	IO107RSB2
P10	IO104RSB2
P11	IO97RSB2
P12	VMV1
P13	TCK
P14	VPUMP
P15	TRST
P16	GDA0/IO88NDB1
R1	GEA1/IO144PDB3
R2	GEA0/IO144NDB3
R3	IO139RSB2
R4	GEC2/IO141RSB2

FG256	
Pin Number	**AGL1000 Function**
R5	IO168RSB2
R6	IO163RSB2
R7	IO157RSB2
R8	IO149RSB2
R9	IO143RSB2
R10	IO138RSB2
R11	IO131RSB2
R12	IO125RSB2
R13	GDB2/IO115RSB2
R14	TDI
R15	GNDQ
R16	TDO
T1	GND
T2	IO183RSB2
T3	FF/GEB2/IO186RSB2
T4	IO172RSB2
T5	IO170RSB2
T6	IO164RSB2
T7	IO158RSB2
T8	IO153RSB2
T9	IO142RSB2
T10	IO135RSB2
T11	IO130RSB2
T12	GDC2/IO116RSB2
T13	IO120RSB2
T14	GDA2/IO114RSB2
T15	TMS
T16	GND

FG484	
Pin Number	**AGL400 Function**
Y7	NC
Y8	VCC
Y9	VCC
Y10	NC
Y11	NC
Y12	NC
Y13	NC
Y14	VCC
Y15	VCC
Y16	NC
Y17	NC
Y18	GND
Y19	NC
Y20	NC
Y21	NC
Y22	VCCIB1

FG484	
Pin Number	**AGL1000 Function**
N17	IO100NPB1
N18	IO102NDB1
N19	IO102PDB1
N20	NC
N21	IO101NPB1
N22	IO103PDB1
P1	NC
P2	IO199PDB3
P3	IO199NDB3
P4	IO202NDB3
P5	IO202PDB3
P6	IO196PPB3
P7	IO193PPB3
P8	VCCIB3
P9	GND
P10	VCC
P11	VCC
P12	VCC
P13	VCC
P14	GND
P15	VCCIB1
P16	GDB0/IO112NPB1
P17	IO106NDB1
P18	IO106PDB1
P19	IO107PDB1
P20	NC
P21	IO104PDB1
P22	IO103NDB1
R1	NC
R2	IO197PPB3
R3	VCC
R4	IO197NPB3
R5	IO196NPB3
R6	IO193NPB3
R7	GEC0/IO190NPB3
R8	VMV3