



Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	24576
Total RAM Bits	147456
Number of I/O	97
Number of Gates	1000000
Voltage - Supply	1.14V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	144-LBGA
Supplier Device Package	144-FPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/agl1000v2-fgg144i

- Wide input frequency range (f_{IN_CCC}) = 1.5 MHz up to 250 MHz
- Output frequency range (f_{OUT_CCC}) = 0.75 MHz up to 250 MHz
- 2 programmable delay types for clock skew minimization
- Clock frequency synthesis (for PLL only)

Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°. Output phase shift depends on the output divider configuration (for PLL only).
- Output duty cycle = 50% $\pm$ 1.5% or better (for PLL only)
- Low output jitter: worst case < 2.5% $\times$ clock period peak-to-peak period jitter when single global network used (for PLL only)
- Maximum acquisition time is 300 μ s (for PLL only)
- Exceptional tolerance to input period jitter—allowable input jitter is up to 1.5 ns (for PLL only)
- Four precise phases; maximum misalignment between adjacent phases of 40 ps $\times$ 250 MHz / f_{OUT_CCC} (for PLL only)

Global Clocking

IGLOO devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there is a comprehensive global clock distribution network.

Each VersaTile input and output port has access to nine VersaNets: six chip (main) and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via multiplexers (MUXes). The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high-fanout nets.

I/Os with Advanced I/O Standards

The IGLOO family of FPGAs features a flexible I/O structure, supporting a range of voltages (1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.0 V wide range, and 3.3 V). IGLOO FPGAs support many different I/O standards—single-ended and differential.

The I/Os are organized into banks, with two or four banks per device. The configuration of these banks determines the I/O standards supported (Table 1-1).

Table 1-1 • I/O Standards Supported

I/O Bank Type	Device and Bank Location	I/O Standards Supported		
		LVTTL/ LVCMOS	PCI/PCI-X	LVPECL, LVDS, B-LVDS, M-LVDS
Advanced	East and west banks of AGL250 and larger devices	✓	✓	✓
Standard Plus	North and south banks of AGL250 and larger devices All banks of AGL060 and AGL125K	✓	✓	Not supported
Standard	All banks of AGL015 and AGL030	✓	Not supported	Not supported

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of the following:

- Single-Data-Rate applications
- Double-Data-Rate applications—DDR LVDS, B-LVDS, and M-LVDS I/Os for point-to-point communications

IGLOO banks for the AGL250 device and above support LVPECL, LVDS, B-LVDS, and M-LVDS. B-LVDS and M-LVDS can support up to 20 loads.

Hot-swap (also called hot-plug, or hot-insertion) is the operation of hot-insertion or hot-removal of a card in a powered-up system.

Cold-sparing (also called cold-swap) refers to the ability of a device to leave system data undisturbed when the system is powered up, while the component itself is powered down, or when power supplies are floating.

Wide Range I/O Support

IGLOO devices support JEDEC-defined wide range I/O operation. IGLOO devices support both the JESD8-B specification, covering 3 V and 3.3 V supplies, for an effective operating range of 2.7 V to 3.6 V, and JESD8-12 with its 1.2 V nominal, supporting an effective operating range of 1.14 V to 1.575 V.

Wider I/O range means designers can eliminate power supplies or power conditioning components from the board or move to less costly components with greater tolerances. Wide range eases I/O bank management and provides enhanced protection from system voltage spikes, while providing the flexibility to easily run custom voltage applications.

Specifying I/O States During Programming

You can modify the I/O states during programming in FlashPro. In FlashPro, this feature is supported for PDB files generated from Designer v8.5 or greater. See the *FlashPro User Guide* for more information.

Note: PDB files generated from Designer v8.1 to Designer v8.4 (including all service packs) have limited display of Pin Numbers only.

1. Load a PDB from the FlashPro GUI. You must have a PDB loaded to modify the I/O states during programming.
2. From the FlashPro GUI, click PDB Configuration. A FlashPoint – Programming File Generator window appears.
3. Click the Specify I/O States During Programming button to display the Specify I/O States During Programming dialog box.
4. Sort the pins as desired by clicking any of the column headers to sort the entries by that header. Select the I/Os you wish to modify (Figure 1-5 on page 1-9).
5. Set the I/O Output State. You can set Basic I/O settings if you want to use the default I/O settings for your pins, or use Custom I/O settings to customize the settings for each pin. Basic I/O state settings:

1 – I/O is set to drive out logic High

0 – I/O is set to drive out logic Low

Last Known State – I/O is set to the last value that was driven out prior to entering the programming mode, and then held at that value during programming

Z -Tri-State: I/O is tristated

Ramping up (V2 devices): $0.65\text{ V} < \text{trip_point_up} < 1.05\text{ V}$
 Ramping down (V2 devices): $0.55\text{ V} < \text{trip_point_down} < 0.95\text{ V}$

VCC and VCCI ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to VCCI.
- JTAG supply, PLL power supplies, and charge pump VPUMP supply have no influence on I/O behavior.

PLL Behavior at Brownout Condition

Microsemi recommends using monotonic power supplies or voltage regulators to ensure proper power-up behavior. Power ramp-up should be monotonic at least until VCC and VCCPLX exceed brownout activation levels (see Figure 2-1 and Figure 2-2 on page 2-5 for more details).

When PLL power supply voltage and/or VCC levels drop below the VCC brownout levels ($0.75\text{ V} \pm 0.25\text{ V}$ for V5 devices, and $0.75\text{ V} \pm 0.2\text{ V}$ for V2 devices), the PLL output lock signal goes low and/or the output clock is lost. Refer to the Brownout Voltage section in the "Power-Up/-Down Behavior of Low Power Flash Devices" chapter of the ProASIC®3 and ProASIC3E FPGA fabric user guides for information on clock and lock recovery.

Internal Power-Up Activation Sequence

1. Core
2. Input buffers
3. Output buffers, after 200 ns delay from input buffer activation

To make sure the transition from input buffers to output buffers is clean, ensure that there is no path longer than 100 ns from input buffer to output buffer in your design.

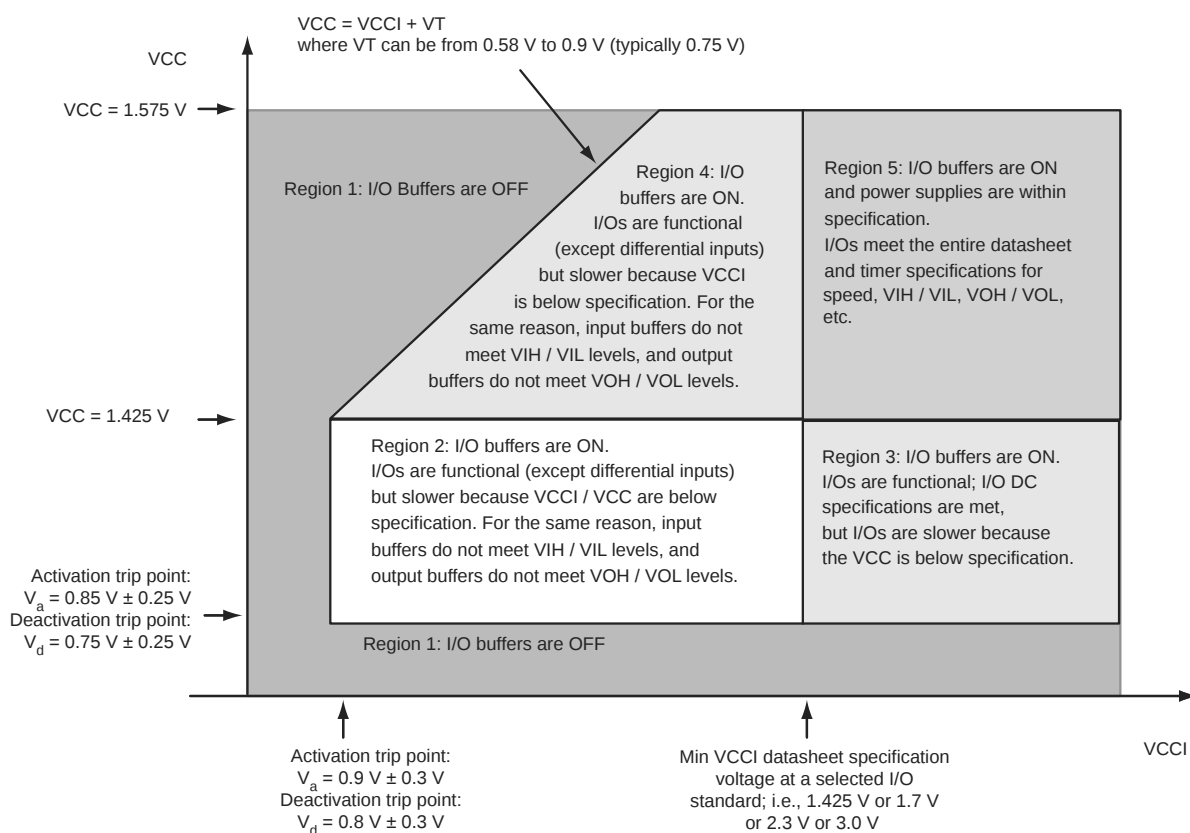


Figure 2-1 • V5 Devices – I/O State as a Function of VCCI and VCC Voltage Levels

User I/O Characteristics

Timing Model

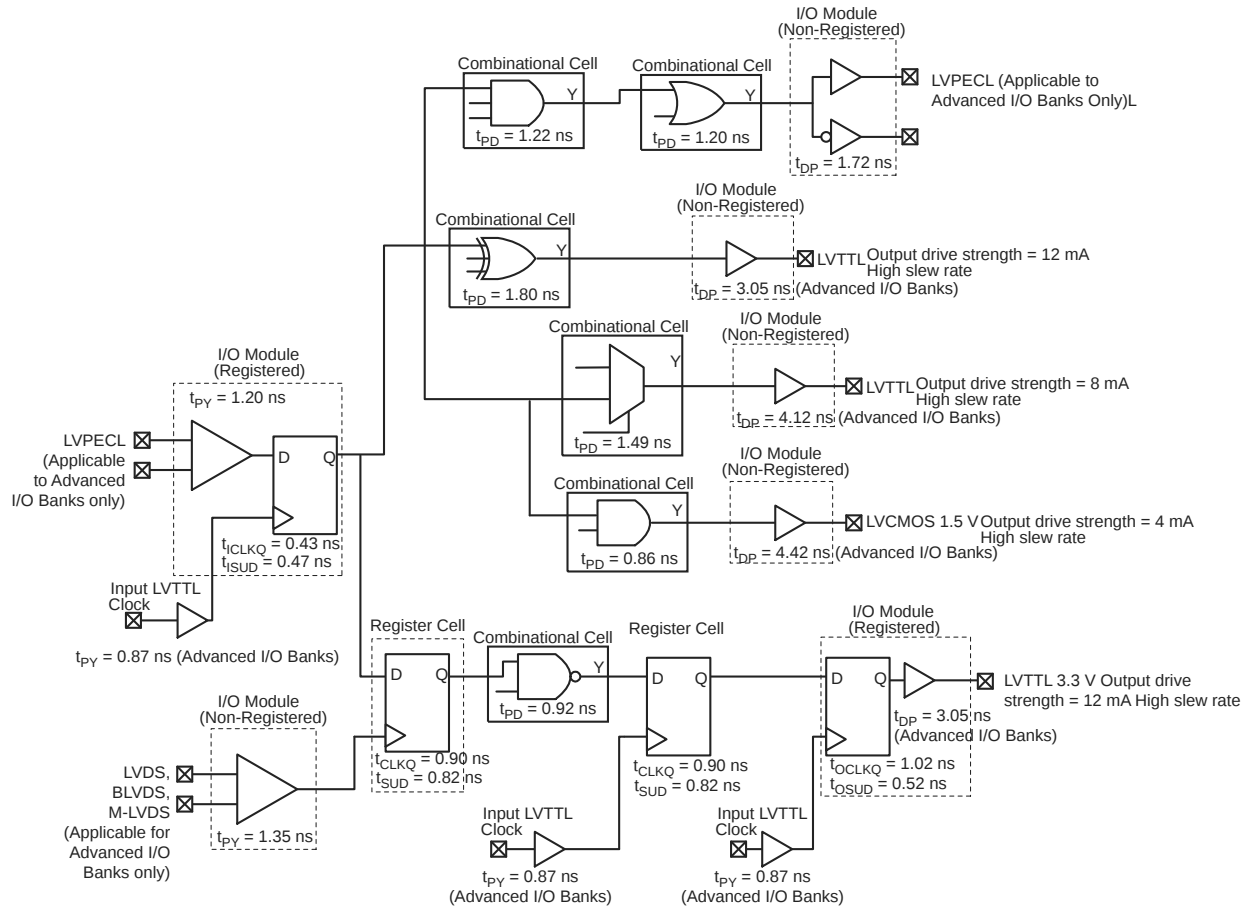


Figure 2-3 • Timing Model

Operating Conditions: Std. Speed, Commercial Temperature Range ($T_J = 70^\circ\text{C}$), Worst-Case $V_{CC} = 1.425$ V, for DC 1.5 V Core Voltage, Applicable to V2 and V5 Devices

Overview of I/O Performance

Summary of I/O DC Input and Output Levels – Default I/O Software Settings

Table 2-25 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings
Applicable to Advanced I/O Banks

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength Option ²	Slew Rate	VIL		VIH		VOL	VOH	IOL ¹	IOH ¹
				Min.V	Max. V	Min. V	Max.V	Max. V	Min. V	mA	mA
3.3 V LVTTTL / 3.3 V LVCMOS	12 mA	12 mA	High	−0.3	0.8	2	3.6	0.4	2.4	12	12
3.3 V LVCMOS Wide Range ³	100 μ A	12 mA	High	−0.3	0.8	2	3.6	0.2	VCCI − 0.2	0.1	0.1
2.5 V LVCMOS	12 mA	12 mA	High	−0.3	0.7	1.7	2.7	0.7	1.7	12	12
1.8 V LVCMOS	12 mA	12 mA	High	−0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI − 0.45	12	12
1.5 V LVCMOS	12 mA	12 mA	High	−0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	12	12
1.2 V LVCMOS ⁴	2 mA	2 mA	High	−0.3	0.35 * VCCI	0.65 * VCCI	1.26	0.25 * VCCI	0.75 * VCCI	2	2
1.2 V LVCMOS Wide Range ^{4,5}	100 μ A	2 mA	High	−0.3	0.3 * VCCI	0.7 * VCCI	1.575	0.1	VCCI − 0.1	0.1	0.1
3.3 V PCI	Per PCI specifications										
3.3 V PCI-X	Per PCI-X specifications										

Notes:

1. Currents are measured at 85°C junction temperature.
2. The minimum drive strength for any LVCMOS 1.2 V or LVCMOS 3.3 V software configuration when run in wide range is $\pm 100 \mu$ A. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
3. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.
4. Applicable to V2 Devices operating at VCCI $\geq$ VCC.
5. All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification.

Table 2-49 • Minimum and Maximum DC Input and Output Levels
Applicable to Standard I/O Banks

3.3 V LVTTTL / 3.3 V LVCMOS	VIL		VIH		V _{OL}	VOH	IOL	IOH	IOSL	IOSH	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	−0.3	0.8	2	3.6	0.4	2.4	2	2	25	27	10	10
4 mA	−0.3	0.8	2	3.6	0.4	2.4	4	4	25	27	10	10
6 mA	−0.3	0.8	2	3.6	0.4	2.4	6	6	51	54	10	10
8 mA	−0.3	0.8	2	3.6	0.4	2.4	8	8	51	54	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

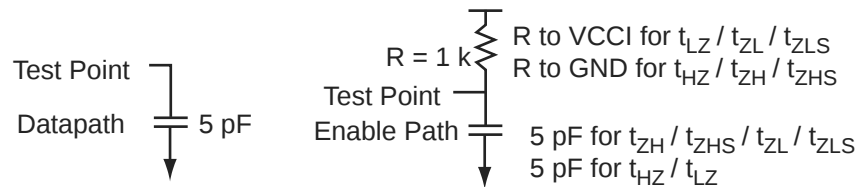


Figure 2-7 • AC Loading

Table 2-50 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C _{LOAD} (pF)
0	3.3	1.4	5

Note: *Measuring point = V_{trip}. See Table 2-29 on page 2-28 for a complete table of trip points.

Table 2-107 • 1.8 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V****Applicable to Standard Plus Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	6.32	0.26	1.11	1.10	6.43	5.81	2.47	2.16	12.22	11.60	ns
4 mA	Std.	1.55	5.27	0.26	1.11	1.10	5.35	5.01	2.78	2.92	11.14	10.79	ns
6 mA	Std.	1.55	4.56	0.26	1.11	1.10	4.64	4.44	3.00	3.30	10.42	10.22	ns
8 mA	Std.	1.55	4.56	0.26	1.11	1.10	4.64	4.44	3.00	3.30	10.42	10.22	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-108 • 1.8 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V****Applicable to Standard Plus Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	3.22	0.26	1.11	1.10	3.26	3.18	2.47	2.20	9.05	8.97	ns
4 mA	Std.	1.55	2.72	0.26	1.11	1.10	2.75	2.50	2.78	3.01	8.54	8.29	ns
6 mA	Std.	1.55	2.43	0.26	1.11	1.10	2.47	2.16	2.99	3.39	8.25	7.94	ns
8 mA	Std.	1.55	2.43	0.26	1.11	1.10	2.47	2.16	2.99	3.39	8.25	7.94	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-109 • 1.8 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V****Applicable to Standard Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	1.55	6.13	0.26	1.08	1.10	6.24	5.79	2.08	1.78	ns
4 mA	Std.	1.55	5.17	0.26	1.08	1.10	5.26	4.98	2.38	2.54	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-110 • 1.8 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V****Applicable to Standard Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	3.06	0.26	1.08	1.10	3.10	3.01	2.08	1.83	3.06	ns
4 mA	Std.	2.60	0.26	1.08	1.10	2.64	2.33	2.38	2.62	2.60	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-119 • 1.5 V LVC MOS Low Slew – Applies to 1.5 V DC Core Voltage**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V****Applicable to Standard Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.97	5.88	0.18	1.14	0.66	6.00	5.45	2.00	1.94	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-120 • 1.5 V LVC MOS High Slew – Applies to 1.5 V DC Core Voltage**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V****Applicable to Standard Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.97	2.51	0.18	1.14	0.66	2.56	2.21	1.99	2.03	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

1.2 V DC Core Voltage**Table 2-121 • 1.5 V LVC MOS Low Slew – Applies to 1.2 V DC Core Voltage****Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V****Applicable to Advanced I/O Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	7.17	0.26	1.27	1.10	7.29	6.60	3.33	3.03	13.07	12.39	ns
4 mA	Std.	1.55	6.27	0.26	1.27	1.10	6.37	5.86	3.61	3.51	12.16	11.64	ns
6 mA	Std.	1.55	5.94	0.26	1.27	1.10	6.04	5.70	3.67	3.64	11.82	11.48	ns
8 mA	Std.	1.55	5.86	0.26	1.27	1.10	5.96	5.71	2.83	4.11	11.74	11.50	ns
12 mA	Std.	1.55	5.86	0.26	1.27	1.10	5.96	5.71	2.83	4.11	11.74	11.50	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-122 • 1.5 V LVC MOS High Slew – Applies to 1.2 V DC Core Voltage**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V****Applicable to Advanced I/O Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	3.44	0.26	1.27	1.10	3.49	3.35	3.32	3.12	9.28	9.14	ns
4 mA	Std.	1.55	3.06	0.26	1.27	1.10	3.10	2.89	3.60	3.61	8.89	8.67	ns
6 mA	Std.	1.55	2.98	0.26	1.27	1.10	3.02	2.80	3.66	3.74	8.81	8.58	ns
8 mA	Std.	1.55	2.96	0.26	1.27	1.10	3.00	2.70	3.75	4.23	8.78	8.48	ns
12 mA	Std.	1.55	2.96	0.26	1.27	1.10	3.00	2.70	3.75	4.23	8.78	8.48	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Input Register

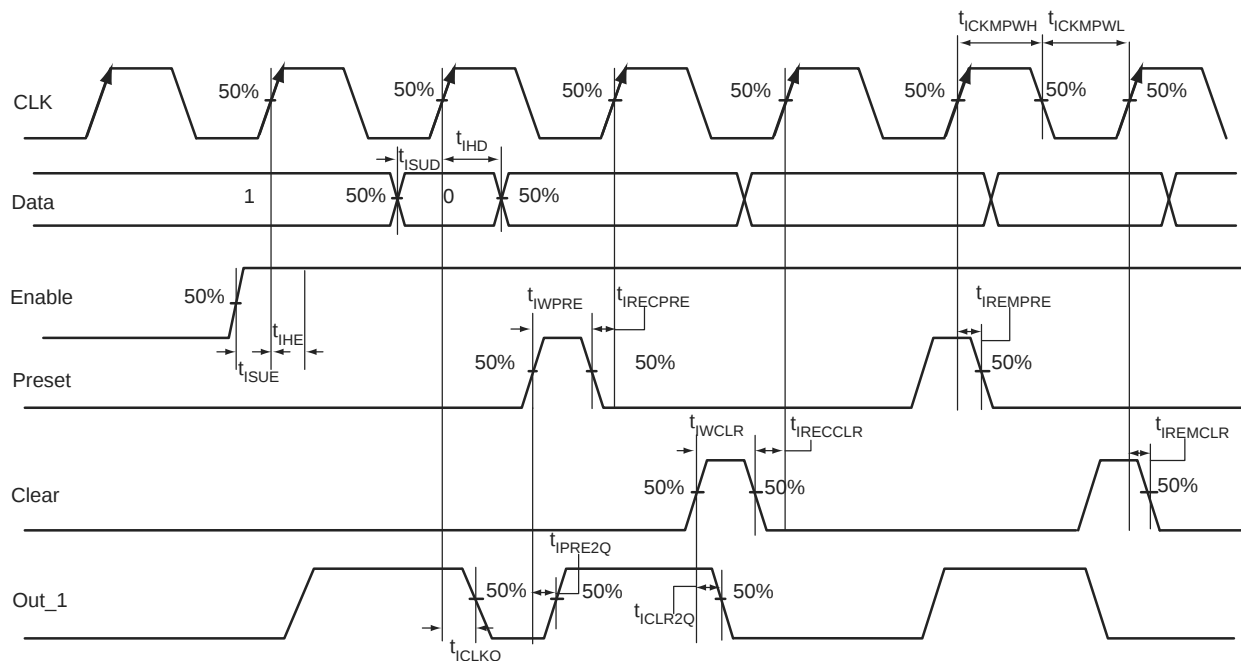


Figure 2-18 • Input Register Timing Diagram

Timing Characteristics

1.5 V DC Core Voltage

Table 2-157 • Input Data Register Propagation Delays

Commercial-Case Conditions: $T_j = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.42	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.47	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	ns
t_{ISUE}	Enable Setup Time for the Input Data Register	0.67	ns
t_{IHE}	Enable Hold Time for the Input Data Register	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.79	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.79	ns
t_{IEMCLR}	Asynchronous Clear Removal Time for the Input Data Register	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.24	ns
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.24	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.19	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.19	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width High for the Input Data Register	0.31	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width Low for the Input Data Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

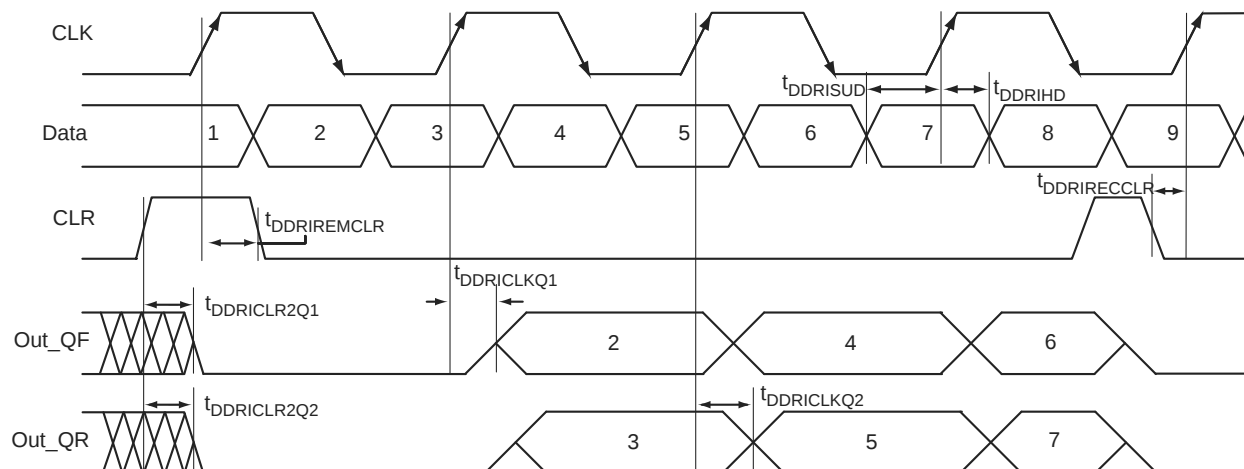


Figure 2-22 • Input DDR Timing Diagram

Timing Characteristics

1.5 V DC Core Voltage

Table 2-164 • Input DDR Propagation Delays

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.	Units
t_{DDRCLKQ1}	Clock-to-Out Out_QR for Input DDR	0.48	ns
t_{DDRCLKQ2}	Clock-to-Out Out_QF for Input DDR	0.65	ns
t_{DDRISUD1}	Data Setup for Input DDR (negedge)	0.50	ns
t_{DDRISUD2}	Data Setup for Input DDR (posedge)	0.40	ns
t_{DDRHD1}	Data Hold for Input DDR (negedge)	0.00	ns
t_{DDRHD2}	Data Hold for Input DDR (posedge)	0.00	ns
$t_{\text{DDRCLR2Q1}}$	Asynchronous Clear-to-Out Out_QR for Input DDR	0.82	ns
$t_{\text{DDRCLR2Q2}}$	Asynchronous Clear-to-Out Out_QF for Input DDR	0.98	ns
$t_{\text{DDRREMCLR}}$	Asynchronous Clear Removal Time for Input DDR	0.00	ns
$t_{\text{DDRRECCLR}}$	Asynchronous Clear Recovery Time for Input DDR	0.23	ns
t_{DDRWCLR}	Asynchronous Clear Minimum Pulse Width for Input DDR	0.19	ns
$t_{\text{DDRICKMPWH}}$	Clock Minimum Pulse Width High for Input DDR	0.31	ns
$t_{\text{DDRICKMPWL}}$	Clock Minimum Pulse Width Low for Input DDR	0.28	ns
F_{DDRIMAX}	Maximum Frequency for Input DDR	250.00	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

1.2 V DC Core Voltage**Table 2-165 • Input DDR Propagation Delays****Commercial-Case Conditions: $T_J = 70^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$**

Parameter	Description	Std.	Units
t_{DDRICKQ1}	Clock-to-Out Out_QR for Input DDR	0.76	ns
t_{DDRICKQ2}	Clock-to-Out Out_QF for Input DDR	0.94	ns
t_{DDRISUD1}	Data Setup for Input DDR (negedge)	0.93	ns
t_{DDRISUD2}	Data Setup for Input DDR (posedge)	0.84	ns
t_{DDRILD1}	Data Hold for Input DDR (negedge)	0.00	ns
t_{DDRILD2}	Data Hold for Input DDR (posedge)	0.00	ns
$t_{\text{DDRICLR2Q1}}$	Asynchronous Clear-to-Out Out_QR for Input DDR	1.23	ns
$t_{\text{DDRICLR2Q2}}$	Asynchronous Clear-to-Out Out_QF for Input DDR	1.42	ns
$t_{\text{DDRIREMCLR}}$	Asynchronous Clear Removal Time for Input DDR	0.00	ns
$t_{\text{DDRIRECCLR}}$	Asynchronous Clear Recovery Time for Input DDR	0.24	ns
t_{DDRIWCLR}	Asynchronous Clear Minimum Pulse Width for Input DDR	0.19	ns
$t_{\text{DDRICKMPWH}}$	Clock Minimum Pulse Width High for Input DDR	0.31	ns
$t_{\text{DDRICKMPWL}}$	Clock Minimum Pulse Width Low for Input DDR	0.28	ns
F_{DDRIMAX}	Maximum Frequency for Input DDR	160.00	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

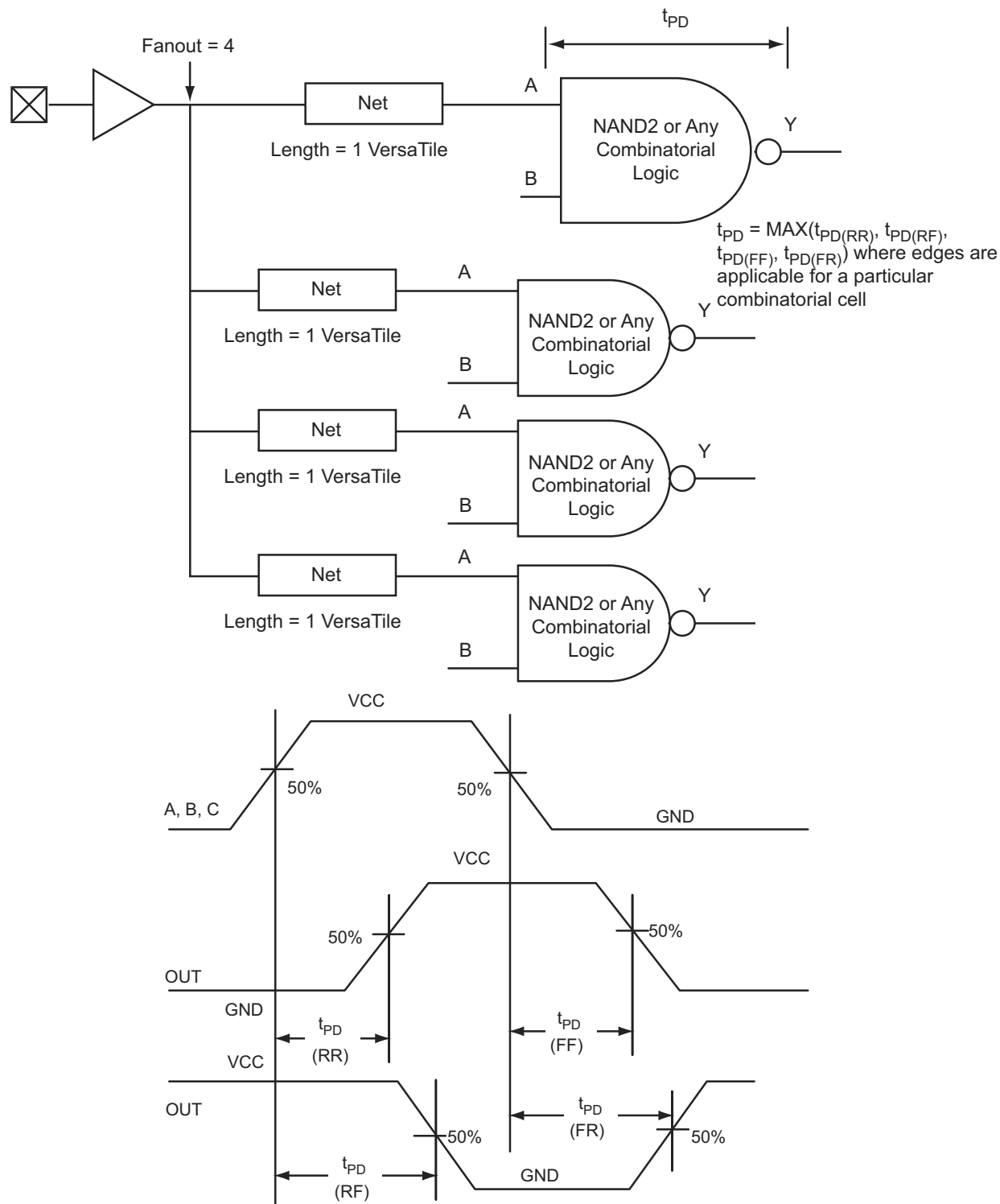


Figure 2-26 • Timing Model and Waveforms

Global Tree Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard-dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to the "Clock Conditioning Circuits" section on page 2-115. Table 2-173 to Table 2-188 on page 2-114 present minimum and maximum global clock delays within each device. Minimum and maximum delays are measured with minimum and maximum loading.

Timing Characteristics

1.5 V DC Core Voltage

Table 2-173 • AGL015 Global Resource

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.		Units
		Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	1.21	1.42	ns
t_{RCKH}	Input High Delay for Global Clock	1.23	1.49	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.18		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.27	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-174 • AGL030 Global Resource

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.		Units
		Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	1.21	1.42	ns
t_{RCKH}	Input High Delay for Global Clock	1.23	1.49	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.18		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.27	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Timing Waveforms

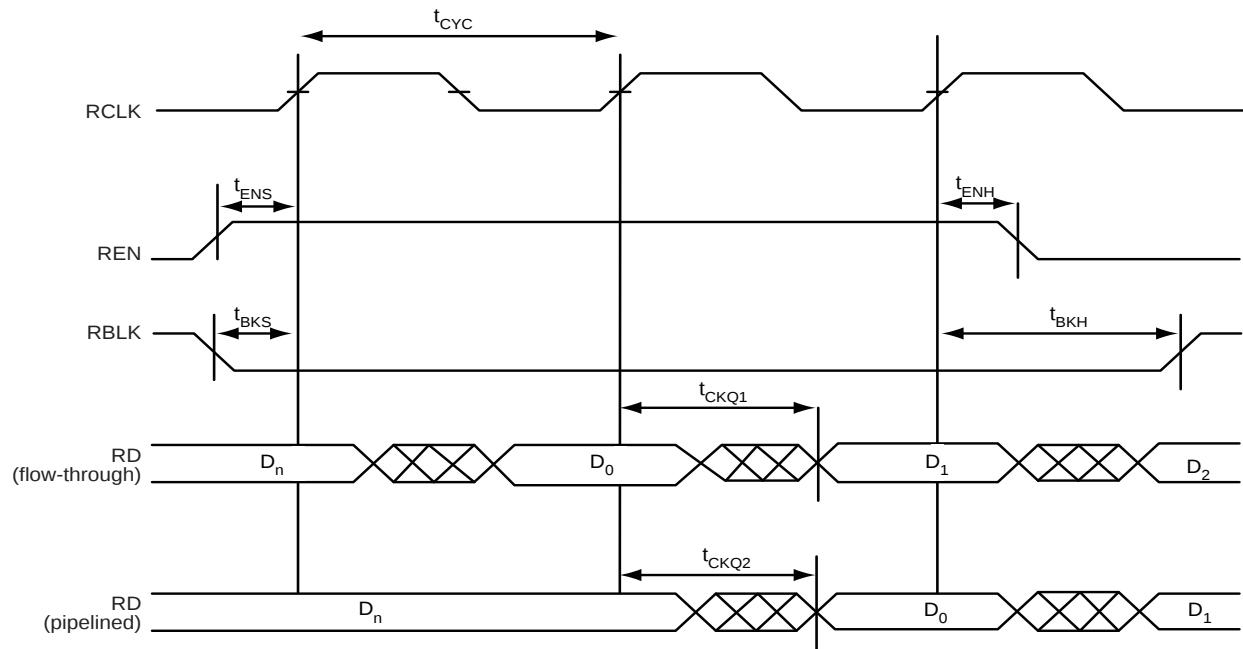


Figure 2-38 • FIFO Read

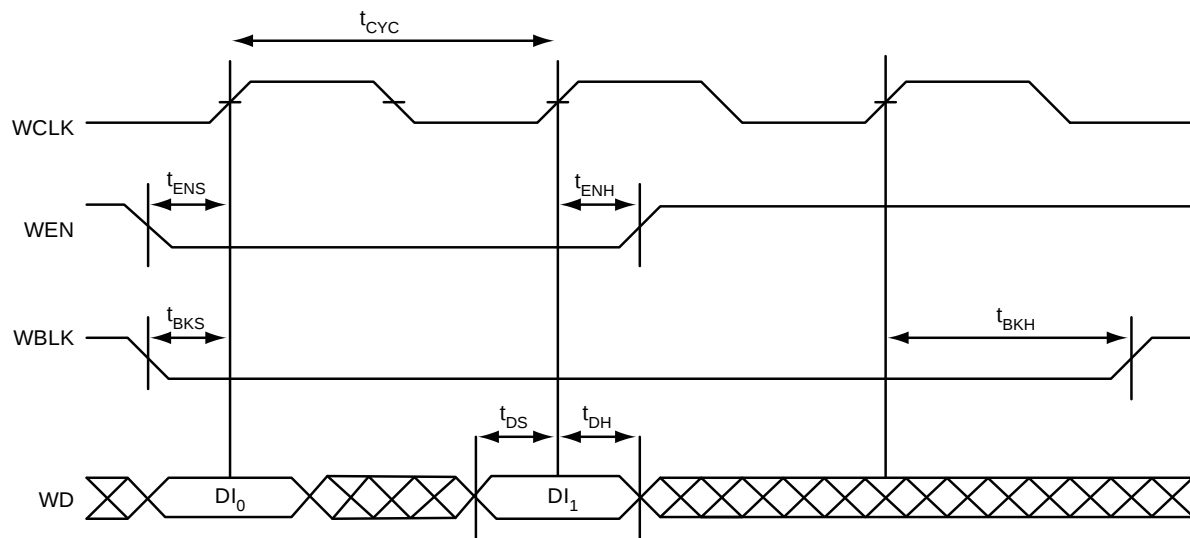
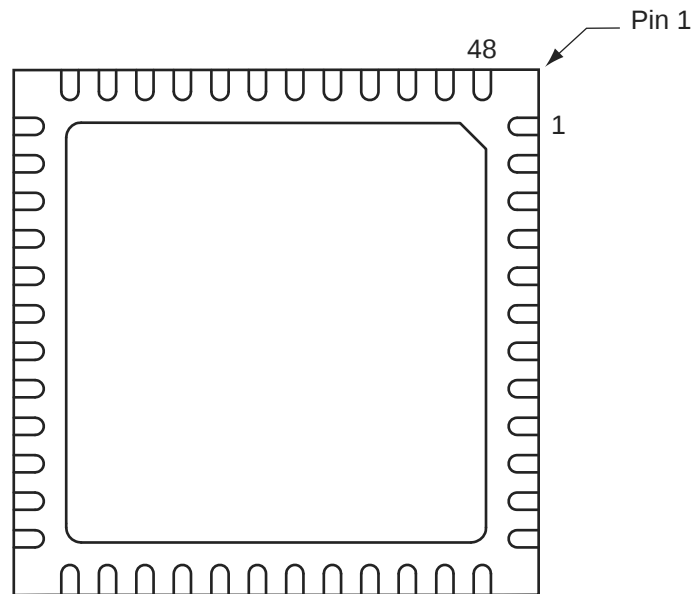


Figure 2-39 • FIFO Write

QN48



Notes:

1. This is the bottom view of the package.
 2. The die attach paddle center of the package is tied to ground (GND).
-

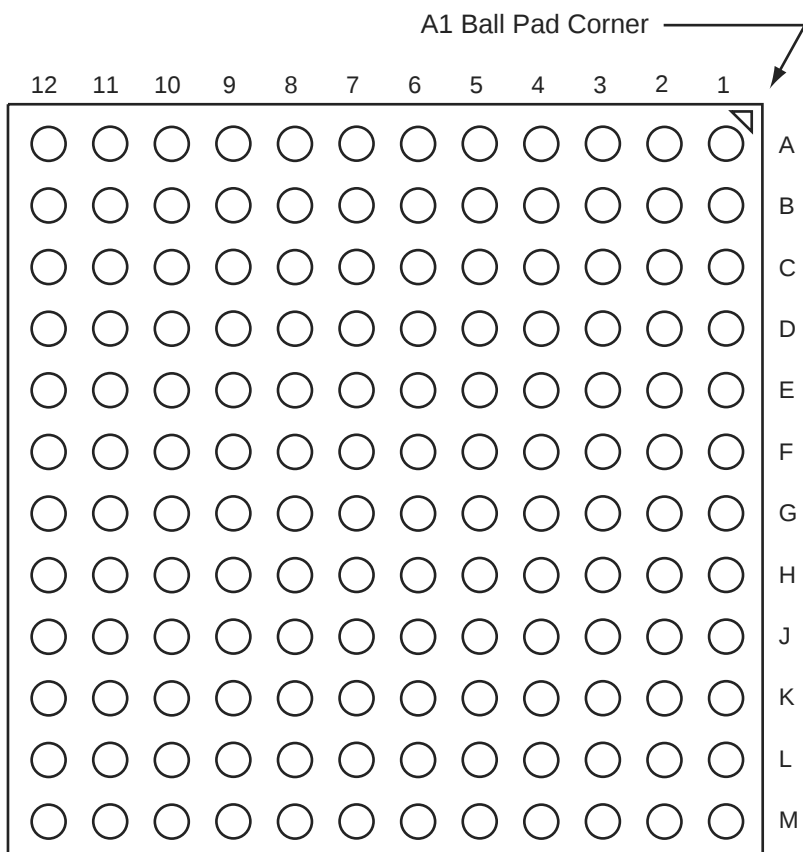
Note

For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

QN68	
Pin Number	AGL030 Function
1	IO82RSB1
2	IO80RSB1
3	IO78RSB1
4	IO76RSB1
5	GEC0/IO73RSB1
6	GEA0/IO72RSB1
7	GEB0/IO71RSB1
8	VCC
9	GND
10	VCCIB1
11	IO68RSB1
12	IO67RSB1
13	IO66RSB1
14	IO65RSB1
15	IO64RSB1
16	IO63RSB1
17	IO62RSB1
18	FF/IO60RSB1
19	IO58RSB1
20	IO56RSB1
21	IO54RSB1
22	IO52RSB1
23	IO51RSB1
24	VCC
25	GND
26	VCCIB1
27	IO50RSB1
28	IO48RSB1
29	IO46RSB1
30	IO44RSB1
31	IO42RSB1
32	TCK
33	TDI
34	TMS
35	VPUMP
36	TDO

QN68	
Pin Number	AGL030 Function
37	TRST
38	VJTAG
39	IO40RSB0
40	IO37RSB0
41	GDB0/IO34RSB0
42	GDA0/IO33RSB0
43	GDC0/IO32RSB0
44	VCCIB0
45	GND
46	VCC
47	IO31RSB0
48	IO29RSB0
49	IO28RSB0
50	IO27RSB0
51	IO25RSB0
52	IO24RSB0
53	IO22RSB0
54	IO21RSB0
55	IO19RSB0
56	IO17RSB0
57	IO15RSB0
58	IO14RSB0
59	VCCIB0
60	GND
61	VCC
62	IO12RSB0
63	IO10RSB0
64	IO08RSB0
65	IO06RSB0
66	IO04RSB0
67	IO02RSB0
68	IO00RSB0

FG144



Note: This is the bottom view of the package.

Note

For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

FG256	
Pin Number	AGL1000 Function
R5	IO168RSB2
R6	IO163RSB2
R7	IO157RSB2
R8	IO149RSB2
R9	IO143RSB2
R10	IO138RSB2
R11	IO131RSB2
R12	IO125RSB2
R13	GDB2/IO115RSB2
R14	TDI
R15	GNDQ
R16	TDO
T1	GND
T2	IO183RSB2
T3	FF/GEB2/IO186RSB2
T4	IO172RSB2
T5	IO170RSB2
T6	IO164RSB2
T7	IO158RSB2
T8	IO153RSB2
T9	IO142RSB2
T10	IO135RSB2
T11	IO130RSB2
T12	GDC2/IO116RSB2
T13	IO120RSB2
T14	GDA2/IO114RSB2
T15	TMS
T16	GND

FG484	
Pin Number	AGL400 Function
B7	NC
B8	NC
B9	NC
B10	NC
B11	NC
B12	NC
B13	NC
B14	NC
B15	NC
B16	NC
B17	NC
B18	NC
B19	NC
B20	NC
B21	VCCIB1
B22	GND
C1	VCCIB3
C2	NC
C3	NC
C4	NC
C5	GND
C6	NC
C7	NC
C8	VCC
C9	VCC
C10	NC
C11	NC
C12	NC
C13	NC
C14	VCC
C15	VCC
C16	NC
C17	NC
C18	GND
C19	NC
C20	NC

FG484	
Pin Number	AGL1000 Function
C21	NC
C22	VCCIB1
D1	IO219PDB3
D2	IO220NDB3
D3	NC
D4	GND
D5	GAA0/IO00RSB0
D6	GAA1/IO01RSB0
D7	GAB0/IO02RSB0
D8	IO16RSB0
D9	IO22RSB0
D10	IO28RSB0
D11	IO35RSB0
D12	IO45RSB0
D13	IO50RSB0
D14	IO55RSB0
D15	IO61RSB0
D16	GBB1/IO75RSB0
D17	GBA0/IO76RSB0
D18	GBA1/IO77RSB0
D19	GND
D20	NC
D21	NC
D22	NC
E1	IO219NDB3
E2	NC
E3	GND
E4	GAB2/IO224PDB3
E5	GAA2/IO225PDB3
E6	GNDQ
E7	GAB1/IO03RSB0
E8	IO17RSB0
E9	IO21RSB0
E10	IO27RSB0
E11	IO34RSB0
E12	IO44RSB0