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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	24576
Total RAM Bits	147456
Number of I/O	300
Number of Gates	1000000
Voltage - Supply	1.14V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/agl1000v2-fgg484

Package Thermal Characteristics

The device junction-to-case thermal resistivity is θ_{jc} and the junction-to-ambient air thermal resistivity is θ_{ja} . The thermal characteristics for θ_{ja} are shown for two air flow rates. The absolute maximum junction temperature is 100°C. EQ 2 shows a sample calculation of the absolute maximum power dissipation allowed for the AGL1000-FG484 package at commercial temperature and in still air.

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja}(\text{°C/W})} = \frac{100^{\circ}\text{C} - 70^{\circ}\text{C}}{23.3^{\circ}\text{C/W}} = 1.28 \text{ W}$$

EQ 2

Table 2-5 • Package Thermal Resistivities

Package Type	Device	Pin Count	θ_{jc}	θ_{ja}			Unit
				Still Air	1 m/s	2.5 m/s	
Quad Flat No Lead (QN)	AGL030	132	13.1	21.4	16.8	15.3	C/W
	AGL060	132	11.0	21.2	16.6	15.0	C/W
	AGL125	132	9.2	21.1	16.5	14.9	C/W
	AGL250	132	8.9	21.0	16.4	14.8	C/W
	AGL030	68	13.4	68.4	45.8	43.1	C/W
Very Thin Quad Flat Pack (VQ)*		100	10.0	35.3	29.4	27.1	C/W
Chip Scale Package (CS)	AGL1000	281	6.0	28.0	22.8	21.5	C/W
	AGL400	196	7.2	37.1	31.1	28.9	C/W
	AGL250	196	7.6	38.3	32.2	30.0	C/W
	AGL125	196	8.0	39.5	33.4	31.1	C/W
	AGL030	81	12.4	32.8	28.5	27.2	C/W
	AGL060	81	11.1	28.8	24.8	23.5	C/W
	AGL250	81	10.4	26.9	22.3	20.9	C/W
Micro Chip Scale Package (UC)	AGL030	81	16.9	40.6	35.2	33.7	C/W
Fine Pitch Ball Grid Array (FG)	AGL060	144	18.6	55.2	49.4	47.2	C/W
	AGL1000	144	6.3	31.6	26.2	24.2	C/W
	AGL400	144	6.8	37.6	31.2	29.0	C/W
	AGL250	256	12.0	38.6	34.7	33.0	C/W
	AGL1000	256	6.6	28.1	24.4	22.7	C/W
	AGL1000	484	8.0	23.3	19.0	16.7	C/W

Note: *Thermal resistances for other device-package combinations will be posted in a later revision.

Disclaimer:

The simulation for determining the junction-to-air thermal resistance is based on JEDEC standards (JESD51) and assumptions made in building the model. Junction-to-case is based on SEMI G38-88. JESD51 is only used for comparing one package to another package, provided the two tests use the same condition. They have little relevance in actual application and therefore should be used with a degree of caution.

Table 2-10 • Quiescent Supply Current (IDD) Characteristics, IGLOO Sleep Mode*

	Core Voltage	AGL015	AGL030	AGL060	AGL125	AGL250	AGL400	AGL600	AGL1000	Units
VCCI/VJTAG = 1.2 V (per bank) Typical (25°C)	1.2 V	1.7	1.7	1.7	1.7	1.7	1.7	1.7	1.7	μA
VCCI/VJTAG = 1.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8	μA
VCCI/VJTAG = 1.8 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.9	1.9	1.9	1.9	1.9	1.9	1.9	1.9	μA
VCCI/VJTAG = 2.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2	μA
VCCI/VJTAG = 3.3 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	μA

Note: $IDD = N_{BANKS} \times ICCI$. Values do not include I/O static contribution, which is shown in Table 2-13 on page 2-10 through Table 2-15 on page 2-11 and Table 2-16 on page 2-11 through Table 2-18 on page 2-12 (PDC6 and PDC7).

Table 2-11 • Quiescent Supply Current (IDD) Characteristics, IGLOO Shutdown Mode

	Core Voltage	AGL015	AGL030	Units
Typical (25°C)	1.2 V / 1.5 V	0	0	μA

Table 2-12 • Quiescent Supply Current (IDD), No IGLOO Flash*Freeze Mode¹

	Core Voltage	AGL015	AGL030	AGL060	AGL125	AGL250	AGL400	AGL600	AGL1000	Units
ICCA Current²										
Typical (25°C)	1.2 V	5	6	10	13	18	25	28	42	μA
	1.5 V	14	16	20	28	44	66	82	137	μA
ICCI or IJTAG Current³										
VCCI/VJTAG = 1.2 V (per bank) Typical (25°C)	1.2 V	1.7	1.7	1.7	1.7	1.7	1.7	1.7	1.7	μA
VCCI/VJTAG = 1.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8	μA
VCCI/VJTAG = 1.8 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.9	1.9	1.9	1.9	1.9	1.9	1.9	1.9	μA
VCCI/VJTAG = 2.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2	μA
VCCI/VJTAG = 3.3 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	μA

Notes:

1. $IDD = N_{BANKS} \times ICCI + ICCA$. JTAG counts as one bank when powered.
2. Includes VCC, VPUMP, and VCCPLL currents.
3. Values do not include I/O static contribution (PDC6 and PDC7).

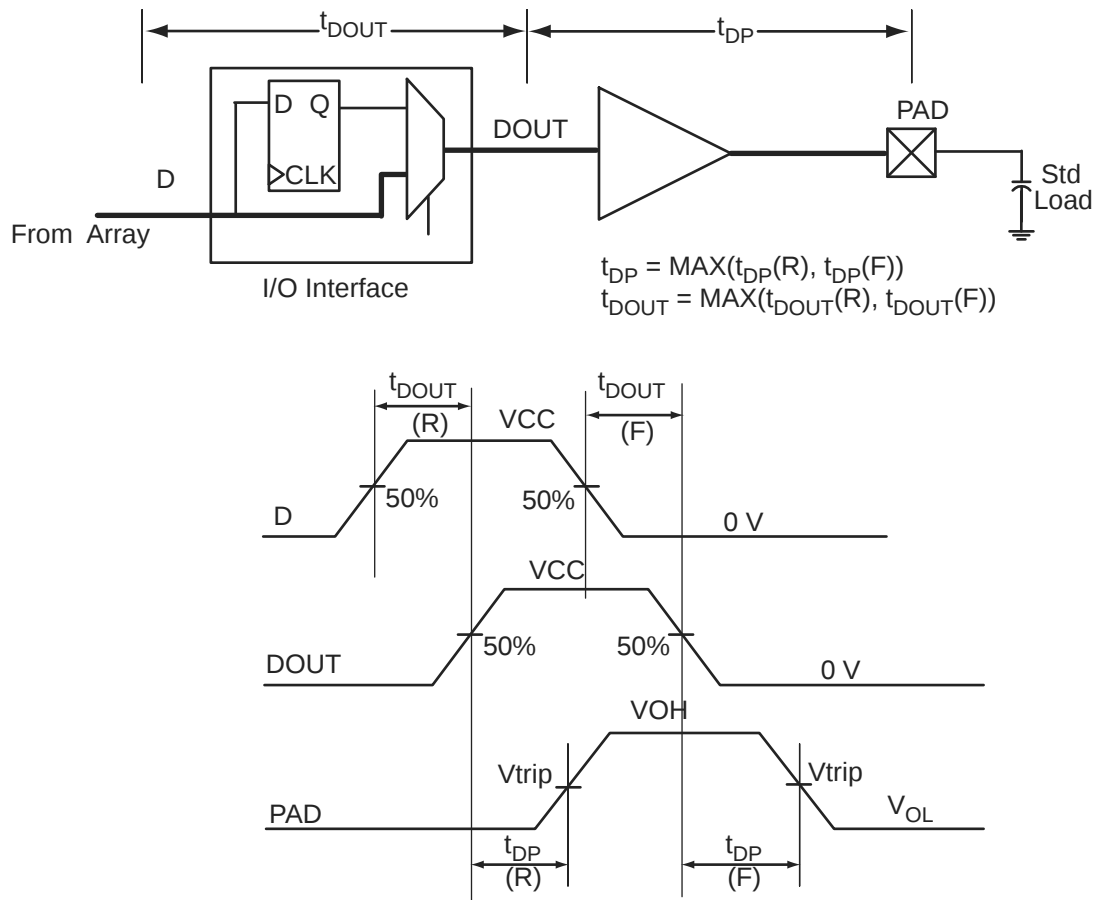


Figure 2-5 • Output Buffer Model and Delays (example)

Table 2-31 • Summary of I/O Timing Characteristics—Software Default Settings, Std. Speed Grade, Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case V_{CCI} (per standard)
Applicable to Advanced I/O Banks

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength Option ¹ (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTTL / 3.3 V LVCMOS	12 mA	12	High	5	–	0.97	2.09	0.18	0.85	0.66	2.14	1.68	2.67	3.05	5.73	5.27	ns
3.3 V LVCMOS Wide Range ²	100 μA	12	High	5	–	0.97	2.93	0.18	1.19	0.66	2.95	2.27	3.81	4.30	6.54	5.87	ns
2.5 V LVCMOS	12 mA	12	High	5	–	0.97	2.09	0.18	1.08	0.66	2.14	1.83	2.73	2.93	5.73	5.43	ns
1.8 V LVCMOS	12 mA	12	High	5	–	0.97	2.24	0.18	1.01	0.66	2.29	2.00	3.02	3.40	5.88	5.60	ns
1.5 V LVCMOS	12 mA	12	High	5	–	0.97	2.50	0.18	1.17	0.66	2.56	2.27	3.21	3.48	6.15	5.86	ns
3.3 V PCI	Per PCI spec	–	High	10	25 ²	0.97	2.32	0.18	0.74	0.66	2.37	1.78	2.67	3.05	5.96	5.38	ns
3.3 V PCI-X	Per PCI-X spec	–	High	10	25 ²	0.97	2.32	0.19	0.70	0.66	2.37	1.78	2.67	3.05	5.96	5.38	ns
LVDS	24 mA	–	High	–	–	0.97	1.74	0.19	1.35	–	–	–	–	–	–	–	ns
LVPECL	24 mA	–	High	–	–	0.97	1.68	0.19	1.16	–	–	–	–	–	–	–	ns

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is $\pm 100\text{ }\mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.
3. Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-12 on page 2-79 for connectivity. This resistor is not required during normal operation.
4. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-34 • Summary of I/O Timing Characteristics—Software Default Settings, Std. Speed Grade, Commercial-Case
Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$, Worst-Case V_{CCI} (per standard)
Applicable to Advanced I/O Banks

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength Option ¹	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{BOUT} (ns)	t_{BP} (ns)	t_{BIN} (ns)	t_{BY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTTL / 3.3 V LVCMOS	12 mA	12 mA	High	5	—	1.55	2.67	0.26	0.98	1.10	2.71	2.18	3.25	3.93	8.50	7.97	ns
3.3 V LVCMOS Wide Range ²	100 μA	12 mA	High	5	—	1.55	3.73	0.26	1.32	1.10	3.73	2.91	4.51	5.43	9.52	8.69	ns
2.5 V LVCMOS	12 mA	12 mA	High	5	—	1.55	2.64	0.26	1.20	1.10	2.67	2.29	3.30	3.79	8.46	8.08	ns
1.8 V LVCMOS	12 mA	12 mA	High	5	—	1.55	2.72	0.26	1.11	1.10	2.76	2.43	3.58	4.19	8.55	8.22	ns
1.5 V LVCMOS	12 mA	12 mA	High	5	—	1.55	2.96	0.26	1.27	1.10	3.00	2.70	3.75	4.23	8.78	8.48	ns
1.2 V LVCMOS	2 mA	2 mA	High	5	—	1.55	3.60	0.26	1.60	1.10	3.47	3.36	3.93	3.65	9.26	9.14	ns
1.2 V LVCMOS Wide Range ³	100 μA	2 mA	High	5	—	1.55	3.60	0.26	1.60	1.10	3.47	3.36	3.93	3.65	9.26	9.14	ns
3.3 V PCI	Per PCI spec	—	High	10	25 ²	1.55	2.91	0.26	0.86	1.10	2.95	2.29	3.25	3.93	8.74	8.08	ns
3.3 V PCI-X	Per PCI-X spec	—	High	10	25 ²	1.55	2.91	0.25	0.86	1.10	2.95	2.29	3.25	3.93	8.74	8.08	ns
LVDS	24 mA	—	High	—	—	1.55	2.27	0.25	1.57	—	—	—	—	—	—	—	ns
LVPECL	24 mA	—	High	—	—	1.55	2.24	0.25	1.38	—	—	—	—	—	—	—	ns

Notes:

1. The minimum drive strength for any LVCMOS 1.2 V or LVCMOS 3.3 V software configuration when run in wide range is $\pm 100\text{ }\mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.
3. All LVCMOS 1.2 V software macros support LVCMOS 1.2 V wide range as specified in the JESD8-12 specification
4. Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-12 on page 2-79 for connectivity. This resistor is not required during normal operation.
5. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-40 • I/O Output Buffer Maximum Resistances¹
Applicable to Standard I/O Banks

Standard	Drive Strength	$R_{PULL-DOWN}$ (Ω) ²	$R_{PULL-UP}$ (Ω) ³
3.3 V LVTTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
3.3 V LVCMOS Wide Range	100 μ A	Same as regular 3.3 V LVCMOS	Same as regular 3.3 V LVCMOS
2.5 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
1.5 V LVCMOS	2 mA	200	224
1.2 V LVCMOS	1 mA	158	164
1.2 V LVCMOS Wide Range ⁴	100 μ A	Same as regular 1.2 V LVCMOS	Same as regular 1.2 V LVCMOS

Notes:

1. These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCI, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located at <http://www.microsemi.com/soc/download/ibis/default.aspx>.
2. $R_{(PULL-DOWN-MAX)} = (VOL_{spec}) / I_{OL_{spec}}$
3. $R_{(PULL-UP-MAX)} = (VCCImax - VOH_{spec}) / I_{OH_{spec}}$

Table 2-41 • I/O Weak Pull-Up/Pull-Down Resistances
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values

VCCI	$R_{(WEAK PULL-UP)}$ ¹ (Ω)		$R_{(WEAK PULL-DOWN)}$ ² (Ω)	
	Min.	Max.	Min.	Max.
3.3 V	10 K	45 K	10 K	45 K
3.3 V Wide Range I/Os	10 K	45 K	10 K	45 K
2.5 V	11 K	55 K	12 K	74 K
1.8 V	18 K	70 K	17 K	110 K
1.5 V	19 K	90 K	19 K	140 K
1.2 V	25 K	110 K	25 K	150 K
1.2 V Wide Range I/Os	19 K	110 K	19 K	150 K

Notes:

1. $R_{(WEAK PULL-UP-MAX)} = (VCCImax - VOH_{spec}) / I_{(WEAK PULL-UP-MIN)}$
2. $R_{(WEAK PULLDOWN-MAX)} = (VOL_{spec}) / I_{(WEAK PULLDOWN-MIN)}$

Table 2-60 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	2.89	0.26	0.97	1.10	2.93	2.38	2.53	2.96	8.72	8.17	ns
4 mA	Std.	1.55	2.89	0.26	0.97	1.10	2.93	2.38	2.53	2.96	8.72	8.17	ns
6 mA	Std.	1.55	2.50	0.26	0.97	1.10	2.54	2.04	2.77	3.37	8.33	7.82	ns
8 mA	Std.	1.55	2.50	0.26	0.97	1.10	2.54	2.04	2.77	3.37	8.33	7.82	ns
12 mA	Std.	1.55	2.31	0.26	0.97	1.10	2.34	1.86	2.93	3.64	8.12	7.65	ns
16 mA	Std.	1.55	2.31	0.26	0.97	1.10	2.34	1.86	2.93	3.64	8.12	7.65	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-61 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	1.55	4.39	0.26	0.94	1.10	4.46	3.91	2.17	2.44	ns
4 mA	Std.	1.55	4.39	0.26	0.94	1.10	4.46	3.91	2.17	2.44	ns
6 mA	Std.	1.55	3.72	0.26	0.94	1.10	3.78	3.43	2.40	2.85	ns
8 mA	Std.	1.55	3.72	0.26	0.94	1.10	3.78	3.43	2.40	2.85	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-62 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	1.55	2.74	0.26	0.94	1.10	2.78	2.26	2.17	2.55	ns
4 mA	Std.	1.55	2.74	0.26	0.94	1.10	2.78	2.26	2.17	2.55	ns
6 mA	Std.	1.55	2.38	0.26	0.94	1.10	2.41	1.92	2.40	2.96	ns
8 mA	Std.	1.55	2.38	0.26	0.94	1.10	2.41	1.92	2.40	2.96	ns

Notes:

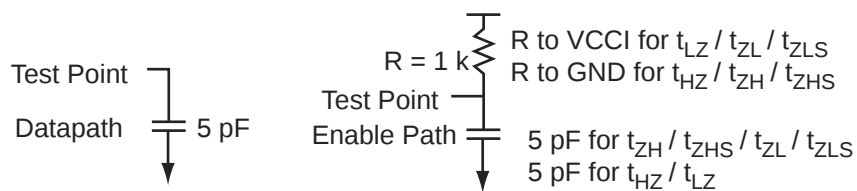
1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-81 • Minimum and Maximum DC Input and Output Levels
Applicable to Standard I/O Banks

2.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	−0.3	0.7	1.7	3.6	0.7	1.7	2	2	16	18	10	10
4 mA	−0.3	0.7	1.7	3.6	0.7	1.7	4	4	16	18	10	10
6 mA	−0.3	0.7	1.7	3.6	0.7	1.7	6	6	32	37	10	10
8 mA	−0.3	0.7	1.7	3.6	0.7	1.7	8	8	32	37	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

**Figure 2-8 • AC Loading****Table 2-82 • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	C _{LOAD} (pF)
0	2.5	1.2	5

Note: *Measuring point = Vtrip. See Table 2-29 on page 2-28 for a complete table of trip points.

1.2 V DC Core Voltage**Table 2-162 • Output Enable Register Propagation Delays****Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$**

Parameter	Description	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	1.10	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	1.15	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	ns
t_{OESUE}	Enable Setup Time for the Output Enable Register	1.22	ns
t_{OEHE}	Enable Hold Time for the Output Enable Register	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	1.65	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	1.65	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	ns
$t_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.24	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	ns
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.24	ns
$t_{OEWCCLR}$	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.19	ns
$t_{OEWPRES}$	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.19	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width High for the Output Enable Register	0.31	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width Low for the Output Enable Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

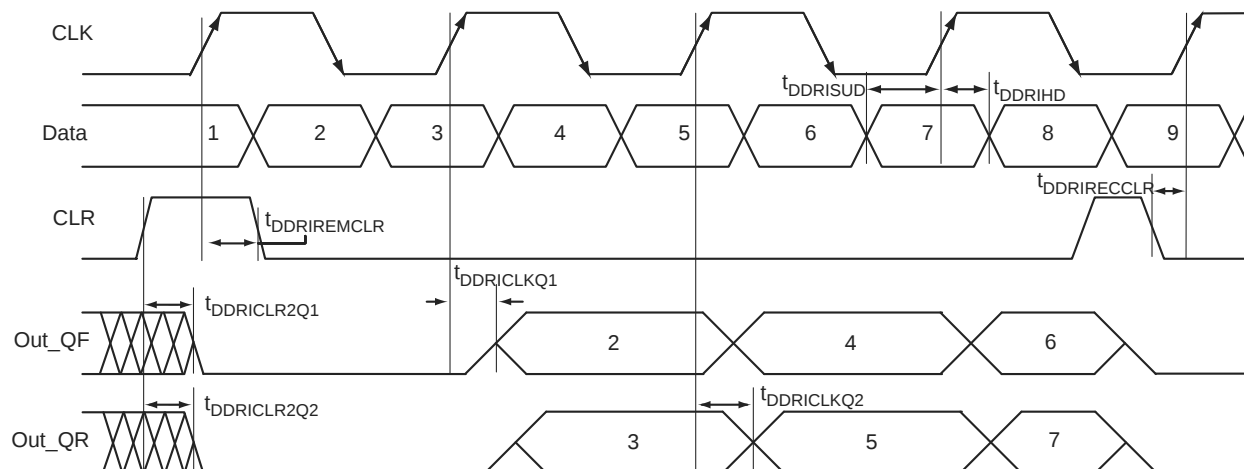


Figure 2-22 • Input DDR Timing Diagram

Timing Characteristics

1.5 V DC Core Voltage

Table 2-164 • Input DDR Propagation Delays

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.	Units
t_{DDRCLKQ1}	Clock-to-Out Out_QR for Input DDR	0.48	ns
t_{DDRCLKQ2}	Clock-to-Out Out_QF for Input DDR	0.65	ns
t_{DDRISUD1}	Data Setup for Input DDR (negedge)	0.50	ns
t_{DDRISUD2}	Data Setup for Input DDR (posedge)	0.40	ns
t_{DDRHD1}	Data Hold for Input DDR (negedge)	0.00	ns
t_{DDRHD2}	Data Hold for Input DDR (posedge)	0.00	ns
$t_{\text{DDRCLR2Q1}}$	Asynchronous Clear-to-Out Out_QR for Input DDR	0.82	ns
$t_{\text{DDRCLR2Q2}}$	Asynchronous Clear-to-Out Out_QF for Input DDR	0.98	ns
$t_{\text{DDRREMCLR}}$	Asynchronous Clear Removal Time for Input DDR	0.00	ns
$t_{\text{DDRRECCLR}}$	Asynchronous Clear Recovery Time for Input DDR	0.23	ns
t_{DDRWCLR}	Asynchronous Clear Minimum Pulse Width for Input DDR	0.19	ns
$t_{\text{DDRICKMPWH}}$	Clock Minimum Pulse Width High for Input DDR	0.31	ns
$t_{\text{DDRICKMPWL}}$	Clock Minimum Pulse Width Low for Input DDR	0.28	ns
F_{DDRIMAX}	Maximum Frequency for Input DDR	250.00	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

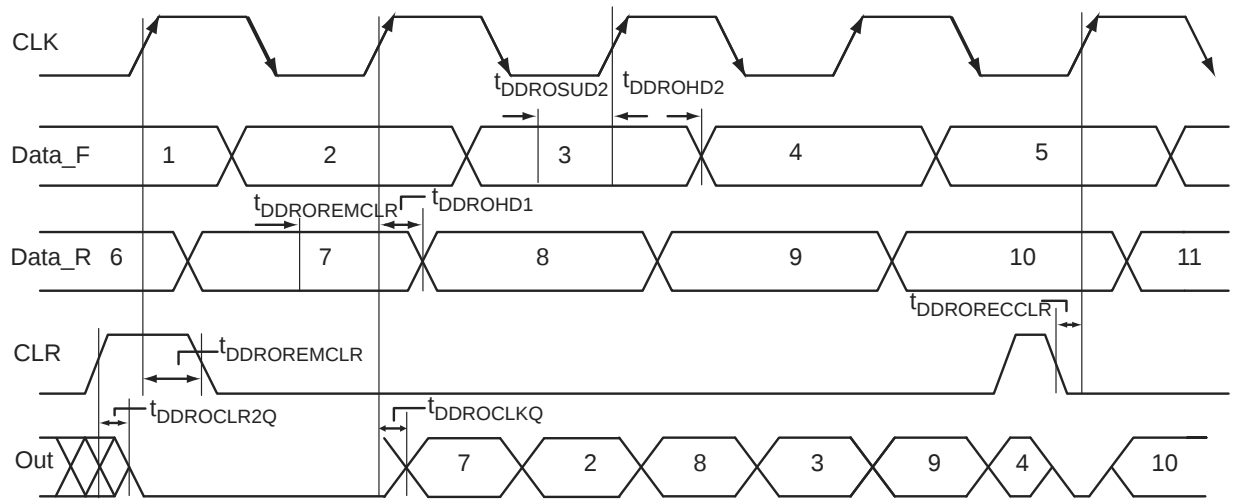


Figure 2-24 • Output DDR Timing Diagram

Timing Characteristics

1.5 V DC Core Voltage

Table 2-167 • Output DDR Propagation Delays

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.	Units
t_{DDROCLKQ}	Clock-to-Out of DDR for Output DDR	1.07	ns
t_{DDROSUD1}	Data_F Data Setup for Output DDR	0.67	ns
t_{DDROSUD2}	Data_R Data Setup for Output DDR	0.67	ns
t_{DDROHD1}	Data_F Data Hold for Output DDR	0.00	ns
t_{DDROHD2}	Data_R Data Hold for Output DDR	0.00	ns
$t_{\text{DDROCLR2Q}}$	Asynchronous Clear-to-Out for Output DDR	1.38	ns
$t_{\text{DDROEMCLR}}$	Asynchronous Clear Removal Time for Output DDR	0.00	ns
$t_{\text{DDROECCLR}}$	Asynchronous Clear Recovery Time for Output DDR	0.23	ns
$t_{\text{DDROWCLR1}}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.19	ns
$t_{\text{DDROCKMPWH}}$	Clock Minimum Pulse Width High for the Output DDR	0.31	ns
$t_{\text{DDROCKMPWL}}$	Clock Minimum Pulse Width Low for the Output DDR	0.28	ns
F_{DDOMAX}	Maximum Frequency for the Output DDR	250.00	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-187 • AGL600 Global Resource**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.14\text{ V}$**

Parameter	Description	Std.		Units
		Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	2.22	2.67	ns
t_{RCKH}	Input High Delay for Global Clock	2.32	2.93	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.61	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-188 • AGL1000 Global Resource**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.14\text{ V}$**

Parameter	Description	Std.		Units
		Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	2.31	2.76	ns
t_{RCKH}	Input High Delay for Global Clock	2.42	3.03	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.61	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

QN68	
Pin Number	AGL015 Function
1	IO82RSB1
2	IO80RSB1
3	IO78RSB1
4	IO76RSB1
5	GEC0/IO73RSB1
6	GEA0/IO72RSB1
7	GEB0/IO71RSB1
8	VCC
9	GND
10	VCCIB1
11	IO68RSB1
12	IO67RSB1
13	IO66RSB1
14	IO65RSB1
15	IO64RSB1
16	IO63RSB1
17	IO62RSB1
18	FF/IO60RSB1
19	IO58RSB1
20	IO56RSB1
21	IO54RSB1
22	IO52RSB1
23	IO51RSB1
24	VCC
25	GND
26	VCCIB1
27	IO50RSB1
28	IO48RSB1
29	IO46RSB1
30	IO44RSB1
31	IO42RSB1
32	TCK
33	TDI
34	TMS
35	VPUMP
36	TDO

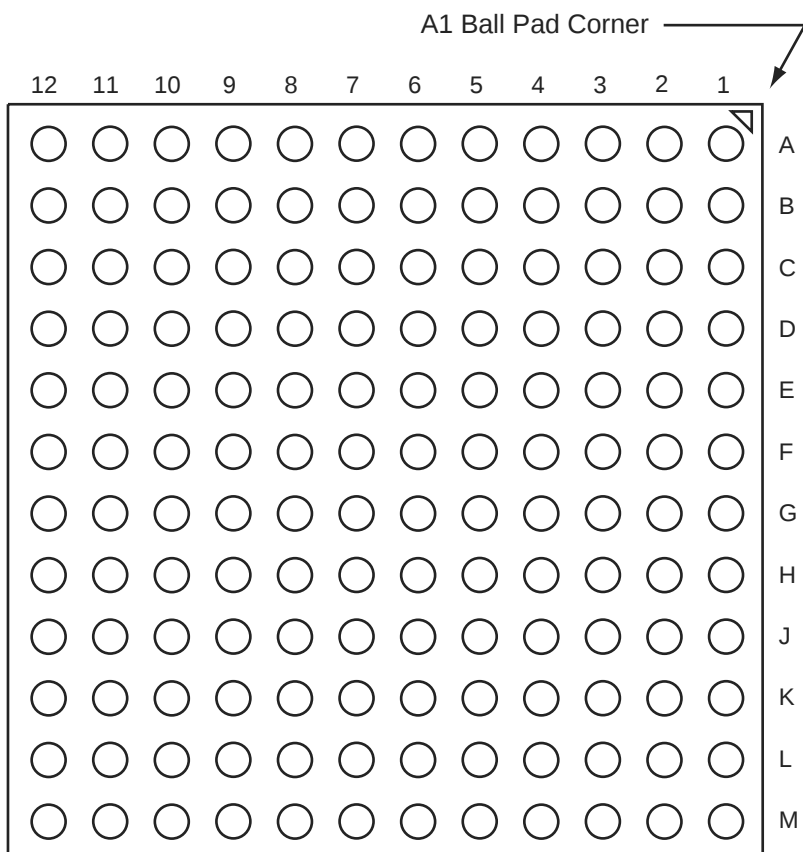
QN68	
Pin Number	AGL015 Function
37	TRST
38	VJTAG
39	IO40RSB0
40	IO37RSB0
41	GDB0/IO34RSB0
42	GDA0/IO33RSB0
43	GDC0/IO32RSB0
44	VCCIB0
45	GND
46	VCC
47	IO31RSB0
48	IO29RSB0
49	IO28RSB0
50	IO27RSB0
51	IO25RSB0
52	IO24RSB0
53	IO22RSB0
54	IO21RSB0
55	IO19RSB0
56	IO17RSB0
57	IO15RSB0
58	IO14RSB0
59	VCCIB0
60	GND
61	VCC
62	IO12RSB0
63	IO10RSB0
64	IO08RSB0
65	IO06RSB0
66	IO04RSB0
67	IO02RSB0
68	IO00RSB0

VQ100	
Pin Number	AGL250 Function
1	GND
2	GAA2/IO118UDB3
3	IO118VDB3
4	GAB2/IO117UDB3
5	IO117VDB3
6	GAC2/IO116UDB3
7	IO116VDB3
8	IO112PSB3
9	GND
10	GFB1/IO109PDB3
11	GFB0/IO109NDB3
12	VCOMPLF
13	GFA0/IO108NPB3
14	VCCPLF
15	GFA1/IO108PPB3
16	GFA2/IO107PSB3
17	VCC
18	VCCIB3
19	GFC2/IO105PSB3
20	GEC1/IO100PDB3
21	GEC0/IO100NDB3
22	GEA1/IO98PDB3
23	GEA0/IO98NDB3
24	VMV3
25	GNDQ
26	GEA2/IO97RSB2
27	FF/GE2/IO96RSB2
28	GEC2/IO95RSB2
29	IO93RSB2
30	IO92RSB2
31	IO91RSB2
32	IO90RSB2
33	IO88RSB2
34	IO86RSB2
35	IO85RSB2
36	IO84RSB2

VQ100	
Pin Number	AGL250 Function
37	VCC
38	GND
39	VCCIB2
40	IO77RSB2
41	IO74RSB2
42	IO71RSB2
43	GDC2/IO63RSB2
44	GDB2/IO62RSB2
45	GDA2/IO61RSB2
46	GNDQ
47	TCK
48	TDI
49	TMS
50	VMV2
51	GND
52	VPUMP
53	NC
54	TDO
55	TRST
56	VJTAG
57	GDA1/IO60USB1
58	GDC0/IO58VDB1
59	GDC1/IO58UDB1
60	IO52NDB1
61	GCB2/IO52PDB1
62	GCA1/IO50PDB1
63	GCA0/IO50NDB1
64	GCC0/IO48NDB1
65	GCC1/IO48PDB1
66	VCCIB1
67	GND
68	VCC
69	IO43NDB1
70	GBC2/IO43PDB1
71	GGB2/IO42PSB1
72	IO41NDB1

VQ100	
Pin Number	AGL250 Function
73	GBA2/IO41PDB1
74	VMV1
75	GNDQ
76	GBA1/IO40RSB0
77	GBA0/IO39RSB0
78	GGB1/IO38RSB0
79	GGB0/IO37RSB0
80	GBC1/IO36RSB0
81	GBC0/IO35RSB0
82	IO29RSB0
83	IO27RSB0
84	IO25RSB0
85	IO23RSB0
86	IO21RSB0
87	VCCIB0
88	GND
89	VCC
90	IO15RSB0
91	IO13RSB0
92	IO11RSB0
93	GAC1/IO05RSB0
94	GAC0/IO04RSB0
95	GAB1/IO03RSB0
96	GAB0/IO02RSB0
97	GAA1/IO01RSB0
98	GAA0/IO00RSB0
99	GNDQ
100	VMV0

FG144



Note: This is the bottom view of the package.

Note

For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

FG484	
Pin Number	AGL400 Function
M3	NC
M4	GFA2/IO144PPB3
M5	GFA1/IO145PDB3
M6	VCCPLF
M7	IO143NDB3
M8	GFB2/IO143PDB3
M9	VCC
M10	GND
M11	GND
M12	GND
M13	GND
M14	VCC
M15	GCB2/IO71PPB1
M16	GCA1/IO69PPB1
M17	GCC2/IO72PPB1
M18	NC
M19	GCA2/IO70PDB1
M20	NC
M21	NC
M22	NC
N1	NC
N2	NC
N3	NC
N4	GFC2/IO142PDB3
N5	IO144NPB3
N6	IO141PPB3
N7	IO120RSB2
N8	VCCIB3
N9	VCC
N10	GND
N11	GND
N12	GND
N13	GND
N14	VCC
N15	VCCIB1
N16	IO71NPB1

FG484	
Pin Number	AGL600 Function
H19	IO66PDB1
H20	VCC
H21	NC
H22	NC
J1	NC
J2	NC
J3	NC
J4	IO166NDB3
J5	IO168NPB3
J6	IO167PPB3
J7	IO169PDB3
J8	VCCIB3
J9	GND
J10	VCC
J11	VCC
J12	VCC
J13	VCC
J14	GND
J15	VCCIB1
J16	IO62NDB1
J17	IO64NPB1
J18	IO65PPB1
J19	IO66NDB1
J20	NC
J21	IO68PDB1
J22	IO68NDB1
K1	IO157PDB3
K2	IO157NDB3
K3	NC
K4	IO165NDB3
K5	IO165PDB3
K6	IO168PPB3
K7	GFC1/IO164PPB3
K8	VCCIB3
K9	VCC
K10	GND

FG484	
Pin Number	AGL600 Function
Y7	NC
Y8	VCC
Y9	VCC
Y10	NC
Y11	NC
Y12	NC
Y13	NC
Y14	VCC
Y15	VCC
Y16	NC
Y17	NC
Y18	GND
Y19	NC
Y20	NC
Y21	NC
Y22	VCCIB1

5 – Datasheet Information

List of Changes

The following tables list critical changes that were made in each revision of the IGLOO datasheet.

Revision	Changes	Page
Revision 27 (May 2016)	Added the deleted package FG144 from AGL125 device in "IGLOO Devices" (SAR 79355).	1-I
Revision 26 (March 2016)	Updated "IGLOO Ordering Information" and "Temperature Grade Offerings" notes by: - Replacing Commercial (0°C to +70°C Ambient Temperature) with Commercial (0°C to +85°C Junction Temperature) (SAR 48352). - Replacing Industrial (-40°C to +85°C Ambient Temperature) with Industrial (-40°C to +100°C Junction Temperature) (SAR 48352).	1-III and 1-IV
	Ambient temperature row removed in Table 2-2 (SAR 48352).	2-2
	Updated Table 2-2 note 2 from "To ensure targeted reliability standards are met across ambient and junction operating temperatures, Microsemi recommends that the user follow best design practices using Microsemi's timing and power simulation tools." to "Software Default Junction Temperature Range in the Libero SoC software is set to 0°C to +70°C for commercial, and -40°C to +85°C for industrial. To ensure targeted reliability standards are met across the full range of junction temperatures, Microsemi recommends using custom settings for temperature range before running timing and power analysis tools. For more information on custom settings, refer to the New Project Dialog Box in the Libero SoC Online Help." (SAR 77087).	2-2
	Updated Table 2-2 note 9 from "VMV pins must be connected to the corresponding VCCI pins. See the "Pin Descriptions" chapter of the IGLOO FPGA Fabric User Guide for further information." to "VMV and VCCI must be at the same voltage within a given I/O bank. VMV pins must be connected to the corresponding VCCI pins. See the "VMVx I/O Supply Voltage (quiet)" on page 3-1 for further information." (SAR 77087)	2-2
	Added 2 mA drive strengths in tables same as 4 mA (SAR 57179).	NA
	Added reference of Package Mechanical Drawings document in all package pin assignment notes (76777).	NA
Revision 25 (June 2015)	Removed package FG144 from AGL060 device in the following tables: "IGLOO Devices", "I/Os Per Package1" and "Temperature Grade Offerings" (SAR 68517)	I, II, and IV
	Removed Package Pin Assignment table of AGL060 device from FG144.(SAR 68517)	-
Revision 24 (March 2014)	Note added for the discontinuance of QN132 package to the following tables: "IGLOO Devices", "I/Os Per Package1", "IGLOO FPGAs Package Sizes Dimensions", and "Temperature Grade Offerings" and "QN132" section (SAR 55117, PDN 1306).	I, II, IV, and 4-28
	Removed packages CS81 and QN132 from AGL250 device in the following tables: "IGLOO Devices", "I/Os Per Package1", and "Temperature Grade Offerings" (SAR 49472).	I, II, and IV

Revision / Version	Changes	Page
Revision 18 (Nov 2009)	The version changed to v2.0 for IGLOO datasheet chapters, indicating the datasheet contains information based on final characterization. Please review the datasheet carefully as most tables were updated with new data.	N/A
Revision 17 (Sep 2009) Product Brief v1.6	The "Reprogrammable Flash Technology" section was modified to add "250 MHz (1.5 V systems) and 160 MHz (1.2 V systems) System Performance."	I
	"IGLOO Ordering Information" was revised to note that halogen-free packages are available with RoHS-compliant packaging.	III
	Table 1-1 • I/O Standards Supported is new.	1-7
	The definitions of hot-swap and cold-sparing were added to the "I/Os with Advanced I/O Standards" section.	1-7
Revision 16 (Apr 2009) Product Brief v1.5	M1AGL400 is no longer offered and was removed from the "IGLOO Devices" product table, "IGLOO Ordering Information", and "Temperature Grade Offerings".	I, III, IV
	The –F speed grade is no longer offered for IGLOO devices. The speed grade column and note regarding –F speed grade were removed from "IGLOO Ordering Information". The "Speed Grade and Temperature Grade Matrix" section was removed.	III, IV
	This datasheet now has fully characterized data and has moved from being Advance to a Production version. The version number changed from Advance v0.5 to v2.0. Please review the datasheet carefully as most tables were updated with new data.	N/A
DC and Switching Characteristics Advance v0.6	3.3 V LVCMOS and 1.2 V LVCMOS Wide Range support was added to the datasheet. This affects all tables that contained 3.3 V LVCMOS and 1.2 V LVCMOS data.	
	I_{IL} and I_{IH} input leakage current information was added to all "Minimum and Maximum DC Input and Output Levels" tables.	N/A
	–F was removed from the datasheet. The speed grade is no longer supported.	N/A
	The notes in Table 2-2 • Recommended Operating Conditions 1 were updated.	2-2
	Table 2-4 • Overshoot and Undershoot Limits 1 was updated.	2-3
	Table 2-5 • Package Thermal Resistivities was updated.	2-6
	Table 2-6 • Temperature and Voltage Derating Factors for Timing Delays (normalized to $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$) and Table 2-7 • Temperature and Voltage Derating Factors for Timing Delays (normalized to $T_J = 70^\circ\text{C}$, $V_{CC} = 1.14\text{ V}$) were updated.	2-7
	In Table 2-191 • RAM4K9 and Table 2-193 • RAM4K9, the following specifications were removed: t_{WRO} t_{CCKH}	2-122 and 2-124
	In Table 2-192 • RAM512X18 and Table 2-194 • RAM512X18, the following specifications were removed: t_{WRO} t_{CCKH}	2-123 and 2-125
Revision 15 (Feb 2009) Packaging v1.9	The "QN132" pin table for the AGL060 device is new.	4-31