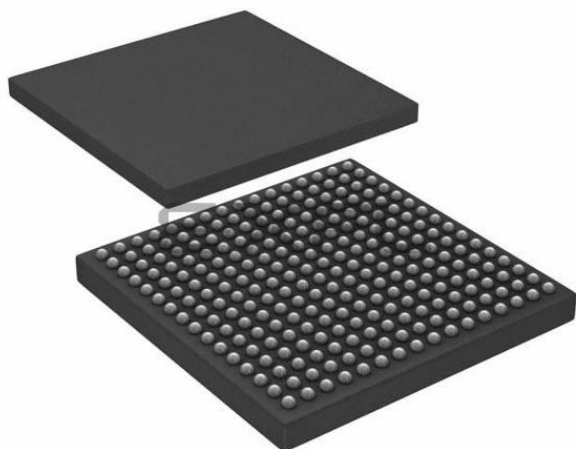




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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	24576
Total RAM Bits	147456
Number of I/O	177
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/agl1000v5-fg256

Temperature and Voltage Derating Factors

Table 2-6 • Temperature and Voltage Derating Factors for Timing Delays (normalized to $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$)
For IGLOO V2 or V5 devices, 1.5 V DC Core Supply Voltage

Array Voltage VCC (V)	Junction Temperature ($^\circ\text{C}$)					
	-40°C	0°C	25°C	70°C	85°C	100°C
1.425	0.934	0.953	0.971	1.000	1.007	1.013
1.500	0.855	0.874	0.891	0.917	0.924	0.929
1.575	0.799	0.816	0.832	0.857	0.864	0.868

Table 2-7 • Temperature and Voltage Derating Factors for Timing Delays (normalized to $T_J = 70^\circ\text{C}$, $V_{CC} = 1.14\text{ V}$)
For IGLOO V2, 1.2 V DC Core Supply Voltage

Array Voltage VCC (V)	Junction Temperature ($^\circ\text{C}$)					
	-40°C	0°C	25°C	70°C	85°C	100°C
1.14	0.967	0.978	0.991	1.000	1.006	1.010
1.20	0.864	0.874	0.885	0.894	0.899	0.902
1.26	0.794	0.803	0.814	0.821	0.827	0.830

Calculating Power Dissipation

Quiescent Supply Current

Quiescent supply current (I_{DD}) calculation depends on multiple factors, including operating voltages (V_{CC} , V_{CCI} , and V_{JTAG}), operating temperature, system clock frequency, and power modes usage. Microsemi recommends using the PowerCalculator and SmartPower software estimation tools to evaluate the projected static and active power based on the user design, power mode usage, operating voltage, and temperature.

Table 2-8 • Power Supply State per Mode

Modes/power supplies	Power Supply Configurations				
	VCC	VCCPLL	VCCI	VJTAG	VPUMP
Flash*Freeze	On	On	On	On	On/off/floating
Sleep	Off	Off	On	Off	Off
Shutdown	Off	Off	Off	Off	Off
No Flash*Freeze	On	On	On	On	On/off/floating

Note: Off: Power supply level = 0 V

Table 2-9 • Quiescent Supply Current (I_{DD}) Characteristics, IGLOO Flash*Freeze Mode*

	Core Voltage	AGL015	AGL030	AGL060	AGL125	AGL250	AGL400	AGL600	AGL1000	Units
Typical (25°C)	1.2 V	4	4	8	13	20	27	30	44	μA
	1.5 V	6	6	10	18	34	51	72	127	μA

Note: * I_{DD} includes VCC, VPUMP, VCCI, VCCPLL, and VMV currents. Values do not include I/O static contribution, which is shown in Table 2-13 on page 2-10 through Table 2-15 on page 2-11 and Table 2-16 on page 2-11 through Table 2-18 on page 2-12 (PDC6 and PDC7).

Table 2-20 • Different Components Contributing to the Static Power Consumption in IGLOO Devices
For IGLOO V2 or V5 Devices, 1.5 V DC Core Supply Voltage

Parameter	Definition	Device-Specific Static Power (mW)							
		AGL1000	AGL600	AGL400	AGL250	AGL125	AGL060	AGL030	AGL015
PDC1	Array static power in Active mode	See Table 2-12 on page 2-9.							
PDC2	Array static power in Static (Idle) mode	See Table 2-11 on page 2-8.							
PDC3	Array static power in Flash*Freeze mode	See Table 2-9 on page 2-7.							
PDC4	Static PLL contribution	1.84							
PDC5	Bank quiescent power (V_{CC1} -dependent)	See Table 2-12 on page 2-9.							
PDC6	I/O input pin static power (standard-dependent)	See Table 2-13 on page 2-10 through Table 2-15 on page 2-11.							
PDC7	I/O output pin static power (standard-dependent)	See Table 2-16 on page 2-11 through Table 2-18 on page 2-12.							

*Note: *For a different output load, drive strength, or slew rate, Microsemi recommends using the Microsemi power spreadsheet calculator or SmartPower tool in Libero SoC.*

Combinatorial Cells Contribution— P_{C-CELL}

$$P_{C-CELL} = N_{C-CELL} * \alpha_1 / 2 * P_{AC7} * F_{CLK}$$

N_{C-CELL} is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-23 on page 2-19.

F_{CLK} is the global clock signal frequency.

Routing Net Contribution— P_{NET}

$$P_{NET} = (N_{S-CELL} + N_{C-CELL}) * \alpha_1 / 2 * P_{AC8} * F_{CLK}$$

N_{S-CELL} is the number of VersaTiles used as sequential modules in the design.

N_{C-CELL} is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-23 on page 2-19.

F_{CLK} is the global clock signal frequency.

I/O Input Buffer Contribution— P_{INPUTS}

$$P_{INPUTS} = N_{INPUTS} * \alpha_2 / 2 * P_{AC9} * F_{CLK}$$

N_{INPUTS} is the number of I/O input buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-23 on page 2-19.

F_{CLK} is the global clock signal frequency.

I/O Output Buffer Contribution— $P_{OUTPUTS}$

$$P_{OUTPUTS} = N_{OUTPUTS} * \alpha_2 / 2 * \beta_1 * P_{AC10} * F_{CLK}$$

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-23 on page 2-19.

β_1 is the I/O buffer enable rate—guidelines are provided in Table 2-24 on page 2-19.

F_{CLK} is the global clock signal frequency.

RAM Contribution— P_{MEMORY}

$$P_{MEMORY} = P_{AC11} * N_{BLOCKS} * F_{READ-CLOCK} * \beta_2 + P_{AC12} * N_{BLOCK} * F_{WRITE-CLOCK} * \beta_3$$

N_{BLOCKS} is the number of RAM blocks used in the design.

$F_{READ-CLOCK}$ is the memory read clock frequency.

β_2 is the RAM enable rate for read operations.

$F_{WRITE-CLOCK}$ is the memory write clock frequency.

β_3 is the RAM enable rate for write operations—guidelines are provided in Table 2-24 on page 2-19.

PLL Contribution— P_{PLL}

$$P_{PLL} = P_{DC4} + P_{AC13} * F_{CLKOUT}$$

F_{CLKOUT} is the output clock frequency.[†]

[†] If a PLL is used to generate more than one output clock, include each output clock in the formula by adding its corresponding contribution ($P_{AC13} * F_{CLKOUT}$ product) to the total PLL contribution.

Table 2-31 • Summary of I/O Timing Characteristics—Software Default Settings, Std. Speed Grade, Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case V_{CCI} (per standard)
Applicable to Advanced I/O Banks

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength Option ¹ (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTTL / 3.3 V LVCMOS	12 mA	12	High	5	–	0.97	2.09	0.18	0.85	0.66	2.14	1.68	2.67	3.05	5.73	5.27	ns
3.3 V LVCMOS Wide Range ²	100 μA	12	High	5	–	0.97	2.93	0.18	1.19	0.66	2.95	2.27	3.81	4.30	6.54	5.87	ns
2.5 V LVCMOS	12 mA	12	High	5	–	0.97	2.09	0.18	1.08	0.66	2.14	1.83	2.73	2.93	5.73	5.43	ns
1.8 V LVCMOS	12 mA	12	High	5	–	0.97	2.24	0.18	1.01	0.66	2.29	2.00	3.02	3.40	5.88	5.60	ns
1.5 V LVCMOS	12 mA	12	High	5	–	0.97	2.50	0.18	1.17	0.66	2.56	2.27	3.21	3.48	6.15	5.86	ns
3.3 V PCI	Per PCI spec	–	High	10	25 ²	0.97	2.32	0.18	0.74	0.66	2.37	1.78	2.67	3.05	5.96	5.38	ns
3.3 V PCI-X	Per PCI-X spec	–	High	10	25 ²	0.97	2.32	0.19	0.70	0.66	2.37	1.78	2.67	3.05	5.96	5.38	ns
LVDS	24 mA	–	High	–	–	0.97	1.74	0.19	1.35	–	–	–	–	–	–	–	ns
LVPECL	24 mA	–	High	–	–	0.97	1.68	0.19	1.16	–	–	–	–	–	–	–	ns

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is $\pm 100\text{ }\mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.
3. Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-12 on page 2-79 for connectivity. This resistor is not required during normal operation.
4. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-43 • I/O Short Currents IOSH/IOSL
Applicable to Standard Plus I/O Banks

	Drive Strength	IOSL (mA)*	IOSH (mA)*
3.3 V LVTTTL / 3.3 V LVCMOS	2 mA	25	27
	4 mA	25	27
	6 mA	51	54
	8 mA	51	54
	12 mA	103	109
	16 mA	103	109
3.3 V LVCMOS Wide Range	100 μ A	Same as regular 3.3 V LVCMOS	Same as regular 3.3 V LVCMOS
2.5 V LVCMOS	2 mA	16	18
	4 mA	16	18
	6 mA	32	37
	8 mA	32	37
	12 mA	65	74
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
	6 mA	35	44
	8 mA	35	44
1.5 V LVCMOS	2 mA	13	16
	4 mA	25	33
1.2 V LVCMOS	2 mA	20	26
1.2 V LVCMOS Wide Range	100 μ A	20	26
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	103	109

Note: * $T_J = 100^{\circ}\text{C}$

Applies to 1.2 V DC Core Voltage

Table 2-73 • 3.3 V LVC MOS Wide Range Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$, Worst-Case $V_{CCI} = 2.7\text{ V}$
Applicable to Advanced Banks

Drive Strength	Equivalent Software Default Drive Strength Option ¹	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 μA	2 mA	Std.	1.55	7.52	0.26	1.32	1.10	7.52	6.38	3.84	4.02	13.31	12.16	ns
100 μA	4 mA	Std.	1.55	7.52	0.26	1.32	1.10	7.52	6.38	3.84	4.02	13.31	12.16	ns
100 μA	6 mA	Std.	1.55	6.37	0.26	1.32	1.10	6.37	5.57	4.23	4.73	12.16	11.35	ns
100 μA	8 mA	Std.	1.55	6.37	0.26	1.32	1.10	6.37	5.57	4.23	4.73	12.16	11.35	ns
100 μA	12 mA	Std.	1.55	5.55	0.26	1.32	1.10	5.55	4.96	4.50	5.18	11.34	10.75	ns
100 μA	16 mA	Std.	1.55	5.32	0.26	1.32	1.10	5.32	4.82	4.56	5.29	11.10	10.61	ns
100 μA	24 mA	Std.	1.55	5.19	0.26	1.32	1.10	5.19	4.85	4.63	5.74	10.98	10.63	ns

Notes:

1. The minimum drive strength for any LVC MOS 3.3 V software configuration when run in wide range is $\pm 100\text{ }\mu\text{A}$. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-74 • 3.3 V LVC MOS Wide Range High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$, Worst-Case $V_{CCI} = 2.7$
Applicable to Advanced Banks

Drive Strength	Equivalent Software Default Drive Strength Option ¹	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 μA	2 mA	Std.	1.55	4.75	0.26	1.32	1.10	4.75	3.77	3.84	4.27	10.54	9.56	ns
100 μA	4 mA	Std.	1.55	4.75	0.26	1.32	1.10	4.75	3.77	3.84	4.27	10.54	9.56	ns
100 μA	6 mA	Std.	1.55	4.10	0.26	1.32	1.10	4.10	3.19	4.24	4.98	9.88	8.98	ns
100 μA	8 mA	Std.	1.55	4.10	0.26	1.32	1.10	4.10	3.19	4.24	4.98	9.88	8.98	ns
100 μA	12 mA	Std.	1.55	3.73	0.26	1.32	1.10	3.73	2.91	4.51	5.43	9.52	8.69	ns
100 μA	16 mA	Std.	1.55	3.67	0.26	1.32	1.10	3.67	2.85	4.57	5.55	9.46	8.64	ns
100 μA	24 mA	Std.	1.55	3.70	0.26	1.32	1.10	3.70	2.79	4.65	6.01	9.49	8.58	ns

Notes:

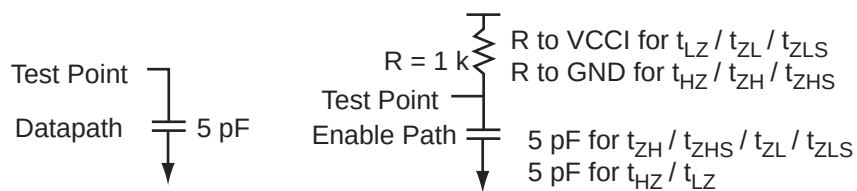
1. The minimum drive strength for any LVC MOS 3.3 V software configuration when run in wide range is $\pm 100\text{ }\mu\text{A}$. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.
3. Software default selection highlighted in gray.

Table 2-81 • Minimum and Maximum DC Input and Output Levels
Applicable to Standard I/O Banks

2.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	−0.3	0.7	1.7	3.6	0.7	1.7	2	2	16	18	10	10
4 mA	−0.3	0.7	1.7	3.6	0.7	1.7	4	4	16	18	10	10
6 mA	−0.3	0.7	1.7	3.6	0.7	1.7	6	6	32	37	10	10
8 mA	−0.3	0.7	1.7	3.6	0.7	1.7	8	8	32	37	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

**Figure 2-8 • AC Loading****Table 2-82 • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	C _{LOAD} (pF)
0	2.5	1.2	5

Note: *Measuring point = Vtrip. See Table 2-29 on page 2-28 for a complete table of trip points.

Table 2-113 • Minimum and Maximum DC Input and Output Levels
Applicable to Standard I/O Banks

1.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	−0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2	13	16	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

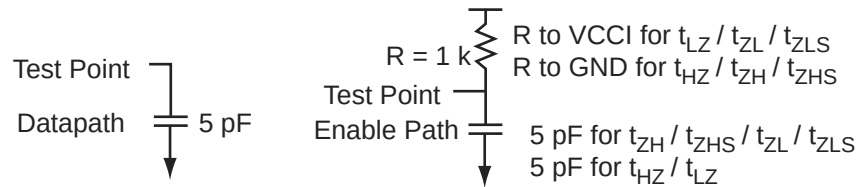


Figure 2-10 • AC Loading

Table 2-114 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C _{LOAD} (pF)
0	1.5	0.75	5

Note: *Measuring point = Vtrip. See Table 2-29 on page 2-28 for a complete table of trip points.

Table 2-155 • Parameter Definition and Measuring Nodes

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	H, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	F, H
t_{OHD}	Data Hold Time for the Output Data Register	F, H
t_{OSUE}	Enable Setup Time for the Output Data Register	G, H
t_{OHE}	Enable Hold Time for the Output Data Register	G, H
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	L, DOUT
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	L, H
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	L, H
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	H, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	J, H
t_{OEHD}	Data Hold Time for the Output Enable Register	J, H
t_{OESUE}	Enable Setup Time for the Output Enable Register	K, H
t_{OEHE}	Enable Hold Time for the Output Enable Register	K, H
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	I, H
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	I, H
t_{ICLKQ}	Clock-to-Q of the Input Data Register	A, E
t_{ISUD}	Data Setup Time for the Input Data Register	C, A
t_{IHD}	Data Hold Time for the Input Data Register	C, A
t_{ISUE}	Enable Setup Time for the Input Data Register	B, A
t_{IHE}	Enable Hold Time for the Input Data Register	B, A
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	D, E
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	D, A
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	D, A

Note: *See Figure 2-16 on page 2-84 for more information.

VersaTile Characteristics

VersaTile Specifications as a Combinatorial Module

The IGLOO library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *IGLOO, Fusion, and ProASIC3 Macro Library Guide*.

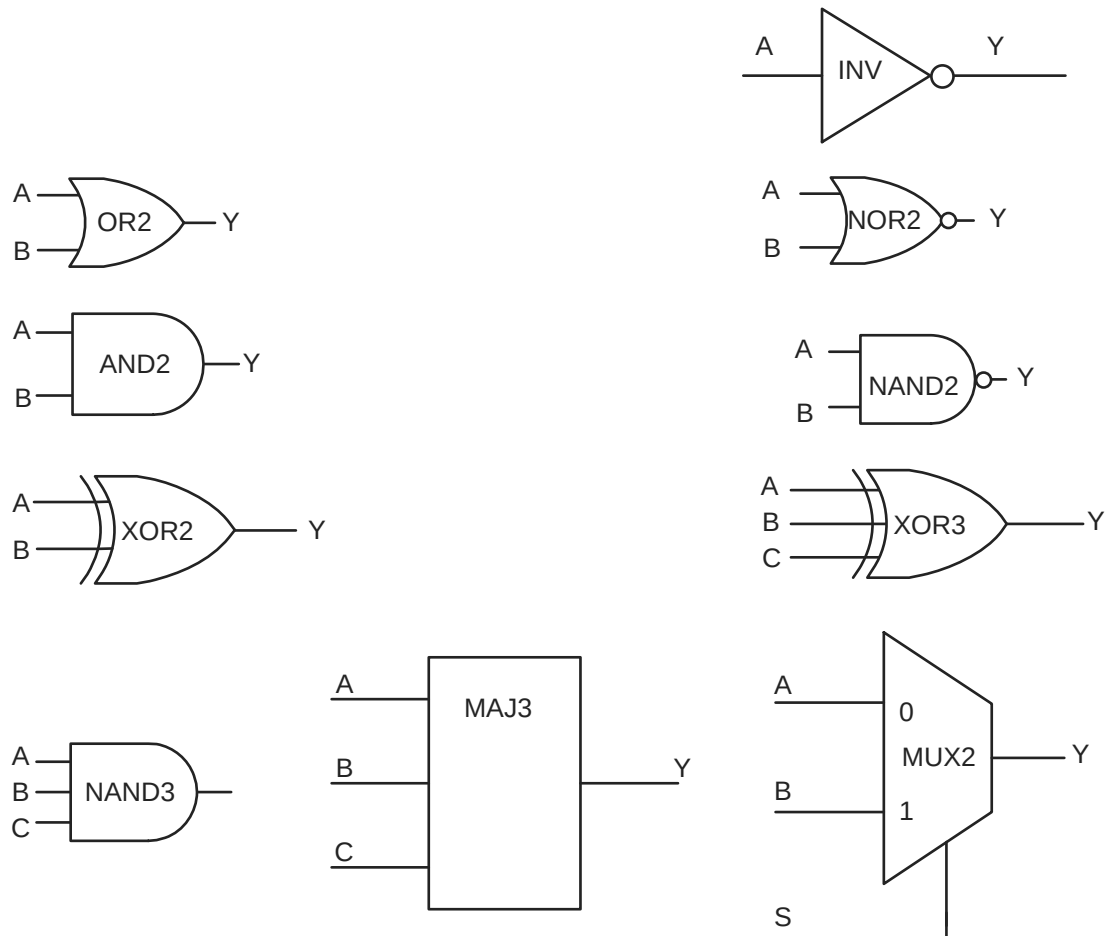


Figure 2-25 • Sample of Combinatorial Cells

Timing Characteristics

1.5 V DC Core Voltage

Table 2-169 • Combinatorial Cell Propagation Delays

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Combinatorial Cell	Equation	Parameter	Std.	Units
INV	$Y = !A$	t_{PD}	0.80	ns
AND2	$Y = A \cdot B$	t_{PD}	0.84	ns
NAND2	$Y = !(A \cdot B)$	t_{PD}	0.90	ns
OR2	$Y = A + B$	t_{PD}	1.19	ns
NOR2	$Y = !(A + B)$	t_{PD}	1.10	ns
XOR2	$Y = A \oplus B$	t_{PD}	1.37	ns
MAJ3	$Y = \text{MAJ}(A, B, C)$	t_{PD}	1.33	ns
XOR3	$Y = A \oplus B \oplus C$	t_{PD}	1.79	ns
MUX2	$Y = A !S + B S$	t_{PD}	1.48	ns
AND3	$Y = A \cdot B \cdot C$	t_{PD}	1.21	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

1.2 V DC Core Voltage

Table 2-170 • Combinatorial Cell Propagation Delays

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$

Combinatorial Cell	Equation	Parameter	Std.	Units
INV	$Y = !A$	t_{PD}	1.34	ns
AND2	$Y = A \cdot B$	t_{PD}	1.43	ns
NAND2	$Y = !(A \cdot B)$	t_{PD}	1.59	ns
OR2	$Y = A + B$	t_{PD}	2.30	ns
NOR2	$Y = !(A + B)$	t_{PD}	2.07	ns
XOR2	$Y = A \oplus B$	t_{PD}	2.46	ns
MAJ3	$Y = \text{MAJ}(A, B, C)$	t_{PD}	2.46	ns
XOR3	$Y = A \oplus B \oplus C$	t_{PD}	3.12	ns
MUX2	$Y = A !S + B S$	t_{PD}	2.83	ns
AND3	$Y = A \cdot B \cdot C$	t_{PD}	2.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Timing Characteristics**1.5 V DC Core Voltage****Table 2-195 • FIFO****Worst Commercial-Case Conditions: $T_J = 70^{\circ}\text{C}$, $V_{CC} = 1.425\text{ V}$**

Parameter	Description	Std.	Units
t_{ENS}	REN, WEN Setup Time	1.99	ns
t_{ENH}	REN, WEN Hold Time	0.16	ns
t_{BKS}	BLK Setup Time	0.30	ns
t_{BKH}	BLK Hold Time	0.00	ns
t_{DS}	Input Data (WD) Setup Time	0.76	ns
t_{DH}	Input Data (WD) Hold Time	0.25	ns
t_{CKQ1}	Clock High to New Data Valid on RD (flow-through)	3.33	ns
t_{CKQ2}	Clock High to New Data Valid on RD (pipelined)	1.80	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	3.53	ns
t_{WCKFF}	WCLK High to Full Flag Valid	3.35	ns
t_{CKAF}	Clock High to Almost Empty/Full Flag Valid	12.85	ns
t_{RSTFG}	RESET Low to Empty/Full Flag Valid	3.48	ns
t_{RSTAF}	RESET Low to Almost Empty/Full Flag Valid	12.72	ns
t_{RSTBQ}	RESET Low to Data Out Low on RD (flow-through)	2.02	ns
	RESET Low to Data Out Low on RD (pipelined)	2.02	ns
t_{REMRSTB}	RESET Removal	0.61	ns
t_{RECRSTB}	RESET Recovery	3.21	ns
t_{MPWRSTB}	RESET Minimum Pulse Width	0.68	ns
t_{CYC}	Clock Cycle Time	6.24	ns
F_{MAX}	Maximum Frequency for FIFO	160	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

UC81	
Pin Number	AGL030 Function
A1	IO00RSB0
A2	IO02RSB0
A3	IO06RSB0
A4	IO11RSB0
A5	IO16RSB0
A6	IO19RSB0
A7	IO22RSB0
A8	IO24RSB0
A9	IO26RSB0
B1	IO81RSB1
B2	IO04RSB0
B3	IO10RSB0
B4	IO13RSB0
B5	IO15RSB0
B6	IO20RSB0
B7	IO21RSB0
B8	IO28RSB0
B9	IO25RSB0
C1	IO79RSB1
C2	IO80RSB1
C3	IO08RSB0
C4	IO12RSB0
C5	IO17RSB0
C6	IO14RSB0
C7	IO18RSB0
C8	IO29RSB0
C9	IO27RSB0
D1	IO74RSB1
D2	IO76RSB1
D3	IO77RSB1
D4	VCC
D5	VCCIB0
D6	GND
D7	IO23RSB0
D8	IO31RSB0
D9	IO30RSB0

UC81	
Pin Number	AGL030 Function
E1	GEB0/IO71RSB1
E2	GEA0/IO72RSB1
E3	GEC0/IO73RSB1
E4	VCCIB1
E5	VCC
E6	VCCIB0
E7	GDC0/IO32RSB0
E8	GDA0/IO33RSB0
E9	GDB0/IO34RSB0
F1	IO68RSB1
F2	IO67RSB1
F3	IO64RSB1
F4	GND
F5	VCCIB1
F6	IO47RSB1
F7	IO36RSB0
F8	IO38RSB0
F9	IO40RSB0
G1	IO65RSB1
G2	IO66RSB1
G3	IO57RSB1
G4	IO53RSB1
G5	IO49RSB1
G6	IO45RSB1
G7	IO46RSB1
G8	VJTAG
G9	TRST
H1	IO62RSB1
H2	FF/IO60RSB1
H3	IO58RSB1
H4	IO54RSB1
H5	IO48RSB1
H6	IO43RSB1
H7	IO42RSB1
H8	TDI
H9	TDO

UC81	
Pin Number	AGL030 Function
J1	IO63RSB1
J2	IO61RSB1
J3	IO59RSB1
J4	IO56RSB1
J5	IO52RSB1
J6	IO44RSB1
J7	TCK
J8	TMS
J9	VPUMP

CS281		CS281		CS281	
Pin Number	AGL600 Function	Pin Number	AGL600 Function	Pin Number	AGL600 Function
A1	GND	B18	VCCIB1	E13	IO46RSB0
A2	GAB0/IO02RSB0	B19	IO61NDB1	E14	GBB1/IO57RSB0
A3	GAC1/IO05RSB0	C1	GAB2/IO173PPB3	E15	IO62NPB1
A4	IO07RSB0	C2	IO174NPB3	E16	IO63PPB1
A5	IO10RSB0	C6	IO12RSB0	E18	IO64PPB1
A6	IO14RSB0	C14	IO50RSB0	E19	IO65NPB1
A7	IO18RSB0	C18	IO60NPB1	F1	IO168NPB3
A8	IO21RSB0	C19	GBB2/IO61PDB1	F2	GND
A9	IO22RSB0	D1	IO170PPB3	F3	IO169PPB3
A10	VCCIB0	D2	IO172NPB3	F4	IO170NPB3
A11	IO33RSB0	D4	GAA0/IO00RSB0	F5	IO173NPB3
A12	IO40RSB0	D5	GAA1/IO01RSB0	F15	IO63NPB1
A13	IO37RSB0	D6	IO09RSB0	F16	IO65PPB1
A14	IO48RSB0	D7	IO16RSB0	F17	IO64NPB1
A15	IO51RSB0	D8	IO19RSB0	F18	GND
A16	IO53RSB0	D9	IO26RSB0	F19	IO68PPB1
A17	GBC1/IO55RSB0	D10	GND	G1	IO167NPB3
A18	GBA0/IO58RSB0	D11	IO34RSB0	G2	IO165NDB3
A19	GND	D12	IO45RSB0	G4	IO168PPB3
B1	GAA2/IO174PPB3	D13	IO49RSB0	G5	IO167PPB3
B2	VCCIB0	D14	IO47RSB0	G7	GAC2/IO172PPB3
B3	GAB1/IO03RSB0	D15	GBB0/IO56RSB0	G8	VCCIB0
B4	GAC0/IO04RSB0	D16	GBA2/IO60PPB1	G9	IO28RSB0
B5	IO06RSB0	D18	GBC2/IO62PPB1	G10	IO32RSB0
B6	GND	D19	IO66NPB1	G11	IO43RSB0
B7	IO15RSB0	E1	IO169NPB3	G12	VCCIB0
B8	IO20RSB0	E2	IO171PPB3	G13	IO66PPB1
B9	IO23RSB0	E4	IO171NPB3	G15	IO67NDB1
B10	IO24RSB0	E5	IO08RSB0	G16	IO67PDB1
B11	IO36RSB0	E6	IO11RSB0	G18	GCC0/IO69NPB1
B12	IO35RSB0	E7	IO13RSB0	G19	GCB1/IO70PPB1
B13	IO44RSB0	E8	IO17RSB0	H1	GFB0/IO163NPB3
B14	GND	E9	IO25RSB0	H2	IO165PDB3
B15	IO52RSB0	E10	IO30RSB0	H4	GFC1/IO164PPB3
B16	GBC0/IO54RSB0	E11	IO41RSB0	H5	GFB1/IO163PPB3
B17	GBA1/IO59RSB0	E12	IO42RSB0	H7	VCCIB3

QN48	
Pin Number	AGL030 Function
1	IO82RSB1
2	GEC0/IO73RSB1
3	GEA0/IO72RSB1
4	GEB0/IO71RSB1
5	GND
6	VCCIB1
7	IO68RSB1
8	IO67RSB1
9	IO66RSB1
10	IO65RSB1
11	IO64RSB1
12	IO62RSB1
13	IO61RSB1
14	FF/IO60RSB1
15	IO57RSB1
16	IO55RSB1
17	IO53RSB1
18	VCC
19	VCCIB1
20	IO46RSB1
21	IO42RSB1
22	TCK
23	TDI
24	TMS
25	VPUMP
26	TDO
27	TRST
28	VJTAG
29	IO38RSB0
30	GDB0/IO34RSB0
31	GDA0/IO33RSB0
32	GDC0/IO32RSB0
33	VCCIB0
34	GND
35	VCC
36	IO25RSB0

QN48	
Pin Number	AGL030 Function
37	IO24RSB0
38	IO22RSB0
39	IO20RSB0
40	IO18RSB0
41	IO16RSB0
42	IO14RSB0
43	IO10RSB0
44	IO08RSB0
45	IO06RSB0
46	IO04RSB0
47	IO02RSB0
48	IO00RSB0

QN132	
Pin Number	AGL060 Function
A1	GAB2/IO00RSB1
A2	IO93RSB1
A3	VCCIB1
A4	GFC1/IO89RSB1
A5	GFB0/IO86RSB1
A6	VCCPLF
A7	GFA1/IO84RSB1
A8	GFC2/IO81RSB1
A9	IO78RSB1
A10	VCC
A11	GEB1/IO75RSB1
A12	GEA0/IO72RSB1
A13	GEC2/IO69RSB1
A14	IO65RSB1
A15	VCC
A16	IO64RSB1
A17	IO63RSB1
A18	IO62RSB1
A19	IO61RSB1
A20	IO58RSB1
A21	GDB2/IO55RSB1
A22	NC
A23	GDA2/IO54RSB1
A24	TDI
A25	TRST
A26	GDC1/IO48RSB0
A27	VCC
A28	IO47RSB0
A29	GCC2/IO46RSB0
A30	GCA2/IO44RSB0
A31	GCA0/IO43RSB0
A32	GCB1/IO40RSB0
A33	IO36RSB0
A34	VCC
A35	IO31RSB0
A36	GBA2/IO28RSB0

QN132	
Pin Number	AGL060 Function
A37	GBB1/IO25RSB0
A38	GBC0/IO22RSB0
A39	VCCIB0
A40	IO21RSB0
A41	IO18RSB0
A42	IO15RSB0
A43	IO14RSB0
A44	IO11RSB0
A45	GAB1/IO08RSB0
A46	NC
A47	GAB0/IO07RSB0
A48	IO04RSB0
B1	IO01RSB1
B2	GAC2/IO94RSB1
B3	GND
B4	GFC0/IO88RSB1
B5	VCOMPLF
B6	GND
B7	GFB2/IO82RSB1
B8	IO79RSB1
B9	GND
B10	GEB0/IO74RSB1
B11	VMV1
B12	FF/GEB2/IO70RSB1
B13	IO67RSB1
B14	GND
B15	NC
B16	NC
B17	GND
B18	IO59RSB1
B19	GDC2/IO56RSB1
B20	GND
B21	GNDQ
B22	TMS
B23	TDO

QN132	
Pin Number	AGL060 Function
B24	GDC0/IO49RSB0
B25	GND
B26	NC
B27	GCB2/IO45RSB0
B28	GND
B29	GCB0/IO41RSB0
B30	GCC1/IO38RSB0
B31	GND
B32	GBB2/IO30RSB0
B33	VMV0
B34	GBA0/IO26RSB0
B35	GBC1/IO23RSB0
B36	GND
B37	IO20RSB0
B38	IO17RSB0
B39	GND
B40	IO12RSB0
B41	GAC0/IO09RSB0
B42	GND
B43	GAA1/IO06RSB0
B44	GNDQ
C1	GAA2/IO02RSB1
C2	IO95RSB1
C3	VCC
C4	GFB1/IO87RSB1
C5	GFA0/IO85RSB1
C6	GFA2/IO83RSB1
C7	IO80RSB1
C8	VCCIB1
C9	GEA1/IO73RSB1
C10	GNDQ
C11	GEA2/IO71RSB1
C12	IO68RSB1
C13	VCCIB1
C14	NC
C15	NC

QN132	
Pin Number	AGL060 Function
C16	IO60RSB1
C17	IO57RSB1
C18	NC
C19	TCK
C20	VMV1
C21	VPUMP
C22	VJTAG
C23	VCCIB0
C24	NC
C25	NC
C26	GCA1/IO42RSB0
C27	GCC0/IO39RSB0
C28	VCCIB0
C29	IO29RSB0
C30	GNDQ
C31	GBA1/IO27RSB0
C32	GBB0/IO24RSB0
C33	VCC
C34	IO19RSB0
C35	IO16RSB0
C36	IO13RSB0
C37	GAC1/IO10RSB0
C38	NC
C39	GAA0/IO05RSB0
C40	VMV0
D1	GND
D2	GND
D3	GND
D4	GND

FG256	
Pin Number	AGL400 Function
A1	GND
A2	GAA0/IO00RSB0
A3	GAA1/IO01RSB0
A4	GAB0/IO02RSB0
A5	IO16RSB0
A6	IO17RSB0
A7	IO22RSB0
A8	IO28RSB0
A9	IO34RSB0
A10	IO37RSB0
A11	IO41RSB0
A12	IO43RSB0
A13	GBB1/IO57RSB0
A14	GBA0/IO58RSB0
A15	GBA1/IO59RSB0
A16	GND
B1	GAB2/IO154UDB3
B2	GAA2/IO155UDB3
B3	IO12RSB0
B4	GAB1/IO03RSB0
B5	IO13RSB0
B6	IO14RSB0
B7	IO21RSB0
B8	IO27RSB0
B9	IO32RSB0
B10	IO38RSB0
B11	IO42RSB0
B12	GBC1/IO55RSB0
B13	GBB0/IO56RSB0
B14	IO44RSB0
B15	GBA2/IO60PDB1
B16	IO60NDB1
C1	IO154VDB3
C2	IO155VDB3
C3	IO11RSB0
C4	IO07RSB0
C5	GAC0/IO04RSB0
C6	GAC1/IO05RSB0

FG256	
Pin Number	AGL400 Function
C7	IO20RSB0
C8	IO24RSB0
C9	IO33RSB0
C10	IO39RSB0
C11	IO45RSB0
C12	GBC0/IO54RSB0
C13	IO48RSB0
C14	VMV0
C15	IO61NPB1
C16	IO63PDB1
D1	IO151VDB3
D2	IO151UDB3
D3	GAC2/IO153UDB3
D4	IO06RSB0
D5	GNDQ
D6	IO10RSB0
D7	IO19RSB0
D8	IO26RSB0
D9	IO30RSB0
D10	IO40RSB0
D11	IO46RSB0
D12	GNDQ
D13	IO47RSB0
D14	GBB2/IO61PPB1
D15	IO53RSB0
D16	IO63NDB1
E1	IO150PDB3
E2	IO08RSB0
E3	IO153VDB3
E4	IO152VDB3
E5	VMV0
E6	VCCIB0
E7	VCCIB0
E8	IO25RSB0
E9	IO31RSB0
E10	VCCIB0
E11	VCCIB0
E12	VMV1

FG256	
Pin Number	AGL400 Function
E13	GBC2/IO62PDB1
E14	IO65RSB1
E15	IO52RSB0
E16	IO66PDB1
F1	IO150NDB3
F2	IO149NPB3
F3	IO09RSB0
F4	IO152UDB3
F5	VCCIB3
F6	GND
F7	VCC
F8	VCC
F9	VCC
F10	VCC
F11	GND
F12	VCCIB1
F13	IO62NDB1
F14	IO49RSB0
F15	IO64PPB1
F16	IO66NDB1
G1	IO148NDB3
G2	IO148PDB3
G3	IO149PPB3
G4	GFC1/IO147PPB3
G5	VCCIB3
G6	VCC
G7	GND
G8	GND
G9	GND
G10	GND
G11	VCC
G12	VCCIB1
G13	GCC1/IO67PPB1
G14	IO64NPB1
G15	IO73PDB1
G16	IO73NDB1
H1	GFB0/IO146NPB3
H2	GFA0/IO145NDB3

Revision	Changes	Page
Revision 19 (continued)	The following sentence was removed from the "Advanced Architecture" section: "In addition, extensive on-chip programming circuitry allows for rapid, single-voltage (3.3 V) programming of IGLOO devices via an IEEE 1532 JTAG interface" (SAR 28756).	1-3
	The "Specifying I/O States During Programming" section is new (SAR 21281).	1-8
	Values for VCCPLL at 1.2 V –1.5 V DC core supply voltage were revised in Table 2-2 • Recommended Operating Conditions 1 (SAR 22356). The value for VPUMP operation was changed from "0 to 3.45 V" to "0 to 3.6 V" (SAR 25220). The value for VCCPLL 1.5 V DC core supply voltage was changed from "1.4 to 1.6 V" to "1.425 to 1.575 V" (SAR 26551). The notes in the table were renumbered in order of their appearance in the table (SAR 21869).	2-2
	The temperature used in EQ 2 was revised from 110°C to 100°C for consistency with the limits given in Table 2-2 • Recommended Operating Conditions 1. The resulting maximum power allowed is thus 1.28 W. Formerly it was 1.71 W (SAR 26259).	2-6
	Values for CS196, CS281, and QN132 packages were added to Table 2-5 • Package Thermal Resistivities (SARs 26228, 32301).	2-6
	Table 2-6 • Temperature and Voltage Derating Factors for Timing Delays (normalized to TJ = 70°C, VCC = 1.425 V) and Table 2-7 • Temperature and Voltage Derating Factors for Timing Delays (normalized to TJ = 70°C, VCC = 1.14 V) were updated to remove the column for –20°C and shift the data over to correct columns (SAR 23041).	2-7
	The tables in the "Quiescent Supply Current" section were updated with revised notes on IDD (SAR 24112). Table 2-8 • Power Supply State per Mode is new.	2-7
	The formulas in the table notes for Table 2-41 • I/O Weak Pull-Up/Pull-Down Resistances were corrected (SAR 21348).	2-37
	The row for 110°C was removed from Table 2-45 • Duration of Short Circuit Event before Failure. The example in the associated paragraph was changed from 110°C to 100°C. Table 2-46 • I/O Input Rise Time, Fall Time, and Related I/O Reliability1 was revised to change 110° to 100°C. (SAR 26259).	2-40
	The notes regarding drive strength in the "Summary of I/O Timing Characteristics – Default I/O Software Settings" section, "3.3 V LVCMOS Wide Range" section and "1.2 V LVCMOS Wide Range" section tables were revised for clarification. They now state that the minimum drive strength for the default software configuration when run in wide range is ±100 µA. The drive strength displayed in software is supported in normal range only. For a detailed I/V curve, refer to the IBIS models (SAR 25700).	2-28, 2-47, 2-77
	The following sentence was deleted from the "2.5 V LVCMOS" section (SAR 24916): "It uses a 5 V–tolerant input buffer and push-pull output buffer."	2-56
	The values for F _{DDRIMAX} and F _{DDOMAX} were updated in the tables in the "Input DDR Module" section and "Output DDR Module" section (SAR 23919).	2-94, 2-97
	The following notes were removed from Table 2-147 • Minimum and Maximum DC Input and Output Levels (SAR 29428): ±5% Differential input voltage = ±350 mV	2-81
	Table 2-189 • IGLOO CCC/PLL Specification and Table 2-190 • IGLOO CCC/PLL Specification were updated. A note was added to both tables indicating that when the CCC/PLL core is generated by Mircosemi core generator software, not all delay values of the specified delay increments are available (SAR 25705).	2-115

Revision / Version	Changes	Page
Revision 18 (Nov 2009)	The version changed to v2.0 for IGLOO datasheet chapters, indicating the datasheet contains information based on final characterization. Please review the datasheet carefully as most tables were updated with new data.	N/A
Revision 17 (Sep 2009) Product Brief v1.6	The "Reprogrammable Flash Technology" section was modified to add "250 MHz (1.5 V systems) and 160 MHz (1.2 V systems) System Performance."	I
	"IGLOO Ordering Information" was revised to note that halogen-free packages are available with RoHS-compliant packaging.	III
	Table 1-1 • I/O Standards Supported is new.	1-7
	The definitions of hot-swap and cold-sparing were added to the "I/Os with Advanced I/O Standards" section.	1-7
Revision 16 (Apr 2009) Product Brief v1.5	M1AGL400 is no longer offered and was removed from the "IGLOO Devices" product table, "IGLOO Ordering Information", and "Temperature Grade Offerings".	I, III, IV
	The –F speed grade is no longer offered for IGLOO devices. The speed grade column and note regarding –F speed grade were removed from "IGLOO Ordering Information". The "Speed Grade and Temperature Grade Matrix" section was removed.	III, IV
	This datasheet now has fully characterized data and has moved from being Advance to a Production version. The version number changed from Advance v0.5 to v2.0. Please review the datasheet carefully as most tables were updated with new data.	N/A
DC and Switching Characteristics Advance v0.6	3.3 V LVCMOS and 1.2 V LVCMOS Wide Range support was added to the datasheet. This affects all tables that contained 3.3 V LVCMOS and 1.2 V LVCMOS data.	
	I_{IL} and I_{IH} input leakage current information was added to all "Minimum and Maximum DC Input and Output Levels" tables.	N/A
	–F was removed from the datasheet. The speed grade is no longer supported.	N/A
	The notes in Table 2-2 • Recommended Operating Conditions 1 were updated.	2-2
	Table 2-4 • Overshoot and Undershoot Limits 1 was updated.	2-3
	Table 2-5 • Package Thermal Resistivities was updated.	2-6
	Table 2-6 • Temperature and Voltage Derating Factors for Timing Delays (normalized to $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$) and Table 2-7 • Temperature and Voltage Derating Factors for Timing Delays (normalized to $T_J = 70^\circ\text{C}$, $V_{CC} = 1.14\text{ V}$) were updated.	2-7
	In Table 2-191 • RAM4K9 and Table 2-193 • RAM4K9, the following specifications were removed: t_{WRO} t_{CCKH}	2-122 and 2-124
	In Table 2-192 • RAM512X18 and Table 2-194 • RAM512X18, the following specifications were removed: t_{WRO} t_{CCKH}	2-123 and 2-125
Revision 15 (Feb 2009) Packaging v1.9	The "QN132" pin table for the AGL060 device is new.	4-31