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### [Understanding Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

#### **Details**

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	24576
Total RAM Bits	147456
Number of I/O	300
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/agl1000v5-fg484">https://www.e-xfl.com/product-detail/microchip-technology/agl1000v5-fg484</a>

**Table 2-10 • Quiescent Supply Current (IDD) Characteristics, IGLOO Sleep Mode\***

	Core Voltage	AGL015	AGL030	AGL060	AGL125	AGL250	AGL400	AGL600	AGL1000	Units
VCCI/VJTAG = 1.2 V (per bank) Typical (25°C)	1.2 V	1.7	1.7	1.7	1.7	1.7	1.7	1.7	1.7	µA
VCCI/VJTAG = 1.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8	µA
VCCI/VJTAG = 1.8 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.9	1.9	1.9	1.9	1.9	1.9	1.9	1.9	µA
VCCI/VJTAG = 2.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2	µA
VCCI/VJTAG = 3.3 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	µA

Note:  $IDD = N_{BANKS} \times ICCI$ . Values do not include I/O static contribution, which is shown in Table 2-10 through Table 2-15 on page 2-11 and Table 2-16 on page 2-11 through Table 2-18 on page 2-12 (PDC6 and PDC7).

**Table 2-11 • Quiescent Supply Current (IDD) Characteristics, IGLOO Shutdown Mode**

	Core Voltage	AGL015	AGL030	Units
Typical (25°C)	1.2 V / 1.5 V	0	0	µA

**Table 2-12 • Quiescent Supply Current (IDD), No IGLOO Flash\*Freeze Mode<sup>1</sup>**

	Core Voltage	AGL015	AGL030	AGL060	AGL125	AGL250	AGL400	AGL600	AGL1000	Units
<b>ICCA Current<sup>2</sup></b>										
Typical (25°C)	1.2 V	5	6	10	13	18	25	28	42	µA
	1.5 V	14	16	20	28	44	66	82	137	µA
<b>ICCI or IJTAG Current<sup>3</sup></b>										
VCCI/VJTAG = 1.2 V (per bank) Typical (25°C)	1.2 V	1.7	1.7	1.7	1.7	1.7	1.7	1.7	1.7	µA
VCCI/VJTAG = 1.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.8	1.8	1.8	1.8	1.8	1.8	1.8	1.8	µA
VCCI/VJTAG = 1.8 V (per bank) Typical (25°C)	1.2 V / 1.5 V	1.9	1.9	1.9	1.9	1.9	1.9	1.9	1.9	µA
VCCI/VJTAG = 2.5 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.2	2.2	2.2	2.2	2.2	2.2	2.2	2.2	µA
VCCI/VJTAG = 3.3 V (per bank) Typical (25°C)	1.2 V / 1.5 V	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	µA

Notes:

1.  $IDD = N_{BANKS} \times ICCI + ICCA$ . JTAG counts as one bank when powered.
2. Includes VCC, VPUMP, and VCCPLL currents.
3. Values do not include I/O static contribution (PDC6 and PDC7).

**Table 2-22 • Different Components Contributing to the Static Power Consumption in IGLOO Device For IGLOO V2 Devices, 1.2 V DC Core Supply Voltage**

Parameter	Definition	Device Specific Static Power (mW)							
		AGL1000	AGL600	AGL400	AGL250	AGL125	AGL060	AGL030	AGL015
PDC1	Array static power in Active mode	See Table 2-12 on page 2-9.							
PDC2	Array static power in Static (Idle) mode	See Table 2-11 on page 2-8.							
PDC3	Array static power in Flash*Freeze mode	See Table 2-9 on page 2-7.							
PDC4	Static PLL contribution	0.90							
PDC5	Bank quiescent power (VCCI-Dependent)	See Table 2-12 on page 2-9.							
PDC6	I/O input pin static power (standard-dependent)	See Table 2-13 on page 2-10 through Table 2-15 on page 2-11.							
PDC7	I/O output pin static power (standard-dependent)	See Table 2-16 on page 2-11 through Table 2-18 on page 2-12.							

Note: For a different output load, drive strength, or slew rate, Microsemi recommends using the Microsemi power spreadsheet calculator or SmartPower tool in Libero SoC.

**Table 2-54 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V

Applicable to Standard Plus Banks

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
2 mA	Std.	0.97	2.32	0.18	0.85	0.66	2.37	1.90	1.98	2.13	5.96	5.49	ns
4 mA	Std.	0.97	2.32	0.18	0.85	0.66	2.37	1.90	1.98	2.13	5.96	5.49	ns
6 mA	Std.	0.97	1.94	0.18	0.85	0.66	1.99	1.57	2.20	2.53	5.58	5.16	ns
8 mA	Std.	0.97	1.94	0.18	0.85	0.66	1.99	1.57	2.20	2.53	5.58	5.16	ns
12 mA	Std.	0.97	1.75	0.18	0.85	0.66	1.79	1.40	2.36	2.79	5.38	4.99	ns
16 mA	Std.	0.97	1.75	0.18	0.85	0.66	1.79	1.40	2.36	2.79	5.38	4.99	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

**Table 2-55 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V

Applicable to Standard Banks

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
2 mA	Std.	0.97	3.80	0.18	0.83	0.66	3.88	3.41	1.74	1.78			ns
4 mA	Std.	0.97	3.80	0.18	0.83	0.66	3.88	3.41	1.74	1.78			ns
6 mA	Std.	0.97	3.15	0.18	0.83	0.66	3.21	2.94	1.96	2.17			ns
8 mA	Std.	0.97	3.15	0.18	0.83	0.66	3.21	2.94	1.96	2.17			ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

**Table 2-56 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V

Applicable to Standard Banks

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
2 mA	Std.	0.97	2.19	0.18	0.83	0.66	2.24	1.79	1.74	1.87			ns
4 mA	Std.	0.97	2.19	0.18	0.83	0.66	2.24	1.79	1.74	1.87			ns
6 mA	Std.	0.97	1.85	0.18	0.83	0.66	1.89	1.46	1.96	2.26			ns
8 mA	Std.	0.97	1.85	0.18	0.83	0.66	1.89	1.46	1.96	2.26			ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

**Table 2-75 • 3.3 V LVCMOS Wide Range Low Slew – Applies to 1.2 V DC Core Voltage**  
**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.7**  
**Applicable to Standard Plus Banks**

Drive Strength	Equivalent Software Default Drive Strength Option <sup>1</sup>	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
100 $\mu\text{A}$	2 mA	Std.	1.55	6.69	0.26	1.32	1.10	6.69	5.73	3.41	3.72	12.48	11.52	ns
100 $\mu\text{A}$	4 mA	Std.	1.55	6.69	0.26	1.32	1.10	6.69	5.73	3.41	3.72	12.48	11.52	ns
100 $\mu\text{A}$	6 mA	Std.	1.55	5.58	0.26	1.32	1.10	5.58	5.01	3.77	4.35	11.36	10.79	ns
100 $\mu\text{A}$	8 mA	Std.	1.55	5.58	0.26	1.32	1.10	5.58	5.01	3.77	4.35	11.36	10.79	ns
100 $\mu\text{A}$	12 mA	Std.	1.55	4.82	0.26	1.32	1.10	4.82	4.44	4.02	4.76	10.61	10.23	ns
100 $\mu\text{A}$	16 mA	Std.	1.55	4.82	0.26	1.32	1.10	4.82	4.44	4.02	4.76	10.61	10.23	ns

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is  $\pm 100 \mu\text{A}$ . Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

**Table 2-76 • 3.3 V LVCMOS Wide Range High Slew – Applies to 1.2 V DC Core Voltage**  
**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.7**  
**Applicable to Standard Plus Banks**

Drive Strength	Equivalent Software Default Drive Strength Option <sup>1</sup>	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
100 $\mu\text{A}$	2 mA	Std.	1.55	4.10	0.26	1.32	1.10	4.10	3.30	3.40	3.92	9.89	9.09	ns
100 $\mu\text{A}$	4 mA	Std.	1.55	4.10	0.26	1.32	1.10	4.10	3.30	3.40	3.92	9.89	9.09	ns
100 $\mu\text{A}$	6 mA	Std.	1.55	3.51	0.26	1.32	1.10	3.51	2.79	3.76	4.56	9.30	8.57	ns
100 $\mu\text{A}$	8 mA	Std.	1.55	3.51	0.26	1.32	1.10	3.51	2.79	3.76	4.56	9.30	8.57	ns
100 $\mu\text{A}$	12 mA	Std.	1.55	3.20	0.26	1.32	1.10	3.20	2.52	4.01	4.97	8.99	8.31	ns
100 $\mu\text{A}$	16 mA	Std.	1.55	3.20	0.26	1.32	1.10	3.20	2.52	4.01	4.97	8.99	8.31	ns

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is  $\pm 100 \mu\text{A}$ . Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.
3. Software default selection highlighted in gray.

## 2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications.

**Table 2-79 • Minimum and Maximum DC Input and Output Levels  
Applicable to Advanced I/O Banks**

2.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL <sup>1</sup>	IIH <sup>2</sup>
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>3</sup>	Max. mA <sup>3</sup>	μA <sup>4</sup>	μA <sup>4</sup>
2 mA	-0.3	0.7	1.7	2.7	0.7	1.7	2	2	16	18	10	10
4 mA	-0.3	0.7	1.7	2.7	0.7	1.7	4	4	16	18	10	10
6 mA	-0.3	0.7	1.7	2.7	0.7	1.7	6	6	32	37	10	10
8 mA	-0.3	0.7	1.7	2.7	0.7	1.7	8	8	32	37	10	10
12 mA	-0.3	0.7	1.7	2.7	0.7	1.7	12	12	65	74	10	10
16 mA	-0.3	0.7	1.7	2.7	0.7	1.7	16	16	83	87	10	10
24 mA	-0.3	0.7	1.7	2.7	0.7	1.7	24	24	169	124	10	10

Notes:

1. *IIL* is the input leakage current per I/O pin over recommended operation conditions where  $-0.3 \text{ V} < \text{VIN} < \text{VIL}$ .
2. *IIH* is the input leakage current per I/O pin over recommended operating conditions  $\text{VIH} < \text{VIN} < \text{VCCI}$ . Input current is larger when operating outside recommended ranges
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

**Table 2-80 • Minimum and Maximum DC Input and Output Levels  
Applicable to Standard Plus I/O Banks**

2.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL <sup>1</sup>	IIH <sup>2</sup>
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>3</sup>	Max. mA <sup>3</sup>	μA <sup>4</sup>	μA <sup>4</sup>
2 mA	-0.3	0.7	1.7	2.7	0.7	1.7	2	2	16	18	10	10
4 mA	-0.3	0.7	1.7	2.7	0.7	1.7	4	4	16	18	10	10
6 mA	-0.3	0.7	1.7	2.7	0.7	1.7	6	6	32	37	10	10
8 mA	-0.3	0.7	1.7	2.7	0.7	1.7	8	8	32	37	10	10
12 mA	-0.3	0.7	1.7	2.7	0.7	1.7	12	12	65	74	10	10

Notes:

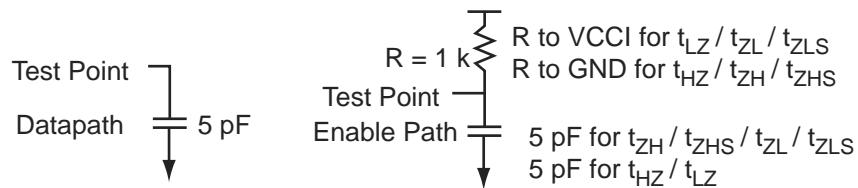
1. *IIL* is the input leakage current per I/O pin over recommended operation conditions where  $-0.3 \text{ V} < \text{VIN} < \text{VIL}$ .
2. *IIH* is the input leakage current per I/O pin over recommended operating conditions  $\text{VIH} < \text{VIN} < \text{VCCI}$ . Input current is larger when operating outside recommended ranges
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

**Table 2-81 • Minimum and Maximum DC Input and Output Levels Applicable to Standard I/O Banks**

2.5 V LVC MOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL <sup>1</sup>	IIH <sup>2</sup>
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>3</sup>	Max. mA <sup>3</sup>	µA <sup>4</sup>	µA <sup>4</sup>
2 mA	-0.3	0.7	1.7	3.6	0.7	1.7	2	2	16	18	10	10
4 mA	-0.3	0.7	1.7	3.6	0.7	1.7	4	4	16	18	10	10
6 mA	-0.3	0.7	1.7	3.6	0.7	1.7	6	6	32	37	10	10
8 mA	-0.3	0.7	1.7	3.6	0.7	1.7	8	8	32	37	10	10

Notes:

1. *IIL* is the input leakage current per I/O pin over recommended operation conditions where  $-0.3 \text{ V} < \text{VIN} < \text{VIL}$ .
2. *IIH* is the input leakage current per I/O pin over recommended operating conditions  $\text{VIH} < \text{VIN} < \text{VCCI}$ . Input current is larger when operating outside recommended ranges
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.



**Figure 2-8 • AC Loading**

**Table 2-82 • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	C <sub>LOAD</sub> (pF)
0	2.5	1.2	5

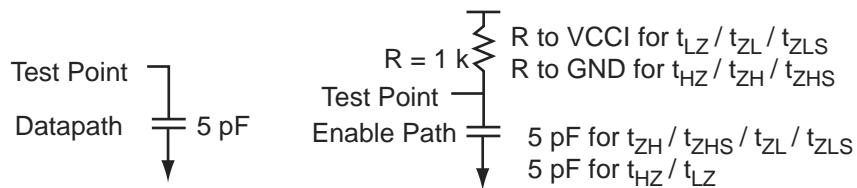
Note: \*Measuring point =  $\text{Vtrip}$ . See Table 2-29 on page 2-28 for a complete table of trip points.

**Table 2-97 • Minimum and Maximum DC Input and Output Levels Applicable to Standard I/O Banks**

1.8 V LVC MOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL <sup>1</sup>	IIH <sup>2</sup>
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>3</sup>	Max. mA <sup>3</sup>	µA <sup>4</sup>	µA <sup>4</sup>
2 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI - 0.45	2	2	9	11	10	10
4 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI - 0.45	4	4	17	22	10	10

Notes:

1. *IIL* is the input leakage current per I/O pin over recommended operation conditions where  $-0.3 \text{ V} < \text{VIN} < \text{VIL}$ .
2. *IIH* is the input leakage current per I/O pin over recommended operating conditions  $\text{VIH} < \text{VIN} < \text{VCCI}$ . Input current is larger when operating outside recommended ranges.
3. Currents are measured at  $100^\circ\text{C}$  junction temperature and maximum voltage.
4. Currents are measured at  $85^\circ\text{C}$  junction temperature.
5. Software default selection highlighted in gray.

**Figure 2-9 • AC Loading****Table 2-98 • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	C <sub>LOAD</sub> (pF)
0	1.8	0.9	5

Note: \*Measuring point = Vtrip. See Table 2-29 on page 2-28 for a complete table of trip points.

**Timing Characteristics****1.5 V DC Core Voltage****Table 2-99 • 1.8 V LVC MOS Low Slew – Applies to 1.5 V DC Core Voltage**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V  
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>ZHS</sub>	Units
2 mA	Std.	0.97	6.38	0.18	1.01	0.66	6.51	5.93	2.33	1.56	10.10	9.53	ns
4 mA	Std.	0.97	5.35	0.18	1.01	0.66	5.46	5.04	2.67	2.38	9.05	8.64	ns
6 mA	Std.	0.97	4.62	0.18	1.01	0.66	4.71	4.44	2.90	2.79	8.31	8.04	ns
8 mA	Std.	0.97	4.37	0.18	1.01	0.66	4.46	4.31	2.95	2.89	8.05	7.90	ns
12 mA	Std.	0.97	4.32	0.18	1.01	0.66	4.37	4.32	3.03	3.30	7.97	7.92	ns
16 mA	Std.	0.97	4.32	0.18	1.01	0.66	4.37	4.32	3.03	3.30	7.97	7.92	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

**Table 2-107 • 1.8 V LVC MOS Low Slew – Applies to 1.2 V DC Core Voltage**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V

Applicable to Standard Plus Banks

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
2 mA	Std.	1.55	6.32	0.26	1.11	1.10	6.43	5.81	2.47	2.16	12.22	11.60	ns
4 mA	Std.	1.55	5.27	0.26	1.11	1.10	5.35	5.01	2.78	2.92	11.14	10.79	ns
6 mA	Std.	1.55	4.56	0.26	1.11	1.10	4.64	4.44	3.00	3.30	10.42	10.22	ns
8 mA	Std.	1.55	4.56	0.26	1.11	1.10	4.64	4.44	3.00	3.30	10.42	10.22	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

**Table 2-108 • 1.8 V LVC MOS High Slew – Applies to 1.2 V DC Core Voltage**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V

Applicable to Standard Plus Banks

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
2 mA	Std.	1.55	3.22	0.26	1.11	1.10	3.26	3.18	2.47	2.20	9.05	8.97	ns
4 mA	Std.	1.55	2.72	0.26	1.11	1.10	2.75	2.50	2.78	3.01	8.54	8.29	ns
6 mA	Std.	1.55	2.43	0.26	1.11	1.10	2.47	2.16	2.99	3.39	8.25	7.94	ns
8 mA	Std.	1.55	2.43	0.26	1.11	1.10	2.47	2.16	2.99	3.39	8.25	7.94	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

**Table 2-109 • 1.8 V LVC MOS Low Slew – Applies to 1.2 V DC Core Voltage**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V

Applicable to Standard Banks

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
2 mA	Std.	1.55	6.13	0.26	1.08	1.10	6.24	5.79	2.08	1.78	ns		
4 mA	Std.	1.55	5.17	0.26	1.08	1.10	5.26	4.98	2.38	2.54	ns		

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

**Table 2-110 • 1.8 V LVC MOS High Slew – Applies to 1.2 V DC Core Voltage**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.7 V

Applicable to Standard Banks

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
2 mA	Std.	3.06	0.26	1.08	1.10	3.10	3.01	2.08	1.83	3.06	ns		
4 mA	Std.	2.60	0.26	1.08	1.10	2.64	2.33	2.38	2.62	2.60	ns		

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

## 1.5 V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.5 V applications. It uses a 1.5 V input buffer and a push-pull output buffer.

**Table 2-111 • Minimum and Maximum DC Input and Output Levels  
Applicable to Advanced I/O Banks**

1.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL <sup>1</sup>	IIH <sup>2</sup>
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>3</sup>	Max. mA <sup>3</sup>	μA <sup>4</sup>	μA <sup>4</sup>
2 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	2	2	13	16	10	10
4 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	4	4	25	33	10	10
6 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	6	6	32	39	10	10
8 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	8	8	66	55	10	10
12 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	12	12	66	55	10	10

Notes:

1. *IIL* is the input leakage current per I/O pin over recommended operation conditions where  $-0.3 \text{ V} < \text{VIN} < \text{VIL}$ .
2. *IIH* is the input leakage current per I/O pin over recommended operating conditions  $\text{VIH} < \text{VIN} < \text{VCCI}$ . Input current is larger when operating outside recommended ranges
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

**Table 2-112 • Minimum and Maximum DC Input and Output Levels  
Applicable to Standard Plus I/O Banks**

1.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL <sup>1</sup>	IIH <sup>2</sup>
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>3</sup>	Max. mA <sup>3</sup>	μA <sup>4</sup>	μA <sup>4</sup>
2 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	2	2	13	16	10	10
4 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	4	4	25	33	10	10

Notes:

1. *IIL* is the input leakage current per I/O pin over recommended operation conditions where  $-0.3 \text{ V} < \text{VIN} < \text{VIL}$ .
2. *IIH* is the input leakage current per I/O pin over recommended operating conditions  $\text{VIH} < \text{VIN} < \text{VCCI}$ . Input current is larger when operating outside recommended ranges
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

## I/O Register Specifications

### Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

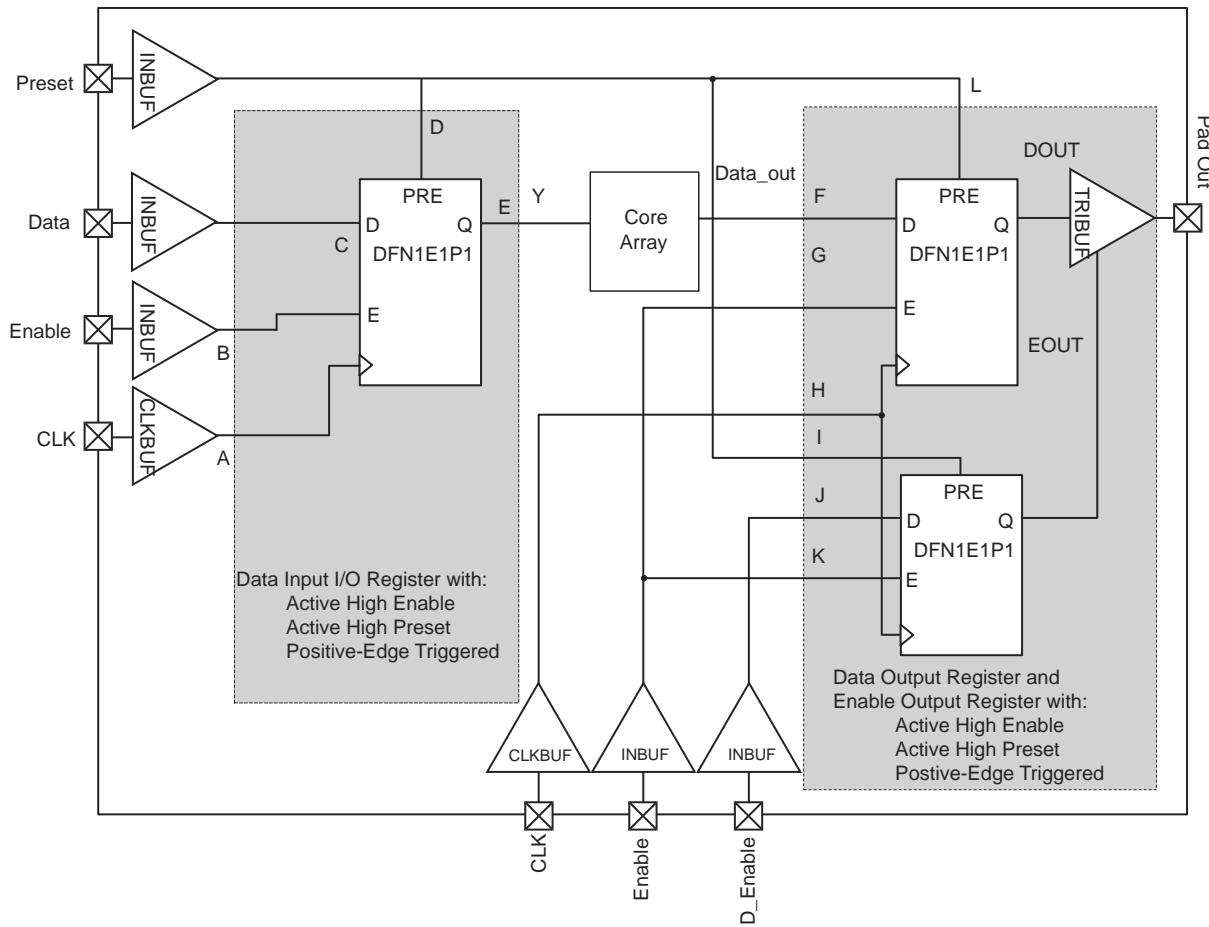


Figure 2-16 • Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

## DDR Module Specifications

### *Input DDR Module*

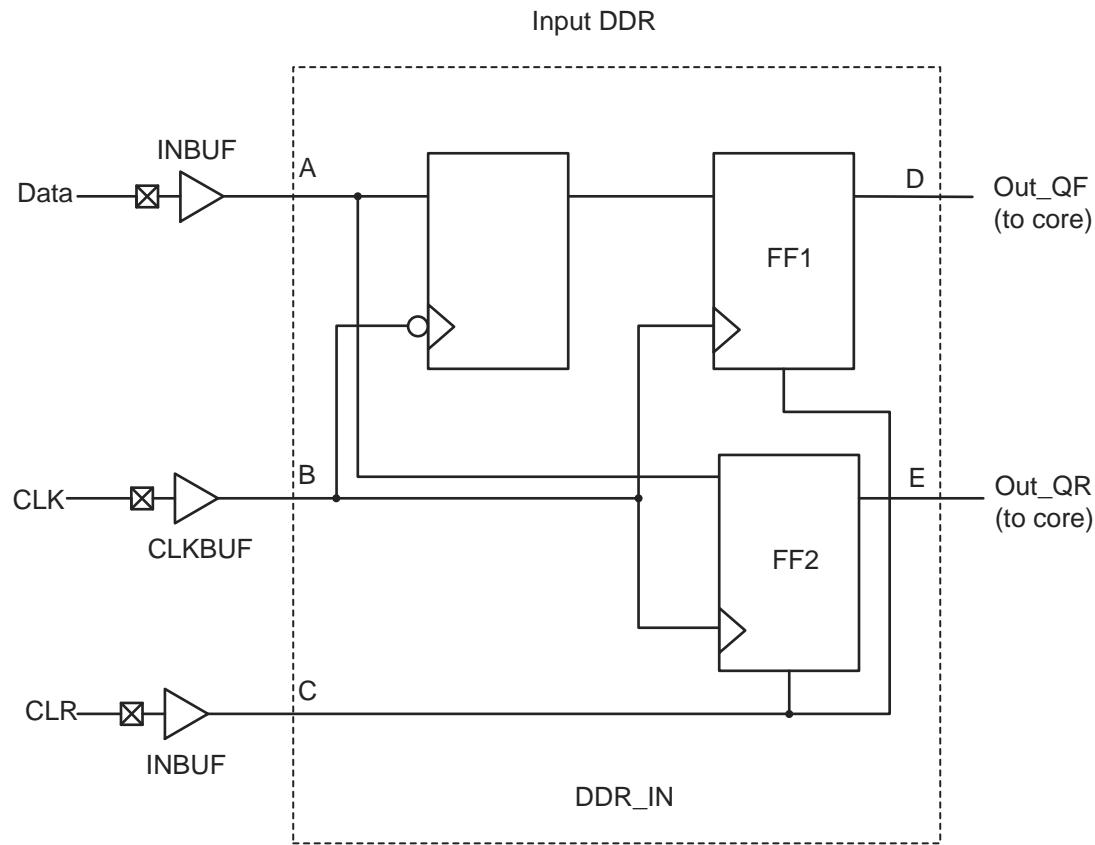


Figure 2-21 • Input DDR Timing Model

Table 2-163 • Parameter Definitions

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR	B, D
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF	B, E
$t_{DDRISUD}$	Data Setup Time of DDR input	A, B
$t_{DDRIHD}$	Data Hold Time of DDR input	A, B
$t_{DDRICLR2Q1}$	Clear-to-Out Out_QR	C, D
$t_{DDRICLR2Q2}$	Clear-to-Out Out_QF	C, E
$t_{DDRIREMCLR}$	Clear Removal	C, B
$t_{DDRIRECCLR}$	Clear Recovery	C, B

## Global Tree Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard-dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to the "Clock Conditioning Circuits" section on page 2-115. Table 2-173 to Table 2-188 on page 2-114 present minimum and maximum global clock delays within each device. Minimum and maximum delays are measured with minimum and maximum loading.

### Timing Characteristics

#### 1.5 V DC Core Voltage

**Table 2-173 • AGL015 Global Resource**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ ,  $V_{CC} = 1.425 \text{ V}$ 

Parameter	Description	Std.		Units
		Min. <sup>1</sup>	Max. <sup>2</sup>	
$t_{RCKL}$	Input Low Delay for Global Clock	1.21	1.42	ns
$t_{RCKH}$	Input High Delay for Global Clock	1.23	1.49	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.18		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.15		ns
$t_{RCKSW}$	Maximum Skew for Global Clock		0.27	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

**Table 2-174 • AGL030 Global Resource**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ ,  $V_{CC} = 1.425 \text{ V}$ 

Parameter	Description	Std.		Units
		Min. <sup>1</sup>	Max. <sup>2</sup>	
$t_{RCKL}$	Input Low Delay for Global Clock	1.21	1.42	ns
$t_{RCKH}$	Input High Delay for Global Clock	1.23	1.49	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.18		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.15		ns
$t_{RCKSW}$	Maximum Skew for Global Clock		0.27	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

**Table 2-183 • AGL060 Global Resource**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ ,  $V_{CC} = 1.14 \text{ V}$ 

Parameter	Description	Std.		Units
		Min. <sup>1</sup>	Max. <sup>2</sup>	
$t_{RCKL}$	Input Low Delay for Global Clock	2.04	2.33	ns
$t_{RCKH}$	Input High Delay for Global Clock	2.10	2.51	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
$t_{RCKSW}$	Maximum Skew for Global Clock		0.40	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

**Table 2-184 • AGL125 Global Resource**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ ,  $V_{CC} = 1.14 \text{ V}$ 

Parameter	Description	Std.		Units
		Min. <sup>1</sup>	Max. <sup>2</sup>	
$t_{RCKL}$	Input Low Delay for Global Clock	2.08	2.54	ns
$t_{RCKH}$	Input High Delay for Global Clock	2.15	2.77	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
$t_{RCKSW}$	Maximum Skew for Global Clock		0.62	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

QN132	
Pin Number	AGL030 Function
A1	IO80RSB1
A2	IO77RSB1
A3	NC
A4	IO76RSB1
A5	GEC0/IO73RSB1
A6	NC
A7	GEB0/IO71RSB1
A8	IO69RSB1
A9	NC
A10	VCC
A11	IO67RSB1
A12	IO64RSB1
A13	IO59RSB1
A14	IO56RSB1
A15	NC
A16	IO55RSB1
A17	IO53RSB1
A18	VCC
A19	IO50RSB1
A20	IO48RSB1
A21	IO45RSB1
A22	IO44RSB1
A23	IO43RSB1
A24	TDI
A25	TRST
A26	IO40RSB0
A27	NC
A28	IO39RSB0
A29	IO38RSB0
A30	IO36RSB0
A31	IO35RSB0
A32	GDC0/IO32RSB0
A33	NC
A34	VCC
A35	IO30RSB0
A36	IO27RSB0

QN132	
Pin Number	AGL030 Function
A37	IO22RSB0
A38	IO19RSB0
A39	NC
A40	IO18RSB0
A41	IO16RSB0
A42	IO14RSB0
A43	VCC
A44	IO11RSB0
A45	IO08RSB0
A46	IO06RSB0
A47	IO05RSB0
A48	IO02RSB0
B1	IO81RSB1
B2	IO78RSB1
B3	GND
B4	IO75RSB1
B5	NC
B6	GND
B7	IO70RSB1
B8	NC
B9	GND
B10	IO66RSB1
B11	IO63RSB1
B12	FF/IO60RSB1
B13	IO57RSB1
B14	GND
B15	IO54RSB1
B16	IO52RSB1
B17	GND
B18	IO49RSB1
B19	IO46RSB1
B20	GND
B21	IO42RSB1
B22	TMS
B23	TDO
B24	IO41RSB0

QN132	
Pin Number	AGL030 Function
B25	GND
B26	NC
B27	IO37RSB0
B28	GND
B29	GDA0/IO33RSB0
B30	NC
B31	GND
B32	IO29RSB0
B33	IO26RSB0
B34	IO23RSB0
B35	IO20RSB0
B36	GND
B37	IO17RSB0
B38	IO15RSB0
B39	GND
B40	IO12RSB0
B41	IO09RSB0
B42	GND
B43	IO04RSB0
B44	IO01RSB0
C1	IO82RSB1
C2	IO79RSB1
C3	NC
C4	IO74RSB1
C5	GEA0/IO72RSB1
C6	NC
C7	NC
C8	VCCIB1
C9	IO65RSB1
C10	IO62RSB1
C11	IO61RSB1
C12	IO58RSB1
C13	NC
C14	NC
C15	IO51RSB1
C16	VCCIB1

<b>VQ100</b>	
<b>Pin Number</b>	<b>AGL250 Function</b>
1	GND
2	GAA2/IO118UDB3
3	IO118VDB3
4	GAB2/IO117UDB3
5	IO117VDB3
6	GAC2/IO116UDB3
7	IO116VDB3
8	IO112PSB3
9	GND
10	GFB1/IO109PDB3
11	GFB0/IO109NDB3
12	VCOMPLF
13	GFA0/IO108NPB3
14	VCCPLF
15	GFA1/IO108PPB3
16	GFA2/IO107PSB3
17	VCC
18	VCCIB3
19	GFC2/IO105PSB3
20	GEC1/IO100PDB3
21	GEC0/IO100NDB3
22	GEA1/IO98PDB3
23	GEA0/IO98NDB3
24	VMV3
25	GNDQ
26	GEA2/IO97RSB2
27	FF/GEB2/IO96RSB2
28	GEC2/IO95RSB2
29	IO93RSB2
30	IO92RSB2
31	IO91RSB2
32	IO90RSB2
33	IO88RSB2
34	IO86RSB2
35	IO85RSB2
36	IO84RSB2

<b>VQ100</b>	
<b>Pin Number</b>	<b>AGL250 Function</b>
37	VCC
38	GND
39	VCCIB2
40	IO77RSB2
41	IO74RSB2
42	IO71RSB2
43	GDC2/IO63RSB2
44	GDB2/IO62RSB2
45	GDA2/IO61RSB2
46	GNDQ
47	TCK
48	TDI
49	TMS
50	VMV2
51	GND
52	VPUMP
53	NC
54	TDO
55	TRST
56	VJTAG
57	GDA1/IO60USB1
58	GDC0/IO58VDB1
59	GDC1/IO58UDB1
60	IO52NDB1
61	GCB2/IO52PDB1
62	GCA1/IO50PDB1
63	GCA0/IO50NDB1
64	GCC0/IO48NDB1
65	GCC1/IO48PDB1
66	VCCIB1
67	GND
68	VCC
69	IO43NDB1
70	GBC2/IO43PDB1
71	GBB2/IO42PSB1
72	IO41NDB1

<b>VQ100</b>	
<b>Pin Number</b>	<b>AGL250 Function</b>
73	GBA2/IO41PDB1
74	VMV1
75	GNDQ
76	GBA1/IO40RSB0
77	GBA0/IO39RSB0
78	GBB1/IO38RSB0
79	GBB0/IO37RSB0
80	GBC1/IO36RSB0
81	GBC0/IO35RSB0
82	IO29RSB0
83	IO27RSB0
84	IO25RSB0
85	IO23RSB0
86	IO21RSB0
87	VCCIB0
88	GND
89	VCC
90	IO15RSB0
91	IO13RSB0
92	IO11RSB0
93	GAC1/IO05RSB0
94	GAC0/IO04RSB0
95	GAB1/IO03RSB0
96	GAB0/IO02RSB0
97	GAA1/IO01RSB0
98	GAA0/IO00RSB0
99	GNDQ
100	VMV0

FG256	
Pin Number	AGL400 Function
A1	GND
A2	GAA0/IO00RSB0
A3	GAA1/IO01RSB0
A4	GAB0/IO02RSB0
A5	IO16RSB0
A6	IO17RSB0
A7	IO22RSB0
A8	IO28RSB0
A9	IO34RSB0
A10	IO37RSB0
A11	IO41RSB0
A12	IO43RSB0
A13	GBB1/IO57RSB0
A14	GBA0/IO58RSB0
A15	GBA1/IO59RSB0
A16	GND
B1	GAB2/IO154UDB3
B2	GAA2/IO155UDB3
B3	IO12RSB0
B4	GAB1/IO03RSB0
B5	IO13RSB0
B6	IO14RSB0
B7	IO21RSB0
B8	IO27RSB0
B9	IO32RSB0
B10	IO38RSB0
B11	IO42RSB0
B12	GBC1/IO55RSB0
B13	GBB0/IO56RSB0
B14	IO44RSB0
B15	GBA2/IO60PDB1
B16	IO60NDB1
C1	IO154VDB3
C2	IO155VDB3
C3	IO11RSB0
C4	IO07RSB0
C5	GAC0/IO04RSB0
C6	GAC1/IO05RSB0

FG256	
Pin Number	AGL400 Function
C7	IO20RSB0
C8	IO24RSB0
C9	IO33RSB0
C10	IO39RSB0
C11	IO45RSB0
C12	GBC0/IO54RSB0
C13	IO48RSB0
C14	VMV0
C15	IO61NPB1
C16	IO63PDB1
D1	IO151VDB3
D2	IO151UDB3
D3	GAC2/IO153UDB3
D4	IO06RSB0
D5	GNDQ
D6	IO10RSB0
D7	IO19RSB0
D8	IO26RSB0
D9	IO30RSB0
D10	IO40RSB0
D11	IO46RSB0
D12	GNDQ
D13	IO47RSB0
D14	GBB2/IO61PPB1
D15	IO53RSB0
D16	IO63NDB1
E1	IO150PDB3
E2	IO08RSB0
E3	IO153VDB3
E4	IO152VDB3
E5	VMV0
E6	VCCIB0
E7	VCCIB0
E8	IO25RSB0
E9	IO31RSB0
E10	VCCIB0
E11	VCCIB0
E12	VMV1

FG256	
Pin Number	AGL400 Function
E13	GBC2/IO62PDB1
E14	IO65RSB1
E15	IO52RSB0
E16	IO66PDB1
F1	IO150NDB3
F2	IO149NPB3
F3	IO09RSB0
F4	IO152UDB3
F5	VCCIB3
F6	GND
F7	VCC
F8	VCC
F9	VCC
F10	VCC
F11	GND
F12	VCCIB1
F13	IO62NDB1
F14	IO49RSB0
F15	IO64PPB1
F16	IO66NDB1
G1	IO148NDB3
G2	IO148PDB3
G3	IO149PPB3
G4	GFC1/IO147PPB3
G5	VCCIB3
G6	VCC
G7	GND
G8	GND
G9	GND
G10	GND
G11	VCC
G12	VCCIB1
G13	GCC1/IO67PPB1
G14	IO64NPB1
G15	IO73PDB1
G16	IO73NDB1
H1	GFB0/IO146NPB3
H2	GFA0/IO145NDB3

<b>FG256</b>	
<b>Pin Number</b>	<b>AGL1000 Function</b>
H3	GFB1/IO208PPB3
H4	VCOMPLF
H5	GFC0/IO209NPB3
H6	VCC
H7	GND
H8	GND
H9	GND
H10	GND
H11	VCC
H12	GCC0/IO91NPB1
H13	GCB1/IO92PPB1
H14	GCA0/IO93NPB1
H15	IO96NPB1
H16	GCB0/IO92NPB1
J1	GFA2/IO206PSB3
J2	GFA1/IO207PDB3
J3	VCCPLF
J4	IO205NDB3
J5	GFB2/IO205PDB3
J6	VCC
J7	GND
J8	GND
J9	GND
J10	GND
J11	VCC
J12	GCB2/IO95PPB1
J13	GCA1/IO93PPB1
J14	GCC2/IO96PPB1
J15	IO100PPB1
J16	GCA2/IO94PSB1
K1	GFC2/IO204PDB3
K2	IO204NDB3
K3	IO203NDB3
K4	IO203PDB3
K5	VCCIB3
K6	VCC
K7	GND
K8	GND

<b>FG256</b>	
<b>Pin Number</b>	<b>AGL1000 Function</b>
K9	GND
K10	GND
K11	VCC
K12	VCCIB1
K13	IO95NPB1
K14	IO100NPB1
K15	IO102NDB1
K16	IO102PDB1
L1	IO202NDB3
L2	IO202PDB3
L3	IO196PPB3
L4	IO193PPB3
L5	VCCIB3
L6	GND
L7	VCC
L8	VCC
L9	VCC
L10	VCC
L11	GND
L12	VCCIB1
L13	GDB0/IO112NPB1
L14	IO106NDB1
L15	IO106PDB1
L16	IO107PDB1
M1	IO197NSB3
M2	IO196NPB3
M3	IO193NPB3
M4	GEC0/IO190NPB3
M5	VMV3
M6	VCCIB2
M7	VCCIB2
M8	IO147RSB2
M9	IO136RSB2
M10	VCCIB2
M11	VCCIB2
M12	VMV2
M13	IO110NDB1
M14	GDB1/IO112PPB1

<b>FG256</b>	
<b>Pin Number</b>	<b>AGL1000 Function</b>
M15	GDC1/IO111PDB1
M16	IO107NDB1
N1	IO194PSB3
N2	IO192PPB3
N3	GEC1/IO190PPB3
N4	IO192NPB3
N5	GNDQ
N6	GEA2/IO187RSB2
N7	IO161RSB2
N8	IO155RSB2
N9	IO141RSB2
N10	IO129RSB2
N11	IO124RSB2
N12	GNDQ
N13	IO110PDB1
N14	VJTAG
N15	GDC0/IO111NDB1
N16	GDA1/IO113PDB1
P1	GEB1/IO189PDB3
P2	GEB0/IO189NDB3
P3	VMV2
P4	IO179RSB2
P5	IO171RSB2
P6	IO165RSB2
P7	IO159RSB2
P8	IO151RSB2
P9	IO137RSB2
P10	IO134RSB2
P11	IO128RSB2
P12	VMV1
P13	TCK
P14	VPUMP
P15	TRST
P16	GDA0/IO113NDB1
R1	GEA1/IO188PDB3
R2	GEA0/IO188NDB3
R3	IO184RSB2
R4	GEC2/IO185RSB2

<b>FG484</b>	
<b>Pin Number</b>	<b>AGL400 Function</b>
N17	IO74RSB1
N18	IO72NPB1
N19	IO70NDB1
N20	NC
N21	NC
N22	NC
P1	NC
P2	NC
P3	NC
P4	IO142NDB3
P5	IO141NPB3
P6	IO125RSB2
P7	IO139RSB3
P8	VCCIB3
P9	GND
P10	VCC
P11	VCC
P12	VCC
P13	VCC
P14	GND
P15	VCCIB1
P16	GDB0/IO78VPB1
P17	IO76VDB1
P18	IO76UDB1
P19	IO75PDB1
P20	NC
P21	NC
P22	NC
R1	NC
R2	NC
R3	VCC
R4	IO140PDB3
R5	IO130RSB2
R6	IO138NPB3
R7	GEC0/IO137NPB3
R8	VMV3

<b>FG484</b>	
<b>Pin Number</b>	<b>AGL600 Function</b>
U1	IO149PDB3
U2	IO149NDB3
U3	NC
U4	GEB1/IO145PDB3
U5	GEB0/IO145NDB3
U6	VMV2
U7	IO138RSB2
U8	IO136RSB2
U9	IO131RSB2
U10	IO124RSB2
U11	IO119RSB2
U12	IO107RSB2
U13	IO104RSB2
U14	IO97RSB2
U15	VMV1
U16	TCK
U17	VPUMP
U18	TRST
U19	GDA0/IO88NDB1
U20	NC
U21	IO83NDB1
U22	NC
V1	NC
V2	NC
V3	GND
V4	GEA1/IO144PDB3
V5	GEA0/IO144NDB3
V6	IO139RSB2
V7	GEC2/IO141RSB2
V8	IO132RSB2
V9	IO127RSB2
V10	IO121RSB2
V11	IO114RSB2
V12	IO109RSB2
V13	IO105RSB2
V14	IO98RSB2

*Package Pin Assignments*

<b>FG484</b>	
<b>Pin Number</b>	<b>AGL1000 Function</b>
B7	IO15RSB0
B8	IO19RSB0
B9	IO24RSB0
B10	IO31RSB0
B11	IO39RSB0
B12	IO48RSB0
B13	IO54RSB0
B14	IO58RSB0
B15	IO63RSB0
B16	IO66RSB0
B17	IO68RSB0
B18	IO70RSB0
B19	NC
B20	NC
B21	VCCIB1
B22	GND
C1	VCCIB3
C2	IO220PDB3
C3	NC
C4	NC
C5	GND
C6	IO10RSB0
C7	IO14RSB0
C8	VCC
C9	VCC
C10	IO30RSB0
C11	IO37RSB0
C12	IO43RSB0
C13	NC
C14	VCC
C15	VCC
C16	NC
C17	NC
C18	GND
C19	NC
C20	NC