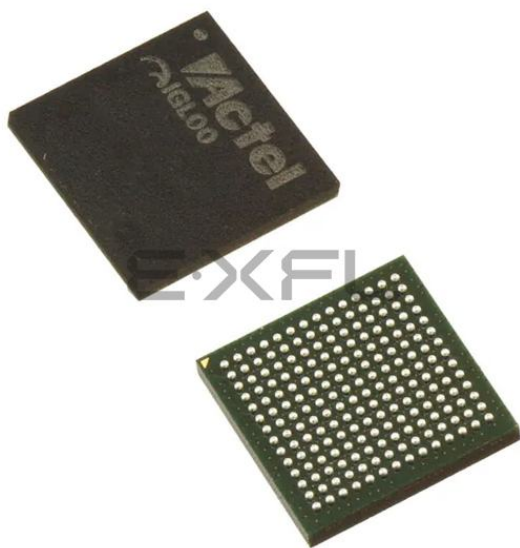




Welcome to [E-XFL.COM](#)

Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	3072
Total RAM Bits	36864
Number of I/O	133
Number of Gates	125000
Voltage - Supply	1.14V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	196-TFBGA, CSBGA
Supplier Device Package	196-CSP (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/agl125v2-cs196

Wide Range I/O Support

IGLOO devices support JEDEC-defined wide range I/O operation. IGLOO devices support both the JESD8-B specification, covering 3 V and 3.3 V supplies, for an effective operating range of 2.7 V to 3.6 V, and JESD8-12 with its 1.2 V nominal, supporting an effective operating range of 1.14 V to 1.575 V.

Wider I/O range means designers can eliminate power supplies or power conditioning components from the board or move to less costly components with greater tolerances. Wide range eases I/O bank management and provides enhanced protection from system voltage spikes, while providing the flexibility to easily run custom voltage applications.

Specifying I/O States During Programming

You can modify the I/O states during programming in FlashPro. In FlashPro, this feature is supported for PDB files generated from Designer v8.5 or greater. See the *FlashPro User Guide* for more information.

Note: PDB files generated from Designer v8.1 to Designer v8.4 (including all service packs) have limited display of Pin Numbers only.

1. Load a PDB from the FlashPro GUI. You must have a PDB loaded to modify the I/O states during programming.
2. From the FlashPro GUI, click PDB Configuration. A FlashPoint – Programming File Generator window appears.
3. Click the Specify I/O States During Programming button to display the Specify I/O States During Programming dialog box.
4. Sort the pins as desired by clicking any of the column headers to sort the entries by that header. Select the I/Os you wish to modify (Figure 1-5 on page 1-9).
5. Set the I/O Output State. You can set Basic I/O settings if you want to use the default I/O settings for your pins, or use Custom I/O settings to customize the settings for each pin. Basic I/O state settings:

1 – I/O is set to drive out logic High

0 – I/O is set to drive out logic Low

Last Known State – I/O is set to the last value that was driven out prior to entering the programming mode, and then held at that value during programming

Z -Tri-State: I/O is tristated

Table 2-17 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings¹
Applicable to Standard Plus I/O Banks

	C _{LOAD} (pF)	VCCI (V)	Static Power PDC7 (mW) ²	Dynamic Power PAC10 (μW/MHz) ³
Single-Ended				
3.3 V LVTTTL / 3.3 V LVCMOS	5	3.3	–	122.16
3.3 V LVCMOS Wide Range ⁴	5	3.3	–	122.16
2.5 V LVCMOS	5	2.5	–	68.37
1.8 V LVCMOS	5	1.8	–	34.53
1.5 V LVCMOS (JESD8-11)	5	1.5	–	23.66
1.2 V LVCMOS ⁵	5	1.2	–	14.90
1.2 V LVCMOS Wide Range ⁵	5	1.2	–	14.90
3.3 V PCI	10	3.3	–	181.06
3.3 V PCI-X	10	3.3	–	181.06

Notes:

1. Dynamic power consumption is given for standard load and software default drive strength and output slew.
2. P_{DC7} is the static power (where applicable) measured on VCCI.
3. P_{AC10} is the total dynamic power measured on VCCI.
4. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.
5. Applicable for IGLOO V2 devices only.

Table 2-18 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings¹
Applicable to Standard I/O Banks

	C _{LOAD} (pF)	VCCI (V)	Static Power PDC7 (mW) ²	Dynamic Power PAC10 (μW/MHz) ³
Single-Ended				
3.3 V LVTTTL / 3.3 V LVCMOS	5	3.3	–	104.38
3.3 V LVCMOS Wide Range ⁴	5	3.3	–	104.38
2.5 V LVCMOS	5	2.5	–	59.86
1.8 V LVCMOS	5	1.8	–	31.26
1.5 V LVCMOS (JESD8-11)	5	1.5	–	21.96
1.2 V LVCMOS ⁵	5	1.2	–	13.49
1.2 V LVCMOS Wide Range ⁵	5	1.2	–	13.49

Notes:

1. Dynamic power consumption is given for standard load and software default drive strength and output slew.
2. PDC7 is the static power (where applicable) measured on VCCI.
3. PAC10 is the total dynamic power measured on VCCI.
4. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.
5. Applicable for IGLOO V2 devices only.

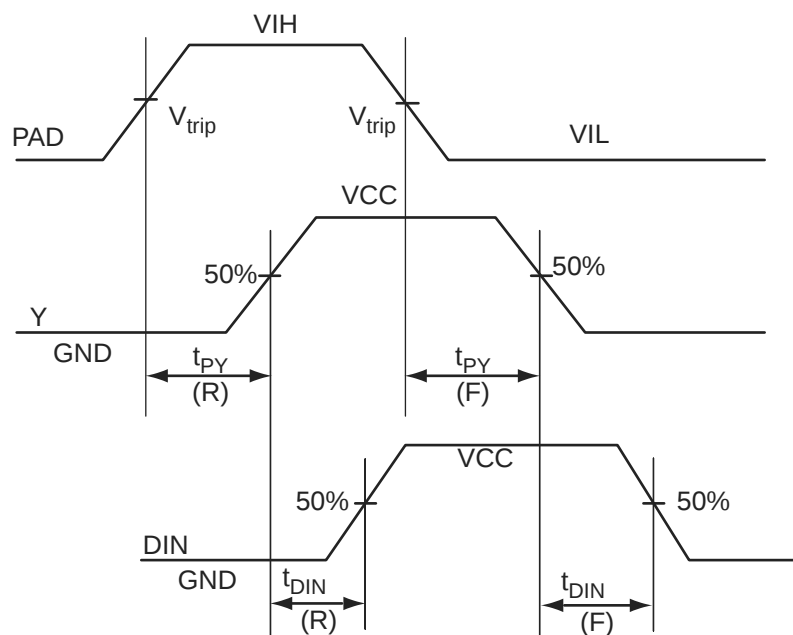
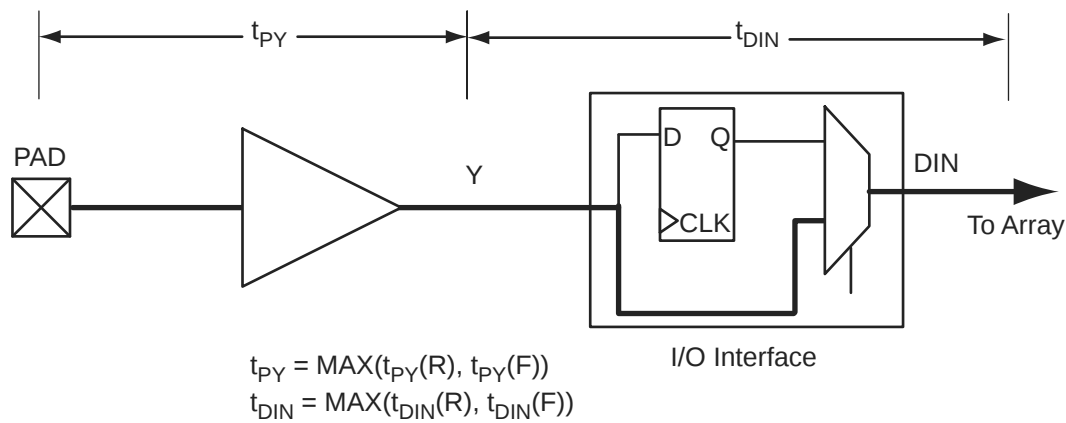


Figure 2-4 • Input Buffer Timing Model and Delays (example)

**Table 2-28 • Summary of Maximum and Minimum DC Input Levels
Applicable to Commercial and Industrial Conditions**

DC I/O Standards	Commercial ¹		Industrial ²	
	IIL ⁴	IIH ⁵	IIL ⁴	IIH ⁵
	μA	μA	μA	μA
3.3 V LVTTTL / 3.3 V LVCMOS	10	10	15	15
3.3 V LVCMOS Wide Range	10	10	15	15
2.5 V LVCMOS	10	10	15	15
1.8 V LVCMOS	10	10	15	15
1.5 V LVCMOS	10	10	15	15
1.2 V LVCMOS ³	10	10	15	15
1.2 V LVCMOS Wide Range ³	10	10	15	15
3.3 V PCI	10	10	15	15
3.3 V PCI-X	10	10	15	15

Notes:

1. Commercial range ($0^{\circ}\text{C} < T_A < 70^{\circ}\text{C}$)
2. Industrial range ($-40^{\circ}\text{C} < T_A < 85^{\circ}\text{C}$)
3. Applicable to V2 Devices operating at $V_{CCI} \geq V_{CC}$.
4. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
5. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges

Table 2-39 • I/O Output Buffer Maximum Resistances¹
Applicable to Standard Plus I/O Banks

Standard	Drive Strength	$R_{PULL-DOWN}$ (Ω) ²	$R_{PULL-UP}$ (Ω) ³
3.3 V LVTTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	25	75
3.3 V LVCMOS Wide Range	100 μ A	Same as regular 3.3 V LVCMOS	Same as regular 3.3 V LVCMOS
2.5 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
	12 mA	25	50
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
1.2 V LVCMOS ⁴	2 mA	158	164
1.2 V LVCMOS Wide Range ⁴	100 μ A	Same as regular 1.2 V LVCMOS	Same as regular 1.2 V LVCMOS
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75

Notes:

1. These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCI, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located at <http://www.microsemi.com/soc/download/ibis/default.aspx>.
2. $R_{(PULL-DOWN-MAX)} = (VOL_{spec}) / I_{OL_{spec}}$
3. $R_{(PULL-UP-MAX)} = (VCCI_{max} - VOH_{spec}) / I_{OH_{spec}}$
4. Applicable to IGLOO V2 Devices operating at $VCCI \geq VCC$

Applies to 1.2 V DC Core Voltage

Table 2-57 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	5.12	0.26	0.98	1.10	5.20	4.46	2.81	3.02	10.99	10.25	ns
4 mA	Std.	1.55	5.12	0.26	0.98	1.10	5.20	4.46	2.81	3.02	10.99	10.25	ns
6 mA	Std.	1.55	4.38	0.26	0.98	1.10	4.45	3.93	3.07	3.48	10.23	9.72	ns
8 mA	Std.	1.55	4.38	0.26	0.98	1.10	4.45	3.93	3.07	3.48	10.23	9.72	ns
12 mA	Std.	1.55	3.85	0.26	0.98	1.10	3.91	3.53	3.24	3.77	9.69	9.32	ns
16 mA	Std.	1.55	3.69	0.26	0.98	1.10	3.75	3.44	3.28	3.84	9.54	9.23	ns
24 mA	Std.	1.55	3.61	0.26	0.98	1.10	3.67	3.46	3.33	4.13	9.45	9.24	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-58 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	3.33	0.26	0.98	1.10	3.38	2.75	2.82	3.18	9.17	8.54	ns
4 mA	Std.	1.55	3.33	0.26	0.98	1.10	3.38	2.75	2.82	3.18	9.17	8.54	ns
6 mA	Std.	1.55	2.91	0.26	0.98	1.10	2.95	2.37	3.07	3.64	8.73	8.15	ns
8 mA	Std.	1.55	2.91	0.26	0.98	1.10	2.95	2.37	3.07	3.64	8.73	8.15	ns
12 mA	Std.	1.55	2.67	0.26	0.98	1.10	2.71	2.18	3.25	3.93	8.50	7.97	ns
16 mA	Std.	1.55	2.63	0.26	0.98	1.10	2.67	2.14	3.28	4.01	8.45	7.93	ns
24 mA	Std.	1.55	2.65	0.26	0.98	1.10	2.69	2.10	3.33	4.31	8.47	7.89	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-59 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	4.56	0.26	0.97	1.10	4.63	3.98	2.54	2.83	10.42	9.76	ns
4 mA	Std.	1.55	4.56	0.26	0.97	1.10	4.63	3.98	2.54	2.83	10.42	9.76	ns
6 mA	Std.	1.55	3.84	0.26	0.97	1.10	3.90	3.50	2.77	3.24	9.69	9.29	ns
8 mA	Std.	1.55	3.84	0.26	0.97	1.10	3.90	3.50	2.77	3.24	9.69	9.29	ns
12 mA	Std.	1.55	3.35	0.26	0.97	1.10	3.40	3.13	2.93	3.51	9.19	8.91	ns
16 mA	Std.	1.55	3.35	0.26	0.97	1.10	3.40	3.13	2.93	3.51	9.19	8.91	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications.

Table 2-79 • Minimum and Maximum DC Input and Output Levels
Applicable to Advanced I/O Banks

2.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	−0.3	0.7	1.7	2.7	0.7	1.7	2	2	16	18	10	10
4 mA	−0.3	0.7	1.7	2.7	0.7	1.7	4	4	16	18	10	10
6 mA	−0.3	0.7	1.7	2.7	0.7	1.7	6	6	32	37	10	10
8 mA	−0.3	0.7	1.7	2.7	0.7	1.7	8	8	32	37	10	10
12 mA	−0.3	0.7	1.7	2.7	0.7	1.7	12	12	65	74	10	10
16 mA	−0.3	0.7	1.7	2.7	0.7	1.7	16	16	83	87	10	10
24 mA	−0.3	0.7	1.7	2.7	0.7	1.7	24	24	169	124	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

Table 2-80 • Minimum and Maximum DC Input and Output Levels
Applicable to Standard Plus I/O Banks

2.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	−0.3	0.7	1.7	2.7	0.7	1.7	2	2	16	18	10	10
4 mA	−0.3	0.7	1.7	2.7	0.7	1.7	4	4	16	18	10	10
6 mA	−0.3	0.7	1.7	2.7	0.7	1.7	6	6	32	37	10	10
8 mA	−0.3	0.7	1.7	2.7	0.7	1.7	8	8	32	37	10	10
12 mA	−0.3	0.7	1.7	2.7	0.7	1.7	12	12	65	74	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

Timing Characteristics

Applies to 1.5 V DC Core Voltage

Table 2-83 • 2.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V

Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	4.96	0.18	1.08	0.66	5.06	4.59	2.26	2.00	8.66	8.19	ns
4 mA	Std.	0.97	4.96	0.18	1.08	0.66	5.06	4.59	2.26	2.00	8.66	8.19	ns
6 mA	Std.	0.97	4.15	0.18	1.08	0.66	4.24	3.94	2.54	2.51	7.83	7.53	ns
8 mA	Std.	0.97	4.15	0.18	1.08	0.66	4.24	3.94	2.54	2.51	7.83	7.53	ns
12 mA	Std.	0.97	3.57	0.18	1.08	0.66	3.65	3.47	2.73	2.84	7.24	7.06	ns
16 mA	Std.	0.97	3.39	0.18	1.08	0.66	3.46	3.36	2.78	2.92	7.06	6.95	ns
24 mA	Std.	0.97	3.38	0.18	1.08	0.66	3.38	3.38	2.83	3.25	6.98	6.98	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-84 • 2.5 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V

Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	2.77	0.18	1.08	0.66	2.83	2.60	2.26	2.08	6.42	6.19	ns
4 mA	Std.	0.97	2.77	0.18	1.08	0.66	2.83	2.60	2.26	2.08	6.42	6.19	ns
6 mA	Std.	0.97	2.34	0.18	1.08	0.66	2.39	2.08	2.54	2.60	5.99	5.68	ns
8 mA	Std.	0.97	2.34	0.18	1.08	0.66	2.39	2.08	2.54	2.60	5.99	5.68	ns
12 mA	Std.	0.97	2.09	0.18	1.08	0.66	2.14	1.83	2.73	2.93	5.73	5.43	ns
16 mA	Std.	0.97	2.05	0.18	1.08	0.66	2.09	1.78	2.78	3.02	5.69	5.38	ns
24 mA	Std.	0.97	2.06	0.18	1.08	0.66	2.10	1.72	2.83	3.35	5.70	5.32	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-85 • 2.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V

Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	4.42	0.18	1.08	0.66	4.51	4.10	1.96	1.85	8.10	7.69	ns
4 mA	Std.	0.97	4.42	0.18	1.08	0.66	4.51	4.10	1.96	1.85	8.10	7.69	ns
6 mA	Std.	0.97	3.62	0.18	1.08	0.66	3.70	3.52	2.21	2.32	7.29	7.11	ns
8 mA	Std.	0.97	3.62	0.18	1.08	0.66	3.70	3.52	2.21	2.32	7.29	7.11	ns
12 mA	Std.	0.97	3.09	0.18	1.08	0.66	3.15	3.09	2.39	2.61	6.74	6.68	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

1.2 V DC Core Voltage

Table 2-158 • Input Data Register Propagation Delays

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$

Parameter	Description	Std.	Units
t_{iCLKQ}	Clock-to-Q of the Input Data Register	0.68	ns
t_{iSUD}	Data Setup Time for the Input Data Register	0.97	ns
t_{iHD}	Data Hold Time for the Input Data Register	0.00	ns
t_{iSUE}	Enable Setup Time for the Input Data Register	1.02	ns
t_{iHE}	Enable Hold Time for the Input Data Register	0.00	ns
t_{iCLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	1.19	ns
t_{iPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	1.19	ns
$t_{iREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	ns
$t_{iRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.24	ns
$t_{iREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	ns
$t_{iRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.24	ns
t_{iWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.19	ns
t_{iWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.19	ns
$t_{iCKMPWH}$	Clock Minimum Pulse Width High for the Input Data Register	0.31	ns
$t_{iCKMPWL}$	Clock Minimum Pulse Width Low for the Input Data Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Output Register

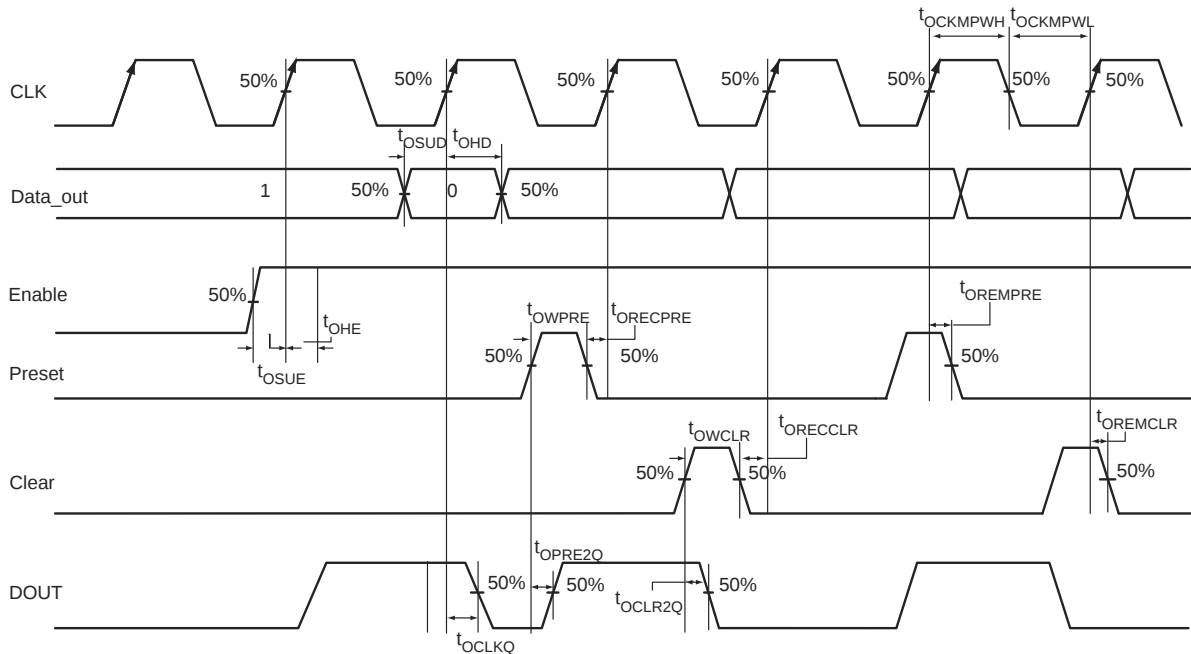


Figure 2-19 • Output Register Timing Diagram

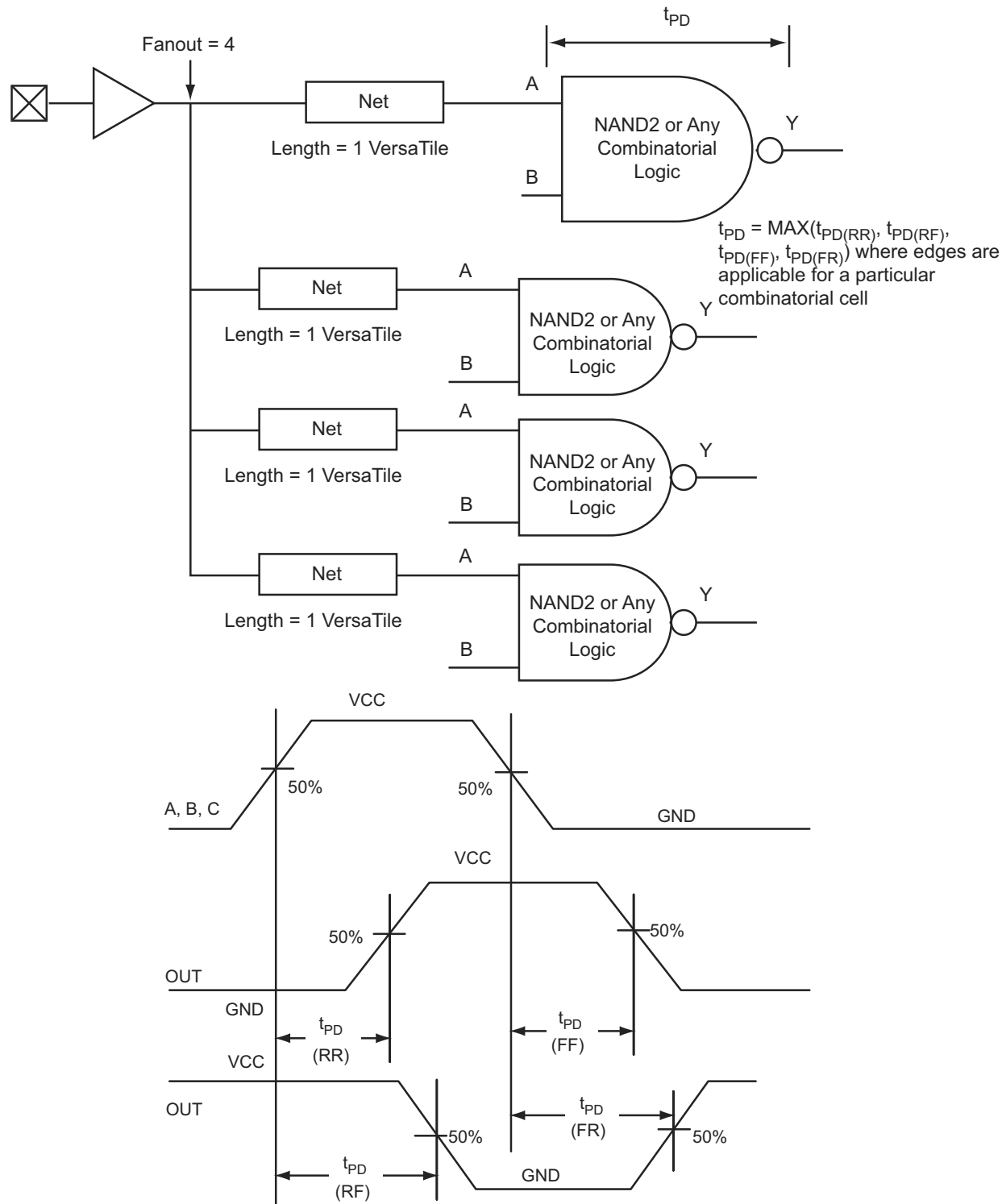


Figure 2-26 • Timing Model and Waveforms

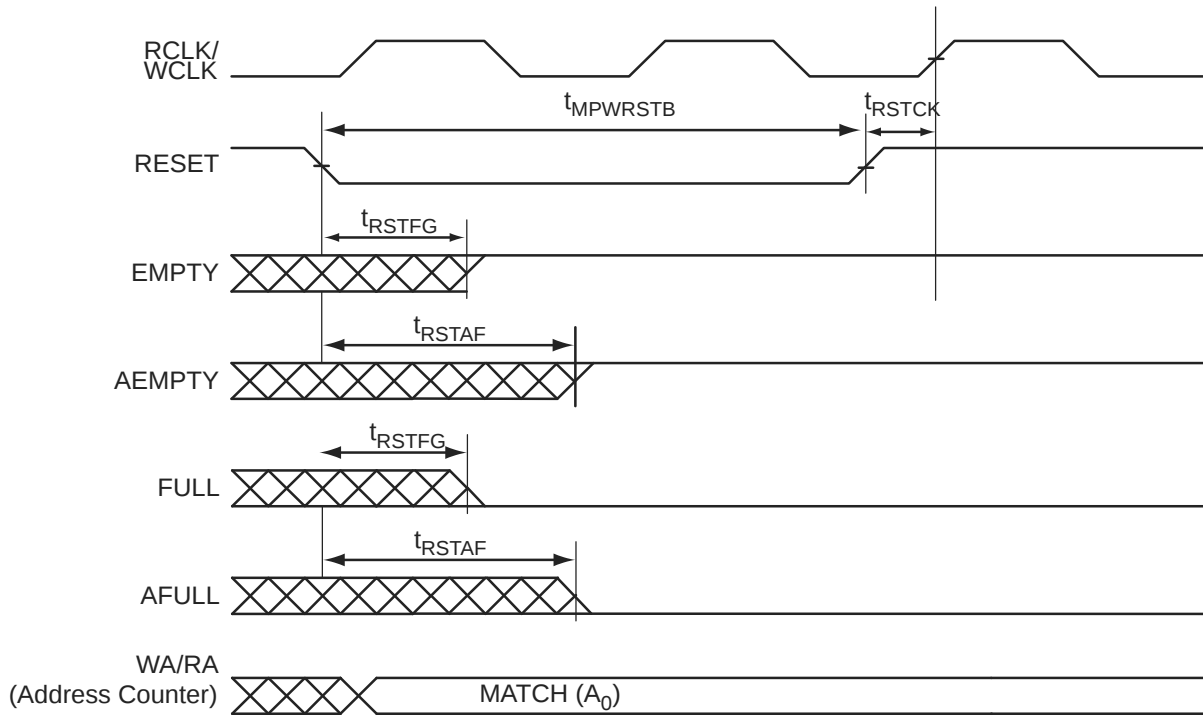


Figure 2-40 • FIFO Reset

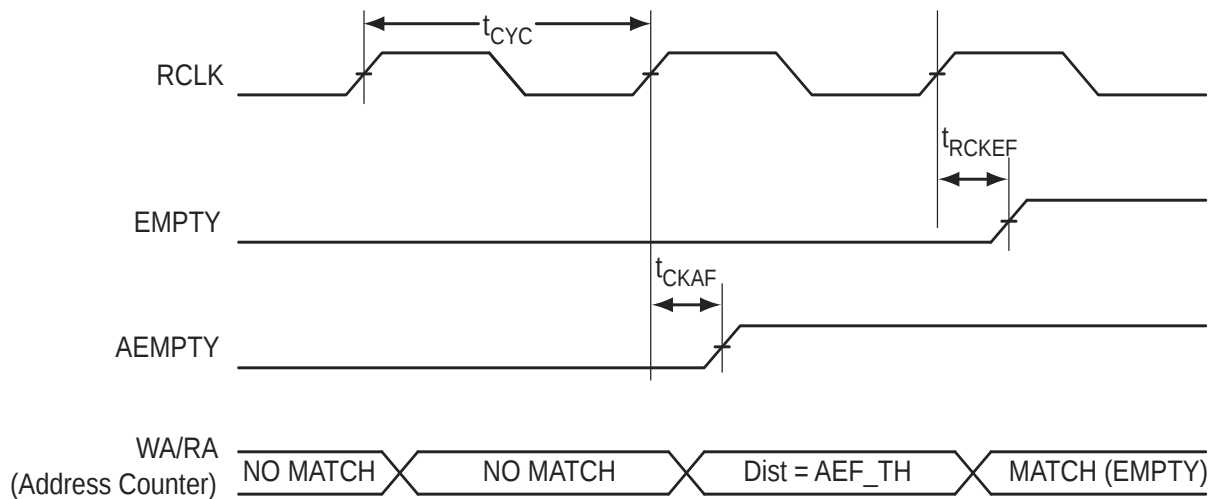


Figure 2-41 • FIFO EMPTY Flag and AEMPTY Flag Assertion

QN132	
Pin Number	AGL125 Function
A1	GAB2/IO69RSB1
A2	IO130RSB1
A3	VCCIB1
A4	GFC1/IO126RSB1
A5	GFB0/IO123RSB1
A6	VCCPLF
A7	GFA1/IO121RSB1
A8	GFC2/IO118RSB1
A9	IO115RSB1
A10	VCC
A11	GEB1/IO110RSB1
A12	GEA0/IO107RSB1
A13	GEC2/IO104RSB1
A14	IO100RSB1
A15	VCC
A16	IO99RSB1
A17	IO96RSB1
A18	IO94RSB1
A19	IO91RSB1
A20	IO85RSB1
A21	IO79RSB1
A22	VCC
A23	GDB2/IO71RSB1
A24	TDI
A25	TRST
A26	GDC1/IO61RSB0
A27	VCC
A28	IO60RSB0
A29	GCC2/IO59RSB0
A30	GCA2/IO57RSB0
A31	GCA0/IO56RSB0
A32	GCB1/IO53RSB0
A33	IO49RSB0
A34	VCC
A35	IO44RSB0
A36	GBA2/IO41RSB0

QN132	
Pin Number	AGL125 Function
A37	GBB1/IO38RSB0
A38	GBC0/IO35RSB0
A39	VCCIB0
A40	IO28RSB0
A41	IO22RSB0
A42	IO18RSB0
A43	IO14RSB0
A44	IO11RSB0
A45	IO07RSB0
A46	VCC
A47	GAC1/IO05RSB0
A48	GAB0/IO02RSB0
B1	IO68RSB1
B2	GAC2/IO131RSB1
B3	GND
B4	GFC0/IO125RSB1
B5	VCOMPLF
B6	GND
B7	GFB2/IO119RSB1
B8	IO116RSB1
B9	GND
B10	GEB0/IO109RSB1
B11	VMV1
B12	FF/GEB2/IO105RSB1
B13	IO101RSB1
B14	GND
B15	IO98RSB1
B16	IO95RSB1
B17	GND
B18	IO87RSB1
B19	IO81RSB1
B20	GND
B21	GNDQ
B22	TMS
B23	TDO
B24	GDC0/IO62RSB0

QN132	
Pin Number	AGL125 Function
B25	GND
B26	NC
B27	GCB2/IO58RSB0
B28	GND
B29	GCB0/IO54RSB0
B30	GCC1/IO51RSB0
B31	GND
B32	GBB2/IO43RSB0
B33	VMV0
B34	GBA0/IO39RSB0
B35	GBC1/IO36RSB0
B36	GND
B37	IO26RSB0
B38	IO21RSB0
B39	GND
B40	IO13RSB0
B41	IO08RSB0
B42	GND
B43	GAC0/IO04RSB0
B44	GNDQ
C1	GAA2/IO67RSB1
C2	IO132RSB1
C3	VCC
C4	GFB1/IO124RSB1
C5	GFA0/IO122RSB1
C6	GFA2/IO120RSB1
C7	IO117RSB1
C8	VCCIB1
C9	GEA1/IO108RSB1
C10	GNDQ
C11	GEA2/IO106RSB1
C12	IO103RSB1
C13	VCCIB1
C14	IO97RSB1
C15	IO93RSB1
C16	IO89RSB1

FG144		FG144		FG144	
Pin Number	AGL400 Function	Pin Number	AGL400 Function	Pin Number	AGL400 Function
A1	GNDQ	D1	IO149NDB3	G1	GFA1/IO145PPB3
A2	VMV0	D2	IO149PDB3	G2	GND
A3	GAB0/IO02RSB0	D3	IO153VDB3	G3	VCCPLF
A4	GAB1/IO03RSB0	D4	GAA2/IO155UPB3	G4	GFA0/IO145NPB3
A5	IO16RSB0	D5	GAC0/IO04RSB0	G5	GND
A6	GND	D6	GAC1/IO05RSB0	G6	GND
A7	IO30RSB0	D7	GBC0/IO54RSB0	G7	GND
A8	VCC	D8	GBC1/IO55RSB0	G8	GDC1/IO77UPB1
A9	IO34RSB0	D9	GBB2/IO61PDB1	G9	IO72NDB1
A10	GBA0/IO58RSB0	D10	IO61NDB1	G10	GCC2/IO72PDB1
A11	GBA1/IO59RSB0	D11	IO62NPB1	G11	IO71NDB1
A12	GNDQ	D12	GCB1/IO68PPB1	G12	GCB2/IO71PDB1
B1	GAB2/IO154UDB3	E1	VCC	H1	VCC
B2	GND	E2	GFC0/IO147NDB3	H2	GFB2/IO143PDB3
B3	GAA0/IO00RSB0	E3	GFC1/IO147PDB3	H3	GFC2/IO142PSB3
B4	GAA1/IO01RSB0	E4	VCCIB3	H4	GEC1/IO137PDB3
B5	IO14RSB0	E5	IO155VPB3	H5	VCC
B6	IO19RSB0	E6	VCCIB0	H6	IO75PDB1
B7	IO23RSB0	E7	VCCIB0	H7	IO75NDB1
B8	IO31RSB0	E8	GCC1/IO67PDB1	H8	GDB2/IO81RSB2
B9	GBB0/IO56RSB0	E9	VCCIB1	H9	GDC0/IO77VPB1
B10	GBB1/IO57RSB0	E10	VCC	H10	VCCIB1
B11	GND	E11	GCA0/IO69NDB1	H11	IO73PSB1
B12	VMV1	E12	IO70NDB1	H12	VCC
C1	IO154VDB3	F1	GFB0/IO146NPB3	J1	GEB1/IO136PDB3
C2	GFA2/IO144PPB3	F2	VCOMPLF	J2	IO143NDB3
C3	GAC2/IO153UDB3	F3	GFB1/IO146PPB3	J3	VCCIB3
C4	VCC	F4	IO144NPB3	J4	GEC0/IO137NDB3
C5	IO12RSB0	F5	GND	J5	IO125RSB2
C6	IO17RSB0	F6	GND	J6	IO116RSB2
C7	IO25RSB0	F7	GND	J7	VCC
C8	IO32RSB0	F8	GCC0/IO67NDB1	J8	TCK
C9	IO53RSB0	F9	GCB0/IO68NPB1	J9	GDA2/IO80RSB2
C10	GBA2/IO60PDB1	F10	GND	J10	TDO
C11	IO60NDB1	F11	GCA1/IO69PDB1	J11	GDA1/IO79UDB1
C12	GBC2/IO62PPB1	F12	GCA2/IO70PDB1	J12	GDB1/IO78UDB1

FG144	
Pin Number	AGL1000 Function
A1	GNDQ
A2	VMV0
A3	GAB0/IO02RSB0
A4	GAB1/IO03RSB0
A5	IO10RSB0
A6	GND
A7	IO44RSB0
A8	VCC
A9	IO69RSB0
A10	GBA0/IO76RSB0
A11	GBA1/IO77RSB0
A12	GNDQ
B1	GAB2/IO224PDB3
B2	GND
B3	GAA0/IO00RSB0
B4	GAA1/IO01RSB0
B5	IO13RSB0
B6	IO26RSB0
B7	IO35RSB0
B8	IO60RSB0
B9	GBB0/IO74RSB0
B10	GBB1/IO75RSB0
B11	GND
B12	VMV1
C1	IO224NDB3
C2	GFA2/IO206PPB3
C3	GAC2/IO223PDB3
C4	VCC
C5	IO16RSB0
C6	IO29RSB0
C7	IO32RSB0
C8	IO63RSB0
C9	IO66RSB0
C10	GBA2/IO78PDB1
C11	IO78NDB1
C12	GBC2/IO80PPB1

FG144	
Pin Number	AGL1000 Function
D1	IO213PDB3
D2	IO213NDB3
D3	IO223NDB3
D4	GAA2/IO225PPB3
D5	GAC0/IO04RSB0
D6	GAC1/IO05RSB0
D7	GBC0/IO72RSB0
D8	GBC1/IO73RSB0
D9	GBB2/IO79PDB1
D10	IO79NDB1
D11	IO80NPB1
D12	GCB1/IO92PPB1
E1	VCC
E2	GFC0/IO209NDB3
E3	GFC1/IO209PDB3
E4	VCCIB3
E5	IO225NPB3
E6	VCCIB0
E7	VCCIB0
E8	GCC1/IO91PDB1
E9	VCCIB1
E10	VCC
E11	GCA0/IO93NDB1
E12	IO94NDB1
F1	GFB0/IO208NPB3
F2	VCOMPLF
F3	GFB1/IO208PPB3
F4	IO206NPB3
F5	GND
F6	GND
F7	GND
F8	GCC0/IO91NDB1
F9	GCB0/IO92NPB1
F10	GND
F11	GCA1/IO93PDB1
F12	GCA2/IO94PDB1

FG144	
Pin Number	AGL1000 Function
G1	GFA1/IO207PPB3
G2	GND
G3	VCCPLF
G4	GFA0/IO207NPB3
G5	GND
G6	GND
G7	GND
G8	GDC1/IO111PPB1
G9	IO96NDB1
G10	GCC2/IO96PDB1
G11	IO95NDB1
G12	GCB2/IO95PDB1
H1	VCC
H2	GFB2/IO205PDB3
H3	GFC2/IO204PSB3
H4	GEC1/IO190PDB3
H5	VCC
H6	IO105PDB1
H7	IO105NDB1
H8	GDB2/IO115RSB2
H9	GDC0/IO111NPB1
H10	VCCIB1
H11	IO101PSB1
H12	VCC
J1	GEB1/IO189PDB3
J2	IO205NDB3
J3	VCCIB3
J4	GEC0/IO190NDB3
J5	IO160RSB2
J6	IO157RSB2
J7	VCC
J8	TCK
J9	GDA2/IO114RSB2
J10	TDO
J11	GDA1/IO113PDB1
J12	GDB1/IO112PDB1

FG256	
Pin Number	AGL600 Function
R5	IO132RSB2
R6	IO127RSB2
R7	IO121RSB2
R8	IO114RSB2
R9	IO109RSB2
R10	IO105RSB2
R11	IO98RSB2
R12	IO96RSB2
R13	GDB2/IO90RSB2
R14	TDI
R15	GNDQ
R16	TDO
T1	GND
T2	IO137RSB2
T3	FF/GEB2/IO142RSB2
T4	IO134RSB2
T5	IO125RSB2
T6	IO123RSB2
T7	IO118RSB2
T8	IO115RSB2
T9	IO111RSB2
T10	IO106RSB2
T11	IO102RSB2
T12	GDC2/IO91RSB2
T13	IO93RSB2
T14	GDA2/IO89RSB2
T15	TMS
T16	GND

FG484	
Pin Number	AGL400 Function
AA15	NC
AA16	NC
AA17	NC
AA18	NC
AA19	NC
AA20	NC
AA21	VCCIB1
AA22	GND
AB1	GND
AB2	GND
AB3	VCCIB2
AB4	NC
AB5	NC
AB6	IO121RSB2
AB7	IO119RSB2
AB8	IO114RSB2
AB9	IO109RSB2
AB10	NC
AB11	NC
AB12	IO104RSB2
AB13	IO103RSB2
AB14	NC
AB15	NC
AB16	IO91RSB2
AB17	IO90RSB2
AB18	NC
AB19	NC
AB20	VCCIB2
AB21	GND
AB22	GND
B1	GND
B2	VCCIB3
B3	NC
B4	NC
B5	NC
B6	NC

FG484	
Pin Number	AGL400 Function
M3	NC
M4	GFA2/IO144PPB3
M5	GFA1/IO145PDB3
M6	VCCPLF
M7	IO143NDB3
M8	GFB2/IO143PDB3
M9	VCC
M10	GND
M11	GND
M12	GND
M13	GND
M14	VCC
M15	GCB2/IO71PPB1
M16	GCA1/IO69PPB1
M17	GCC2/IO72PPB1
M18	NC
M19	GCA2/IO70PDB1
M20	NC
M21	NC
M22	NC
N1	NC
N2	NC
N3	NC
N4	GFC2/IO142PDB3
N5	IO144NPB3
N6	IO141PPB3
N7	IO120RSB2
N8	VCCIB3
N9	VCC
N10	GND
N11	GND
N12	GND
N13	GND
N14	VCC
N15	VCCIB1
N16	IO71NPB1

FG484	
Pin Number	AGL1000 Function
B7	IO15RSB0
B8	IO19RSB0
B9	IO24RSB0
B10	IO31RSB0
B11	IO39RSB0
B12	IO48RSB0
B13	IO54RSB0
B14	IO58RSB0
B15	IO63RSB0
B16	IO66RSB0
B17	IO68RSB0
B18	IO70RSB0
B19	NC
B20	NC
B21	VCCIB1
B22	GND
C1	VCCIB3
C2	IO220PDB3
C3	NC
C4	NC
C5	GND
C6	IO10RSB0
C7	IO14RSB0
C8	VCC
C9	VCC
C10	IO30RSB0
C11	IO37RSB0
C12	IO43RSB0
C13	NC
C14	VCC
C15	VCC
C16	NC
C17	NC
C18	GND
C19	NC
C20	NC

FG484	
Pin Number	AGL1000 Function
G5	IO222PDB3
G6	GAC2/IO223PDB3
G7	IO223NDB3
G8	GNDQ
G9	IO23RSB0
G10	IO29RSB0
G11	IO33RSB0
G12	IO46RSB0
G13	IO52RSB0
G14	IO60RSB0
G15	GNDQ
G16	IO80NDB1
G17	GBB2/IO79PDB1
G18	IO79NDB1
G19	IO82NPB1
G20	IO85PDB1
G21	IO85NDB1
G22	NC
H1	NC
H2	NC
H3	VCC
H4	IO217PDB3
H5	IO218PDB3
H6	IO221NDB3
H7	IO221PDB3
H8	VMV0
H9	VCCIB0
H10	VCCIB0
H11	IO38RSB0
H12	IO47RSB0
H13	VCCIB0
H14	VCCIB0
H15	VMV1
H16	GBC2/IO80PDB1
H17	IO83PPB1
H18	IO86PPB1

FG484	
Pin Number	AGL1000 Function
M3	IO206NDB3
M4	GFA2/IO206PDB3
M5	GFA1/IO207PDB3
M6	VCCPLF
M7	IO205NDB3
M8	GFB2/IO205PDB3
M9	VCC
M10	GND
M11	GND
M12	GND
M13	GND
M14	VCC
M15	GCB2/IO95PPB1
M16	GCA1/IO93PPB1
M17	GCC2/IO96PPB1
M18	IO100PPB1
M19	GCA2/IO94PPB1
M20	IO101PPB1
M21	IO99PPB1
M22	NC
N1	IO201NDB3
N2	IO201PDB3
N3	NC
N4	GFC2/IO204PDB3
N5	IO204NDB3
N6	IO203NDB3
N7	IO203PDB3
N8	VCCIB3
N9	VCC
N10	GND
N11	GND
N12	GND
N13	GND
N14	VCC
N15	VCCIB1
N16	IO95NPB1