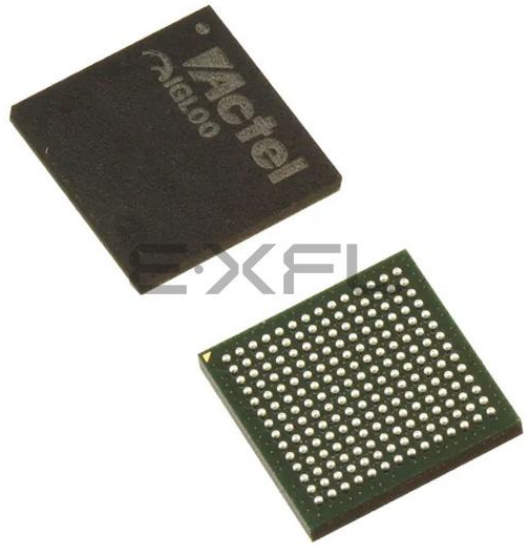

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | 3072 |
| Total RAM Bits | 36864 |
| Number of I/O | 133 |
| Number of Gates | 125000 |
| Voltage - Supply | 1.14V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Package / Case | 196-TFBGA, CSBGA |
| Supplier Device Package | 196-CSP (8x8) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/agl125v2-cs196i |

## Package Thermal Characteristics

The device junction-to-case thermal resistivity is $\theta_{jc}$ and the junction-to-ambient air thermal resistivity is $\theta_{ja}$. The thermal characteristics for $\theta_{ja}$ are shown for two air flow rates. The absolute maximum junction temperature is 100°C. EQ 2 shows a sample calculation of the absolute maximum power dissipation allowed for the AGL1000-FG484 package at commercial temperature and in still air.

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja}(\text{°C/W})} = \frac{100\text{°C} - 70\text{°C}}{23.3\text{°C/W}} = 1.28\ \text{W}$$

*EQ 2*

***Table 2-5 •*** **Package Thermal Resistivities**

| Package Type | Device | Pin Count | $\theta_{jc}$ | $\theta_{ja}$ | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Still Air | 1 m/s | 2.5 m/s | |
| Quad Flat No Lead (QN) | AGL030 | 132 | 13.1 | 21.4 | 16.8 | 15.3 | C/W |
| | AGL060 | 132 | 11.0 | 21.2 | 16.6 | 15.0 | C/W |
| | AGL125 | 132 | 9.2 | 21.1 | 16.5 | 14.9 | C/W |
| | AGL250 | 132 | 8.9 | 21.0 | 16.4 | 14.8 | C/W |
| | AGL030 | 68 | 13.4 | 68.4 | 45.8 | 43.1 | C/W |
| Very Thin Quad Flat Pack (VQ)* | | 100 | 10.0 | 35.3 | 29.4 | 27.1 | C/W |
| Chip Scale Package (CS) | AGL1000 | 281 | 6.0 | 28.0 | 22.8 | 21.5 | C/W |
| | AGL400 | 196 | 7.2 | 37.1 | 31.1 | 28.9 | C/W |
| | AGL250 | 196 | 7.6 | 38.3 | 32.2 | 30.0 | C/W |
| | AGL125 | 196 | 8.0 | 39.5 | 33.4 | 31.1 | C/W |
| | AGL030 | 81 | 12.4 | 32.8 | 28.5 | 27.2 | C/W |
| | AGL060 | 81 | 11.1 | 28.8 | 24.8 | 23.5 | C/W |
| | AGL250 | 81 | 10.4 | 26.9 | 22.3 | 20.9 | C/W |
| Micro Chip Scale Package (UC) | AGL030 | 81 | 16.9 | 40.6 | 35.2 | 33.7 | C/W |
| Fine Pitch Ball Grid Array (FG) | AGL060 | 144 | 18.6 | 55.2 | 49.4 | 47.2 | C/W |
| | AGL1000 | 144 | 6.3 | 31.6 | 26.2 | 24.2 | C/W |
| | AGL400 | 144 | 6.8 | 37.6 | 31.2 | 29.0 | C/W |
| | AGL250 | 256 | 12.0 | 38.6 | 34.7 | 33.0 | C/W |
| | AGL1000 | 256 | 6.6 | 28.1 | 24.4 | 22.7 | C/W |
| | AGL1000 | 484 | 8.0 | 23.3 | 19.0 | 16.7 | C/W |

*Note: *Thermal resistances for other device-package combinations will be posted in a later revision.*

### Disclaimer:

The simulation for determining the junction-to-air thermal resistance is based on JEDEC standards (JESD51) and assumptions made in building the model. Junction-to-case is based on SEMI G38-88. JESD51 is only used for comparing one package to another package, provided the two tests uses the same condition. They have little relevance in actual application and therefore should be used with a degree of caution.

### Temperature and Voltage Derating Factors

**Table 2-6 • Temperature and Voltage Derating Factors for Timing Delays (normalized to $T_J$ = 70°C, VCC = 1.425 V) For IGLOO V2 or V5 devices, 1.5 V DC Core Supply Voltage**

| Array Voltage VCC (V) | Junction Temperature (°C) | | | | | |
|---|---|---|---|---|---|---|
| | –40°C | 0°C | 25°C | 70°C | 85°C | 100°C |
| 1.425 | 0.934 | 0.953 | 0.971 | 1.000 | 1.007 | 1.013 |
| 1.500 | 0.855 | 0.874 | 0.891 | 0.917 | 0.924 | 0.929 |
| 1.575 | 0.799 | 0.816 | 0.832 | 0.857 | 0.864 | 0.868 |

**Table 2-7 • Temperature and Voltage Derating Factors for Timing Delays (normalized to $T_J$ = 70°C, VCC = 1.14 V) For IGLOO V2, 1.2 V DC Core Supply Voltage**

| Array Voltage VCC (V) | Junction Temperature (°C) | | | | | |
|---|---|---|---|---|---|---|
| | –40°C | 0°C | 25°C | 70°C | 85°C | 100°C |
| 1.14 | 0.967 | 0.978 | 0.991 | 1.000 | 1.006 | 1.010 |
| 1.20 | 0.864 | 0.874 | 0.885 | 0.894 | 0.899 | 0.902 |
| 1.26 | 0.794 | 0.803 | 0.814 | 0.821 | 0.827 | 0.830 |

# Calculating Power Dissipation

## Quiescent Supply Current

Quiescent supply current (IDD) calculation depends on multiple factors, including operating voltages (VCC, VCCI, and VJTAG), operating temperature, system clock frequency, and power modes usage. Microsemi recommends using the PowerCalculator and SmartPower software estimation tools to evaluate the projected static and active power based on the user design, power mode usage, operating voltage, and temperature.

**Table 2-8 • Power Supply State per Mode**

| | Power Supply Configurations | | | | |
|---|---|---|---|---|---|
| Modes/power supplies | VCC | VCCPLL | VCCI | VJTAG | VPUMP |
| Flash*Freeze | On | On | On | On | On/off/floating |
| Sleep | Off | Off | On | Off | Off |
| Shutdown | Off | Off | Off | Off | Off |
| No Flash*Freeze | On | On | On | On | On/off/floating |

*Note: Off: Power supply level = 0 V*

**Table 2-9 • Quiescent Supply Current (IDD) Characteristics, IGLOO Flash*Freeze Mode***

| | Core Voltage | AGL015 | AGL030 | AGL060 | AGL125 | AGL250 | AGL400 | AGL600 | AGL1000 | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| Typical (25°C) | 1.2 V | 4 | 4 | 8 | 13 | 20 | 27 | 30 | 44 | µA |
| | 1.5 V | 6 | 6 | 10 | 18 | 34 | 51 | 72 | 127 | µA |

*Note: *IDD includes VCC, VPUMP, VCCI, VCCPLL, and VMV currents. Values do not include I/O static contribution, which is shown in Table 2-13 on page 2-10 through Table 2-15 on page 2-11 and Table 2-16 on page 2-11 through Table 2-18 on page 2-12 (PDC6 and PDC7).*

## Guidelines

### Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that this net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100% because all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
  - Bit 0 (LSB) = 100%
  - Bit 1 = 50%
  - Bit 2 = 25%
  - …
  - Bit 7 (MSB) = 0.78125%
  - Average toggle rate = (100% + 50% + 25% + 12.5% + . . . + 0.78125%) / 8

### Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When nontristate output buffers are used, the enable rate should be 100%.

***Table 2-23 •*** **Toggle Rate Guidelines Recommended for Power Calculation**

| Component | Definition | Guideline |
|---|---|---|
| $\alpha_1$ | Toggle rate of VersaTile outputs | 10% |
| $\alpha_2$ | I/O buffer toggle rate | 10% |

***Table 2-24 •*** **Enable Rate Guidelines Recommended for Power Calculation**

| Component | Definition | Guideline |
|---|---|---|
| $\beta_1$ | I/O output buffer enable rate | 100% |
| $\beta_2$ | RAM enable rate for read operations | 12.5% |
| $\beta_3$ | RAM enable rate for write operations | 12.5% |

### 1.5 V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.5 V applications. It uses a 1.5 V input buffer and a push-pull output buffer.

**Table 2-111 • Minimum and Maximum DC Input and Output Levels Applicable to Advanced I/O Banks**

| 1.5 V LVCMOS | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSH | IOSL | IIL[1] | IIH[2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA[3] | Max. mA[3] | µA[4] | µA[4] |
| 2 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.575 | 0.25 * VCCI | 0.75 * VCCI | 2 | 2 | 13 | 16 | 10 | 10 |
| 4 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.575 | 0.25 * VCCI | 0.75 * VCCI | 4 | 4 | 25 | 33 | 10 | 10 |
| 6 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.575 | 0.25 * VCCI | 0.75 * VCCI | 6 | 6 | 32 | 39 | 10 | 10 |
| 8 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.575 | 0.25 * VCCI | 0.75 * VCCI | 8 | 8 | 66 | 55 | 10 | 10 |
| 12 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.575 | 0.25 * VCCI | 0.75 * VCCI | 12 | 12 | 66 | 55 | 10 | 10 |

*Notes:*

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
3. *Currents are measured at 100°C junction temperature and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

**Table 2-112 • Minimum and Maximum DC Input and Output Levels Applicable to Standard Plus I/O Banks**

| 1.5 V LVCMOS | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSH | IOSL | IIL[1] | IIH[2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA[3] | Max. mA[3] | µA[4] | µA[4] |
| 2 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.575 | 0.25 * VCCI | 0.75 * VCCI | 2 | 2 | 13 | 16 | 10 | 10 |
| 4 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.575 | 0.25 * VCCI | 0.75 * VCCI | 4 | 4 | 25 | 33 | 10 | 10 |

*Notes:*

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
3. *Currents are measured at 100°C junction temperature and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

**Table 2-119 • 1.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V**
**Applicable to Standard Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 0.97 | 5.88 | 0.18 | 1.14 | 0.66 | 6.00 | 5.45 | 2.00 | 1.94 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

**Table 2-120 • 1.5 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V**
**Applicable to Standard Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 0.97 | 2.51 | 0.18 | 1.14 | 0.66 | 2.56 | 2.21 | 1.99 | 2.03 | ns |

*Notes:*

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

### 1.2 V DC Core Voltage

**Table 2-121 • 1.5 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V**
**Applicable to Advanced I/O Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 1.55 | 7.17 | 0.26 | 1.27 | 1.10 | 7.29 | 6.60 | 3.33 | 3.03 | 13.07 | 12.39 | ns |
| 4 mA | Std. | 1.55 | 6.27 | 0.26 | 1.27 | 1.10 | 6.37 | 5.86 | 3.61 | 3.51 | 12.16 | 11.64 | ns |
| 6 mA | Std. | 1.55 | 5.94 | 0.26 | 1.27 | 1.10 | 6.04 | 5.70 | 3.67 | 3.64 | 11.82 | 11.48 | ns |
| 8 mA | Std. | 1.55 | 5.86 | 0.26 | 1.27 | 1.10 | 5.96 | 5.71 | 2.83 | 4.11 | 11.74 | 11.50 | ns |
| 12 mA | Std. | 1.55 | 5.86 | 0.26 | 1.27 | 1.10 | 5.96 | 5.71 | 2.83 | 4.11 | 11.74 | 11.50 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

**Table 2-122 • 1.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V**
**Applicable to Advanced I/O Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 1.55 | 3.44 | 0.26 | 1.27 | 1.10 | 3.49 | 3.35 | 3.32 | 3.12 | 9.28 | 9.14 | ns |
| 4 mA | Std. | 1.55 | 3.06 | 0.26 | 1.27 | 1.10 | 3.10 | 2.89 | 3.60 | 3.61 | 8.89 | 8.67 | ns |
| 6 mA | Std. | 1.55 | 2.98 | 0.26 | 1.27 | 1.10 | 3.02 | 2.80 | 3.66 | 3.74 | 8.81 | 8.58 | ns |
| 8 mA | Std. | 1.55 | 2.96 | 0.26 | 1.27 | 1.10 | 3.00 | 2.70 | 3.75 | 4.23 | 8.78 | 8.48 | ns |
| 12 mA | Std. | 1.55 | 2.96 | 0.26 | 1.27 | 1.10 | 3.00 | 2.70 | 3.75 | 4.23 | 8.78 | 8.48 | ns |

*Notes:*

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

***Table 2-135 •*** **1.2 V LVCMOS High Slew**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V**
**Applicable to Standard Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 mA | Std. | 1.55 | 8.57 | 0.26 | 1.53 | 1.10 | 8.23 | 7.38 | 2.51 | 2.39 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

***Table 2-136 •*** **1.2 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.14 V**
**Applicable to Standard Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 mA | Std. | 1.55 | 3.59 | 0.26 | 1.53 | 1.10 | 3.47 | 3.06 | 2.51 | 2.49 | ns |

*Notes:*

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

## *1.2 V LVCMOS Wide Range*

***Table 2-137 •*** **Minimum and Maximum DC Input and Output Levels for LVCMOS 1.2 V Wide Range**
**Applicable to Advanced I/O Banks**

| 1.2 V LVCMOS Wide Range | | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL[2] | IIH[3] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Equivalent Software Default Drive Strength Option[1] | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | mA | mA | Max. mA[4] | Max. mA[4] | µA[5] | µA[5] |
| 100 µA | 2 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.26 | 0.25 * VCCI | 0.75 * VCCI | 100 | 100 | 20 | 26 | 10 | 10 |

*Notes:*

1. *The minimum drive strength for the default LVCMOS 1.2 V software configuration when run in wide range is ± 100 µA. The drive strength displayed in software is supported in normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
3. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
4. *Currents are measured at 100°C junction temperature and maximum voltage.*
5. *Currents are measured at 85°C junction temperature.*
6. *Software default selection highlighted in gray.*

### 1.2 V DC Core Voltage

**Table 2-158 • Input Data Register Propagation Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{ICLKQ}$ | Clock-to-Q of the Input Data Register | 0.68 | ns |
| $t_{ISUD}$ | Data Setup Time for the Input Data Register | 0.97 | ns |
| $t_{IHD}$ | Data Hold Time for the Input Data Register | 0.00 | ns |
| $t_{ISUE}$ | Enable Setup Time for the Input Data Register | 1.02 | ns |
| $t_{IHE}$ | Enable Hold Time for the Input Data Register | 0.00 | ns |
| $t_{ICLR2Q}$ | Asynchronous Clear-to-Q of the Input Data Register | 1.19 | ns |
| $t_{IPRE2Q}$ | Asynchronous Preset-to-Q of the Input Data Register | 1.19 | ns |
| $t_{IREMCLR}$ | Asynchronous Clear Removal Time for the Input Data Register | 0.00 | ns |
| $t_{IRECCLR}$ | Asynchronous Clear Recovery Time for the Input Data Register | 0.24 | ns |
| $t_{IREMPRE}$ | Asynchronous Preset Removal Time for the Input Data Register | 0.00 | ns |
| $t_{IRECPRE}$ | Asynchronous Preset Recovery Time for the Input Data Register | 0.24 | ns |
| $t_{IWCLR}$ | Asynchronous Clear Minimum Pulse Width for the Input Data Register | 0.19 | ns |
| $t_{IWPRE}$ | Asynchronous Preset Minimum Pulse Width for the Input Data Register | 0.19 | ns |
| $t_{ICKMPWH}$ | Clock Minimum Pulse Width High for the Input Data Register | 0.31 | ns |
| $t_{ICKMPWL}$ | Clock Minimum Pulse Width Low for the Input Data Register | 0.28 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

## Output Register

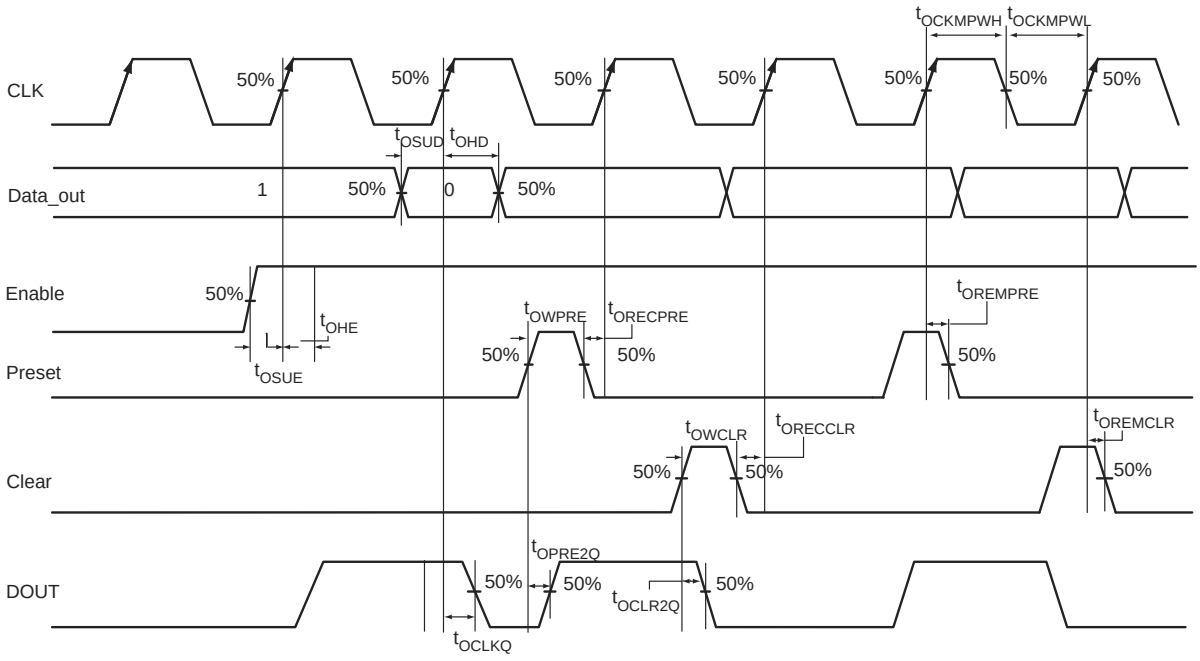



**Figure 2-19 • Output Register Timing Diagram**

## DDR Module Specifications

### *Input DDR Module*

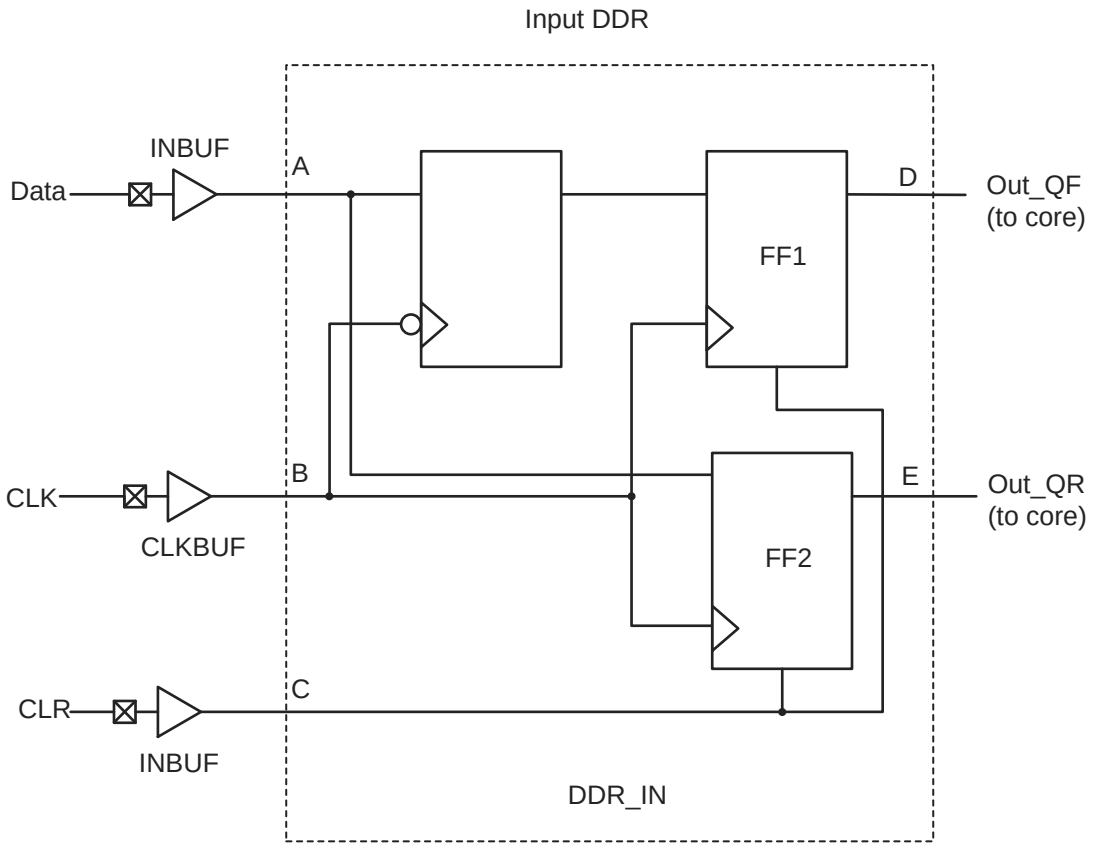



***Figure 2-21 •*** **Input DDR Timing Model**

***Table 2-163 •*** **Parameter Definitions**

| Parameter Name | Parameter Definition | Measuring Nodes (from, to) |
|---|---|---|
| $t_{DDRICLKQ1}$ | Clock-to-Out Out_QR | B, D |
| $t_{DDRICLKQ2}$ | Clock-to-Out Out_QF | B, E |
| $t_{DDRISUD}$ | Data Setup Time of DDR input | A, B |
| $t_{DDRIHD}$ | Data Hold Time of DDR input | A, B |
| $t_{DDRICLR2Q1}$ | Clear-to-Out Out_QR | C, D |
| $t_{DDRICLR2Q2}$ | Clear-to-Out Out_QF | C, E |
| $t_{DDRIREMCLR}$ | Clear Removal | C, B |
| $t_{DDRIRECCLR}$ | Clear Recovery | C, B |

## Output DDR Module

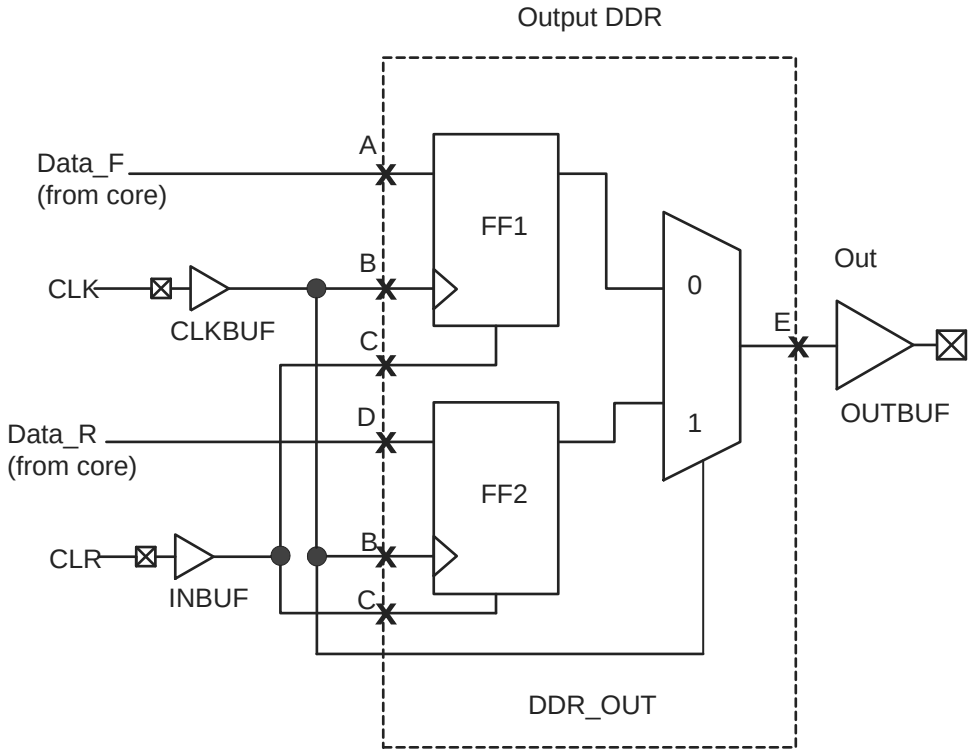



***Figure 2-23 •*** **Output DDR Timing Model**

***Table 2-166 •*** **Parameter Definitions**

| Parameter Name | Parameter Definition | Measuring Nodes (from, to) |
|---|---|---|
| $t_{DDROCLKQ}$ | Clock-to-Out | B, E |
| $t_{DDROCLR2Q}$ | Asynchronous Clear-to-Out | C, E |
| $t_{DDROREMCLR}$ | Clear Removal | C, B |
| $t_{DDRORECCLR}$ | Clear Recovery | C, B |
| $t_{DDROSUD1}$ | Data Setup Data_F | A, B |
| $t_{DDROSUD2}$ | Data Setup Data_R | D, B |
| $t_{DDROHD1}$ | Data Hold Data_F | A, B |
| $t_{DDROHD2}$ | Data Hold Data_R | D, B |

### VJTAG JTAG Supply Voltage

Low power flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND. It should be noted that VCC is required to be powered for JTAG operation; VJTAG alone is insufficient. If a device is in a JTAG chain of interconnected boards, the board containing the device can be powered down, provided both VJTAG and VCC to the part remain powered; otherwise, JTAG signals will not be able to transition the device, even in bypass mode.

Microsemi recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

### VPUMP Programming Supply Voltage

IGLOO devices support single-voltage ISP of the configuration flash and FlashROM. For programming, VPUMP should be 3.3 V nominal. During normal device operation, VPUMP can be left floating or can be tied (pulled up) to any voltage between 0 V and the VPUMP maximum. Programming power supply voltage (VPUMP) range is listed in the datasheet.

When the VPUMP pin is tied to ground, it will shut off the charge pump circuitry, resulting in no sources of oscillation from the charge pump circuitry.

For proper programming, 0.01 µF and 0.33 µF capacitors (both rated at 16 V) are to be connected in parallel across VPUMP and GND, and positioned as close to the FPGA pins as possible.

Microsemi recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

## User Pins

### I/O User Input/Output

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Input and output signal levels are compatible with the I/O standard selected.

During programming, I/Os become tristated and weakly pulled up to VCCI. With VCCI, VMV, and VCC supplies continuously powered up, when the device transitions from programming to operating mode, the I/Os are instantly configured to the desired user configuration.

Unused I/Os are configured as follows:

- Output buffer is disabled (with tristate value of high impedance)
- Input buffer is disabled (with tristate value of high impedance)
- Weak pull-up is programmed

### GL Globals

GL I/Os have access to certain clock conditioning circuitry (and the PLL) and/or have direct access to the global network (spines). Additionally, the global I/Os can be used as regular I/Os, since they have identical capabilities. Unused GL pins are configured as inputs with pull-up resistors.

See more detailed descriptions of global I/O connectivity in the "Clock Conditioning Circuits in Low Power Flash Devices and Mixed Signal FPGAs" chapter of the *IGLOO FPGA Fabric User Guide*. All inputs labeled GC/GF are direct inputs into the quadrant clocks. For example, if GAA0 is used for an input, GAA1 and GAA2 are no longer available for input to the quadrant globals. All inputs labeled GC/GF are direct inputs into the chip-level globals, and the rest are connected to the quadrant globals. The inputs to the global network are multiplexed, and only one input can be used as a global input.

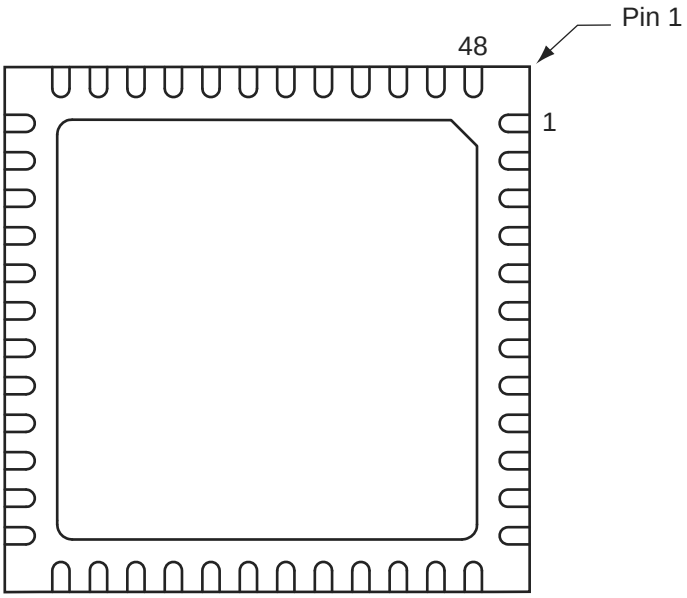
Refer to the "I/O Structures in IGLOO and ProASIC3 Devices" chapter of the *IGLOO FPGA Fabric User Guide* for an explanation of the naming of global pins.

### FF Flash*Freeze Mode Activation Pin

Flash*Freeze mode is available on IGLOO devices. The FF pin is a dedicated input pin used to enter and exit Flash*Freeze mode. The FF pin is active low, has the same characteristics as a single-ended I/O, and must meet the maximum rise and fall times. When Flash*Freeze mode is not used in the design, the FF pin is available as a regular I/O.

When Flash*Freeze mode is used, the FF pin must not be left floating to avoid accidentally entering Flash*Freeze mode. While in Flash*Freeze mode, the Flash*Freeze pin should be constantly asserted.

# QN48




*Notes:*

1. *This is the bottom view of the package.*
2. *The die attach paddle center of the package is tied to ground (GND).*

## *Note*

For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

| QN132 | |
|---|---|
| **Pin Number** | **AGL125 Function** |
| C17 | IO83RSB1 |
| C18 | VCCIB1 |
| C19 | TCK |
| C20 | VMV1 |
| C21 | VPUMP |
| C22 | VJTAG |
| C23 | VCCIB0 |
| C24 | NC |
| C25 | NC |
| C26 | GCA1/IO55RSB0 |
| C27 | GCC0/IO52RSB0 |
| C28 | VCCIB0 |
| C29 | IO42RSB0 |
| C30 | GNDQ |
| C31 | GBA1/IO40RSB0 |
| C32 | GBB0/IO37RSB0 |
| C33 | VCC |
| C34 | IO24RSB0 |
| C35 | IO19RSB0 |
| C36 | IO16RSB0 |
| C37 | IO10RSB0 |
| C38 | VCCIB0 |
| C39 | GAB1/IO03RSB0 |
| C40 | VMV0 |
| D1 | GND |
| D2 | GND |
| D3 | GND |
| D4 | GND |

| FG144 | |
|---|---|
| **Pin Number** | **AGL250 Function** |
| A1 | GNDQ |
| A2 | VMV0 |
| A3 | GAB0/IO02RSB0 |
| A4 | GAB1/IO03RSB0 |
| A5 | IO16RSB0 |
| A6 | GND |
| A7 | IO29RSB0 |
| A8 | VCC |
| A9 | IO33RSB0 |
| A10 | GBA0/IO39RSB0 |
| A11 | GBA1/IO40RSB0 |
| A12 | GNDQ |
| B1 | GAB2/IO117UDB3 |
| B2 | GND |
| B3 | GAA0/IO00RSB0 |
| B4 | GAA1/IO01RSB0 |
| B5 | IO14RSB0 |
| B6 | IO19RSB0 |
| B7 | IO22RSB0 |
| B8 | IO30RSB0 |
| B9 | GBB0/IO37RSB0 |
| B10 | GBB1/IO38RSB0 |
| B11 | GND |
| B12 | VMV1 |
| C1 | IO117VDB3 |
| C2 | GFA2/IO107PPB3 |
| C3 | GAC2/IO116UDB3 |
| C4 | VCC |
| C5 | IO12RSB0 |
| C6 | IO17RSB0 |
| C7 | IO24RSB0 |
| C8 | IO31RSB0 |
| C9 | IO34RSB0 |
| C10 | GBA2/IO41PDB1 |
| C11 | IO41NDB1 |
| C12 | GBC2/IO43PPB1 |

| FG144 | |
|---|---|
| **Pin Number** | **AGL250 Function** |
| D1 | IO112NDB3 |
| D2 | IO112PDB3 |
| D3 | IO116VDB3 |
| D4 | GAA2/IO118UPB3 |
| D5 | GAC0/IO04RSB0 |
| D6 | GAC1/IO05RSB0 |
| D7 | GBC0/IO35RSB0 |
| D8 | GBC1/IO36RSB0 |
| D9 | GBB2/IO42PDB1 |
| D10 | IO42NDB1 |
| D11 | IO43NPB1 |
| D12 | GCB1/IO49PPB1 |
| E1 | VCC |
| E2 | GFC0/IO110NDB3 |
| E3 | GFC1/IO110PDB3 |
| E4 | VCCIB3 |
| E5 | IO118VPB3 |
| E6 | VCCIB0 |
| E7 | VCCIB0 |
| E8 | GCC1/IO48PDB1 |
| E9 | VCCIB1 |
| E10 | VCC |
| E11 | GCA0/IO50NDB1 |
| E12 | IO51NDB1 |
| F1 | GFB0/IO109NPB3 |
| F2 | VCOMPLF |
| F3 | GFB1/IO109PPB3 |
| F4 | IO107NPB3 |
| F5 | GND |
| F6 | GND |
| F7 | GND |
| F8 | GCC0/IO48NDB1 |
| F9 | GCB0/IO49NPB1 |
| F10 | GND |
| F11 | GCA1/IO50PDB1 |
| F12 | GCA2/IO51PDB1 |

| FG144 | |
|---|---|
| **Pin Number** | **AGL250 Function** |
| G1 | GFA1/IO108PPB3 |
| G2 | GND |
| G3 | VCCPLF |
| G4 | GFA0/IO108NPB3 |
| G5 | GND |
| G6 | GND |
| G7 | GND |
| G8 | GDC1/IO58UPB1 |
| G9 | IO53NDB1 |
| G10 | GCC2/IO53PDB1 |
| G11 | IO52NDB1 |
| G12 | GCB2/IO52PDB1 |
| H1 | VCC |
| H2 | GFB2/IO106PDB3 |
| H3 | GFC2/IO105PSB3 |
| H4 | GEC1/IO100PDB3 |
| H5 | VCC |
| H6 | IO79RSB2 |
| H7 | IO65RSB2 |
| H8 | GDB2/IO62RSB2 |
| H9 | GDC0/IO58VPB1 |
| H10 | VCCIB1 |
| H11 | IO54PSB1 |
| H12 | VCC |
| J1 | GEB1/IO99PDB3 |
| J2 | IO106NDB3 |
| J3 | VCCIB3 |
| J4 | GEC0/IO100NDB3 |
| J5 | IO88RSB2 |
| J6 | IO81RSB2 |
| J7 | VCC |
| J8 | TCK |
| J9 | GDA2/IO61RSB2 |
| J10 | TDO |
| J11 | GDA1/IO60UDB1 |
| J12 | GDB1/IO59UDB1 |

| FG256 | |
|---|---|
| **Pin Number** | **AGL600 Function** |
| R5 | IO132RSB2 |
| R6 | IO127RSB2 |
| R7 | IO121RSB2 |
| R8 | IO114RSB2 |
| R9 | IO109RSB2 |
| R10 | IO105RSB2 |
| R11 | IO98RSB2 |
| R12 | IO96RSB2 |
| R13 | GDB2/IO90RSB2 |
| R14 | TDI |
| R15 | GNDQ |
| R16 | TDO |
| T1 | GND |
| T2 | IO137RSB2 |
| T3 | FF/GEB2/IO142RSB2 |
| T4 | IO134RSB2 |
| T5 | IO125RSB2 |
| T6 | IO123RSB2 |
| T7 | IO118RSB2 |
| T8 | IO115RSB2 |
| T9 | IO111RSB2 |
| T10 | IO106RSB2 |
| T11 | IO102RSB2 |
| T12 | GDC2/IO91RSB2 |
| T13 | IO93RSB2 |
| T14 | GDA2/IO89RSB2 |
| T15 | TMS |
| T16 | GND |

| FG484 | |
|---|---|
| **Pin Number** | **AGL400 Function** |
| K11 | GND |
| K12 | GND |
| K13 | GND |
| K14 | VCC |
| K15 | VCCIB1 |
| K16 | GCC1/IO67PPB1 |
| K17 | IO64NPB1 |
| K18 | IO73PDB1 |
| K19 | IO73NDB1 |
| K20 | NC |
| K21 | NC |
| K22 | NC |
| L1 | NC |
| L2 | NC |
| L3 | NC |
| L4 | GFB0/IO146NPB3 |
| L5 | GFA0/IO145NDB3 |
| L6 | GFB1/IO146PPB3 |
| L7 | VCOMPLF |
| L8 | GFC0/IO147NPB3 |
| L9 | VCC |
| L10 | GND |
| L11 | GND |
| L12 | GND |
| L13 | GND |
| L14 | VCC |
| L15 | GCC0/IO67NPB1 |
| L16 | GCB1/IO68PPB1 |
| L17 | GCA0/IO69NPB1 |
| L18 | NC |
| L19 | GCB0/IO68NPB1 |
| L20 | NC |
| L21 | NC |
| L22 | NC |
| M1 | NC |
| M2 | NC |

| FG484 | |
|---|---|
| **Pin Number** | **AGL600 Function** |
| A1 | GND |
| A2 | GND |
| A3 | VCCIB0 |
| A4 | NC |
| A5 | NC |
| A6 | IO09RSB0 |
| A7 | IO15RSB0 |
| A8 | NC |
| A9 | NC |
| A10 | IO22RSB0 |
| A11 | IO23RSB0 |
| A12 | IO29RSB0 |
| A13 | IO35RSB0 |
| A14 | NC |
| A15 | NC |
| A16 | IO46RSB0 |
| A17 | IO48RSB0 |
| A18 | NC |
| A19 | NC |
| A20 | VCCIB0 |
| A21 | GND |
| A22 | GND |
| AA1 | GND |
| AA2 | VCCIB3 |
| AA3 | NC |
| AA4 | NC |
| AA5 | NC |
| AA6 | IO135RSB2 |
| AA7 | IO133RSB2 |
| AA8 | NC |
| AA9 | NC |
| AA10 | NC |
| AA11 | NC |
| AA12 | NC |
| AA13 | NC |
| AA14 | NC |

| FG484 | |
|---|---|
| **Pin Number** | **AGL600 Function** |
| AA15 | NC |
| AA16 | IO101RSB2 |
| AA17 | NC |
| AA18 | NC |
| AA19 | NC |
| AA20 | NC |
| AA21 | VCCIB1 |
| AA22 | GND |
| AB1 | GND |
| AB2 | GND |
| AB3 | VCCIB2 |
| AB4 | NC |
| AB5 | NC |
| AB6 | IO130RSB2 |
| AB7 | IO128RSB2 |
| AB8 | IO122RSB2 |
| AB9 | IO116RSB2 |
| AB10 | NC |
| AB11 | NC |
| AB12 | IO113RSB2 |
| AB13 | IO112RSB2 |
| AB14 | NC |
| AB15 | NC |
| AB16 | IO100RSB2 |
| AB17 | IO95RSB2 |
| AB18 | NC |
| AB19 | NC |
| AB20 | VCCIB2 |
| AB21 | GND |
| AB22 | GND |
| B1 | GND |
| B2 | VCCIB3 |
| B3 | NC |
| B4 | NC |
| B5 | NC |
| B6 | IO08RSB0 |

| FG484 | |
|---|---|
| **Pin Number** | **AGL600 Function** |
| B7 | IO12RSB0 |
| B8 | NC |
| B9 | NC |
| B10 | IO17RSB0 |
| B11 | NC |
| B12 | NC |
| B13 | IO36RSB0 |
| B14 | NC |
| B15 | NC |
| B16 | IO47RSB0 |
| B17 | IO49RSB0 |
| B18 | NC |
| B19 | NC |
| B20 | NC |
| B21 | VCCIB1 |
| B22 | GND |
| C1 | VCCIB3 |
| C2 | NC |
| C3 | NC |
| C4 | NC |
| C5 | GND |
| C6 | NC |
| C7 | NC |
| C8 | VCC |
| C9 | VCC |
| C10 | NC |
| C11 | NC |
| C12 | NC |
| C13 | NC |
| C14 | VCC |
| C15 | VCC |
| C16 | NC |
| C17 | NC |
| C18 | GND |
| C19 | NC |
| C20 | NC |

| FG484 | |
|---|---|
| **Pin Number** | **AGL600 Function** |
| C21 | NC |
| C22 | VCCIB1 |
| D1 | NC |
| D2 | NC |
| D3 | NC |
| D4 | GND |
| D5 | GAA0/IO00RSB0 |
| D6 | GAA1/IO01RSB0 |
| D7 | GAB0/IO02RSB0 |
| D8 | IO11RSB0 |
| D9 | IO16RSB0 |
| D10 | IO18RSB0 |
| D11 | IO28RSB0 |
| D12 | IO34RSB0 |
| D13 | IO37RSB0 |
| D14 | IO41RSB0 |
| D15 | IO43RSB0 |
| D16 | GBB1/IO57RSB0 |
| D17 | GBA0/IO58RSB0 |
| D18 | GBA1/IO59RSB0 |
| D19 | GND |
| D20 | NC |
| D21 | NC |
| D22 | NC |
| E1 | NC |
| E2 | NC |
| E3 | GND |
| E4 | GAB2/IO173PDB3 |
| E5 | GAA2/IO174PDB3 |
| E6 | GNDQ |
| E7 | GAB1/IO03RSB0 |
| E8 | IO13RSB0 |
| E9 | IO14RSB0 |
| E10 | IO21RSB0 |
| E11 | IO27RSB0 |
| E12 | IO32RSB0 |

| FG484 | |
|---|---|
| **Pin Number** | **AGL600 Function** |
| H19 | IO66PDB1 |
| H20 | VCC |
| H21 | NC |
| H22 | NC |
| J1 | NC |
| J2 | NC |
| J3 | NC |
| J4 | IO166NDB3 |
| J5 | IO168NPB3 |
| J6 | IO167PPB3 |
| J7 | IO169PDB3 |
| J8 | VCCIB3 |
| J9 | GND |
| J10 | VCC |
| J11 | VCC |
| J12 | VCC |
| J13 | VCC |
| J14 | GND |
| J15 | VCCIB1 |
| J16 | IO62NDB1 |
| J17 | IO64NPB1 |
| J18 | IO65PPB1 |
| J19 | IO66NDB1 |
| J20 | NC |
| J21 | IO68PDB1 |
| J22 | IO68NDB1 |
| K1 | IO157PDB3 |
| K2 | IO157NDB3 |
| K3 | NC |
| K4 | IO165NDB3 |
| K5 | IO165PDB3 |
| K6 | IO168PPB3 |
| K7 | GFC1/IO164PPB3 |
| K8 | VCCIB3 |
| K9 | VCC |
| K10 | GND |

| FG484 | |
|---|---|
| **Pin Number** | **AGL1000 Function** |
| U1 | IO195PDB3 |
| U2 | IO195NDB3 |
| U3 | IO194NPB3 |
| U4 | GEB1/IO189PDB3 |
| U5 | GEB0/IO189NDB3 |
| U6 | VMV2 |
| U7 | IO179RSB2 |
| U8 | IO171RSB2 |
| U9 | IO165RSB2 |
| U10 | IO159RSB2 |
| U11 | IO151RSB2 |
| U12 | IO137RSB2 |
| U13 | IO134RSB2 |
| U14 | IO128RSB2 |
| U15 | VMV1 |
| U16 | TCK |
| U17 | VPUMP |
| U18 | TRST |
| U19 | GDA0/IO113NDB1 |
| U20 | NC |
| U21 | IO108NDB1 |
| U22 | IO109PDB1 |
| V1 | NC |
| V2 | NC |
| V3 | GND |
| V4 | GEA1/IO188PDB3 |
| V5 | GEA0/IO188NDB3 |
| V6 | IO184RSB2 |
| V7 | GEC2/IO185RSB2 |
| V8 | IO168RSB2 |
| V9 | IO163RSB2 |
| V10 | IO157RSB2 |
| V11 | IO149RSB2 |
| V12 | IO143RSB2 |
| V13 | IO138RSB2 |
| V14 | IO131RSB2 |

| Revision / Version | Changes | Page |
|---|---|---|
| Advance v0.4 (September 2007) | Cortex-M1 device information was added to Table 1 • IGLOO Product Family, the "I/Os Per Package1" table, "IGLOO Ordering Information", and Temperature Grade Offerings. | i, ii, iii, iv |
| | The number of single-ended I/Os for the CS81 package for AGL030 was updated to 66 in the "I/Os Per Package1" table. | ii |
| | The "Power Conservation Techniques" section was updated to recommend that unused I/O signals be left floating. | 2-51 |
| Advance v0.3 (August 2007) | In Table 1 • IGLOO Product Family, the CS81 package was added for AGL030. The CS196 was replaced by the CS121 for AGL060. Table note 3 was moved to the specific packages to which it applies for AGL060: QN132 and FG144. | i |
| | The CS81 and CS121 packages were added to the "I/Os Per Package1" table. The number of single-ended I/Os was removed for the CS196 package in AGL060. Table note 6 was moved to the specific packages to which it applies for AGL060: QN132 and FG144. | ii |
| | The CS81 and CS121 packages were added to the Temperature Grade Offerings table. The temperature grade offerings were removed for the CS196 package in AGL060. Table note 3 was moved to the specific packages to which it applies for AGL060: QN132 and FG144. | iv |
| | The CS81 and CS121 packages were added to Table 2-31 • Flash*Freeze Pin Location in IGLOO Family Packages (device-independent). | 2-61 |
| Advance v0.2 | The words "ambient temperature" were added to the temperature range in the "IGLOO Ordering Information", Temperature Grade Offerings, and "Speed Grade and Temperature Grade Matrix" sections. | iii, iv |
| | The $T_J$ parameter in Table 3-2 • Recommended Operating Conditions was changed to $T_A$, ambient temperature, and table notes 4–6 were added. | 3-2 |