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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	3072
Total RAM Bits	36864
Number of I/O	97
Number of Gates	125000
Voltage - Supply	1.14V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	144-LBGA
Supplier Device Package	144-FPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/agl125v2-fgg144i

Table 2-43 • I/O Short Currents IOSH/IOSL
Applicable to Standard Plus I/O Banks

	Drive Strength	IOSL (mA)*	IOSH (mA)*
3.3 V LVTTTL / 3.3 V LVCMOS	2 mA	25	27
	4 mA	25	27
	6 mA	51	54
	8 mA	51	54
	12 mA	103	109
	16 mA	103	109
3.3 V LVCMOS Wide Range	100 μ A	Same as regular 3.3 V LVCMOS	Same as regular 3.3 V LVCMOS
2.5 V LVCMOS	2 mA	16	18
	4 mA	16	18
	6 mA	32	37
	8 mA	32	37
	12 mA	65	74
1.8 V LVCMOS	2 mA	9	11
	4 mA	17	22
	6 mA	35	44
	8 mA	35	44
1.5 V LVCMOS	2 mA	13	16
	4 mA	25	33
1.2 V LVCMOS	2 mA	20	26
1.2 V LVCMOS Wide Range	100 μ A	20	26
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	103	109

Note: * $T_J = 100^{\circ}\text{C}$

Table 2-49 • Minimum and Maximum DC Input and Output Levels
Applicable to Standard I/O Banks

3.3 V LVTTTL / 3.3 V LVCMOS	VIL		VIH		V _{OL}	VOH	IOL	IOH	IOSL	IOSH	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	−0.3	0.8	2	3.6	0.4	2.4	2	2	25	27	10	10
4 mA	−0.3	0.8	2	3.6	0.4	2.4	4	4	25	27	10	10
6 mA	−0.3	0.8	2	3.6	0.4	2.4	6	6	51	54	10	10
8 mA	−0.3	0.8	2	3.6	0.4	2.4	8	8	51	54	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

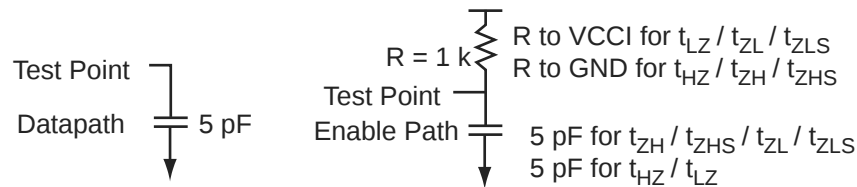


Figure 2-7 • AC Loading

Table 2-50 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C _{LOAD} (pF)
0	3.3	1.4	5

Note: *Measuring point = V_{trip}. See Table 2-29 on page 2-28 for a complete table of trip points.

Applies to 1.2 V Core Voltage**Table 2-89 • 2.5 V LVC MOS Low Slew – Applies to 1.2 V DC Core Voltage**

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V
 Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	5.59	0.26	1.20	1.10	5.68	5.14	2.82	2.80	11.47	10.93	ns
4 mA	Std.	1.55	5.59	0.26	1.20	1.10	5.68	5.14	2.82	2.80	11.47	10.93	ns
6 mA	Std.	1.55	4.76	0.26	1.20	1.10	4.84	4.47	3.10	3.33	10.62	10.26	ns
8 mA	Std.	1.55	4.76	0.26	1.20	1.10	4.84	4.47	3.10	3.33	10.62	10.26	ns
12 mA	Std.	1.55	4.17	0.26	1.20	1.10	4.23	3.99	3.30	3.67	10.02	9.77	ns
16 mA	Std.	1.55	3.98	0.26	1.20	1.10	4.04	3.88	3.34	3.76	9.83	9.66	ns
24 mA	Std.	1.55	3.90	0.26	1.20	1.10	3.96	3.90	3.40	4.09	9.75	9.68	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-90 • 2.5 V LVC MOS High Slew – Applies to 1.2 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V
 Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	3.33	0.26	1.20	1.10	3.38	3.09	2.82	2.91	9.17	8.88	ns
4 mA	Std.	1.55	3.33	0.26	1.20	1.10	3.38	3.09	2.82	2.91	9.17	8.88	ns
6 mA	Std.	1.55	2.89	0.26	1.20	1.10	2.93	2.56	3.10	3.45	8.72	8.34	ns
8 mA	Std.	1.55	2.89	0.26	1.20	1.10	2.93	2.56	3.10	3.45	8.72	8.34	ns
12 mA	Std.	1.55	2.64	0.26	1.20	1.10	2.67	2.29	3.30	3.79	8.46	8.08	ns
16 mA	Std.	1.55	2.59	0.26	1.20	1.10	2.63	2.24	3.34	3.88	8.41	8.03	ns
24 mA	Std.	1.55	2.60	0.26	1.20	1.10	2.64	2.18	3.40	4.22	8.42	7.97	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-91 • 2.5 V LVC MOS Low Slew – Applies to 1.2 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V
 Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	5.02	0.26	1.19	1.10	5.11	4.60	2.50	2.62	10.89	10.38	ns
4 mA	Std.	1.55	5.02	0.26	1.19	1.10	5.11	4.60	2.50	2.62	10.89	10.38	ns
6 mA	Std.	1.55	4.21	0.26	1.19	1.10	4.27	4.00	2.76	3.10	10.06	9.79	ns
8 mA	Std.	1.55	4.21	0.26	1.19	1.10	4.27	4.00	2.76	3.10	10.06	9.79	ns
12 mA	Std.	1.55	3.66	0.26	1.19	1.10	3.71	3.55	2.94	3.41	9.50	9.34	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

1.5 V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.5 V applications. It uses a 1.5 V input buffer and a push-pull output buffer.

Table 2-111 • Minimum and Maximum DC Input and Output Levels
Applicable to Advanced I/O Banks

1.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	2	2	13	16	10	10
4 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	4	4	25	33	10	10
6 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	6	6	32	39	10	10
8 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	8	8	66	55	10	10
12 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	12	12	66	55	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

Table 2-112 • Minimum and Maximum DC Input and Output Levels
Applicable to Standard Plus I/O Banks

1.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSH	IOSL	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	2	2	13	16	10	10
4 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	4	4	25	33	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

Timing Characteristics**1.5 V DC Core Voltage****Table 2-115 • 1.5 V LVC MOS Low Slew – Applies to 1.5 V DC Core Voltage****Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V****Applicable to Advanced I/O Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	6.62	0.18	1.17	0.66	6.75	6.06	2.79	2.31	10.35	9.66	ns
4 mA	Std.	0.97	5.75	0.18	1.17	0.66	5.86	5.34	3.06	2.78	9.46	8.93	ns
6 mA	Std.	0.97	5.43	0.18	1.17	0.66	5.54	5.19	3.12	2.90	9.13	8.78	ns
8 mA	Std.	0.97	5.35	0.18	1.17	0.66	5.46	5.20	2.63	3.36	9.06	8.79	ns
12 mA	Std.	0.97	5.35	0.18	1.17	0.66	5.46	5.20	2.63	3.36	9.06	8.79	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-116 • 1.5 V LVC MOS High Slew – Applies to 1.5 V DC Core Voltage**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V****Applicable to Advanced I/O Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	2.97	0.18	1.17	0.66	3.04	2.90	2.78	2.40	6.63	6.50	ns
4 mA	Std.	0.97	2.60	0.18	1.17	0.66	2.65	2.45	3.05	2.88	6.25	6.05	ns
6 mA	Std.	0.97	2.53	0.18	1.17	0.66	2.58	2.37	3.11	3.00	6.18	5.96	ns
8 mA	Std.	0.97	2.50	0.18	1.17	0.66	2.56	2.27	3.21	3.48	6.15	5.86	ns
12 mA	Std.	0.97	2.50	0.18	1.17	0.66	2.56	2.27	3.21	3.48	6.15	5.86	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-117 • 1.5 V LVC MOS Low Slew – Applies to 1.5 V DC Core Voltage**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V****Applicable to Standard Plus Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	5.93	0.18	1.18	0.66	6.04	5.46	2.30	2.15	9.64	9.06	ns
4 mA	Std.	0.97	5.11	0.18	1.18	0.66	5.21	4.80	2.54	2.58	8.80	8.39	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-118 • 1.5 V LVC MOS High Slew – Applies to 1.5 V DC Core Voltage**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V****Applicable to Standard Plus Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	2.58	0.18	1.18	0.66	2.64	2.41	2.29	2.24	6.23	6.01	ns
4 mA	Std.	0.97	2.25	0.18	1.18	0.66	2.30	2.00	2.53	2.68	5.89	5.59	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-151 • Minimum and Maximum DC Input and Output Levels

DC Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
VCCI	Supply Voltage	3.0		3.3		3.6		V
VOL	Output Low Voltage	0.96	1.27	1.06	1.43	1.30	1.57	V
VOH	Output High Voltage	1.8	2.11	1.92	2.28	2.13	2.41	V
VIL, VIH	Input Low, Input High Voltages	0	3.6	0	3.6	0	3.6	V
V _{ODIFF}	Differential Output Voltage	0.625	0.97	0.625	0.97	0.625	0.97	V
V _{OCM}	Output Common-Mode Voltage	1.762	1.98	1.762	1.98	1.762	1.98	V
V _{ICM}	Input Common-Mode Voltage	1.01	2.57	1.01	2.57	1.01	2.57	V
V _{IDIFF}	Input Differential Voltage	300		300		300		mV

Table 2-152 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)
1.64	1.94	Cross point

Note: *Measuring point = V_{trip}. See Table 2-28 on page 2-104 for a complete table of trip points.

Timing Characteristics

1.5 V DC Core Voltage

Table 2-153 • LVPECL – Applies to 1.5 V DC Core Voltage

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V

Applicable to Standard Banks

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{py}	Units
Std.	0.97	1.67	0.19	1.16	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

1.2 V DC Core Voltage

Table 2-154 • LVPECL – Applies to 1.2 V DC Core Voltage

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 3.0 V

Applicable to Standard Banks

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{py}	Units
Std.	1.55	2.24	0.25	1.37	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

I/O Register Specifications

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

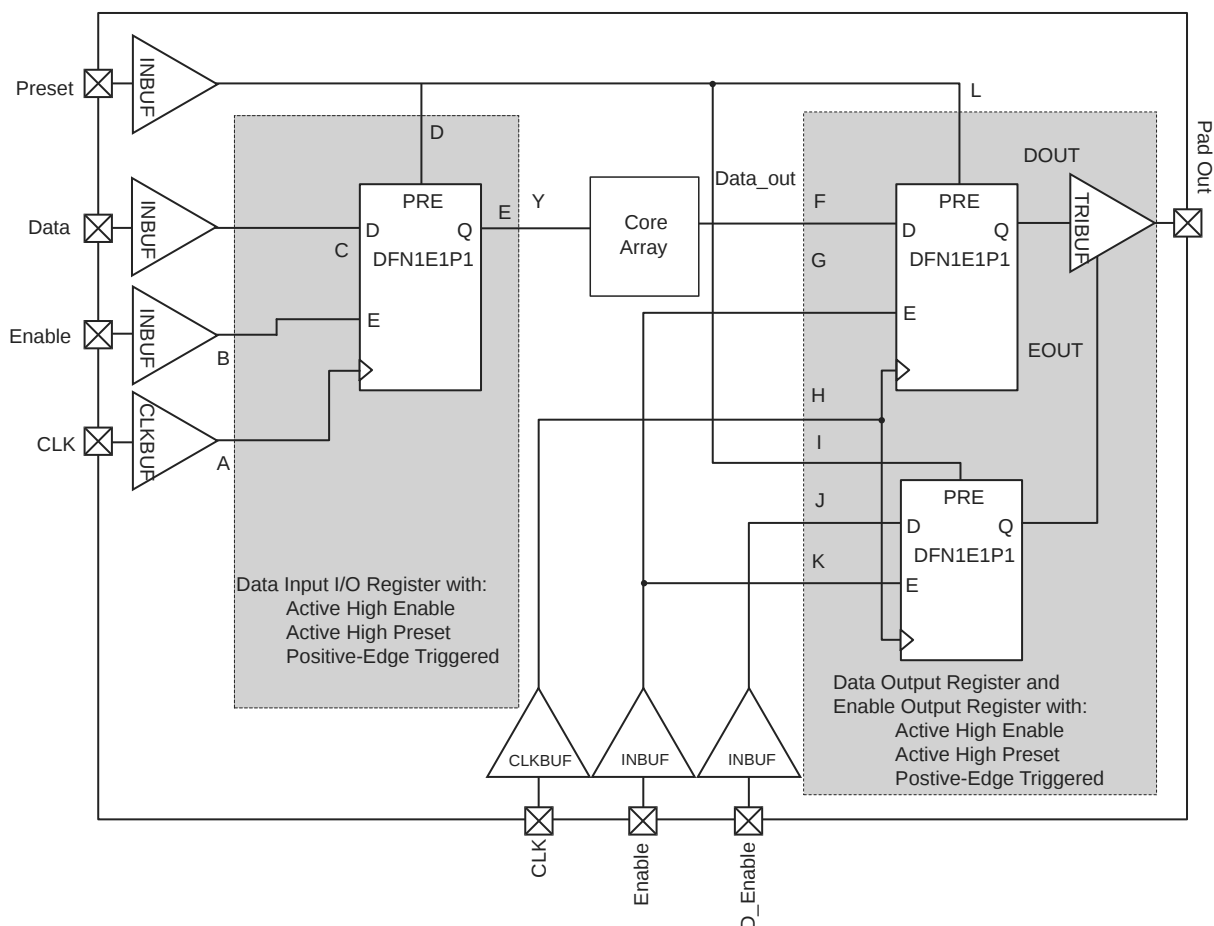


Figure 2-16 • Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

Table 2-155 • Parameter Definition and Measuring Nodes

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	H, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	F, H
t_{OHD}	Data Hold Time for the Output Data Register	F, H
t_{OSUE}	Enable Setup Time for the Output Data Register	G, H
t_{OHE}	Enable Hold Time for the Output Data Register	G, H
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	L, DOUT
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	L, H
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	L, H
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	H, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	J, H
t_{OEHD}	Data Hold Time for the Output Enable Register	J, H
t_{OESUE}	Enable Setup Time for the Output Enable Register	K, H
t_{OEHE}	Enable Hold Time for the Output Enable Register	K, H
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	I, H
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	I, H
t_{ICLKQ}	Clock-to-Q of the Input Data Register	A, E
t_{ISUD}	Data Setup Time for the Input Data Register	C, A
t_{IHD}	Data Hold Time for the Input Data Register	C, A
t_{ISUE}	Enable Setup Time for the Input Data Register	B, A
t_{IHE}	Enable Hold Time for the Input Data Register	B, A
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	D, E
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	D, A
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	D, A

Note: *See Figure 2-16 on page 2-84 for more information.

Timing Waveforms

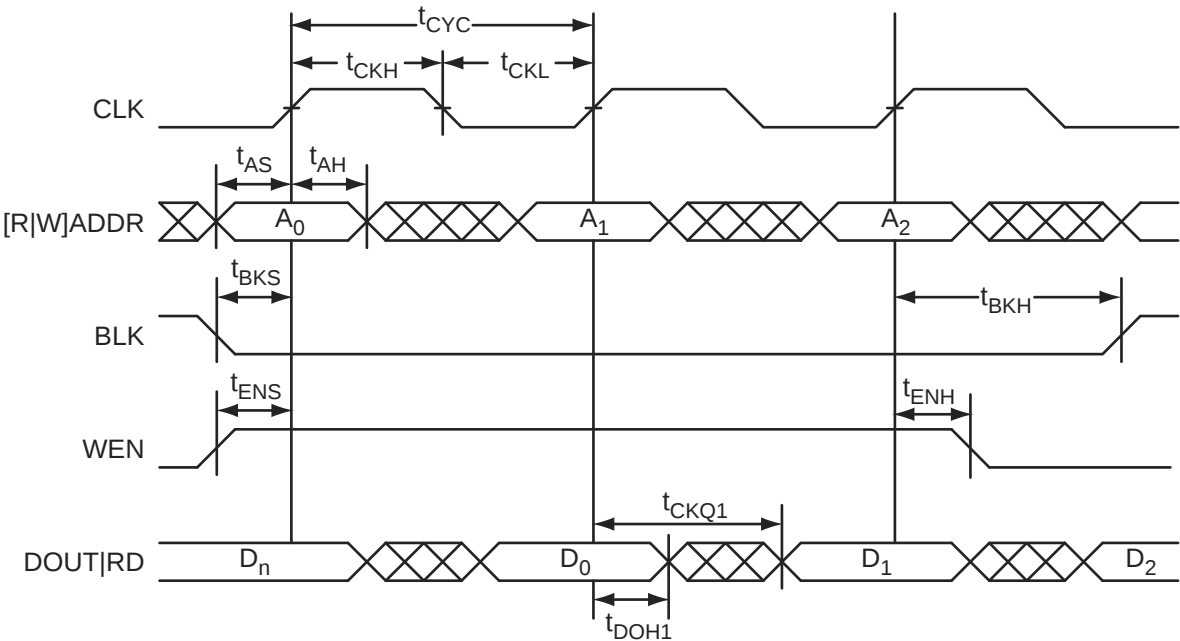


Figure 2-32 • RAM Read for Pass-Through Output. Applicable to Both RAM4K9 and RAM512x18.

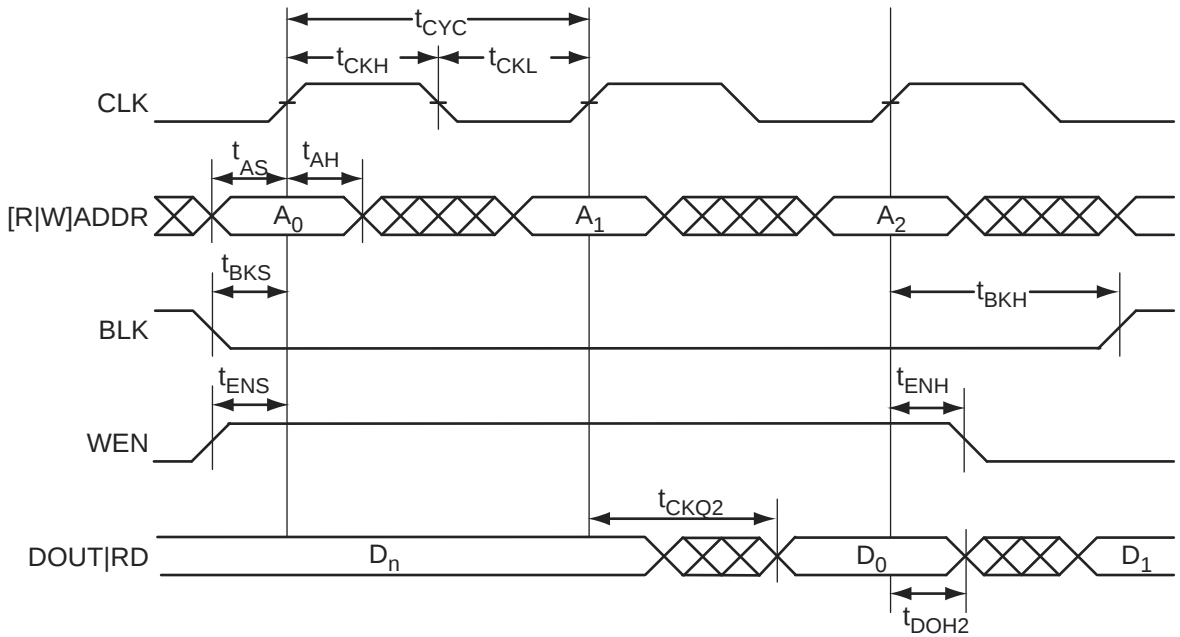


Figure 2-33 • RAM Read for Pipelined Output. Applicable to Both RAM4K9 and RAM512x18.

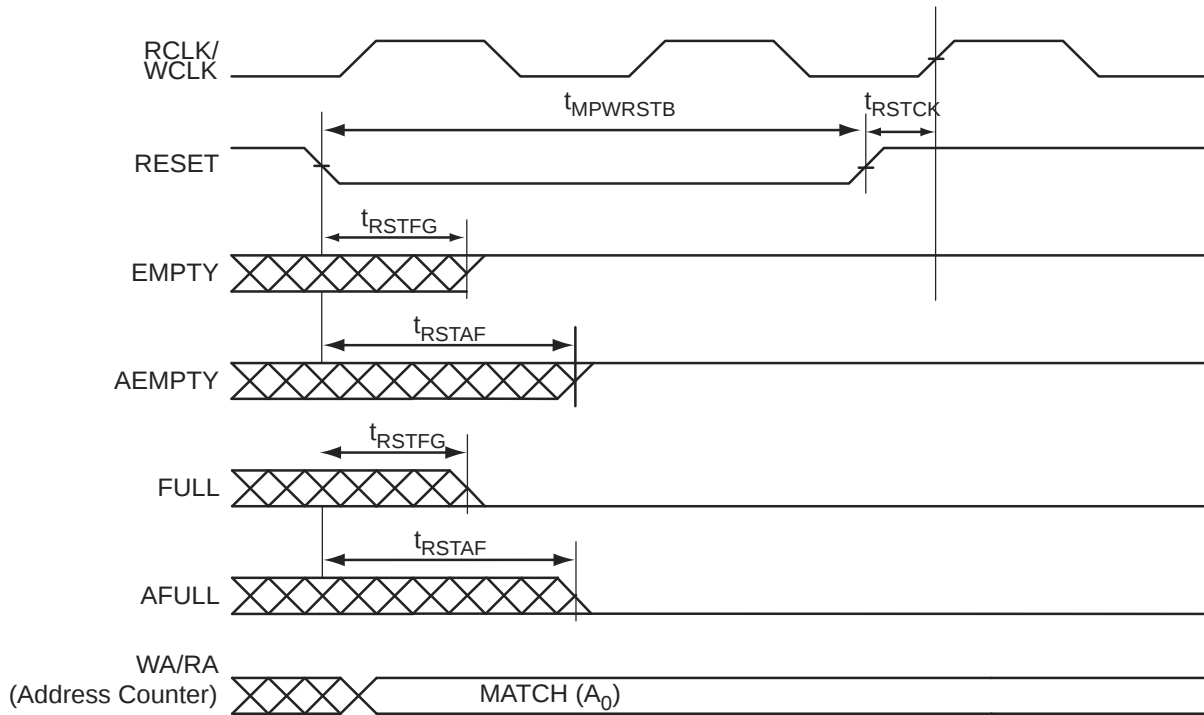


Figure 2-40 • FIFO Reset

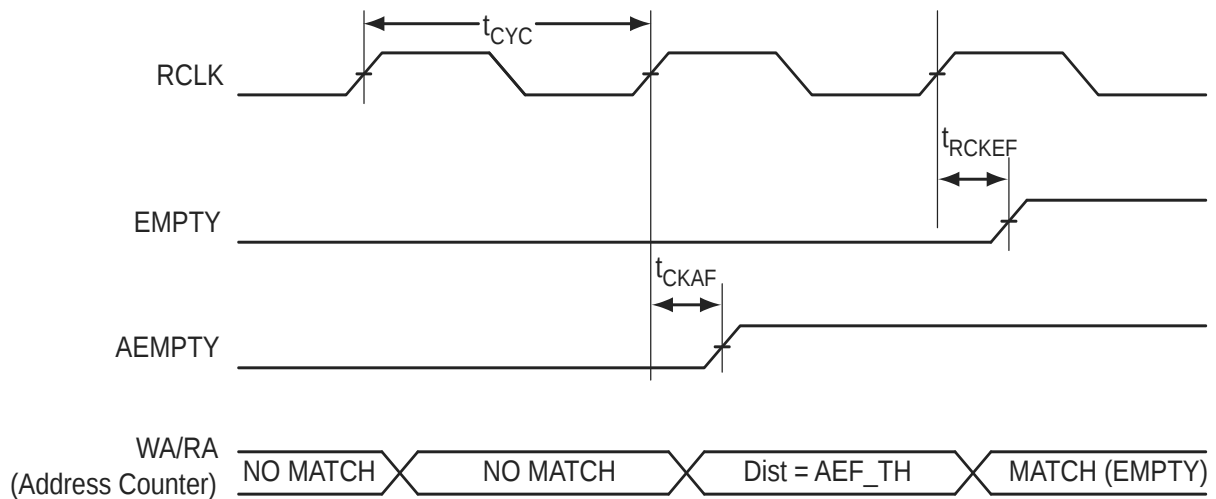


Figure 2-41 • FIFO EMPTY Flag and AEMPTY Flag Assertion

CS196	
Pin Number	AGL400 Function
A1	GND
A2	GAA0/IO00RSB0
A3	GAC0/IO04RSB0
A4	GAC1/IO05RSB0
A5	IO14RSB0
A6	IO18RSB0
A7	IO26RSB0
A8	IO29RSB0
A9	IO36RSB0
A10	GBC0/IO54RSB0
A11	GBB0/IO56RSB0
A12	GBB1/IO57RSB0
A13	GBA1/IO59RSB0
A14	GND
B1	VCCIB3
B2	VMV0
B2	VMV0
B3	GAA1/IO01RSB0
B4	GAB1/IO03RSB0
B5	GND
B6	IO17RSB0
B7	IO25RSB0
B8	IO34RSB0
B9	IO39RSB0
B10	GND
B11	GBC1/IO55RSB0
B12	GBA0/IO58RSB0
B13	GBA2/IO60PPB1
B14	GBB2/IO61PDB1
C1	GAC2/IO153UDB3
C2	GAB2/IO154UDB3
C3	GNDQ
C4	VCCIB0
C5	GAB0/IO02RSB0
C6	IO15RSB0
C7	VCCIB0

CS196	
Pin Number	AGL400 Function
C8	IO31RSB0
C9	IO44RSB0
C10	IO49RSB0
C11	VCCIB0
C12	IO60NPB1
C13	GNDQ
C14	IO61NDB1
D1	IO153VDB3
D2	IO154VDB3
D3	GAA2/IO155UDB3
D4	IO150PPB3
D5	IO11RSB0
D6	IO20RSB0
D7	IO23RSB0
D8	IO28RSB0
D9	IO41RSB0
D10	IO47RSB0
D11	IO63PPB1
D12	VMV1
D13	IO62NDB1
D14	GBC2/IO62PDB1
E1	IO149PDB3
E2	GND
E3	IO155VDB3
E4	VCCIB3
E5	IO151USB3
E6	IO09RSB0
E7	IO12RSB0
E8	IO32RSB0
E9	IO46RSB0
E10	IO51RSB0
E11	VCCIB1
E12	IO63NPB1
E13	GND
E14	IO64PDB1
F1	IO149NDB3

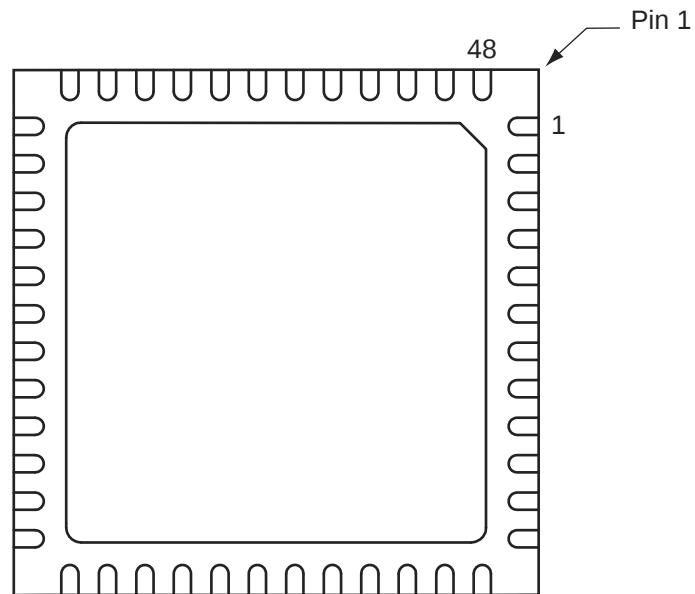
CS196	
Pin Number	AGL400 Function
F2	IO144NPB3
F3	IO148PDB3
F4	IO148NDB3
F5	IO150NPB3
F6	IO07RSB0
F7	VCC
F8	VCC
F9	IO43RSB0
F10	IO73PDB1
F11	IO73NDB1
F12	IO66NDB1
F13	IO66PDB1
F14	IO64NDB1
G1	GFB1/IO146PDB3
G2	GFA0/IO145NDB3
G3	GFA2/IO144PPB3
G4	VCOMPLF
G5	GFC0/IO147NDB3
G6	VCC
G7	GND
G8	GND
G9	VCC
G10	GCC0/IO67NDB1
G11	GCB1/IO68PDB1
G12	GCA0/IO69NDB1
G13	IO72NDB1
G14	GCC2/IO72PDB1
H1	GFB0/IO146NDB3
H2	GFA1/IO145PDB3
H3	VCCPLF
H4	GFB2/IO143PPB3
H5	GFC1/IO147PDB3
H6	VCC
H7	GND
H8	GND
H9	VCC

CS281	
Pin Number	AGL1000 Function
H8	VCC
H9	VCCIB0
H10	VCC
H11	VCCIB0
H12	VCC
H13	VCCIB1
H15	IO90NPB1
H16	GCB0/IO92NPB1
H18	GCA1/IO93PPB1
H19	GCA2/IO94PPB1
J1	VCOMPLF
J2	GFA0/IO207NDB3
J4	VCCPLF
J5	GFC0/IO209NPB3
J7	GFA2/IO206PDB3
J8	VCCIB3
J9	GND
J10	GND
J11	GND
J12	VCCIB1
J13	GCC1/IO91PPB1
J15	GCA0/IO93NPB1
J16	GCB2/IO95PPB1
J18	IO94NPB1
J19	IO102PSB1
K1	VCCIB3
K2	GFA1/IO207PDB3
K4	GND
K5	IO204NPB3
K7	IO206NDB3
K8	VCC
K9	GND
K10	GND
K11	GND
K12	VCC
K13	GCC2/IO96PPB1

CS281	
Pin Number	AGL1000 Function
K15	IO95NPB1
K16	GND
K18	IO96NPB1
K19	VCCIB1
L1	GFB2/IO205PDB3
L2	IO205NDB3
L4	GFC2/IO204PPB3
L5	IO203PPB3
L7	IO203NPB3
L8	VCCIB3
L9	GND
L10	GND
L11	GND
L12	VCCIB1
L13	IO103PPB1
L15	IO103NPB1
L16	IO97PPB1
L18	IO98NPB1
L19	IO97NPB1
M1	IO202PDB3
M2	IO202NDB3
M4	IO201NPB3
M5	IO198PPB3
M7	VCCIB3
M8	VCC
M9	VCCIB2
M10	VCC
M11	VCCIB2
M12	VCC
M13	VCCIB1
M15	IO104NPB1
M16	IO100NPB1
M18	IO104PPB1
M19	IO98PPB1
N1	IO201PPB3
N2	IO198NPB3

CS281	
Pin Number	AGL1000 Function
N4	IO196PPB3
N5	IO197NPB3
N7	GEA2/IO187RSB2
N8	VCCIB2
N9	IO155RSB2
N10	IO154RSB2
N11	IO150RSB2
N12	VCCIB2
N13	VPUMP
N15	IO107PPB1
N16	IO105PPB1
N18	IO107NPB1
N19	IO100PPB1
P1	IO195PDB3
P2	GND
P3	IO195NDB3
P4	IO194PPB3
P5	GEA0/IO188NPB3
P15	IO108NDB1
P16	IO108PDB1
P17	GDC1/IO111PPB1
P18	GND
P19	IO105NPB1
R1	IO196NPB3
R2	IO194NPB3
R4	GEC1/IO190PPB3
R5	GEB1/IO189PPB3
R6	IO184RSB2
R7	IO173RSB2
R8	IO168RSB2
R9	IO160RSB2
R10	IO151RSB2
R11	IO141RSB2
R12	IO136RSB2
R13	IO127RSB2
R14	IO124RSB2

QN48



Notes:

1. This is the bottom view of the package.
 2. The die attach paddle center of the package is tied to ground (GND).
-

Note

For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

QN132	
Pin Number	AGL250 Function
C17	IO74RSB2
C18	VCCIB2
C19	TCK
C20	VMV2
C21	VPUMP
C22	VJTAG
C23	VCCIB1
C24	IO53NSB1
C25	IO51NPB1
C26	GCA1/IO50PPB1
C27	GCC0/IO48NDB1
C28	VCCIB1
C29	IO42NDB1
C30	GNDQ
C31	GBA1/IO40RSB0
C32	GBB0/IO37RSB0
C33	VCC
C34	IO24RSB0
C35	IO19RSB0
C36	IO16RSB0
C37	IO10RSB0
C38	VCCIB0
C39	GAB1/IO03RSB0
C40	VMV0
D1	GND
D2	GND
D3	GND
D4	GND

FG144	
Pin Number	AGL125 Function
A1	GNDQ
A2	VMV0
A3	GAB0/IO02RSB0
A4	GAB1/IO03RSB0
A5	IO11RSB0
A6	GND
A7	IO18RSB0
A8	VCC
A9	IO25RSB0
A10	GBA0/IO39RSB0
A11	GBA1/IO40RSB0
A12	GNDQ
B1	GAB2/IO69RSB1
B2	GND
B3	GAA0/IO00RSB0
B4	GAA1/IO01RSB0
B5	IO08RSB0
B6	IO14RSB0
B7	IO19RSB0
B8	IO22RSB0
B9	GBB0/IO37RSB0
B10	GBB1/IO38RSB0
B11	GND
B12	VMV0
C1	IO132RSB1
C2	GFA2/IO120RSB1
C3	GAC2/IO131RSB1
C4	VCC
C5	IO10RSB0
C6	IO12RSB0
C7	IO21RSB0
C8	IO24RSB0
C9	IO27RSB0
C10	GBA2/IO41RSB0
C11	IO42RSB0
C12	GBC2/IO45RSB0

FG144	
Pin Number	AGL125 Function
D1	IO128RSB1
D2	IO129RSB1
D3	IO130RSB1
D4	GAA2/IO67RSB1
D5	GAC0/IO04RSB0
D6	GAC1/IO05RSB0
D7	GBC0/IO35RSB0
D8	GBC1/IO36RSB0
D9	GBB2/IO43RSB0
D10	IO28RSB0
D11	IO44RSB0
D12	GCB1/IO53RSB0
E1	VCC
E2	GFC0/IO125RSB1
E3	GFC1/IO126RSB1
E4	VCCIB1
E5	IO68RSB1
E6	VCCIB0
E7	VCCIB0
E8	GCC1/IO51RSB0
E9	VCCIB0
E10	VCC
E11	GCA0/IO56RSB0
E12	IO46RSB0
F1	GFB0/IO123RSB1
F2	VCOMPLF
F3	GFB1/IO124RSB1
F4	IO127RSB1
F5	GND
F6	GND
F7	GND
F8	GCC0/IO52RSB0
F9	GCB0/IO54RSB0
F10	GND
F11	GCA1/IO55RSB0
F12	GCA2/IO57RSB0

FG144	
Pin Number	AGL125 Function
G1	GFA1/IO121RSB1
G2	GND
G3	VCCPLF
G4	GFA0/IO122RSB1
G5	GND
G6	GND
G7	GND
G8	GDC1/IO61RSB0
G9	IO48RSB0
G10	GCC2/IO59RSB0
G11	IO47RSB0
G12	GCB2/IO58RSB0
H1	VCC
H2	GFB2/IO119RSB1
H3	GFC2/IO118RSB1
H4	GEC1/IO112RSB1
H5	VCC
H6	IO50RSB0
H7	IO60RSB0
H8	GDB2/IO71RSB1
H9	GDC0/IO62RSB0
H10	VCCIB0
H11	IO49RSB0
H12	VCC
J1	GEB1/IO110RSB1
J2	IO115RSB1
J3	VCCIB1
J4	GEC0/IO111RSB1
J5	IO116RSB1
J6	IO117RSB1
J7	VCC
J8	TCK
J9	GDA2/IO70RSB1
J10	TDO
J11	GDA1/IO65RSB0
J12	GDB1/IO63RSB0

FG144	
Pin Number	AGL400 Function
K1	GEB0/IO136NDB3
K2	GEA1/IO135PDB3
K3	GEA0/IO135NDB3
K4	GEA2/IO134RSB2
K5	IO127RSB2
K6	IO121RSB2
K7	GND
K8	IO104RSB2
K9	GDC2/IO82RSB2
K10	GND
K11	GDA0/IO79VDB1
K12	GDB0/IO78VDB1
L1	GND
L2	VMV3
L3	FF/GEB2/IO133RSB2
L4	IO128RSB2
L5	VCCIB2
L6	IO119RSB2
L7	IO114RSB2
L8	IO110RSB2
L9	TMS
L10	VJTAG
L11	VMV2
L12	TRST
M1	GNDQ
M2	GEC2/IO132RSB2
M3	IO129RSB2
M4	IO126RSB2
M5	IO124RSB2
M6	IO122RSB2
M7	IO117RSB2
M8	IO115RSB2
M9	TDI
M10	VCCIB2
M11	VPUMP
M12	GNDQ

FG484	
Pin Number	AGL400 Function
E13	IO38RSB0
E14	IO42RSB0
E15	GBC1/IO55RSB0
E16	GBB0/IO56RSB0
E17	IO44RSB0
E18	GBA2/IO60PDB1
E19	IO60NDB1
E20	GND
E21	NC
E22	NC
F1	NC
F2	NC
F3	NC
F4	IO154VDB3
F5	IO155VDB3
F6	IO11RSB0
F7	IO07RSB0
F8	GAC0/IO04RSB0
F9	GAC1/IO05RSB0
F10	IO20RSB0
F11	IO24RSB0
F12	IO33RSB0
F13	IO39RSB0
F14	IO45RSB0
F15	GBC0/IO54RSB0
F16	IO48RSB0
F17	VMV0
F18	IO61NPB1
F19	IO63PDB1
F20	NC
F21	NC
F22	NC
G1	NC
G2	NC
G3	NC
G4	IO151VDB3

FG484	
Pin Number	AGL1000 Function
K11	GND
K12	GND
K13	GND
K14	VCC
K15	VCCIB1
K16	GCC1/IO91PPB1
K17	IO90NPB1
K18	IO88PDB1
K19	IO88NDB1
K20	IO94NPB1
K21	IO98NDB1
K22	IO98PDB1
L1	NC
L2	IO200PDB3
L3	IO210NPB3
L4	GFB0/IO208NPB3
L5	GFA0/IO207NDB3
L6	GFB1/IO208PPB3
L7	VCOMPLF
L8	GFC0/IO209NPB3
L9	VCC
L10	GND
L11	GND
L12	GND
L13	GND
L14	VCC
L15	GCC0/IO91NPB1
L16	GCB1/IO92PPB1
L17	GCA0/IO93NPB1
L18	IO96NPB1
L19	GCB0/IO92NPB1
L20	IO97PDB1
L21	IO97NDB1
L22	IO99NPB1
M1	NC
M2	IO200NDB3

FG484	
Pin Number	AGL1000 Function
U1	IO195PDB3
U2	IO195NDB3
U3	IO194NPB3
U4	GEB1/IO189PDB3
U5	GEB0/IO189NDB3
U6	VMV2
U7	IO179RSB2
U8	IO171RSB2
U9	IO165RSB2
U10	IO159RSB2
U11	IO151RSB2
U12	IO137RSB2
U13	IO134RSB2
U14	IO128RSB2
U15	VMV1
U16	TCK
U17	VPUMP
U18	TRST
U19	GDA0/IO113NDB1
U20	NC
U21	IO108NDB1
U22	IO109PDB1
V1	NC
V2	NC
V3	GND
V4	GEA1/IO188PDB3
V5	GEA0/IO188NDB3
V6	IO184RSB2
V7	GEC2/IO185RSB2
V8	IO168RSB2
V9	IO163RSB2
V10	IO157RSB2
V11	IO149RSB2
V12	IO143RSB2
V13	IO138RSB2
V14	IO131RSB2

Revision / Version	Changes	Page
Advance v0.7 (continued)	The former Table 2-16 • Maximum I/O Frequency for Single-Ended and Differential I/Os in All Banks in IGLOO Devices (maximum drive strength and high slew selected) was removed.	N/A
	The "During Flash*Freeze Mode" section was updated to include information about the output of the I/O to the FPGA core.	2-57
	Table 2-31 • Flash*Freeze Pin Location in IGLOO Family Packages (device-independent) was updated to add UC81 and CS281. Flash*Freeze pins were assigned for CS81, CS121, and CS196.	2-61
	Figure 2-40 • Flash*Freeze Mode Type 2 – Timing Diagram was updated to modify the LSICC Signal.	2-55
	Information regarding calculation of the quiescent supply current was added to the "Quiescent Supply Current" section.	3-6
	Table 3-8 • Quiescent Supply Current (I_{DD}) Characteristics, IGLOO Flash*Freeze Mode [†] was updated.	3-6
	Table 3-9 • Quiescent Supply Current (I_{DD}) Characteristics, IGLOO Sleep Mode ($V_{CC} = 0\text{ V}$) [†] was updated.	3-6
	Table 3-11 • Quiescent Supply Current (I_{DD}), No IGLOO Flash*Freeze Mode ¹ was updated.	3-7
	Table 3-115 • Minimum and Maximum DC Input and Output Levels was updated.	3-58
	Table 3-156 • JTAG 1532 was updated and Table 3-155 • JTAG 1532 is new.	3-104
	The "121-Pin CSP" and "281-Pin CSP" packages are new.	4-5, 4-7
	The "81-Pin CSP" table for the AGL030 device was updated to change the G6 pin function to IO44RSB1 and the JG pin function to IO45RSB1.	4-4
	The "121-Pin CSP" table for the AGL060 device is new.	4-6
	The "256-Pin FBGA" table for the AGL1000 device is new.	4-34
	The "281-Pin CSP" table for the AGL 600 device is new.	4-8
	The "100-Pin VQFP" table for the AGL060 device is new.	4-18
	The "144-Pin FBGA" table for the AGL250 device is new.	4-24
	The "144-Pin FBGA" table for the AGL1000 device is new.	4-28
	The "484-Pin FBGA" table for the AGL600 device is new.	4-38
	The "484-Pin FBGA" table for the AGL1000 device is new.	4-43
Advance v0.6 (November 2007)	Table 1 • IGLOO Product Family, the "I/Os Per Package ¹ " table, and the "IGLOO Ordering Information", and the Temperature Grade Offerings table were updated to add the UC81 package.	i, ii, iii, iv
	The "81-Pin μ CSP" table for the AGL030 device is new.	4-3
	The "81-Pin CSP" table for the AGL030 device is new.	4-1
Advance v0.5 (September 2007)	Table 1 • IGLOO Product Family was updated for AGL030 in the Package Pins section to change CS181 to CS81.	i