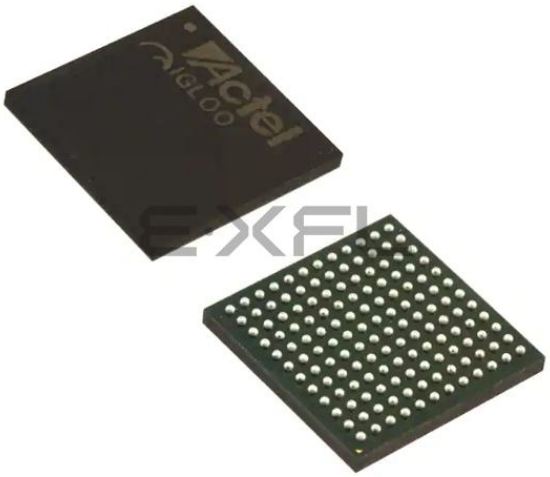

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

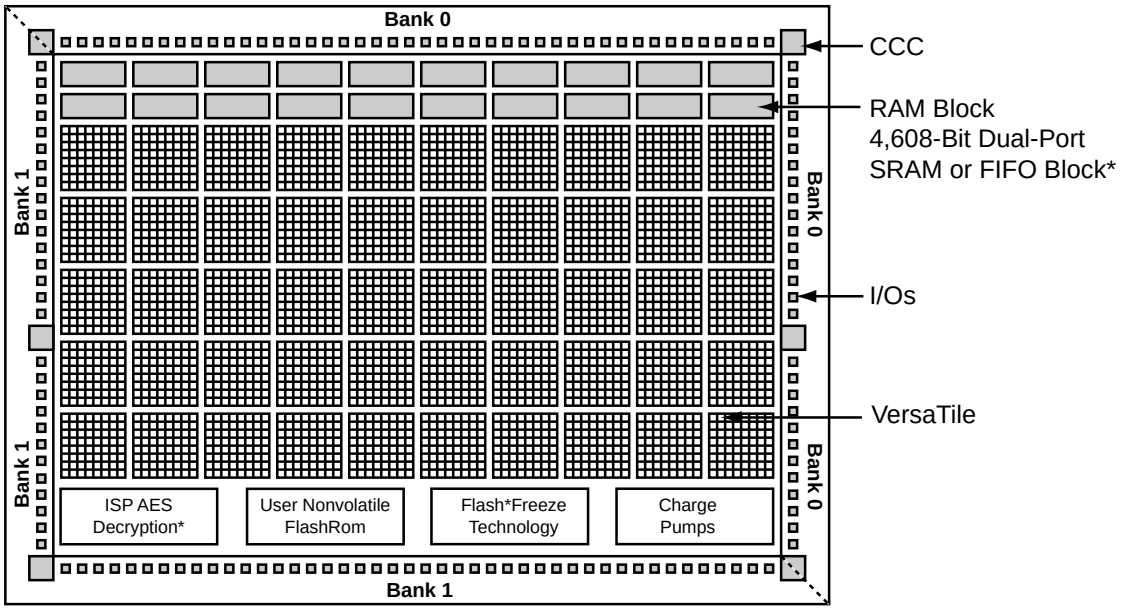
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | 3072 |
| Total RAM Bits | 36864 |
| Number of I/O | 97 |
| Number of Gates | 125000 |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Package / Case | 144-LBGA |
| Supplier Device Package | 144-FPBGA (13x13) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/agl125v5-fg144 |

VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.




*Note: *Not supported by AGL015 and AGL030 devices*

***Figure 1-1 •*** **IGLOO Device Architecture Overview with Two I/O Banks (AGL015, AGL030, AGL060, and AGL125)**

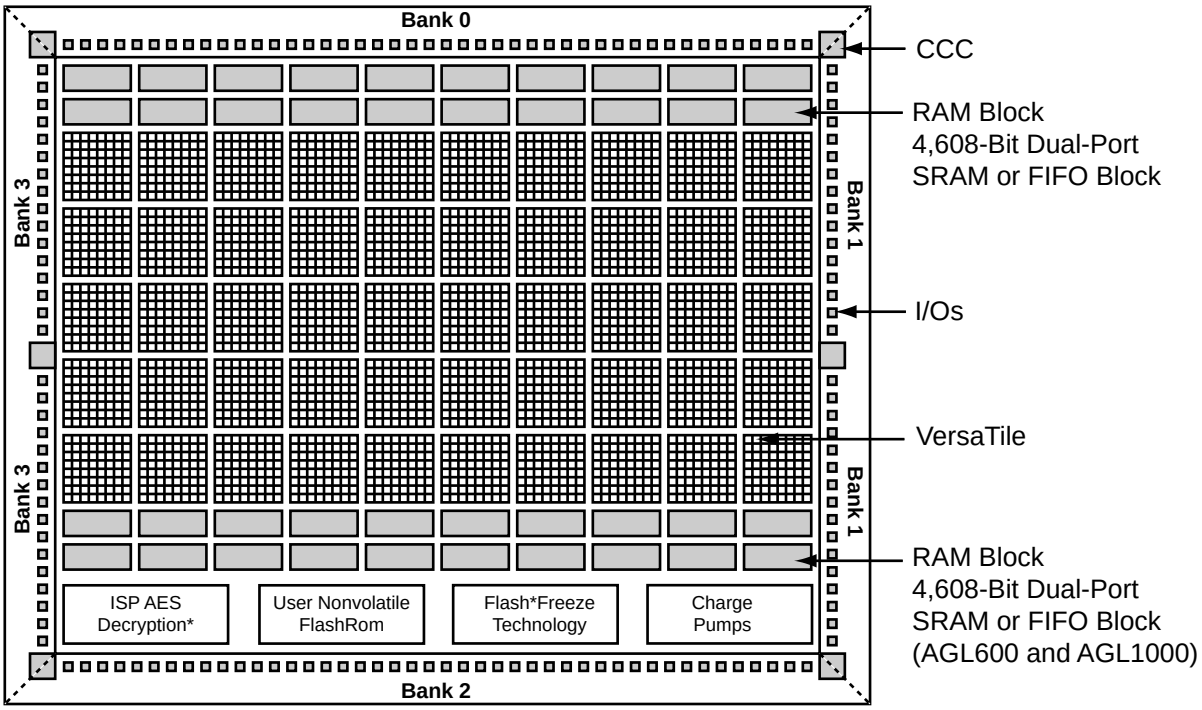



***Figure 1-2 •*** **IGLOO Device Architecture Overview with Four I/O Banks (AGL250, AGL600, AGL400, and AGL1000)**

- Wide input frequency range ($f_{IN\_CCC}$) = 1.5 MHz up to 250 MHz
- Output frequency range ($f_{OUT\_CCC}$) = 0.75 MHz up to 250 MHz
- 2 programmable delay types for clock skew minimization
- Clock frequency synthesis (for PLL only)

Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°. Output phase shift depends on the output divider configuration (for PLL only).
- Output duty cycle = 50% ± 1.5% or better (for PLL only)
- Low output jitter: worst case < 2.5% × clock period peak-to-peak period jitter when single global network used (for PLL only)
- Maximum acquisition time is 300 µs (for PLL only)
- Exceptional tolerance to input period jitter—allowable input jitter is up to 1.5 ns (for PLL only)
- Four precise phases; maximum misalignment between adjacent phases of 40 ps × 250 MHz / $f_{OUT\_CCC}$ (for PLL only)

### *Global Clocking*

IGLOO devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there is a comprehensive global clock distribution network.

Each VersaTile input and output port has access to nine VersaNets: six chip (main) and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via multiplexers (MUXes). The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high-fanout nets.

## *I/Os with Advanced I/O Standards*

The IGLOO family of FPGAs features a flexible I/O structure, supporting a range of voltages (1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.0 V wide range, and 3.3 V). IGLOO FPGAs support many different I/O standards—single-ended and differential.

The I/Os are organized into banks, with two or four banks per device. The configuration of these banks determines the I/O standards supported (Table 1-1).

***Table 1-1 •*** **I/O Standards Supported**

| I/O Bank Type | Device and Bank Location | I/O Standards Supported | | |
|---|---|---|---|---|
| | | LVTTL/ LVCMOS | PCI/PCI-X | LVPECL, LVDS, B-LVDS, M-LVDS |
| Advanced | East and west banks of AGL250 and larger devices | ✓ | ✓ | ✓ |
| Standard Plus | North and south banks of AGL250 and larger devices<br>All banks of AGL060 and AGL125K | ✓ | ✓ | Not supported |
| Standard | All banks of AGL015 and AGL030 | ✓ | Not supported | Not supported |

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of the following:

- Single-Data-Rate applications
- Double-Data-Rate applications—DDR LVDS, B-LVDS, and M-LVDS I/Os for point-to-point communications

IGLOO banks for the AGL250 device and above support LVPECL, LVDS, B-LVDS, and M-LVDS. B-LVDS and M-LVDS can support up to 20 loads.

Hot-swap (also called hot-plug, or hot-insertion) is the operation of hot-insertion or hot-removal of a card in a powered-up system.

Cold-sparing (also called cold-swap) refers to the ability of a device to leave system data undisturbed when the system is powered up, while the component itself is powered down, or when power supplies are floating.

## Wide Range I/O Support

IGLOO devices support JEDEC-defined wide range I/O operation. IGLOO devices support both the JESD8-B specification, covering 3 V and 3.3 V supplies, for an effective operating range of 2.7 V to 3.6 V, and JESD8-12 with its 1.2 V nominal, supporting an effective operating range of 1.14 V to 1.575 V.

Wider I/O range means designers can eliminate power supplies or power conditioning components from the board or move to less costly components with greater tolerances. Wide range eases I/O bank management and provides enhanced protection from system voltage spikes, while providing the flexibility to easily run custom voltage applications.

## Specifying I/O States During Programming

You can modify the I/O states during programming in FlashPro. In FlashPro, this feature is supported for PDB files generated from Designer v8.5 or greater. See the *FlashPro User Guide* for more information.

Note: PDB files generated from Designer v8.1 to Designer v8.4 (including all service packs) have limited display of Pin Numbers only.

1. Load a PDB from the FlashPro GUI. You must have a PDB loaded to modify the I/O states during programming.
2. From the FlashPro GUI, click PDB Configuration. A FlashPoint – Programming File Generator window appears.
3. Click the Specify I/O States During Programming button to display the Specify I/O States During Programming dialog box.
4. Sort the pins as desired by clicking any of the column headers to sort the entries by that header. Select the I/Os you wish to modify (Figure 1-5 on page 1-9).
5. Set the I/O Output State. You can set Basic I/O settings if you want to use the default I/O settings for your pins, or use Custom I/O settings to customize the settings for each pin. Basic I/O state settings:

   1 – I/O is set to drive out logic High

   0 – I/O is set to drive out logic Low

   Last Known State – I/O is set to the last value that was driven out prior to entering the programming mode, and then held at that value during programming

   Z -Tri-State: I/O is tristated

# 2 – IGLOO DC and Switching Characteristics

## General Specifications

### Operating Conditions

Stresses beyond those listed in Table 2-1 may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute Maximum Ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in Table 2-2 on page 2-2 is not implied.

***Table 2-1 •*** **Absolute Maximum Ratings**

| Symbol | Parameter | Limits[1] | Units |
|---|---|---|---|
| VCC | DC core supply voltage | –0.3 to 1.65 | V |
| VJTAG | JTAG DC voltage | –0.3 to 3.75 | V |
| VPUMP | Programming voltage | –0.3 to 3.75 | V |
| VCCPLL | Analog power supply (PLL) | –0.3 to 1.65 | V |
| VCCI and VMV [2] | DC I/O buffer supply voltage | –0.3 to 3.75 | V |
| VI | I/O input voltage | –0.3 V to 3.6 V (when I/O hot insertion mode is enabled)<br>–0.3 V to (VCCI + 1 V) or 3.6 V, whichever voltage is lower (when I/O hot-insertion mode is disabled) | V |
| $T_{STG}$ [3] | Storage Temperature | –65 to +150 | °C |
| $T_J$ [3] | Junction Temperature | +125 | °C |

*Notes:*

1. *The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 2-4 on page 2-3.*
2. *VMV pins must be connected to the corresponding VCCI pins. See the "Pin Descriptions" chapter of the* IGLOO FPGA Fabric User Guide *for further information.*
3. *For flash programming and retention, maximum limits refer to Table 2-3 on page 2-3, and for recommended operating limits, refer to Table 2-2 on page 2-2.*

### Temperature and Voltage Derating Factors

**Table 2-6 • Temperature and Voltage Derating Factors for Timing Delays (normalized to $T_J$ = 70°C, VCC = 1.425 V) For IGLOO V2 or V5 devices, 1.5 V DC Core Supply Voltage**

| Array Voltage VCC (V) | Junction Temperature (°C) | | | | | |
|---|---|---|---|---|---|---|
| | –40°C | 0°C | 25°C | 70°C | 85°C | 100°C |
| 1.425 | 0.934 | 0.953 | 0.971 | 1.000 | 1.007 | 1.013 |
| 1.500 | 0.855 | 0.874 | 0.891 | 0.917 | 0.924 | 0.929 |
| 1.575 | 0.799 | 0.816 | 0.832 | 0.857 | 0.864 | 0.868 |

**Table 2-7 • Temperature and Voltage Derating Factors for Timing Delays (normalized to $T_J$ = 70°C, VCC = 1.14 V) For IGLOO V2, 1.2 V DC Core Supply Voltage**

| Array Voltage VCC (V) | Junction Temperature (°C) | | | | | |
|---|---|---|---|---|---|---|
| | –40°C | 0°C | 25°C | 70°C | 85°C | 100°C |
| 1.14 | 0.967 | 0.978 | 0.991 | 1.000 | 1.006 | 1.010 |
| 1.20 | 0.864 | 0.874 | 0.885 | 0.894 | 0.899 | 0.902 |
| 1.26 | 0.794 | 0.803 | 0.814 | 0.821 | 0.827 | 0.830 |

# Calculating Power Dissipation

## Quiescent Supply Current

Quiescent supply current (IDD) calculation depends on multiple factors, including operating voltages (VCC, VCCI, and VJTAG), operating temperature, system clock frequency, and power modes usage. Microsemi recommends using the PowerCalculator and SmartPower software estimation tools to evaluate the projected static and active power based on the user design, power mode usage, operating voltage, and temperature.

**Table 2-8 • Power Supply State per Mode**

| | Power Supply Configurations | | | | |
|---|---|---|---|---|---|
| Modes/power supplies | VCC | VCCPLL | VCCI | VJTAG | VPUMP |
| Flash*Freeze | On | On | On | On | On/off/floating |
| Sleep | Off | Off | On | Off | Off |
| Shutdown | Off | Off | Off | Off | Off |
| No Flash*Freeze | On | On | On | On | On/off/floating |

*Note: Off: Power supply level = 0 V*

**Table 2-9 • Quiescent Supply Current (IDD) Characteristics, IGLOO Flash*Freeze Mode***

| | Core Voltage | AGL015 | AGL030 | AGL060 | AGL125 | AGL250 | AGL400 | AGL600 | AGL1000 | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| Typical (25°C) | 1.2 V | 4 | 4 | 8 | 13 | 20 | 27 | 30 | 44 | µA |
| | 1.5 V | 6 | 6 | 10 | 18 | 34 | 51 | 72 | 127 | µA |

*Note: *IDD includes VCC, VPUMP, VCCI, VCCPLL, and VMV currents. Values do not include I/O static contribution, which is shown in Table 2-13 on page 2-10 through Table 2-15 on page 2-11 and Table 2-16 on page 2-11 through Table 2-18 on page 2-12 (PDC6 and PDC7).*

## Guidelines

### Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that this net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100% because all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
  - Bit 0 (LSB) = 100%
  - Bit 1 = 50%
  - Bit 2 = 25%
  - …
  - Bit 7 (MSB) = 0.78125%
  - Average toggle rate = (100% + 50% + 25% + 12.5% + . . . + 0.78125%) / 8

### Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When nontristate output buffers are used, the enable rate should be 100%.

***Table 2-23 •*** **Toggle Rate Guidelines Recommended for Power Calculation**

| Component | Definition | Guideline |
|---|---|---|
| $\alpha_1$ | Toggle rate of VersaTile outputs | 10% |
| $\alpha_2$ | I/O buffer toggle rate | 10% |

***Table 2-24 •*** **Enable Rate Guidelines Recommended for Power Calculation**

| Component | Definition | Guideline |
|---|---|---|
| $\beta_1$ | I/O output buffer enable rate | 100% |
| $\beta_2$ | RAM enable rate for read operations | 12.5% |
| $\beta_3$ | RAM enable rate for write operations | 12.5% |

***Table 2-43 •*** **I/O Short Currents IOSH/IOSL**
**Applicable to Standard Plus I/O Banks**

| | Drive Strength | IOSL (mA)* | IOSH (mA)* |
|---|---|---|---|
| 3.3 V LVTTL / 3.3 V LVCMOS | 2 mA | 25 | 27 |
| | 4 mA | 25 | 27 |
| | 6 mA | 51 | 54 |
| | 8 mA | 51 | 54 |
| | 12 mA | 103 | 109 |
| | 16 mA | 103 | 109 |
| 3.3 V LVCMOS Wide Range | 100 µA | Same as regular 3.3 V LVCMOS | Same as regular 3.3 V LVCMOS |
| 2.5 V LVCMOS | 2 mA | 16 | 18 |
| | 4 mA | 16 | 18 |
| | 6 mA | 32 | 37 |
| | 8 mA | 32 | 37 |
| | 12 mA | 65 | 74 |
| 1.8 V LVCMOS | 2 mA | 9 | 11 |
| | 4 mA | 17 | 22 |
| | 6 mA | 35 | 44 |
| | 8 mA | 35 | 44 |
| 1.5 V LVCMOS | 2 mA | 13 | 16 |
| | 4 mA | 25 | 33 |
| 1.2 V LVCMOS | 2 mA | 20 | 26 |
| 1.2 V LVCMOS Wide Range | 100 µA | 20 | 26 |
| 3.3 V PCI/PCI-X | Per PCI/PCI-X specification | 103 | 109 |

*Note: *$T_J$ = 100°C*

***Table 2-64 •*** **Minimum and Maximum DC Input and Output Levels for LVCMOS 3.3 V Wide Range Applicable to Standard Plus I/O Banks**

| 3.3 V LVCMOS Wide Range | | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL[2] | IIH[3] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Equivalent Software Default Drive Strength Option[1] | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | µA | µA | Max. mA[4] | Max. mA[4] | µA[5] | µA[5] |
| 100 µA | 2 mA | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD – 0.2 | 100 | 100 | 25 | 27 | 10 | 10 |
| 100 µA | 4 mA | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD – 0.2 | 100 | 100 | 25 | 27 | 10 | 10 |
| 100 µA | 6 mA | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD – 0.2 | 100 | 100 | 51 | 54 | 10 | 10 |
| 100 µA | 8 mA | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD – 0.2 | 100 | 100 | 51 | 54 | 10 | 10 |
| 100 µA | 12 mA | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD – 0.2 | 100 | 100 | 103 | 109 | 10 | 10 |
| 100 µA | 16 mA | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD – 0.2 | 100 | 100 | 103 | 109 | 10 | 10 |

*Notes:*

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ± 100 µA. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
3. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
4. *Currents are measured at 100°C junction temperature and maximum voltage.*
5. *Currents are measured at 85°C junction temperature.*
6. *Software default selection highlighted in gray.*

***Table 2-65 •*** **Minimum and Maximum DC Input and Output Levels for LVCMOS 3.3 V Wide Range Applicable to Standard I/O Banks**

| 3.3 V LVCMOS Wide Range | | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL[2] | IIH[3] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Equivalent Software Default Drive Strength Option[1] | Min. V | Max. V | Min. V | Max. V | Max. V | Min. V | µA | µA | Max. mA[4] | Max. mA[4] | µA[5] | µA[5] |
| 100 µA | 2 mA | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD – 0.2 | 100 | 100 | 25 | 27 | 10 | 10 |
| 100 µA | 4 mA | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD – 0.2 | 100 | 100 | 25 | 27 | 10 | 10 |
| 100 µA | 6 mA | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD – 0.2 | 100 | 100 | 51 | 54 | 10 | 10 |
| 100 µA | 8 mA | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD – 0.2 | 100 | 100 | 51 | 54 | 10 | 10 |

*Notes:*

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ± 100 µA. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
3. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
4. *Currents are measured at 100°C junction temperature and maximum voltage.*
5. *Currents are measured at 85°C junction temperature.*
6. *Software default selection highlighted in gray.*

***Table 2-66 •*** **3.3 V LVCMOS Wide Range AC Waveforms, Measuring Points, and Capacitive Loads**

| Input Low (V) | Input High (V) | Measuring Point* (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|
| 0 | 3.3 | 1.4 | 5 |

*Note: *Measuring point = Vtrip. See Table 2-29 on page 2-28 for a complete table of trip points.*

***Table 2-69 •*** **3.3 V LVCMOS Wide Range Low Slew – Applies to 1.5 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.7 V**
**Applicable to Standard Plus Banks**

| Drive Strength | Equivalent Software Default Drive Strength Option[1] | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 100 µA | 2 mA | Std. | 0.97 | 5.84 | 0.18 | 1.20 | 0.66 | 5.86 | 5.04 | 2.74 | 2.71 | 9.46 | 8.64 | ns |
| 100 µA | 4 mA | Std. | 0.97 | 5.84 | 0.18 | 1.20 | 0.66 | 5.86 | 5.04 | 2.74 | 2.71 | 9.46 | 8.64 | ns |
| 100 µA | 6 mA | Std. | 0.97 | 4.76 | 0.18 | 1.20 | 0.66 | 4.78 | 4.33 | 3.09 | 3.33 | 8.37 | 7.93 | ns |
| 100 µA | 8 mA | Std. | 0.97 | 4.76 | 0.18 | 1.20 | 0.66 | 4.78 | 4.33 | 3.09 | 3.33 | 8.37 | 7.93 | ns |
| 100 µA | 12 mA | Std. | 0.97 | 4.02 | 0.18 | 1.20 | 0.66 | 4.04 | 3.78 | 3.33 | 3.73 | 7.64 | 7.37 | ns |
| 100 µA | 16 mA | Std. | 0.97 | 4.02 | 0.18 | 1.20 | 0.66 | 4.04 | 3.78 | 3.33 | 3.73 | 7.64 | 7.37 | ns |

*Notes:*

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ± 100 µA. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

***Table 2-70 •*** **3.3 V LVCMOS Wide Range High Slew – Applies to 1.5 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.7 V**
**Applicable to Standard Plus Banks**

| Drive Strength | Equivalent Software Default Drive Strength Option[1] | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 100 µA | 2 mA | Std. | 0.97 | 3.33 | 0.18 | 1.20 | 0.66 | 3.35 | 2.68 | 2.73 | 2.88 | 6.94 | 6.27 | ns |
| 100 µA | 4 mA | Std. | 0.97 | 3.33 | 0.18 | 1.20 | 0.66 | 3.35 | 2.68 | 2.73 | 2.88 | 6.94 | 6.27 | ns |
| 100 µA | 6 mA | Std. | 0.97 | 2.75 | 0.18 | 1.20 | 0.66 | 2.77 | 2.17 | 3.08 | 3.50 | 6.36 | 5.77 | ns |
| 100 µA | 8 mA | Std. | 0.97 | 2.75 | 0.18 | 1.20 | 0.66 | 2.77 | 2.17 | 3.08 | 3.50 | 6.36 | 5.77 | ns |
| 100 µA | 12 mA | Std. | 0.97 | 2.45 | 0.18 | 1.20 | 0.66 | 2.47 | 1.92 | 3.33 | 3.90 | 6.06 | 5.51 | ns |
| 100 µA | 16 mA | Std. | 0.97 | 2.45 | 0.18 | 1.20 | 0.66 | 2.47 | 1.92 | 3.33 | 3.90 | 6.06 | 5.51 | ns |

*Notes:*

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ± 100 µA. Drive strengths displayed in software are supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*
3. *Software default selection highlighted in gray.*

**Table 2-119 • 1.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V**
**Applicable to Standard Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 0.97 | 5.88 | 0.18 | 1.14 | 0.66 | 6.00 | 5.45 | 2.00 | 1.94 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

**Table 2-120 • 1.5 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V**
**Applicable to Standard Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 0.97 | 2.51 | 0.18 | 1.14 | 0.66 | 2.56 | 2.21 | 1.99 | 2.03 | ns |

*Notes:*

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

### 1.2 V DC Core Voltage

**Table 2-121 • 1.5 V LVCMOS Low Slew – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V**
**Applicable to Advanced I/O Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 1.55 | 7.17 | 0.26 | 1.27 | 1.10 | 7.29 | 6.60 | 3.33 | 3.03 | 13.07 | 12.39 | ns |
| 4 mA | Std. | 1.55 | 6.27 | 0.26 | 1.27 | 1.10 | 6.37 | 5.86 | 3.61 | 3.51 | 12.16 | 11.64 | ns |
| 6 mA | Std. | 1.55 | 5.94 | 0.26 | 1.27 | 1.10 | 6.04 | 5.70 | 3.67 | 3.64 | 11.82 | 11.48 | ns |
| 8 mA | Std. | 1.55 | 5.86 | 0.26 | 1.27 | 1.10 | 5.96 | 5.71 | 2.83 | 4.11 | 11.74 | 11.50 | ns |
| 12 mA | Std. | 1.55 | 5.86 | 0.26 | 1.27 | 1.10 | 5.96 | 5.71 | 2.83 | 4.11 | 11.74 | 11.50 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

**Table 2-122 • 1.5 V LVCMOS High Slew – Applies to 1.2 V DC Core Voltage**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V**
**Applicable to Advanced I/O Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 1.55 | 3.44 | 0.26 | 1.27 | 1.10 | 3.49 | 3.35 | 3.32 | 3.12 | 9.28 | 9.14 | ns |
| 4 mA | Std. | 1.55 | 3.06 | 0.26 | 1.27 | 1.10 | 3.10 | 2.89 | 3.60 | 3.61 | 8.89 | 8.67 | ns |
| 6 mA | Std. | 1.55 | 2.98 | 0.26 | 1.27 | 1.10 | 3.02 | 2.80 | 3.66 | 3.74 | 8.81 | 8.58 | ns |
| 8 mA | Std. | 1.55 | 2.96 | 0.26 | 1.27 | 1.10 | 3.00 | 2.70 | 3.75 | 4.23 | 8.78 | 8.48 | ns |
| 12 mA | Std. | 1.55 | 2.96 | 0.26 | 1.27 | 1.10 | 3.00 | 2.70 | 3.75 | 4.23 | 8.78 | 8.48 | ns |

*Notes:*

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

### 1.2 V DC Core Voltage

**Table 2-162 • Output Enable Register Propagation Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{OECLKQ}$ | Clock-to-Q of the Output Enable Register | 1.10 | ns |
| $t_{OESUD}$ | Data Setup Time for the Output Enable Register | 1.15 | ns |
| $t_{OEHD}$ | Data Hold Time for the Output Enable Register | 0.00 | ns |
| $t_{OESUE}$ | Enable Setup Time for the Output Enable Register | 1.22 | ns |
| $t_{OEHE}$ | Enable Hold Time for the Output Enable Register | 0.00 | ns |
| $t_{OECLR2Q}$ | Asynchronous Clear-to-Q of the Output Enable Register | 1.65 | ns |
| $t_{OEPRE2Q}$ | Asynchronous Preset-to-Q of the Output Enable Register | 1.65 | ns |
| $t_{OEREMCLR}$ | Asynchronous Clear Removal Time for the Output Enable Register | 0.00 | ns |
| $t_{ORECCLR}$ | Asynchronous Clear Recovery Time for the Output Enable Register | 0.24 | ns |
| $t_{OEREMPRE}$ | Asynchronous Preset Removal Time for the Output Enable Register | 0.00 | ns |
| $t_{ORECPRE}$ | Asynchronous Preset Recovery Time for the Output Enable Register | 0.24 | ns |
| $t_{OEWCLR}$ | Asynchronous Clear Minimum Pulse Width for the Output Enable Register | 0.19 | ns |
| $t_{OEWPRE}$ | Asynchronous Preset Minimum Pulse Width for the Output Enable Register | 0.19 | ns |
| $t_{OECKMPWH}$ | Clock Minimum Pulse Width High for the Output Enable Register | 0.31 | ns |
| $t_{OECKMPWL}$ | Clock Minimum Pulse Width Low for the Output Enable Register | 0.28 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

## Timing Characteristics

### 1.5 V DC Core Voltage

**Table 2-169 • Combinatorial Cell Propagation Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V**

| Combinatorial Cell | Equation | Parameter | Std. | Units |
|---|---|---|---|---|
| INV | Y =!A | $t_{PD}$ | 0.80 | ns |
| AND2 | Y = A · B | $t_{PD}$ | 0.84 | ns |
| NAND2 | Y =!(A · B) | $t_{PD}$ | 0.90 | ns |
| OR2 | Y = A + B | $t_{PD}$ | 1.19 | ns |
| NOR2 | Y = !(A + B) | $t_{PD}$ | 1.10 | ns |
| XOR2 | Y = A ⊕ B | $t_{PD}$ | 1.37 | ns |
| MAJ3 | Y = MAJ(A, B, C) | $t_{PD}$ | 1.33 | ns |
| XOR3 | Y = A ⊕ B ⊕ C | $t_{PD}$ | 1.79 | ns |
| MUX2 | Y = A !S + B S | $t_{PD}$ | 1.48 | ns |
| AND3 | Y = A · B · C | $t_{PD}$ | 1.21 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

### 1.2 V DC Core Voltage

**Table 2-170 • Combinatorial Cell Propagation Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.14 V**

| Combinatorial Cell | Equation | Parameter | Std. | Units |
|---|---|---|---|---|
| INV | Y = !A | $t_{PD}$ | 1.34 | ns |
| AND2 | Y = A · B | $t_{PD}$ | 1.43 | ns |
| NAND2 | Y = !(A · B) | $t_{PD}$ | 1.59 | ns |
| OR2 | Y = A + B | $t_{PD}$ | 2.30 | ns |
| NOR2 | Y = !(A + B) | $t_{PD}$ | 2.07 | ns |
| XOR2 | Y = A ⊕ B | $t_{PD}$ | 2.46 | ns |
| MAJ3 | Y = MAJ(A, B, C) | $t_{PD}$ | 2.46 | ns |
| XOR3 | Y = A ⊕ B ⊕ C | $t_{PD}$ | 3.12 | ns |
| MUX2 | Y = A !S + B S | $t_{PD}$ | 2.83 | ns |
| AND3 | Y = A · B · C | $t_{PD}$ | 2.28 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.*

***Table 2-192 •*** **RAM512X18**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V**

| Parameter | Description | Std. | Units |
|---|---|---|---|
| $t_{AS}$ | Address setup time | 0.83 | ns |
| $t_{AH}$ | Address hold time | 0.16 | ns |
| $t_{ENS}$ | REN, WEN setup time | 0.73 | ns |
| $t_{ENH}$ | REN, WEN hold time | 0.08 | ns |
| $t_{DS}$ | Input data (WD) setup time | 0.71 | ns |
| $t_{DH}$ | Input data (WD) hold time | 0.36 | ns |
| $t_{CKQ1}$ | Clock High to new data valid on RD (output retained) | 4.21 | ns |
| $t_{CKQ2}$ | Clock High to new data valid on RD (pipelined) | 1.71 | ns |
| $t_{C2CRWH}$[1] | Address collision clk-to-clk delay for reliable read access after write on same address - Applicable to Opening Edge | 0.35 | ns |
| $t_{C2CWRH}$[1] | Address collision clk-to-clk delay for reliable write access after read on same address - Applicable to Opening Edge | 0.42 | ns |
| $t_{RSTBQ}$ | RESET Low to data out Low on RD (flow-through) | 2.06 | ns |
| | RESET Low to data out Low on RD (pipelined) | 2.06 | ns |
| $t_{REMRSTB}$ | RESET removal | 0.61 | ns |
| $t_{RECRSTB}$ | RESET recovery | 3.21 | ns |
| $t_{MPWRSTB}$ | RESET minimum pulse width | 0.68 | ns |
| $t_{CYC}$ | Clock cycle time | 6.24 | ns |
| $F_{MAX}$ | Maximum frequency | 160 | MHz |

*Notes:*

1. *For more information, refer to the application note* Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.*

# 3 – Pin Descriptions

## Supply Pins

**GND** **Ground**

Ground supply voltage to the core, I/O outputs, and I/O logic.

**GNDQ** **Ground (quiet)**

Quiet ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package and improves input signal integrity. GNDQ must always be connected to GND on the board.

**VCC** **Core Supply Voltage**

Supply voltage to the FPGA core, nominally 1.5 V for IGLOO V5 devices, and 1.2 V or 1.5 V for IGLOO V2 devices. VCC is required for powering the JTAG state machine in addition to VJTAG. Even when a device is in bypass mode in a JTAG chain of interconnected devices, both VCC and VJTAG must remain powered to allow JTAG signals to pass through the device.

For IGLOO V2 devices, VCC can be switched dynamically from 1.2 V to 1.5 V or vice versa. This allows in-system programming (ISP) when VCC is at 1.5 V and the benefit of low power operation when VCC is at 1.2 V.

**VCCIBx** **I/O Supply Voltage**

Supply voltage to the bank's I/O output buffers and I/O logic. Bx is the I/O bank number. There are up to eight I/O banks on IGLOO devices plus a dedicated VJTAG bank. Each bank can have a separate VCCI connection. All I/Os in a bank will run off the same VCCIBx supply. VCCI can be 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VCCI pins tied to GND.

**VMVx** **I/O Supply Voltage (quiet)**

Quiet supply voltage to the input buffers of each I/O bank. *x* is the bank number. Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks. This minimizes the noise transfer within the package and improves input signal integrity. Each bank must have at least one VMV connection, and no VMV should be left unconnected. All I/Os in a bank run off the same VMVx supply. VMV is used to provide a quiet supply voltage to the input buffers of each I/O bank. VMVx can be 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VMV pins tied to GND. VMV and VCCI should be at the same voltage within a given I/O bank. Used VMV pins must be connected to the corresponding VCCI pins of the same bank (i.e., VMV0 to VCCIB0, VMV1 to VCCIB1, etc.).

**VCCPLA/B/C/D/E/F** **PLL Supply Voltage**

Supply voltage to analog PLL, nominally 1.5 V or 1.2 V.

- 1.5 V for IGLOO V5 devices
- 1.2 V or 1.5 V for IGLOO V2 devices

When the PLLs are not used, the Microsemi Designer place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground. Microsemi recommends tying VCCPLx to VCC and using proper filtering circuits to decouple VCC noise from the PLLs. Refer to the PLL Power Supply Decoupling section of the "Clock Conditioning Circuits in Low Power Flash Devices and Mixed Signal FPGAs" chapter of the *IGLOO FPGA Fabric User Guide* for a complete board solution for the PLL analog power supply and ground.

- There is one VCCPLF pin on IGLOO devices.

**VCOMPLA/B/C/D/E/F** **PLL Ground**

Ground to analog PLL power supplies. When the PLLs are not used, the Microsemi Designer place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground.

There is one VCOMPLF pin on IGLOO devices.

| QN132 | |
|---|---|
| **Pin Number** | **AGL060 Function** |
| A1 | GAB2/IO00RSB1 |
| A2 | IO93RSB1 |
| A3 | VCCIB1 |
| A4 | GFC1/IO89RSB1 |
| A5 | GFB0/IO86RSB1 |
| A6 | VCCPLF |
| A7 | GFA1/IO84RSB1 |
| A8 | GFC2/IO81RSB1 |
| A9 | IO78RSB1 |
| A10 | VCC |
| A11 | GEB1/IO75RSB1 |
| A12 | GEA0/IO72RSB1 |
| A13 | GEC2/IO69RSB1 |
| A14 | IO65RSB1 |
| A15 | VCC |
| A16 | IO64RSB1 |
| A17 | IO63RSB1 |
| A18 | IO62RSB1 |
| A19 | IO61RSB1 |
| A20 | IO58RSB1 |
| A21 | GDB2/IO55RSB1 |
| A22 | NC |
| A23 | GDA2/IO54RSB1 |
| A24 | TDI |
| A25 | TRST |
| A26 | GDC1/IO48RSB0 |
| A27 | VCC |
| A28 | IO47RSB0 |
| A29 | GCC2/IO46RSB0 |
| A30 | GCA2/IO44RSB0 |
| A31 | GCA0/IO43RSB0 |
| A32 | GCB1/IO40RSB0 |
| A33 | IO36RSB0 |
| A34 | VCC |
| A35 | IO31RSB0 |
| A36 | GBA2/IO28RSB0 |

| QN132 | |
|---|---|
| **Pin Number** | **AGL060 Function** |
| A37 | GBB1/IO25RSB0 |
| A38 | GBC0/IO22RSB0 |
| A39 | VCCIB0 |
| A40 | IO21RSB0 |
| A41 | IO18RSB0 |
| A42 | IO15RSB0 |
| A43 | IO14RSB0 |
| A44 | IO11RSB0 |
| A45 | GAB1/IO08RSB0 |
| A46 | NC |
| A47 | GAB0/IO07RSB0 |
| A48 | IO04RSB0 |
| B1 | IO01RSB1 |
| B2 | GAC2/IO94RSB1 |
| B3 | GND |
| B4 | GFC0/IO88RSB1 |
| B5 | VCOMPLF |
| B6 | GND |
| B7 | GFB2/IO82RSB1 |
| B8 | IO79RSB1 |
| B9 | GND |
| B10 | GEB0/IO74RSB1 |
| B11 | VMV1 |
| B12 | FF/GEB2/IO70RSB1 |
| B13 | IO67RSB1 |
| B14 | GND |
| B15 | NC |
| B16 | NC |
| B17 | GND |
| B18 | IO59RSB1 |
| B19 | GDC2/IO56RSB1 |
| B20 | GND |
| B21 | GNDQ |
| B22 | TMS |
| B23 | TDO |

| QN132 | |
|---|---|
| **Pin Number** | **AGL060 Function** |
| B24 | GDC0/IO49RSB0 |
| B25 | GND |
| B26 | NC |
| B27 | GCB2/IO45RSB0 |
| B28 | GND |
| B29 | GCB0/IO41RSB0 |
| B30 | GCC1/IO38RSB0 |
| B31 | GND |
| B32 | GBB2/IO30RSB0 |
| B33 | VMV0 |
| B34 | GBA0/IO26RSB0 |
| B35 | GBC1/IO23RSB0 |
| B36 | GND |
| B37 | IO20RSB0 |
| B38 | IO17RSB0 |
| B39 | GND |
| B40 | IO12RSB0 |
| B41 | GAC0/IO09RSB0 |
| B42 | GND |
| B43 | GAA1/IO06RSB0 |
| B44 | GNDQ |
| C1 | GAA2/IO02RSB1 |
| C2 | IO95RSB1 |
| C3 | VCC |
| C4 | GFB1/IO87RSB1 |
| C5 | GFA0/IO85RSB1 |
| C6 | GFA2/IO83RSB1 |
| C7 | IO80RSB1 |
| C8 | VCCIB1 |
| C9 | GEA1/IO73RSB1 |
| C10 | GNDQ |
| C11 | GEA2/IO71RSB1 |
| C12 | IO68RSB1 |
| C13 | VCCIB1 |
| C14 | NC |
| C15 | NC |

| QN132 | |
|---|---|
| **Pin Number** | **AGL060 Function** |
| C16 | IO60RSB1 |
| C17 | IO57RSB1 |
| C18 | NC |
| C19 | TCK |
| C20 | VMV1 |
| C21 | VPUMP |
| C22 | VJTAG |
| C23 | VCCIB0 |
| C24 | NC |
| C25 | NC |
| C26 | GCA1/IO42RSB0 |
| C27 | GCC0/IO39RSB0 |
| C28 | VCCIB0 |
| C29 | IO29RSB0 |
| C30 | GNDQ |
| C31 | GBA1/IO27RSB0 |
| C32 | GBB0/IO24RSB0 |
| C33 | VCC |
| C34 | IO19RSB0 |
| C35 | IO16RSB0 |
| C36 | IO13RSB0 |
| C37 | GAC1/IO10RSB0 |
| C38 | NC |
| C39 | GAA0/IO05RSB0 |
| C40 | VMV0 |
| D1 | GND |
| D2 | GND |
| D3 | GND |
| D4 | GND |

| FG256 | |
|---|---|
| **Pin Number** | **AGL400 Function** |
| R5 | IO123RSB2 |
| R6 | IO118RSB2 |
| R7 | IO112RSB2 |
| R8 | IO106RSB2 |
| R9 | IO100RSB2 |
| R10 | IO96RSB2 |
| R11 | IO89RSB2 |
| R12 | IO85RSB2 |
| R13 | GDB2/IO81RSB2 |
| R14 | TDI |
| R15 | NC |
| R16 | TDO |
| T1 | GND |
| T2 | IO126RSB2 |
| T3 | FF/GEB2/IO133RSB2 |
| T4 | IO124RSB2 |
| T5 | IO116RSB2 |
| T6 | IO113RSB2 |
| T7 | IO107RSB2 |
| T8 | IO105RSB2 |
| T9 | IO102RSB2 |
| T10 | IO97RSB2 |
| T11 | IO92RSB2 |
| T12 | GDC2/IO82RSB2 |
| T13 | IO86RSB2 |
| T14 | GDA2/IO80RSB2 |
| T15 | TMS |
| T16 | GND |

| FG484 | |
|---|---|
| **Pin Number** | **AGL400 Function** |
| C21 | NC |
| C22 | VCCIB1 |
| D1 | NC |
| D2 | NC |
| D3 | NC |
| D4 | GND |
| D5 | GAA0/IO00RSB0 |
| D6 | GAA1/IO01RSB0 |
| D7 | GAB0/IO02RSB0 |
| D8 | IO16RSB0 |
| D9 | IO17RSB0 |
| D10 | IO22RSB0 |
| D11 | IO28RSB0 |
| D12 | IO34RSB0 |
| D13 | IO37RSB0 |
| D14 | IO41RSB0 |
| D15 | IO43RSB0 |
| D16 | GBB1/IO57RSB0 |
| D17 | GBA0/IO58RSB0 |
| D18 | GBA1/IO59RSB0 |
| D19 | GND |
| D20 | NC |
| D21 | NC |
| D22 | NC |
| E1 | NC |
| E2 | NC |
| E3 | GND |
| E4 | GAB2/IO154UDB3 |
| E5 | GAA2/IO155UDB3 |
| E6 | IO12RSB0 |
| E7 | GAB1/IO03RSB0 |
| E8 | IO13RSB0 |
| E9 | IO14RSB0 |
| E10 | IO21RSB0 |
| E11 | IO27RSB0 |
| E12 | IO32RSB0 |

# 5 – Datasheet Information

## List of Changes

The following tables list critical changes that were made in each revision of the IGLOO datasheet.

| Revision | Changes | Page |
|---|---|---|
| Revision 27 (May 2016) | Added the deleted package FG144 from AGL125 device in "IGLOO Devices" (SAR 79355). | 1-I |
| Revision 26 (March 2016) | Updated "IGLOO Ordering Information" and "Temperature Grade Offerings" notes by:<br>• Replacing Commercial (0°C to +70°C Ambient Temperature) with Commercial (0°C to +85°C Junction Temperature) (SAR 48352).<br>• Replacing Industrial (–40°C to +85°C Ambient Temperature) with Industrial (–40°C to +100°C Junction Temperature) (SAR 48352). | 1-III and 1-IV |
| | Ambient temperature row removed in Table 2-2 (SAR 48352). | 2-2 |
| | Updated Table 2-2 note 2 from "To ensure targeted reliability standards are met across ambient and junction operating temperatures, Microsemi recommends that the user follow best design practices using Microsemi's timing and power simulation tools." to "Software Default Junction Temperature Range in the Libero SoC software is set to 0°C to +70°C for commercial, and -40°C to +85°C for industrial. To ensure targeted reliability standards are met across the full range of junction temperatures, Microsemi recommends using custom settings for temperature range before running timing and power analysis tools. For more information on custom settings, refer to the New Project Dialog Box in the Libero SoC Online Help." (SAR 77087). | 2-2 |
| | Updated Table 2-2 note 9 from "VMV pins must be connected to the corresponding VCCI pins. See the "Pin Descriptions" chapter of the IGLOO FPGA Fabric User Guide for further information." to "VMV and VCCI must be at the same voltage within a given I/O bank. VMV pins must be connected to the corresponding VCCI pins. See the "VMVx I/O Supply Voltage (quiet)" on page 3-1 for further information." (SAR 77087) | 2-2 |
| | Added 2 mA drive strengths in tables same as 4 mA (SAR 57179). | NA |
| | Added reference of Package Mechanical Drawings document in all package pin assignment notes (76777). | NA |
| Revision 25 (June2015) | Removed package FG144 from AGL060 device in the following tables: "IGLOO Devices", "I/Os Per Package1" and "Temperature Grade Offerings" (SAR 68517) | I, II, and IV |
| | Removed Package Pin Assignment table of AGL060 device from FG144.(SAR 68517) | - |
| Revision 24 (March 2014) | Note added for the discontinuance of QN132 package to the following tables: "IGLOO Devices", "I/Os Per Package1", "IGLOO FPGAs Package Sizes Dimensions", and"Temperature Grade Offerings" and "QN132" section (SAR 55117, PDN 1306). | I, II, IV, and 4-28 |
| | Removed packages CS81 and QN132 from AGL250 device in the following tables: "IGLOO Devices", "I/Os Per Package1", and "Temperature Grade Offerings" (SAR 49472). | I, II, and IV |