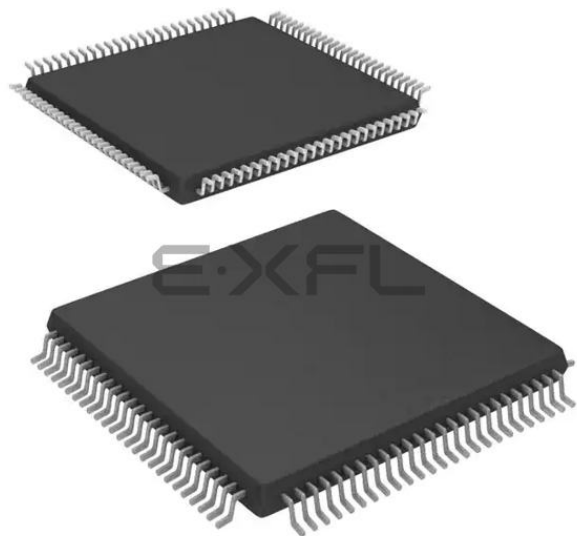




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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	3072
Total RAM Bits	36864
Number of I/O	71
Number of Gates	250000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 85°C (TA)
Package / Case	100-TQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/agl125v5-vqg100i

Combinatorial Cells Contribution— P_{C-CELL}

$$P_{C-CELL} = N_{C-CELL} * \alpha_1 / 2 * P_{AC7} * F_{CLK}$$

N_{C-CELL} is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-23 on page 2-19.

F_{CLK} is the global clock signal frequency.

Routing Net Contribution— P_{NET}

$$P_{NET} = (N_{S-CELL} + N_{C-CELL}) * \alpha_1 / 2 * P_{AC8} * F_{CLK}$$

N_{S-CELL} is the number of VersaTiles used as sequential modules in the design.

N_{C-CELL} is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-23 on page 2-19.

F_{CLK} is the global clock signal frequency.

I/O Input Buffer Contribution— P_{INPUTS}

$$P_{INPUTS} = N_{INPUTS} * \alpha_2 / 2 * P_{AC9} * F_{CLK}$$

N_{INPUTS} is the number of I/O input buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-23 on page 2-19.

F_{CLK} is the global clock signal frequency.

I/O Output Buffer Contribution— $P_{OUTPUTS}$

$$P_{OUTPUTS} = N_{OUTPUTS} * \alpha_2 / 2 * \beta_1 * P_{AC10} * F_{CLK}$$

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-23 on page 2-19.

β_1 is the I/O buffer enable rate—guidelines are provided in Table 2-24 on page 2-19.

F_{CLK} is the global clock signal frequency.

RAM Contribution— P_{MEMORY}

$$P_{MEMORY} = P_{AC11} * N_{BLOCKS} * F_{READ-CLOCK} * \beta_2 + P_{AC12} * N_{BLOCK} * F_{WRITE-CLOCK} * \beta_3$$

N_{BLOCKS} is the number of RAM blocks used in the design.

$F_{READ-CLOCK}$ is the memory read clock frequency.

β_2 is the RAM enable rate for read operations.

$F_{WRITE-CLOCK}$ is the memory write clock frequency.

β_3 is the RAM enable rate for write operations—guidelines are provided in Table 2-24 on page 2-19.

PLL Contribution— P_{PLL}

$$P_{PLL} = P_{DC4} + P_{AC13} * F_{CLKOUT}$$

F_{CLKOUT} is the output clock frequency.[†]

[†] If a PLL is used to generate more than one output clock, include each output clock in the formula by adding its corresponding contribution ($P_{AC13} * F_{CLKOUT}$ product) to the total PLL contribution.

Guidelines

Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that this net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100% because all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
 - Bit 0 (LSB) = 100%
 - Bit 1 = 50%
 - Bit 2 = 25%
 - ...
 - Bit 7 (MSB) = 0.78125%
 - Average toggle rate = $(100\% + 50\% + 25\% + 12.5\% + \dots + 0.78125\%) / 8$

Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When nontristate output buffers are used, the enable rate should be 100%.

Table 2-23 • Toggle Rate Guidelines Recommended for Power Calculation

Component	Definition	Guideline
α_1	Toggle rate of VersaTile outputs	10%
α_2	I/O buffer toggle rate	10%

Table 2-24 • Enable Rate Guidelines Recommended for Power Calculation

Component	Definition	Guideline
β_1	I/O output buffer enable rate	100%
β_2	RAM enable rate for read operations	12.5%
β_3	RAM enable rate for write operations	12.5%

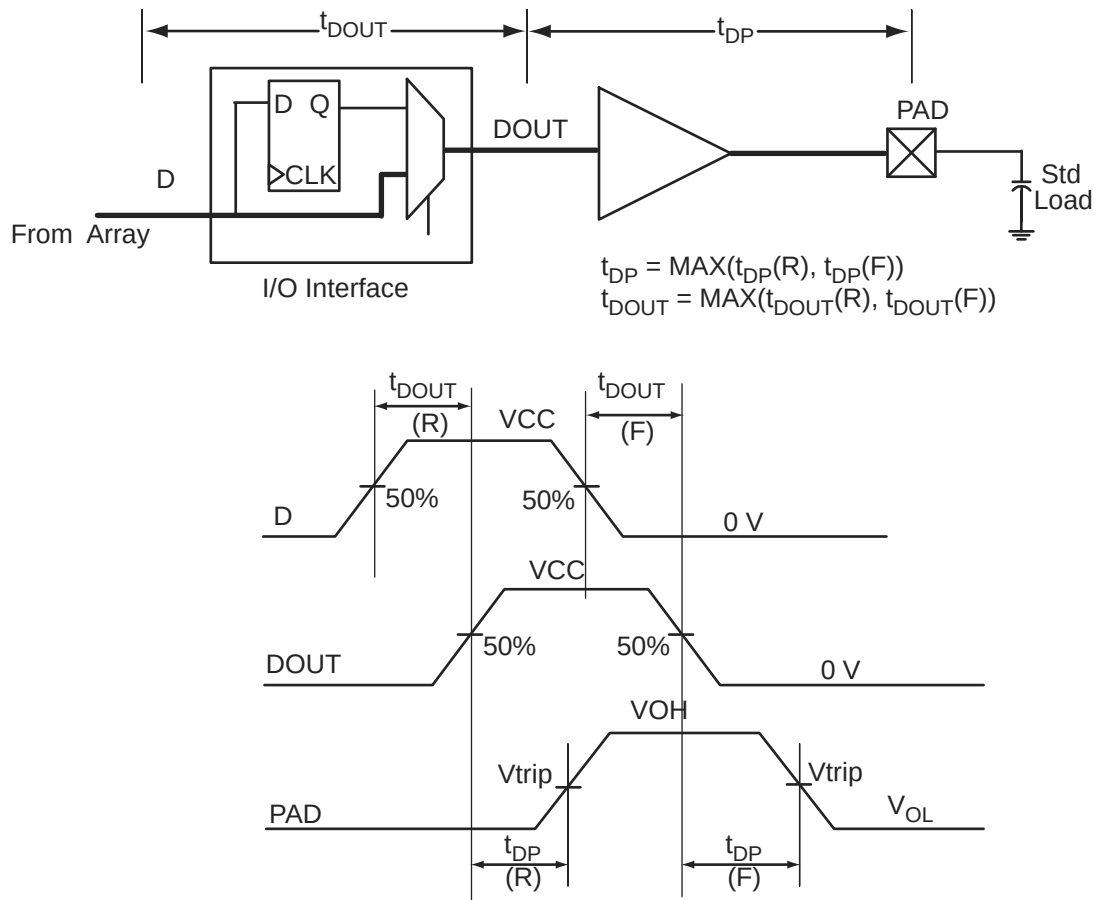


Figure 2-5 • Output Buffer Model and Delays (example)

Table 2-32 • Summary of I/O Timing Characteristics—Software Default Settings, Std. Speed Grade, Commercial-Case
Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case V_{CCI} (per standard)
Applicable to Standard Plus I/O Banks

I/O Standard	Drive Strength	Equivalent Software Default Drive Strength Option ¹ (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{bOUT} (ns)	t_{bP} (ns)	t_{bIN} (ns)	t_{pY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTTL / 3.3 V LVCMOS	12 mA	12	High	5	—	0.97	1.75	0.18	0.85	0.66	1.79	1.40	2.36	2.79	5.38	4.99	ns
3.3 V LVCMOS Wide Range ²	100 μA	12	High	5	—	0.97	2.45	0.18	1.20	0.66	2.47	1.92	3.33	3.90	6.06	5.51	ns
2.5 V LVCMOS	12 mA	12	High	5	—	0.97	1.75	0.18	1.08	0.66	1.79	1.52	2.38	2.70	5.39	5.11	ns
1.8 V LVCMOS	8 mA	8	High	5	—	0.97	1.97	0.18	1.01	0.66	2.02	1.76	2.46	2.66	5.61	5.36	ns
1.5 V LVCMOS	4 mA	4	High	5	—	0.97	2.25	0.18	1.18	0.66	2.30	2.00	2.53	2.68	5.89	5.59	ns
3.3 V PCI	Per PCI spec	—	High	10	25 ²	0.97	1.97	0.18	0.73	0.66	2.01	1.50	2.36	2.79	5.61	5.10	ns
3.3 V PCI-X	Per PCI-X spec	—	High	10	25 ²	0.97	1.97	0.19	0.70	0.66	2.01	1.50	2.36	2.79	5.61	5.10	ns

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is $\pm 100\text{ }\mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.
3. Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-12 on page 2-79 for connectivity. This resistor is not required during normal operation.
4. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Timing Characteristics

Applies to 1.5 V DC Core Voltage

Table 2-83 • 2.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V

Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	4.96	0.18	1.08	0.66	5.06	4.59	2.26	2.00	8.66	8.19	ns
4 mA	Std.	0.97	4.96	0.18	1.08	0.66	5.06	4.59	2.26	2.00	8.66	8.19	ns
6 mA	Std.	0.97	4.15	0.18	1.08	0.66	4.24	3.94	2.54	2.51	7.83	7.53	ns
8 mA	Std.	0.97	4.15	0.18	1.08	0.66	4.24	3.94	2.54	2.51	7.83	7.53	ns
12 mA	Std.	0.97	3.57	0.18	1.08	0.66	3.65	3.47	2.73	2.84	7.24	7.06	ns
16 mA	Std.	0.97	3.39	0.18	1.08	0.66	3.46	3.36	2.78	2.92	7.06	6.95	ns
24 mA	Std.	0.97	3.38	0.18	1.08	0.66	3.38	3.38	2.83	3.25	6.98	6.98	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-84 • 2.5 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V

Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	2.77	0.18	1.08	0.66	2.83	2.60	2.26	2.08	6.42	6.19	ns
4 mA	Std.	0.97	2.77	0.18	1.08	0.66	2.83	2.60	2.26	2.08	6.42	6.19	ns
6 mA	Std.	0.97	2.34	0.18	1.08	0.66	2.39	2.08	2.54	2.60	5.99	5.68	ns
8 mA	Std.	0.97	2.34	0.18	1.08	0.66	2.39	2.08	2.54	2.60	5.99	5.68	ns
12 mA	Std.	0.97	2.09	0.18	1.08	0.66	2.14	1.83	2.73	2.93	5.73	5.43	ns
16 mA	Std.	0.97	2.05	0.18	1.08	0.66	2.09	1.78	2.78	3.02	5.69	5.38	ns
24 mA	Std.	0.97	2.06	0.18	1.08	0.66	2.10	1.72	2.83	3.35	5.70	5.32	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-85 • 2.5 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V

Applicable to Standard Plus Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	4.42	0.18	1.08	0.66	4.51	4.10	1.96	1.85	8.10	7.69	ns
4 mA	Std.	0.97	4.42	0.18	1.08	0.66	4.51	4.10	1.96	1.85	8.10	7.69	ns
6 mA	Std.	0.97	3.62	0.18	1.08	0.66	3.70	3.52	2.21	2.32	7.29	7.11	ns
8 mA	Std.	0.97	3.62	0.18	1.08	0.66	3.70	3.52	2.21	2.32	7.29	7.11	ns
12 mA	Std.	0.97	3.09	0.18	1.08	0.66	3.15	3.09	2.39	2.61	6.74	6.68	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-100 • 1.8 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V****Applicable to Advanced I/O Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	3.25	0.18	1.01	0.66	3.21	3.25	2.33	1.61	6.80	6.85	ns
4 mA	Std.	0.97	2.62	0.18	1.01	0.66	2.68	2.51	2.66	2.46	6.27	6.11	ns
6 mA	Std.	0.97	2.31	0.18	1.01	0.66	2.36	2.15	2.90	2.87	5.95	5.75	ns
8 mA	Std.	0.97	2.25	0.18	1.01	0.66	2.30	2.08	2.95	2.98	5.89	5.68	ns
12 mA	Std.	0.97	2.24	0.18	1.01	0.66	2.29	2.00	3.02	3.40	5.88	5.60	ns
16 mA	Std.	0.97	2.24	0.18	1.01	0.66	2.29	2.00	3.02	3.40	5.88	5.60	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-101 • 1.8 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V****Applicable to Standard Plus Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	5.78	0.18	1.01	0.66	5.90	5.32	1.95	1.47	9.49	8.91	ns
4 mA	Std.	0.97	4.75	0.18	1.01	0.66	4.85	4.54	2.25	2.21	8.44	8.13	ns
6 mA	Std.	0.97	4.07	0.18	1.01	0.66	4.15	3.98	2.46	2.58	7.75	7.57	ns
8 mA	Std.	0.97	4.07	0.18	1.01	0.66	4.15	3.98	2.46	2.58	7.75	7.57	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-102 • 1.8 V LVCMOS High Slew – Applies to 1.5 V DC Core Voltage**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V****Applicable to Standard Plus Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.97	2.76	0.18	1.01	0.66	2.79	2.76	1.94	1.51	6.39	6.35	ns
4 mA	Std.	0.97	2.25	0.18	1.01	0.66	2.30	2.09	2.24	2.29	5.89	5.69	ns
6 mA	Std.	0.97	1.97	0.18	1.01	0.66	2.02	1.76	2.46	2.66	5.61	5.36	ns
8 mA	Std.	0.97	1.97	0.18	1.01	0.66	2.02	1.76	2.46	2.66	5.61	5.36	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-103 • 1.8 V LVCMOS Low Slew – Applies to 1.5 V DC Core Voltage**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V****Applicable to Standard Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.97	5.63	0.18	0.98	0.66	5.74	5.30	1.68	1.24	ns
4 mA	Std.	0.97	4.69	0.18	0.98	0.66	4.79	4.52	1.97	1.98	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Global Tree Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard-dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to the "Clock Conditioning Circuits" section on page 2-115. Table 2-173 to Table 2-188 on page 2-114 present minimum and maximum global clock delays within each device. Minimum and maximum delays are measured with minimum and maximum loading.

Timing Characteristics

1.5 V DC Core Voltage

Table 2-173 • AGL015 Global Resource

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.		Units
		Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	1.21	1.42	ns
t_{RCKH}	Input High Delay for Global Clock	1.23	1.49	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.18		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.27	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-174 • AGL030 Global Resource

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.		Units
		Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	1.21	1.42	ns
t_{RCKH}	Input High Delay for Global Clock	1.23	1.49	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.18		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.27	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-183 • AGL060 Global Resource**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.14\text{ V}$**

Parameter	Description	Std.		Units
		Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	2.04	2.33	ns
t_{RCKH}	Input High Delay for Global Clock	2.10	2.51	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.40	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-184 • AGL125 Global Resource**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.14\text{ V}$**

Parameter	Description	Std.		Units
		Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	2.08	2.54	ns
t_{RCKH}	Input High Delay for Global Clock	2.15	2.77	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.62	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-185 • AGL250 Global Resource**Commercial-Case Conditions: $T_J = 70^{\circ}\text{C}$, $V_{CC} = 1.14\text{ V}$**

Parameter	Description	Std.		Units
		Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	2.11	2.57	ns
t_{RCKH}	Input High Delay for Global Clock	2.19	2.81	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.62	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-186 • AGL400 Global Resource**Commercial-Case Conditions: $T_J = 70^{\circ}\text{C}$, $V_{CC} = 1.14\text{ V}$**

Parameter	Description	Std.		Units
		Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	2.18	2.64	ns
t_{RCKH}	Input High Delay for Global Clock	2.27	2.89	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.40		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.65		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.62	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

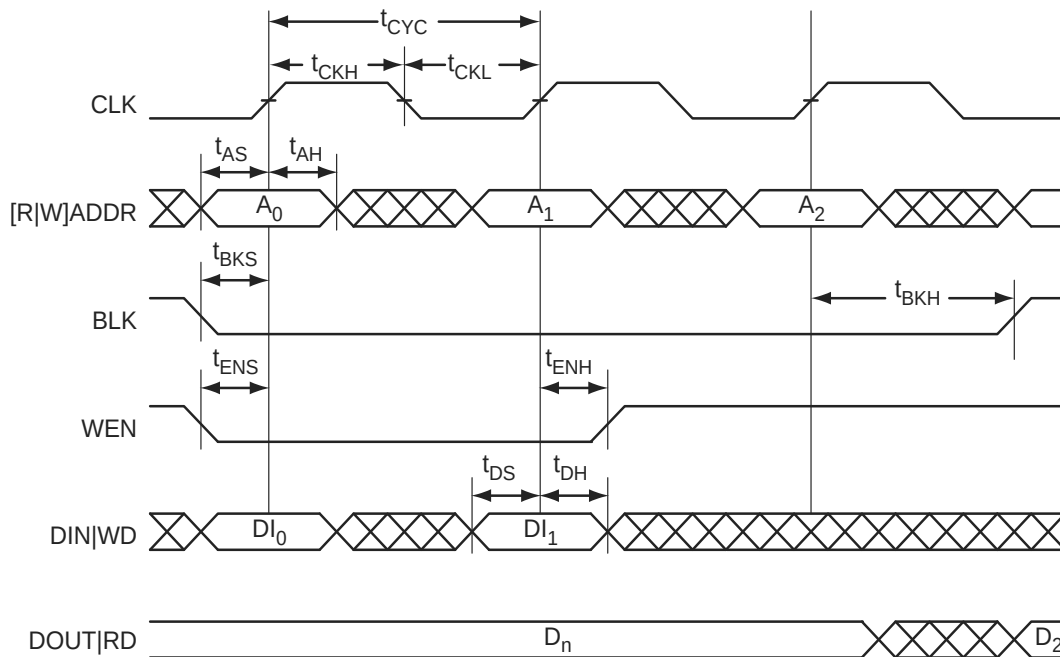


Figure 2-34 • RAM Write, Output Retained. Applicable to Both RAM4K9 and RAM512x18.

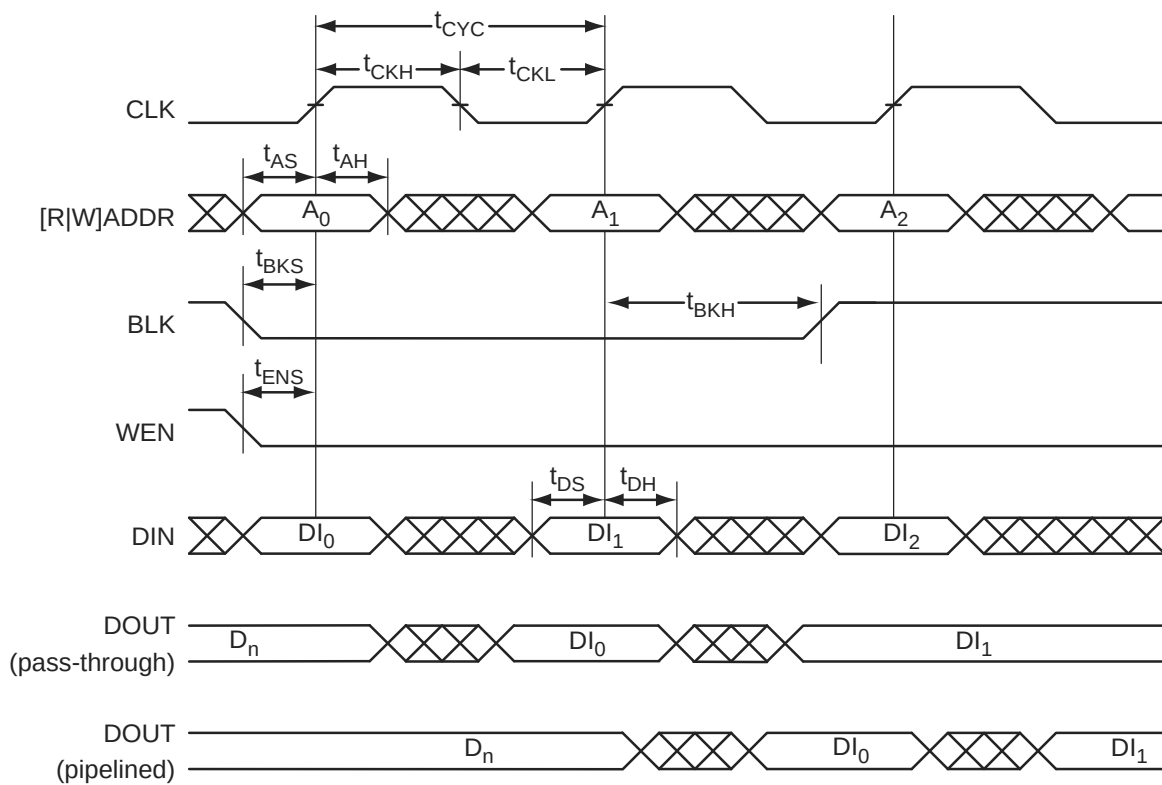


Figure 2-35 • RAM Write, Output as Write Data (WMODE = 1). Applicable to RAM4K9 only.

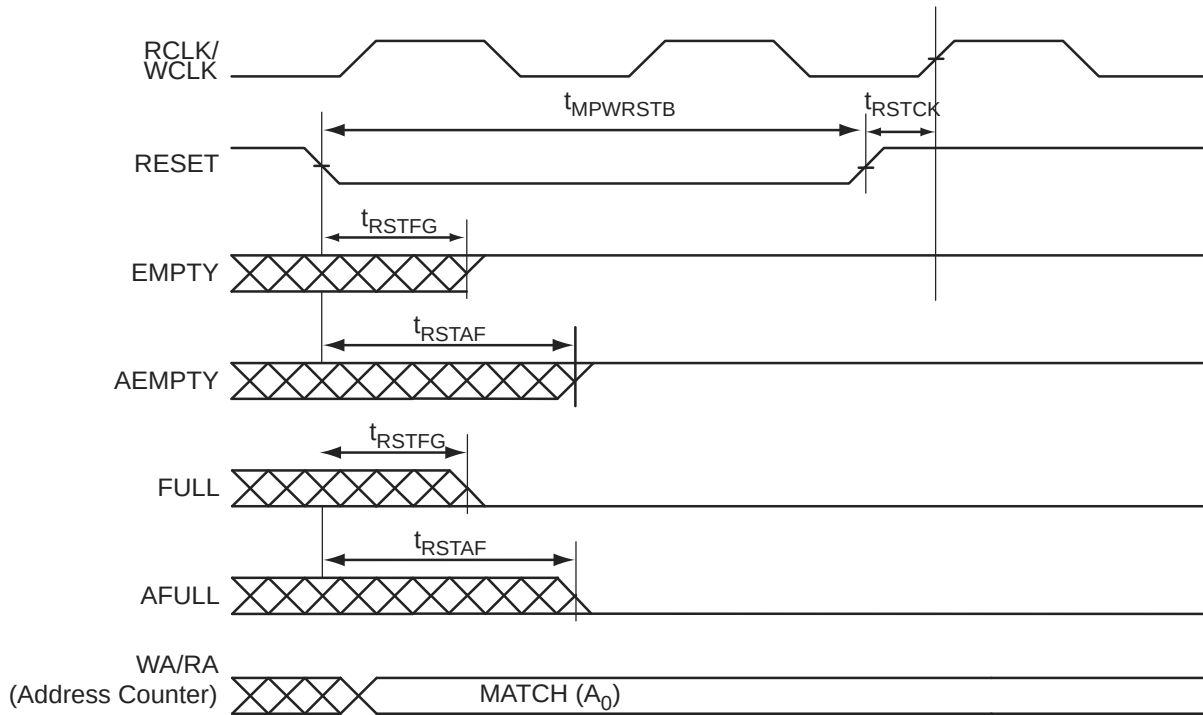


Figure 2-40 • FIFO Reset

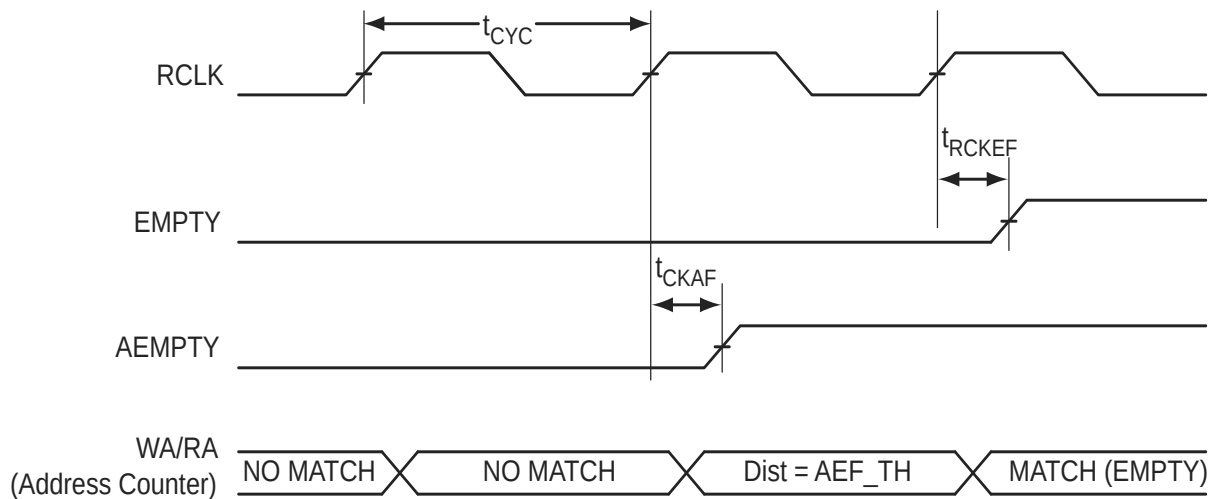


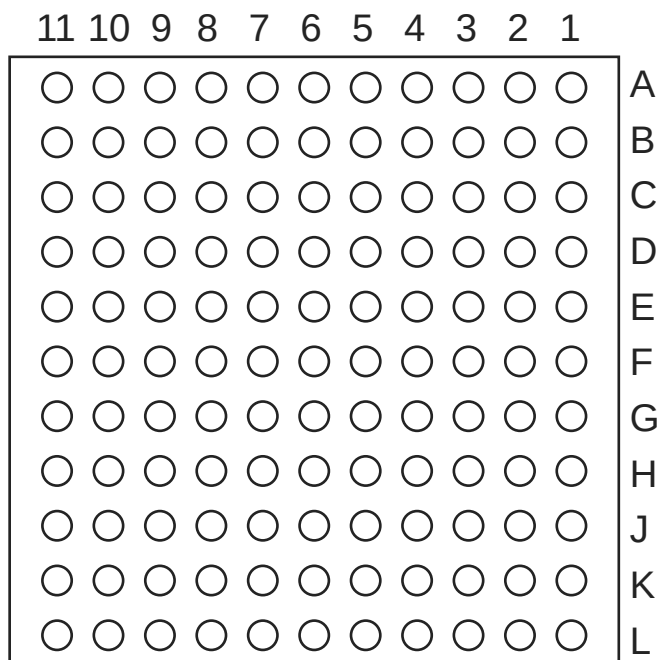
Figure 2-41 • FIFO EMPTY Flag and AEMPTY Flag Assertion

CS81	
Pin Number	AGL250 Function
A1	GAA0/IO00RSB0
A2	GAA1/IO01RSB0
A3	GAC0/IO04RSB0
A4	IO13RSB0
A5	IO21RSB0
A6	IO27RSB0
A7	GBB0/IO37RSB0
A8	GBA1/IO40RSB0
A9	GBA2/IO41PPB1
B1	GAA2/IO118UPB3
B2	GAB0/IO02RSB0
B3	GAC1/IO05RSB0
B4	IO11RSB0
B5	IO23RSB0
B6	GBC0/IO35RSB0
B7	GBB1/IO38RSB0
B8	IO41NPB1
B9	GBB2/IO42PSB1
C1	GAB2/IO117UPB3
C2	IO118VPB3
C3	GND
C4	IO15RSB0
C5	IO25RSB0
C6	GND
C7	GBA0/IO39RSB0
C8	GBC2/IO43PDB1
C9	IO43NDB1
D1	GAC2/IO116USB3
D2	IO117VPB3
D3	GFA2/IO107PSB3
D4	VCC
D5	VCCIB0
D6	GND
D7	IO52NPB1
D8	GCC1/IO48PDB1
D9	GCC0/IO48NDB1

CS81	
Pin Number	AGL250 Function
E1	GFB0/IO109NDB3
E2	GFB1/IO109PDB3
E3	GFA1/IO108PSB3
E4	VCCIB3
E5	VCC
E6	VCCIB1
E7	GCA0/IO50NDB1
E8	GCA1/IO50PDB1
E9	GCB2/IO52PPB1
F1	VCCPLF
F2	VCOMPLF
F3	GND
F4	GND
F5	VCCIB2
F6	GND
F7	GDA1/IO60USB1
F8	GDC1/IO58UDB1
F9	GDC0/IO58VDB1
G1	GEA0/IO98NDB3
G2	GEC1/IO100PDB3
G3	GEC0/IO100NDB3
G4	IO91RSB2
G5	IO86RSB2
G6	IO71RSB2
G7	GDB2/IO62RSB2
G8	VJTAG
G9	TRST
H1	GEA1/IO98PDB3
H2	FF/GEB2/IO96RSB2
H3	IO93RSB2
H4	IO90RSB2
H5	IO85RSB2
H6	IO77RSB2
H7	GDA2/IO61RSB2
H8	TDI
H9	TDO

CS81	
Pin Number	AGL250 Function
J1	GEA2/IO97RSB2
J2	GEC2/IO95RSB2
J3	IO92RSB2
J4	IO88RSB2
J5	IO84RSB2
J6	IO74RSB2
J7	TCK
J8	TMS
J9	VPUMP

CS121



Note: This is the bottom view of the package.

Note

For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

CS196	
Pin Number	AGL125 Function
A1	GND
A2	GAA0/IO00RSB0
A3	GAC0/IO04RSB0
A4	GAC1/IO05RSB0
A5	IO09RSB0
A6	IO15RSB0
A7	IO18RSB0
A8	IO22RSB0
A9	IO27RSB0
A10	GBC0/IO35RSB0
A11	GBB0/IO37RSB0
A12	GBB1/IO38RSB0
A13	GBA1/IO40RSB0
A14	GND
B1	VCCIB1
B2	VMV0
B3	GAA1/IO01RSB0
B4	GAB1/IO03RSB0
B5	GND
B6	IO16RSB0
B7	IO20RSB0
B8	IO24RSB0
B9	IO28RSB0
B10	GND
B11	GBC1/IO36RSB0
B12	GBA0/IO39RSB0
B13	GBA2/IO41RSB0
B14	GBB2/IO43RSB0
C1	GAC2/IO128RSB1
C2	GAB2/IO130RSB1
C3	GNDQ
C4	VCCIB0
C5	GAB0/IO02RSB0
C6	IO14RSB0
C7	VCCIB0
C8	NC

CS196	
Pin Number	AGL125 Function
C9	IO23RSB0
C10	IO29RSB0
C11	VCCIB0
C12	IO42RSB0
C13	GNDQ
C14	IO44RSB0
D1	IO127RSB1
D2	IO129RSB1
D3	GAA2/IO132RSB1
D4	IO126RSB1
D5	IO06RSB0
D6	IO13RSB0
D7	IO19RSB0
D8	IO21RSB0
D9	IO26RSB0
D10	IO31RSB0
D11	IO30RSB0
D12	VMV0
D13	IO46RSB0
D14	GBC2/IO45RSB0
E1	IO125RSB1
E2	GND
E3	IO131RSB1
E4	VCCIB1
E5	NC
E6	IO08RSB0
E7	IO17RSB0
E8	IO12RSB0
E9	IO11RSB0
E10	NC
E11	VCCIB0
E12	IO32RSB0
E13	GND
E14	IO34RSB0
F1	IO124RSB1
F2	IO114RSB1

CS196	
Pin Number	AGL125 Function
F3	IO113RSB1
F4	IO112RSB1
F5	IO111RSB1
F6	NC
F7	VCC
F8	VCC
F9	NC
F10	IO07RSB0
F11	IO25RSB0
F12	IO10RSB0
F13	IO33RSB0
F14	IO47RSB0
G1	GFB1/IO121RSB1
G2	GFA0/IO119RSB1
G3	GFA2/IO117RSB1
G4	VCOMPLF
G5	GFC0/IO122RSB1
G6	VCC
G7	GND
G8	GND
G9	VCC
G10	GCC0/IO52RSB0
G11	GCB1/IO53RSB0
G12	GCA0/IO56RSB0
G13	IO48RSB0
G14	GCC2/IO59RSB0
H1	GFB0/IO120RSB1
H2	GFA1/IO118RSB1
H3	VCCPLF
H4	GFB2/IO116RSB1
H5	GFC1/IO123RSB1
H6	VCC
H7	GND
H8	GND
H9	VCC
H10	GCC1/IO51RSB0

CS196	
Pin Number	AGL400 Function
A1	GND
A2	GAA0/IO00RSB0
A3	GAC0/IO04RSB0
A4	GAC1/IO05RSB0
A5	IO14RSB0
A6	IO18RSB0
A7	IO26RSB0
A8	IO29RSB0
A9	IO36RSB0
A10	GBC0/IO54RSB0
A11	GBB0/IO56RSB0
A12	GBB1/IO57RSB0
A13	GBA1/IO59RSB0
A14	GND
B1	VCCIB3
B2	VMV0
B2	VMV0
B3	GAA1/IO01RSB0
B4	GAB1/IO03RSB0
B5	GND
B6	IO17RSB0
B7	IO25RSB0
B8	IO34RSB0
B9	IO39RSB0
B10	GND
B11	GBC1/IO55RSB0
B12	GBA0/IO58RSB0
B13	GBA2/IO60PPB1
B14	GGB2/IO61PDB1
C1	GAC2/IO153UDB3
C2	GAB2/IO154UDB3
C3	GNDQ
C4	VCCIB0
C5	GAB0/IO02RSB0
C6	IO15RSB0
C7	VCCIB0

CS196	
Pin Number	AGL400 Function
C8	IO31RSB0
C9	IO44RSB0
C10	IO49RSB0
C11	VCCIB0
C12	IO60NPB1
C13	GNDQ
C14	IO61NDB1
D1	IO153VDB3
D2	IO154VDB3
D3	GAA2/IO155UDB3
D4	IO150PPB3
D5	IO11RSB0
D6	IO20RSB0
D7	IO23RSB0
D8	IO28RSB0
D9	IO41RSB0
D10	IO47RSB0
D11	IO63PPB1
D12	VMV1
D13	IO62NDB1
D14	GBC2/IO62PDB1
E1	IO149PDB3
E2	GND
E3	IO155VDB3
E4	VCCIB3
E5	IO151USB3
E6	IO09RSB0
E7	IO12RSB0
E8	IO32RSB0
E9	IO46RSB0
E10	IO51RSB0
E11	VCCIB1
E12	IO63NPB1
E13	GND
E14	IO64PDB1
F1	IO149NDB3

CS196	
Pin Number	AGL400 Function
F2	IO144NPB3
F3	IO148PDB3
F4	IO148NDB3
F5	IO150NPB3
F6	IO07RSB0
F7	VCC
F8	VCC
F9	IO43RSB0
F10	IO73PDB1
F11	IO73NDB1
F12	IO66NDB1
F13	IO66PDB1
F14	IO64NDB1
G1	GFB1/IO146PDB3
G2	GFA0/IO145NDB3
G3	GFA2/IO144PPB3
G4	VCOMPLF
G5	GFC0/IO147NDB3
G6	VCC
G7	GND
G8	GND
G9	VCC
G10	GCC0/IO67NDB1
G11	GCB1/IO68PDB1
G12	GCA0/IO69NDB1
G13	IO72NDB1
G14	GCC2/IO72PDB1
H1	GFB0/IO146NDB3
H2	GFA1/IO145PDB3
H3	VCCPLF
H4	GFB2/IO143PPB3
H5	GFC1/IO147PDB3
H6	VCC
H7	GND
H8	GND
H9	VCC

CS281	
Pin Number	AGL1000 Function
H8	VCC
H9	VCCIB0
H10	VCC
H11	VCCIB0
H12	VCC
H13	VCCIB1
H15	IO90NPB1
H16	GCB0/IO92NPB1
H18	GCA1/IO93PPB1
H19	GCA2/IO94PPB1
J1	VCOMPLF
J2	GFA0/IO207NDB3
J4	VCCPLF
J5	GFC0/IO209NPB3
J7	GFA2/IO206PDB3
J8	VCCIB3
J9	GND
J10	GND
J11	GND
J12	VCCIB1
J13	GCC1/IO91PPB1
J15	GCA0/IO93NPB1
J16	GCB2/IO95PPB1
J18	IO94NPB1
J19	IO102PSB1
K1	VCCIB3
K2	GFA1/IO207PDB3
K4	GND
K5	IO204NPB3
K7	IO206NDB3
K8	VCC
K9	GND
K10	GND
K11	GND
K12	VCC
K13	GCC2/IO96PPB1

CS281	
Pin Number	AGL1000 Function
K15	IO95NPB1
K16	GND
K18	IO96NPB1
K19	VCCIB1
L1	GFB2/IO205PDB3
L2	IO205NDB3
L4	GFC2/IO204PPB3
L5	IO203PPB3
L7	IO203NPB3
L8	VCCIB3
L9	GND
L10	GND
L11	GND
L12	VCCIB1
L13	IO103PPB1
L15	IO103NPB1
L16	IO97PPB1
L18	IO98NPB1
L19	IO97NPB1
M1	IO202PDB3
M2	IO202NDB3
M4	IO201NPB3
M5	IO198PPB3
M7	VCCIB3
M8	VCC
M9	VCCIB2
M10	VCC
M11	VCCIB2
M12	VCC
M13	VCCIB1
M15	IO104NPB1
M16	IO100NPB1
M18	IO104PPB1
M19	IO98PPB1
N1	IO201PPB3
N2	IO198NPB3

CS281	
Pin Number	AGL1000 Function
N4	IO196PPB3
N5	IO197NPB3
N7	GEA2/IO187RSB2
N8	VCCIB2
N9	IO155RSB2
N10	IO154RSB2
N11	IO150RSB2
N12	VCCIB2
N13	VPUMP
N15	IO107PPB1
N16	IO105PPB1
N18	IO107NPB1
N19	IO100PPB1
P1	IO195PDB3
P2	GND
P3	IO195NDB3
P4	IO194PPB3
P5	GEA0/IO188NPB3
P15	IO108NDB1
P16	IO108PDB1
P17	GDC1/IO111PPB1
P18	GND
P19	IO105NPB1
R1	IO196NPB3
R2	IO194NPB3
R4	GEC1/IO190PPB3
R5	GEB1/IO189PPB3
R6	IO184RSB2
R7	IO173RSB2
R8	IO168RSB2
R9	IO160RSB2
R10	IO151RSB2
R11	IO141RSB2
R12	IO136RSB2
R13	IO127RSB2
R14	IO124RSB2

QN132	
Pin Number	AGL125 Function
A1	GAB2/IO69RSB1
A2	IO130RSB1
A3	VCCIB1
A4	GFC1/IO126RSB1
A5	GFB0/IO123RSB1
A6	VCCPLF
A7	GFA1/IO121RSB1
A8	GFC2/IO118RSB1
A9	IO115RSB1
A10	VCC
A11	GEB1/IO110RSB1
A12	GEA0/IO107RSB1
A13	GEC2/IO104RSB1
A14	IO100RSB1
A15	VCC
A16	IO99RSB1
A17	IO96RSB1
A18	IO94RSB1
A19	IO91RSB1
A20	IO85RSB1
A21	IO79RSB1
A22	VCC
A23	GDB2/IO71RSB1
A24	TDI
A25	TRST
A26	GDC1/IO61RSB0
A27	VCC
A28	IO60RSB0
A29	GCC2/IO59RSB0
A30	GCA2/IO57RSB0
A31	GCA0/IO56RSB0
A32	GCB1/IO53RSB0
A33	IO49RSB0
A34	VCC
A35	IO44RSB0
A36	GBA2/IO41RSB0

QN132	
Pin Number	AGL125 Function
A37	GBB1/IO38RSB0
A38	GBC0/IO35RSB0
A39	VCCIB0
A40	IO28RSB0
A41	IO22RSB0
A42	IO18RSB0
A43	IO14RSB0
A44	IO11RSB0
A45	IO07RSB0
A46	VCC
A47	GAC1/IO05RSB0
A48	GAB0/IO02RSB0
B1	IO68RSB1
B2	GAC2/IO131RSB1
B3	GND
B4	GFC0/IO125RSB1
B5	VCOMPLF
B6	GND
B7	GFB2/IO119RSB1
B8	IO116RSB1
B9	GND
B10	GEB0/IO109RSB1
B11	VMV1
B12	FF/GEB2/IO105RSB1
B13	IO101RSB1
B14	GND
B15	IO98RSB1
B16	IO95RSB1
B17	GND
B18	IO87RSB1
B19	IO81RSB1
B20	GND
B21	GNDQ
B22	TMS
B23	TDO
B24	GDC0/IO62RSB0

QN132	
Pin Number	AGL125 Function
B25	GND
B26	NC
B27	GCB2/IO58RSB0
B28	GND
B29	GCB0/IO54RSB0
B30	GCC1/IO51RSB0
B31	GND
B32	GBB2/IO43RSB0
B33	VMV0
B34	GBA0/IO39RSB0
B35	GBC1/IO36RSB0
B36	GND
B37	IO26RSB0
B38	IO21RSB0
B39	GND
B40	IO13RSB0
B41	IO08RSB0
B42	GND
B43	GAC0/IO04RSB0
B44	GNDQ
C1	GAA2/IO67RSB1
C2	IO132RSB1
C3	VCC
C4	GFB1/IO124RSB1
C5	GFA0/IO122RSB1
C6	GFA2/IO120RSB1
C7	IO117RSB1
C8	VCCIB1
C9	GEA1/IO108RSB1
C10	GNDQ
C11	GEA2/IO106RSB1
C12	IO103RSB1
C13	VCCIB1
C14	IO97RSB1
C15	IO93RSB1
C16	IO89RSB1

FG484	
Pin Number	AGL400 Function
N17	IO74RSB1
N18	IO72NPB1
N19	IO70NDB1
N20	NC
N21	NC
N22	NC
P1	NC
P2	NC
P3	NC
P4	IO142NDB3
P5	IO141NPB3
P6	IO125RSB2
P7	IO139RSB3
P8	VCCIB3
P9	GND
P10	VCC
P11	VCC
P12	VCC
P13	VCC
P14	GND
P15	VCCIB1
P16	GDB0/IO78VPB1
P17	IO76VDB1
P18	IO76UDB1
P19	IO75PDB1
P20	NC
P21	NC
P22	NC
R1	NC
R2	NC
R3	VCC
R4	IO140PDB3
R5	IO130RSB2
R6	IO138NPB3
R7	GEC0/IO137NPB3
R8	VMV3

FG484	
Pin Number	AGL400 Function
U1	NC
U2	NC
U3	NC
U4	GEB1/IO136PDB3
U5	GEB0/IO136NDB3
U6	VMV2
U7	IO129RSB2
U8	IO128RSB2
U9	IO122RSB2
U10	IO115RSB2
U11	IO110RSB2
U12	IO98RSB2
U13	IO95RSB2
U14	IO88RSB2
U15	IO84RSB2
U16	TCK
U17	VPUMP
U18	TRST
U19	GDA0/IO79VDB1
U20	NC
U21	NC
U22	NC
V1	NC
V2	NC
V3	GND
V4	GEA1/IO135PDB3
V5	GEA0/IO135NDB3
V6	IO127RSB2
V7	GEC2/IO132RSB2
V8	IO123RSB2
V9	IO118RSB2
V10	IO112RSB2
V11	IO106RSB2
V12	IO100RSB2
V13	IO96RSB2
V14	IO89RSB2

FG484	
Pin Number	AGL600 Function
M3	IO158NPB3
M4	GFA2/IO161PPB3
M5	GFA1/IO162PDB3
M6	VCCPLF
M7	IO160NDB3
M8	GFB2/IO160PDB3
M9	VCC
M10	GND
M11	GND
M12	GND
M13	GND
M14	VCC
M15	GCB2/IO73PPB1
M16	GCA1/IO71PPB1
M17	GCC2/IO74PPB1
M18	IO80PPB1
M19	GCA2/IO72PDB1
M20	IO79PPB1
M21	IO78PPB1
M22	NC
N1	IO154NDB3
N2	IO154PDB3
N3	NC
N4	GFC2/IO159PDB3
N5	IO161NPB3
N6	IO156PPB3
N7	IO129RSB2
N8	VCCIB3
N9	VCC
N10	GND
N11	GND
N12	GND
N13	GND
N14	VCC
N15	VCCIB1
N16	IO73NPB1