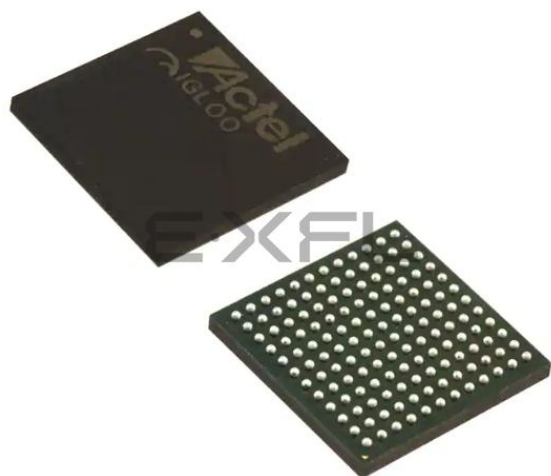




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	6144
Total RAM Bits	36864
Number of I/O	97
Number of Gates	250000
Voltage - Supply	1.14V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 70°C (TA)
Package / Case	144-LBGA
Supplier Device Package	144-FPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/agl250v2-fg144

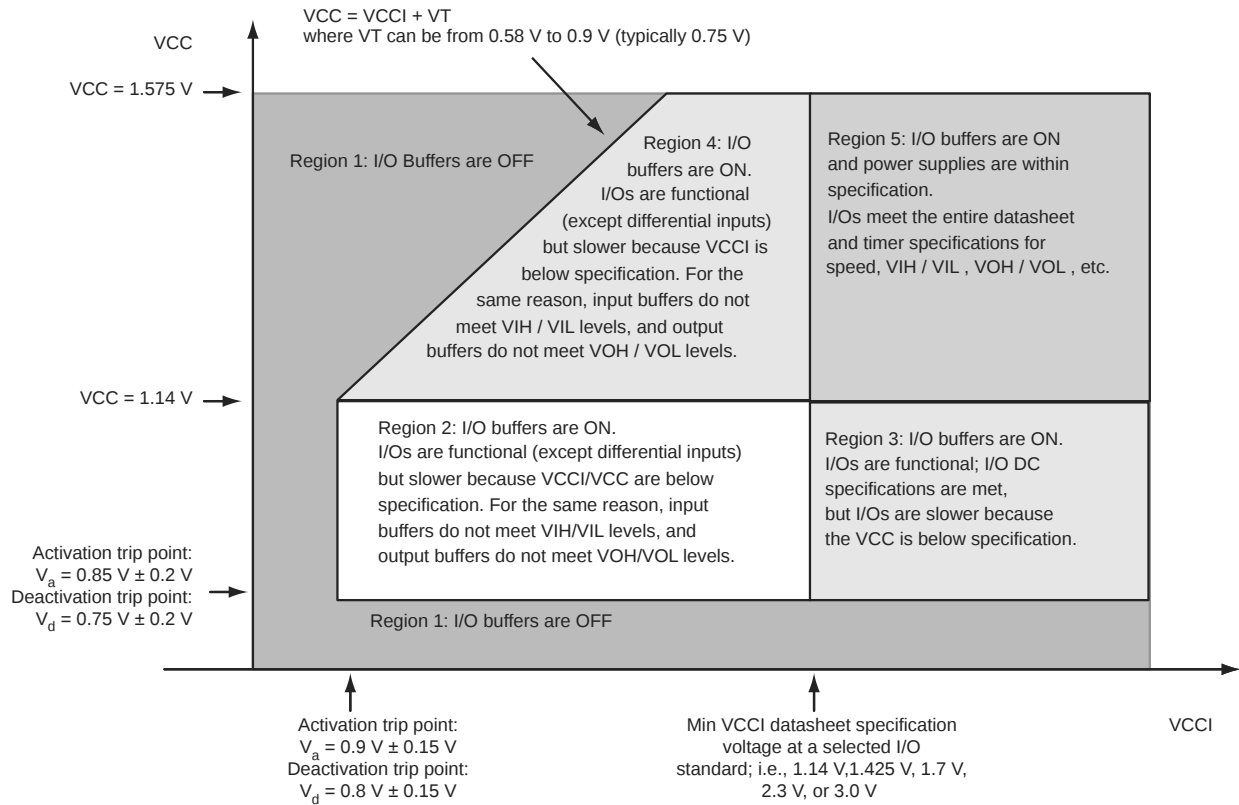


Figure 2-2 • V2 Devices – I/O State as a Function of VCCI and VCC Voltage Levels

Thermal Characteristics

Introduction

The temperature variable in the Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because dynamic and static power consumption cause the chip junction to be higher than the ambient temperature.

EQ 1 can be used to calculate junction temperature.

$$T_J = \text{Junction Temperature} = \Delta T + T_A$$

EQ 1

where:

T_A = Ambient Temperature

ΔT = Temperature gradient between junction (silicon) and ambient $\Delta T = \theta_{ja} * P$

θ_{ja} = Junction-to-ambient of the package. θ_{ja} numbers are located in Table 2-5 on page 2-6.

P = Power dissipation

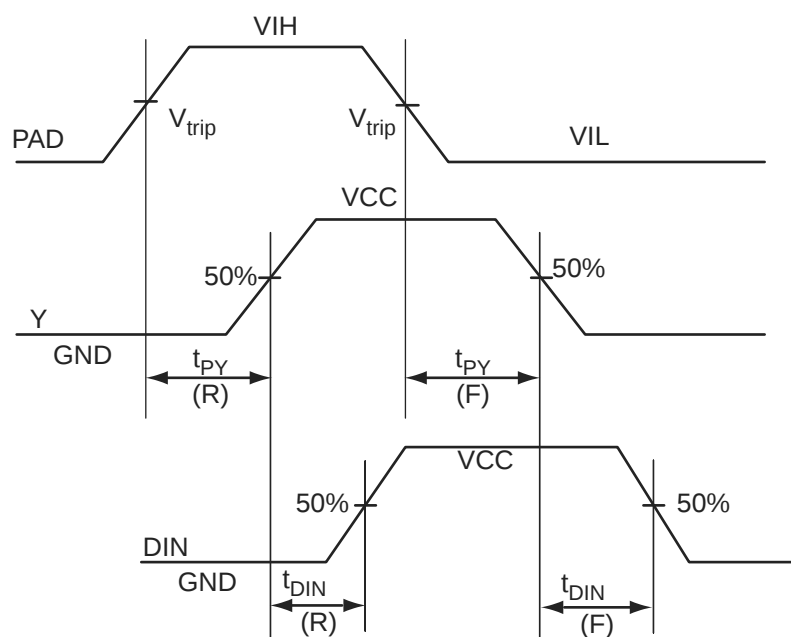
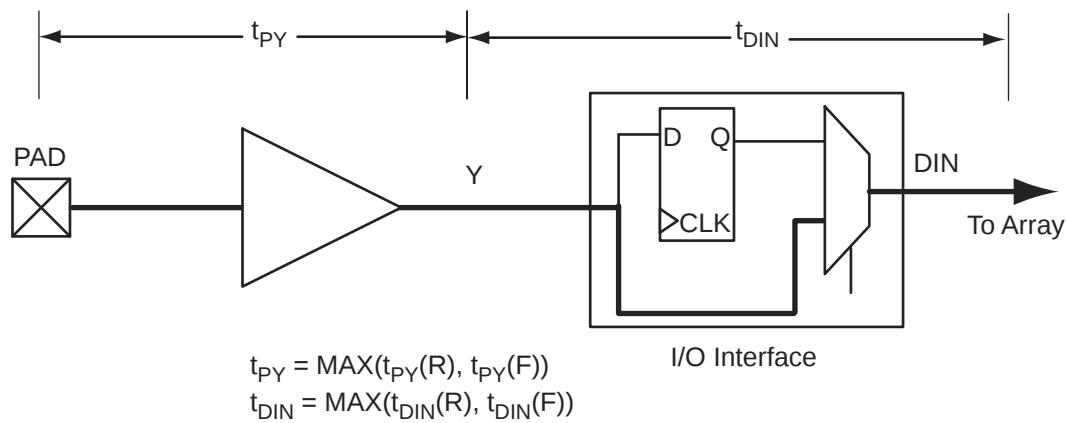


Figure 2-4 • Input Buffer Timing Model and Delays (example)

Table 2-119 • 1.5 V LVC MOS Low Slew – Applies to 1.5 V DC Core Voltage**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V****Applicable to Standard Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.97	5.88	0.18	1.14	0.66	6.00	5.45	2.00	1.94	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-120 • 1.5 V LVC MOS High Slew – Applies to 1.5 V DC Core Voltage**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V****Applicable to Standard Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.97	2.51	0.18	1.14	0.66	2.56	2.21	1.99	2.03	ns

Notes:

- Software default selection highlighted in gray.
- For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

1.2 V DC Core Voltage**Table 2-121 • 1.5 V LVC MOS Low Slew – Applies to 1.2 V DC Core Voltage****Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V****Applicable to Advanced I/O Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	7.17	0.26	1.27	1.10	7.29	6.60	3.33	3.03	13.07	12.39	ns
4 mA	Std.	1.55	6.27	0.26	1.27	1.10	6.37	5.86	3.61	3.51	12.16	11.64	ns
6 mA	Std.	1.55	5.94	0.26	1.27	1.10	6.04	5.70	3.67	3.64	11.82	11.48	ns
8 mA	Std.	1.55	5.86	0.26	1.27	1.10	5.96	5.71	2.83	4.11	11.74	11.50	ns
12 mA	Std.	1.55	5.86	0.26	1.27	1.10	5.96	5.71	2.83	4.11	11.74	11.50	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-122 • 1.5 V LVC MOS High Slew – Applies to 1.2 V DC Core Voltage**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 1.4 V****Applicable to Advanced I/O Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	1.55	3.44	0.26	1.27	1.10	3.49	3.35	3.32	3.12	9.28	9.14	ns
4 mA	Std.	1.55	3.06	0.26	1.27	1.10	3.10	2.89	3.60	3.61	8.89	8.67	ns
6 mA	Std.	1.55	2.98	0.26	1.27	1.10	3.02	2.80	3.66	3.74	8.81	8.58	ns
8 mA	Std.	1.55	2.96	0.26	1.27	1.10	3.00	2.70	3.75	4.23	8.78	8.48	ns
12 mA	Std.	1.55	2.96	0.26	1.27	1.10	3.00	2.70	3.75	4.23	8.78	8.48	ns

Notes:

- Software default selection highlighted in gray.
- For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Table 2-147 • Minimum and Maximum DC Input and Output Levels

DC Parameter	Description	Min.	Typ.	Max.	Units
VCCI	Supply Voltage	2.375	2.5	2.625	V
VOL	Output Low Voltage	0.9	1.075	1.25	V
VOH	Output High Voltage	1.25	1.425	1.6	V
IOL ¹	Output Lower Current	0.65	0.91	1.16	mA
IOH ¹	Output High Current	0.65	0.91	1.16	mA
VI	Input Voltage	0		2.925	V
IIH ²	Input High Leakage Current			10	μA
IIL ²	Input Low Leakage Current			10	μA
VODIFF	Differential Output Voltage	250	350	450	mV
VOCM	Output Common-Mode Voltage	1.125	1.25	1.375	V
VICM	Input Common-Mode Voltage	0.05	1.25	2.35	V
VIDIFF ⁴	Input Differential Voltage	100	350		mV

Notes:

1. IOL/IOH is defined by VODIFF/(resistor network)
2. Currents are measured at 85°C junction temperature.

Table 2-148 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)
1.075	1.325	Cross point

Note: *Measuring point = Vtrip. See Table 2-29 on page 2-28 for a complete table of trip points.

Timing Characteristics**1.5 V DC Core Voltage****Table 2-149 • LVDS – Applies to 1.5 V DC Core Voltage**

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Standard Banks

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{py}	Units
Std.	0.97	1.67	0.19	1.31	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 and Table 2-7 on page 2-7 for derating values.

1.2 V DC Core Voltage**Table 2-150 • LVDS – Applies to 1.5 V DC Core Voltage**

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.14 V, Worst-Case VCCI = 2.3 V
Applicable to Standard Banks

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{py}	Units
Std.	1.55	2.19	0.25	1.52	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 and Table 2-7 on page 2-7 for derating values.

B-LVDS/M-LVDS

Bus LVDS (B-LVDS) and Multipoint LVDS (M-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers. Microsemi LVDS drivers provide the higher drive current required by B-LVDS and M-LVDS to accommodate the loading. The drivers require series terminations for better signal quality and to control voltage swing. Termination is also required at both ends of the bus since the driver can be located anywhere on the bus. These configurations can be implemented using the TRIBUF_LVDS and BIBUF_LVDS macros along with appropriate terminations. Multipoint designs using Microsemi LVDS macros can achieve up to 200 MHz with a maximum of 20 loads. A sample application is given in Figure 2-14. The input and output buffer delays are available in the LVDS section in Table 2-149 on page 2-81 and Table 2-150 on page 2-81.

Example: For a bus consisting of 20 equidistant loads, the following terminations provide the required differential voltage, in worst-case Industrial operating conditions, at the farthest receiver: $R_S = 60\ \Omega$ and $R_T = 70\ \Omega$, given $Z_0 = 50\ \Omega$ (2") and $Z_{stub} = 50\ \Omega$ (~1.5").

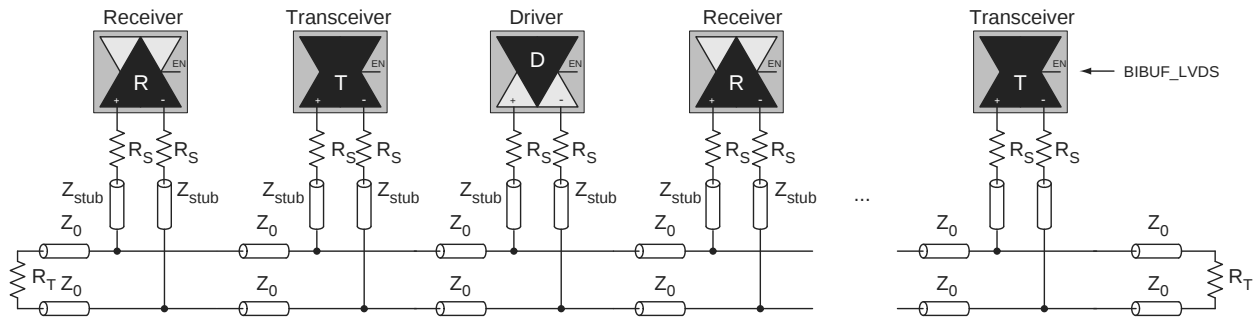


Figure 2-14 • B-LVDS/M-LVDS Multipoint Application Using LVDS I/O Buffers

LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Like LVDS, two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-15. The building blocks of the LVPECL transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVDS implementation because the output standard specifications are different.

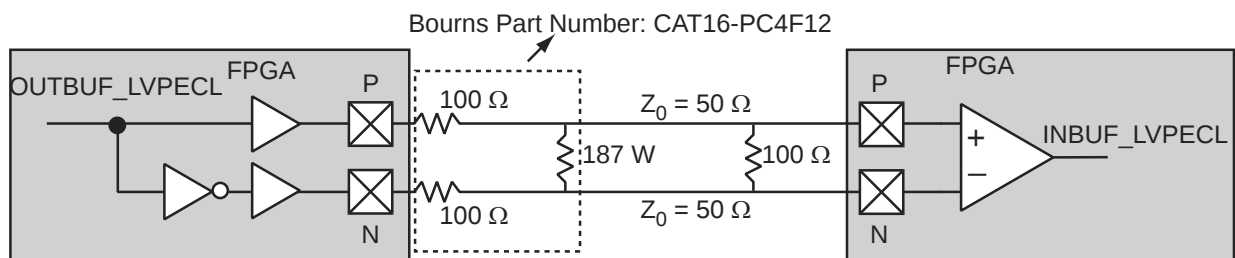


Figure 2-15 • LVPECL Circuit Diagram and Board-Level Implementation

1.2 V DC Core Voltage**Table 2-162 • Output Enable Register Propagation Delays****Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$**

Parameter	Description	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	1.10	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	1.15	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	ns
t_{OESUE}	Enable Setup Time for the Output Enable Register	1.22	ns
t_{OEHE}	Enable Hold Time for the Output Enable Register	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	1.65	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	1.65	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	ns
$t_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.24	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	ns
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.24	ns
$t_{OEWCCLR}$	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.19	ns
$t_{OEWPRES}$	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.19	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width High for the Output Enable Register	0.31	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width Low for the Output Enable Register	0.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Timing Characteristics

1.5 V DC Core Voltage

Table 2-169 • Combinatorial Cell Propagation Delays

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Combinatorial Cell	Equation	Parameter	Std.	Units
INV	$Y = !A$	t_{PD}	0.80	ns
AND2	$Y = A \cdot B$	t_{PD}	0.84	ns
NAND2	$Y = !(A \cdot B)$	t_{PD}	0.90	ns
OR2	$Y = A + B$	t_{PD}	1.19	ns
NOR2	$Y = !(A + B)$	t_{PD}	1.10	ns
XOR2	$Y = A \oplus B$	t_{PD}	1.37	ns
MAJ3	$Y = \text{MAJ}(A, B, C)$	t_{PD}	1.33	ns
XOR3	$Y = A \oplus B \oplus C$	t_{PD}	1.79	ns
MUX2	$Y = A !S + B S$	t_{PD}	1.48	ns
AND3	$Y = A \cdot B \cdot C$	t_{PD}	1.21	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

1.2 V DC Core Voltage

Table 2-170 • Combinatorial Cell Propagation Delays

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.14\text{ V}$

Combinatorial Cell	Equation	Parameter	Std.	Units
INV	$Y = !A$	t_{PD}	1.34	ns
AND2	$Y = A \cdot B$	t_{PD}	1.43	ns
NAND2	$Y = !(A \cdot B)$	t_{PD}	1.59	ns
OR2	$Y = A + B$	t_{PD}	2.30	ns
NOR2	$Y = !(A + B)$	t_{PD}	2.07	ns
XOR2	$Y = A \oplus B$	t_{PD}	2.46	ns
MAJ3	$Y = \text{MAJ}(A, B, C)$	t_{PD}	2.46	ns
XOR3	$Y = A \oplus B \oplus C$	t_{PD}	3.12	ns
MUX2	$Y = A !S + B S$	t_{PD}	2.83	ns
AND3	$Y = A \cdot B \cdot C$	t_{PD}	2.28	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-7 for derating values.

Global Tree Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard-dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to the "Clock Conditioning Circuits" section on page 2-115. Table 2-173 to Table 2-188 on page 2-114 present minimum and maximum global clock delays within each device. Minimum and maximum delays are measured with minimum and maximum loading.

Timing Characteristics

1.5 V DC Core Voltage

Table 2-173 • AGL015 Global Resource

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.		Units
		Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	1.21	1.42	ns
t_{RCKH}	Input High Delay for Global Clock	1.23	1.49	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.18		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.27	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

Table 2-174 • AGL030 Global Resource

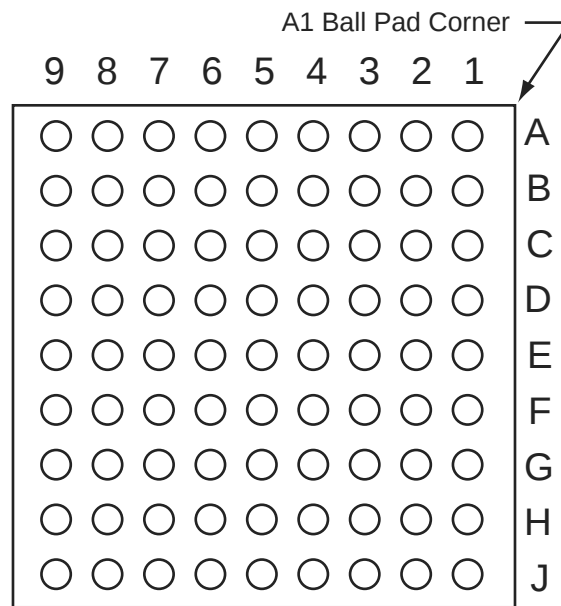
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	Std.		Units
		Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	1.21	1.42	ns
t_{RCKH}	Input High Delay for Global Clock	1.23	1.49	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	1.18		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	1.15		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.27	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-7 for derating values.

CS81



Note: This is the bottom view of the package.

Note

For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

CS196	
Pin Number	AGL400 Function
H10	GCC1/IO67PDB1
H11	GCB0/IO68NDB1
H12	GCA1/IO69PDB1
H13	IO70NDB1
H14	GCA2/IO70PDB1
J1	GFC2/IO142PDB3
J2	IO141PPB3
J3	IO143NPB3
J4	IO140PDB3
J5	IO140NDB3
J6	IO109RSB2
J7	VCC
J8	VCC
J9	IO84RSB2
J10	IO75PDB1
J11	GCB2/IO71PDB1
J12	IO71NDB1
J13	GDC1/IO77UDB1
J14	GDC0/IO77VDB1
K1	IO142NDB3
K2	GND
K3	IO141NPB3
K4	VCCIB3
K5	IO138PPB3
K6	IO125RSB2
K7	IO110RSB2
K8	IO98RSB2
K9	IO104RSB2
K10	IO75NDB1
K11	VCCIB1
K12	GDA1/IO79UPB1
K13	GND
K14	GDB1/IO78UDB1
L1	GEB1/IO136PDB3
L2	GEC1/IO137PDB3
L3	GEC0/IO137NDB3

CS196	
Pin Number	AGL400 Function
L4	IO138NPB3
L5	IO122RSB2
L6	IO128RSB2
L7	IO101RSB2
L8	IO88RSB2
L9	IO86RSB2
L10	IO94RSB2
L11	VPUMP
L12	VJTAG
L13	GDA0/IO79VPB1
L14	GDB0/IO78VDB1
M1	GEB0/IO136NDB3
M2	GEA1/IO135PPB3
M3	GNDQ
M4	VCCIB2
M5	IO120RSB2
M6	IO119RSB2
M7	IO112RSB2
M8	VCCIB2
M9	IO89RSB2
M10	GDB2/IO81RSB2
M11	VCCIB2
M12	VMV2
M12	VMV2
M13	TRST
M14	VCCIB1
N1	GEA0/IO135NPB3
N2	VMV3
N3	GEC2/IO132RSB2
N4	IO130RSB2
N5	GND
N6	IO117RSB2
N7	IO106RSB2
N8	IO100RSB2
N9	IO92RSB2
N10	GND

CS196	
Pin Number	AGL400 Function
N11	TCK
N12	TDI
N13	GNDQ
N14	TDO
P1	GND
P2	GEA2/IO134RSB2
P3	FF/GEB2/IO133RSB2
P4	IO123RSB2
P5	IO116RSB2
P6	IO114RSB2
P7	IO107RSB2
P8	IO103RSB2
P9	IO95RSB2
P10	IO91RSB2
P11	GDC2/IO82RSB2
P12	GDA2/IO80RSB2
P13	TMS
P14	GND

CS281	
Pin Number	AGL600 Function
A1	GND
A2	GAB0/IO02RSB0
A3	GAC1/IO05RSB0
A4	IO07RSB0
A5	IO10RSB0
A6	IO14RSB0
A7	IO18RSB0
A8	IO21RSB0
A9	IO22RSB0
A10	VCCIB0
A11	IO33RSB0
A12	IO40RSB0
A13	IO37RSB0
A14	IO48RSB0
A15	IO51RSB0
A16	IO53RSB0
A17	GBC1/IO55RSB0
A18	GBA0/IO58RSB0
A19	GND
B1	GAA2/IO174PPB3
B2	VCCIB0
B3	GAB1/IO03RSB0
B4	GAC0/IO04RSB0
B5	IO06RSB0
B6	GND
B7	IO15RSB0
B8	IO20RSB0
B9	IO23RSB0
B10	IO24RSB0
B11	IO36RSB0
B12	IO35RSB0
B13	IO44RSB0
B14	GND
B15	IO52RSB0
B16	GBC0/IO54RSB0
B17	GBA1/IO59RSB0

CS281	
Pin Number	AGL600 Function
B18	VCCIB1
B19	IO61NDB1
C1	GAB2/IO173PPB3
C2	IO174NPB3
C6	IO12RSB0
C14	IO50RSB0
C18	IO60NPB1
C19	GBB2/IO61PDB1
D1	IO170PPB3
D2	IO172NPB3
D4	GAA0/IO00RSB0
D5	GAA1/IO01RSB0
D6	IO09RSB0
D7	IO16RSB0
D8	IO19RSB0
D9	IO26RSB0
D10	GND
D11	IO34RSB0
D12	IO45RSB0
D13	IO49RSB0
D14	IO47RSB0
D15	GBB0/IO56RSB0
D16	GBA2/IO60PPB1
D18	GBC2/IO62PPB1
D19	IO66NPB1
E1	IO169NPB3
E2	IO171PPB3
E4	IO171NPB3
E5	IO08RSB0
E6	IO11RSB0
E7	IO13RSB0
E8	IO17RSB0
E9	IO25RSB0
E10	IO30RSB0
E11	IO41RSB0
E12	IO42RSB0

CS281	
Pin Number	AGL600 Function
E13	IO46RSB0
E14	GBB1/IO57RSB0
E15	IO62NPB1
E16	IO63PPB1
E18	IO64PPB1
E19	IO65NPB1
F1	IO168NPB3
F2	GND
F3	IO169PPB3
F4	IO170NPB3
F5	IO173NPB3
F15	IO63NPB1
F16	IO65PPB1
F17	IO64NPB1
F18	GND
F19	IO68PPB1
G1	IO167NPB3
G2	IO165NDB3
G4	IO168PPB3
G5	IO167PPB3
G7	GAC2/IO172PPB3
G8	VCCIB0
G9	IO28RSB0
G10	IO32RSB0
G11	IO43RSB0
G12	VCCIB0
G13	IO66PPB1
G15	IO67NDB1
G16	IO67PDB1
G18	GCC0/IO69NPB1
G19	GCB1/IO70PPB1
H1	GFB0/IO163NPB3
H2	IO165PDB3
H4	GFC1/IO164PPB3
H5	GFB1/IO163PPB3
H7	VCCIB3

VQ100	
Pin Number	AGL125 Function
1	GND
2	GAA2/IO67RSB1
3	IO68RSB1
4	GAB2/IO69RSB1
5	IO132RSB1
6	GAC2/IO131RSB1
7	IO130RSB1
8	IO129RSB1
9	GND
10	GFB1/IO124RSB1
11	GFB0/IO123RSB1
12	VCOMPLF
13	GFA0/IO122RSB1
14	VCCPLF
15	GFA1/IO121RSB1
16	GFA2/IO120RSB1
17	VCC
18	VCCIB1
19	GEC0/IO111RSB1
20	GEB1/IO110RSB1
21	GEB0/IO109RSB1
22	GEA1/IO108RSB1
23	GEA0/IO107RSB1
24	VMV1
25	GNDQ
26	GEA2/IO106RSB1
27	FF/GEB2/IO105RSB1
28	GEC2/IO104RSB1
29	IO102RSB1
30	IO100RSB1
31	IO99RSB1
32	IO97RSB1
33	IO96RSB1
34	IO95RSB1
35	IO94RSB1

VQ100	
Pin Number	AGL125 Function
36	IO93RSB1
37	VCC
38	GND
39	VCCIB1
40	IO87RSB1
41	IO84RSB1
42	IO81RSB1
43	IO75RSB1
44	GDC2/IO72RSB1
45	GDB2/IO71RSB1
46	GDA2/IO70RSB1
47	TCK
48	TDI
49	TMS
50	VMV1
51	GND
52	VPUMP
53	NC
54	TDO
55	TRST
56	VJTAG
57	GDA1/IO65RSB0
58	GDC0/IO62RSB0
59	GDC1/IO61RSB0
60	GCC2/IO59RSB0
61	GCB2/IO58RSB0
62	GCA0/IO56RSB0
63	GCA1/IO55RSB0
64	GCC0/IO52RSB0
65	GCC1/IO51RSB0
66	VCCIB0
67	GND
68	VCC
69	IO47RSB0
70	GBC2/IO45RSB0
71	GBB2/IO43RSB0

VQ100	
Pin Number	AGL125 Function
72	IO42RSB0
73	GBA2/IO41RSB0
74	VMV0
75	GNDQ
76	GBA1/IO40RSB0
77	GBA0/IO39RSB0
78	GBB1/IO38RSB0
79	GBB0/IO37RSB0
80	GBC1/IO36RSB0
81	GBC0/IO35RSB0
82	IO32RSB0
83	IO28RSB0
84	IO25RSB0
85	IO22RSB0
86	IO19RSB0
87	VCCIB0
88	GND
89	VCC
90	IO15RSB0
91	IO13RSB0
92	IO11RSB0
93	IO09RSB0
94	IO07RSB0
95	GAC1/IO05RSB0
96	GAC0/IO04RSB0
97	GAB1/IO03RSB0
98	GAB0/IO02RSB0
99	GAA1/IO01RSB0
100	GAA0/IO00RSB0

FG144	
Pin Number	AGL125 Function
A1	GNDQ
A2	VMV0
A3	GAB0/IO02RSB0
A4	GAB1/IO03RSB0
A5	IO11RSB0
A6	GND
A7	IO18RSB0
A8	VCC
A9	IO25RSB0
A10	GBA0/IO39RSB0
A11	GBA1/IO40RSB0
A12	GNDQ
B1	GAB2/IO69RSB1
B2	GND
B3	GAA0/IO00RSB0
B4	GAA1/IO01RSB0
B5	IO08RSB0
B6	IO14RSB0
B7	IO19RSB0
B8	IO22RSB0
B9	GBB0/IO37RSB0
B10	GBB1/IO38RSB0
B11	GND
B12	VMV0
C1	IO132RSB1
C2	GFA2/IO120RSB1
C3	GAC2/IO131RSB1
C4	VCC
C5	IO10RSB0
C6	IO12RSB0
C7	IO21RSB0
C8	IO24RSB0
C9	IO27RSB0
C10	GBA2/IO41RSB0
C11	IO42RSB0
C12	GBC2/IO45RSB0

FG144	
Pin Number	AGL125 Function
D1	IO128RSB1
D2	IO129RSB1
D3	IO130RSB1
D4	GAA2/IO67RSB1
D5	GAC0/IO04RSB0
D6	GAC1/IO05RSB0
D7	GBC0/IO35RSB0
D8	GBC1/IO36RSB0
D9	GBB2/IO43RSB0
D10	IO28RSB0
D11	IO44RSB0
D12	GCB1/IO53RSB0
E1	VCC
E2	GFC0/IO125RSB1
E3	GFC1/IO126RSB1
E4	VCCIB1
E5	IO68RSB1
E6	VCCIB0
E7	VCCIB0
E8	GCC1/IO51RSB0
E9	VCCIB0
E10	VCC
E11	GCA0/IO56RSB0
E12	IO46RSB0
F1	GFB0/IO123RSB1
F2	VCOMPLF
F3	GFB1/IO124RSB1
F4	IO127RSB1
F5	GND
F6	GND
F7	GND
F8	GCC0/IO52RSB0
F9	GCB0/IO54RSB0
F10	GND
F11	GCA1/IO55RSB0
F12	GCA2/IO57RSB0

FG144	
Pin Number	AGL125 Function
G1	GFA1/IO121RSB1
G2	GND
G3	VCCPLF
G4	GFA0/IO122RSB1
G5	GND
G6	GND
G7	GND
G8	GDC1/IO61RSB0
G9	IO48RSB0
G10	GCC2/IO59RSB0
G11	IO47RSB0
G12	GCB2/IO58RSB0
H1	VCC
H2	GFB2/IO119RSB1
H3	GFC2/IO118RSB1
H4	GEC1/IO112RSB1
H5	VCC
H6	IO50RSB0
H7	IO60RSB0
H8	GDB2/IO71RSB1
H9	GDC0/IO62RSB0
H10	VCCIB0
H11	IO49RSB0
H12	VCC
J1	GEB1/IO110RSB1
J2	IO115RSB1
J3	VCCIB1
J4	GEC0/IO111RSB1
J5	IO116RSB1
J6	IO117RSB1
J7	VCC
J8	TCK
J9	GDA2/IO70RSB1
J10	TDO
J11	GDA1/IO65RSB0
J12	GDB1/IO63RSB0

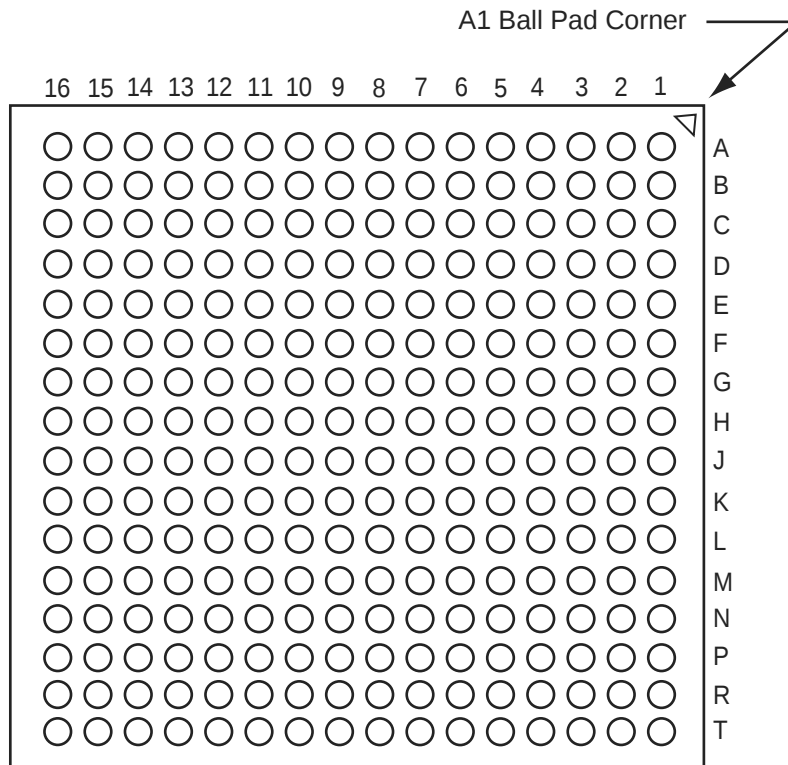
FG144	
Pin Number	AGL400 Function
K1	GEB0/IO136NDB3
K2	GEA1/IO135PDB3
K3	GEA0/IO135NDB3
K4	GEA2/IO134RSB2
K5	IO127RSB2
K6	IO121RSB2
K7	GND
K8	IO104RSB2
K9	GDC2/IO82RSB2
K10	GND
K11	GDA0/IO79VDB1
K12	GDB0/IO78VDB1
L1	GND
L2	VMV3
L3	FF/GEB2/IO133RSB2
L4	IO128RSB2
L5	VCCIB2
L6	IO119RSB2
L7	IO114RSB2
L8	IO110RSB2
L9	TMS
L10	VJTAG
L11	VMV2
L12	TRST
M1	GNDQ
M2	GEC2/IO132RSB2
M3	IO129RSB2
M4	IO126RSB2
M5	IO124RSB2
M6	IO122RSB2
M7	IO117RSB2
M8	IO115RSB2
M9	TDI
M10	VCCIB2
M11	VPUMP
M12	GNDQ

FG144	
Pin Number	AGL600 Function
A1	GNDQ
A2	VMV0
A3	GAB0/IO02RSB0
A4	GAB1/IO03RSB0
A5	IO10RSB0
A6	GND
A7	IO34RSB0
A8	VCC
A9	IO50RSB0
A10	GBA0/IO58RSB0
A11	GBA1/IO59RSB0
A12	GNDQ
B1	GAB2/IO173PDB3
B2	GND
B3	GAA0/IO00RSB0
B4	GAA1/IO01RSB0
B5	IO13RSB0
B6	IO19RSB0
B7	IO31RSB0
B8	IO39RSB0
B9	GBB0/IO56RSB0
B10	GBB1/IO57RSB0
B11	GND
B12	VMV1
C1	IO173NDB3
C2	GFA2/IO161PPB3
C3	GAC2/IO172PDB3
C4	VCC
C5	IO16RSB0
C6	IO25RSB0
C7	IO28RSB0
C8	IO42RSB0
C9	IO45RSB0
C10	GBA2/IO60PDB1
C11	IO60NDB1
C12	GBC2/IO62PPB1

FG144	
Pin Number	AGL600 Function
D1	IO169PDB3
D2	IO169NDB3
D3	IO172NDB3
D4	GAA2/IO174PPB3
D5	GAC0/IO04RSB0
D6	GAC1/IO05RSB0
D7	GBC0/IO54RSB0
D8	GBC1/IO55RSB0
D9	GBB2/IO61PDB1
D10	IO61NDB1
D11	IO62NPB1
D12	GCB1/IO70PPB1
E1	VCC
E2	GFC0/IO164NDB3
E3	GFC1/IO164PDB3
E4	VCCIB3
E5	IO174NPB3
E6	VCCIB0
E7	VCCIB0
E8	GCC1/IO69PDB1
E9	VCCIB1
E10	VCC
E11	GCA0/IO71NDB1
E12	IO72NDB1
F1	GFB0/IO163NPB3
F2	VCOMPLF
F3	GFB1/IO163PPB3
F4	IO161NPB3
F5	GND
F6	GND
F7	GND
F8	GCC0/IO69NDB1
F9	GCB0/IO70NPB1
F10	GND
F11	GCA1/IO71PDB1
F12	GCA2/IO72PDB1

FG144	
Pin Number	AGL600 Function
G1	GFA1/IO162PPB3
G2	GND
G3	VCCPLF
G4	GFA0/IO162NPB3
G5	GND
G6	GND
G7	GND
G8	GDC1/IO86PPB1
G9	IO74NDB1
G10	GCC2/IO74PDB1
G11	IO73NDB1
G12	GCB2/IO73PDB1
H1	VCC
H2	GFB2/IO160PDB3
H3	GFC2/IO159PSB3
H4	GEC1/IO146PDB3
H5	VCC
H6	IO80PDB1
H7	IO80NDB1
H8	GDB2/IO90RSB2
H9	GDC0/IO86NPB1
H10	VCCIB1
H11	IO84PSB1
H12	VCC
J1	GEB1/IO145PDB3
J2	IO160NDB3
J3	VCCIB3
J4	GEC0/IO146NDB3
J5	IO129RSB2
J6	IO131RSB2
J7	VCC
J8	TCK
J9	GDA2/IO89RSB2
J10	TDO
J11	GDA1/IO88PDB1
J12	GDB1/IO87PDB1

FG256



Note: This is the bottom view of the package.

Note

For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

FG484	
Pin Number	AGL400 Function
AA15	NC
AA16	NC
AA17	NC
AA18	NC
AA19	NC
AA20	NC
AA21	VCCIB1
AA22	GND
AB1	GND
AB2	GND
AB3	VCCIB2
AB4	NC
AB5	NC
AB6	IO121RSB2
AB7	IO119RSB2
AB8	IO114RSB2
AB9	IO109RSB2
AB10	NC
AB11	NC
AB12	IO104RSB2
AB13	IO103RSB2
AB14	NC
AB15	NC
AB16	IO91RSB2
AB17	IO90RSB2
AB18	NC
AB19	NC
AB20	VCCIB2
AB21	GND
AB22	GND
B1	GND
B2	VCCIB3
B3	NC
B4	NC
B5	NC
B6	NC

FG484	
Pin Number	AGL600 Function
V15	IO96RSB2
V16	GDB2/IO90RSB2
V17	TDI
V18	GNDQ
V19	TDO
V20	GND
V21	NC
V22	NC
W1	NC
W2	IO148PDB3
W3	NC
W4	GND
W5	IO137RSB2
W6	FF/GEB2/IO142RSB2
W7	IO134RSB2
W8	IO125RSB2
W9	IO123RSB2
W10	IO118RSB2
W11	IO115RSB2
W12	IO111RSB2
W13	IO106RSB2
W14	IO102RSB2
W15	GDC2/IO91RSB2
W16	IO93RSB2
W17	GDA2/IO89RSB2
W18	TMS
W19	GND
W20	NC
W21	NC
W22	NC
Y1	VCCIB3
Y2	IO148NDB3
Y3	NC
Y4	NC
Y5	GND
Y6	NC

FG484	
Pin Number	AGL1000 Function
H19	IO87PDB1
H20	VCC
H21	NC
H22	NC
J1	IO212NDB3
J2	IO212PDB3
J3	NC
J4	IO217NDB3
J5	IO218NDB3
J6	IO216PDB3
J7	IO216NDB3
J8	VCCIB3
J9	GND
J10	VCC
J11	VCC
J12	VCC
J13	VCC
J14	GND
J15	VCCIB1
J16	IO83NPB1
J17	IO86NPB1
J18	IO90PPB1
J19	IO87NDB1
J20	NC
J21	IO89PDB1
J22	IO89NDB1
K1	IO211PDB3
K2	IO211NDB3
K3	NC
K4	IO210PPB3
K5	IO213NDB3
K6	IO213PDB3
K7	GFC1/IO209PPB3
K8	VCCIB3
K9	VCC
K10	GND

Revision	Changes	Page
Revision 19 (continued)	The following sentence was removed from the "Advanced Architecture" section: "In addition, extensive on-chip programming circuitry allows for rapid, single-voltage (3.3 V) programming of IGLOO devices via an IEEE 1532 JTAG interface" (SAR 28756).	1-3
	The "Specifying I/O States During Programming" section is new (SAR 21281).	1-8
	Values for VCCPLL at 1.2 V –1.5 V DC core supply voltage were revised in Table 2-2 • Recommended Operating Conditions 1 (SAR 22356). The value for VPUMP operation was changed from "0 to 3.45 V" to "0 to 3.6 V" (SAR 25220). The value for VCCPLL 1.5 V DC core supply voltage was changed from "1.4 to 1.6 V" to "1.425 to 1.575 V" (SAR 26551). The notes in the table were renumbered in order of their appearance in the table (SAR 21869).	2-2
	The temperature used in EQ 2 was revised from 110°C to 100°C for consistency with the limits given in Table 2-2 • Recommended Operating Conditions 1. The resulting maximum power allowed is thus 1.28 W. Formerly it was 1.71 W (SAR 26259).	2-6
	Values for CS196, CS281, and QN132 packages were added to Table 2-5 • Package Thermal Resistivities (SARs 26228, 32301).	2-6
	Table 2-6 • Temperature and Voltage Derating Factors for Timing Delays (normalized to TJ = 70°C, VCC = 1.425 V) and Table 2-7 • Temperature and Voltage Derating Factors for Timing Delays (normalized to TJ = 70°C, VCC = 1.14 V) were updated to remove the column for –20°C and shift the data over to correct columns (SAR 23041).	2-7
	The tables in the "Quiescent Supply Current" section were updated with revised notes on IDD (SAR 24112). Table 2-8 • Power Supply State per Mode is new.	2-7
	The formulas in the table notes for Table 2-41 • I/O Weak Pull-Up/Pull-Down Resistances were corrected (SAR 21348).	2-37
	The row for 110°C was removed from Table 2-45 • Duration of Short Circuit Event before Failure. The example in the associated paragraph was changed from 110°C to 100°C. Table 2-46 • I/O Input Rise Time, Fall Time, and Related I/O Reliability1 was revised to change 110° to 100°C. (SAR 26259).	2-40
	The notes regarding drive strength in the "Summary of I/O Timing Characteristics – Default I/O Software Settings" section, "3.3 V LVCMOS Wide Range" section and "1.2 V LVCMOS Wide Range" section tables were revised for clarification. They now state that the minimum drive strength for the default software configuration when run in wide range is ±100 µA. The drive strength displayed in software is supported in normal range only. For a detailed I/V curve, refer to the IBIS models (SAR 25700).	2-28, 2-47, 2-77
	The following sentence was deleted from the "2.5 V LVCMOS" section (SAR 24916): "It uses a 5 V–tolerant input buffer and push-pull output buffer."	2-56
	The values for F _{DDRIMAX} and F _{DDOMAX} were updated in the tables in the "Input DDR Module" section and "Output DDR Module" section (SAR 23919).	2-94, 2-97
	The following notes were removed from Table 2-147 • Minimum and Maximum DC Input and Output Levels (SAR 29428): ±5% Differential input voltage = ±350 mV	2-81
	Table 2-189 • IGLOO CCC/PLL Specification and Table 2-190 • IGLOO CCC/PLL Specification were updated. A note was added to both tables indicating that when the CCC/PLL core is generated by Mircosemi core generator software, not all delay values of the specified delay increments are available (SAR 25705).	2-115